

[54] **CONTROL DEVICES FOR DISPLAY APPARATUS**

[72] Inventors: **Shigenori Matsushita**, Yokohama;
Fumitaka Sato, Kawasaki; **Hisao**
Chujo; **Minori Horiike**, both of
Yokohama, all of Japan

[73] Assignee: **Tokyo Shibaura Electric Co., Ltd.,
Kawasaki-shi, Japan**

[22] Filed: July 1, 1971

[21] Appl. No.: 158,846

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 724,558, April 26, 1968, abandoned.

[52] U.S. Cl.....340/324 A, 340/172.5

[51] Int. Cl. G06f 3/14

[58] **Field of Search** 340/324 A, 152 R, 154

[56] References Cited

UNITED STATES PATENTS

3,406,387	10/1968	Werme.....	340/324 A
3,422,420	1/1969	Clark.....	340/324 A
3,439,218	4/1969	Savinese et al.....	340/324 A X
3,555,520	1/1971	Helbig et al.....	340/324 A
3,593,310	7/1971	Kievit.....	340/324 A X

3,611,348	10/1971	Rogers.....	340/324 A
3,614,766	10/1971	Kievit	340/324 A

Primary Examiner—John W. Caldwell

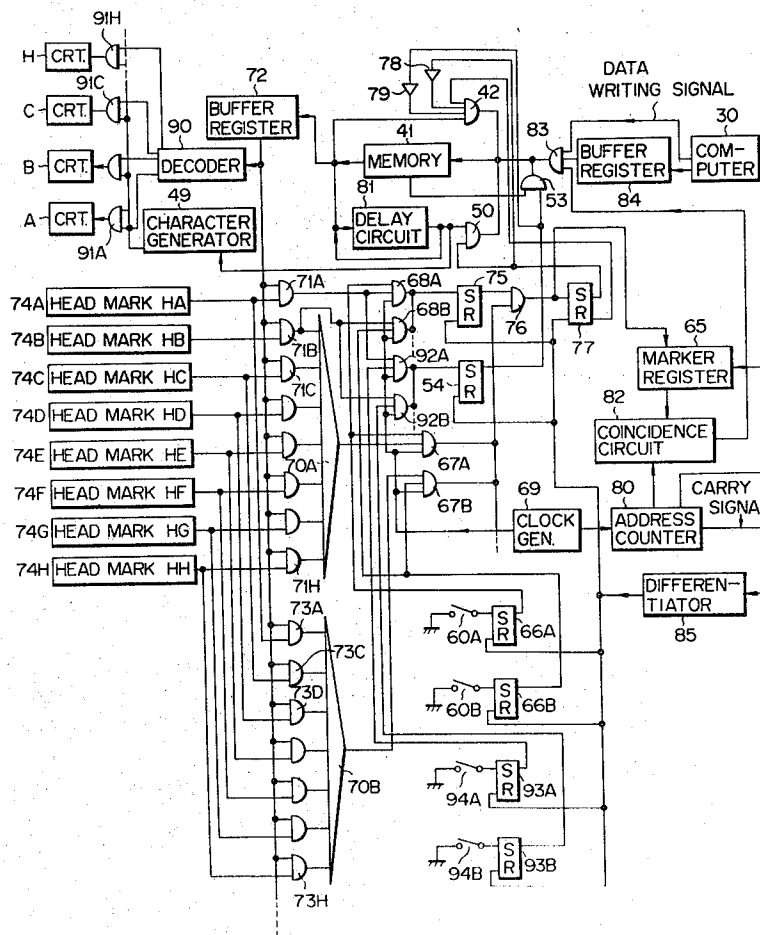
Assistant Examiner—David L. Trafton

Attorney—George B. Oujevolk

[57] ABSTRACT

Character data for a plurality of scanned cathode ray tube displays are stored in a recirculating magnetostriuctive delay line memory by character lines identified for their particular display tubes. Decoder means continuously gates character data to the appropriate display tubes. The recirculating memory has three feedback circuits — one for the normal memory function, the second having a recirculating delay sufficient for scanning a line of characters, and the third for advancing each character line to the position in the memory previously occupied by a preceding displayed character line. The three feedback circuits are controlled by gating means to give static character line readout for all the display tubes, to delete specified character lines and thereby contract the display and advance the other character lines to new positions on the appropriate display tubes, or to add new character lines and thereby expand the display on the appropriate display tubes.

1 Claim, 21 Drawing Figures



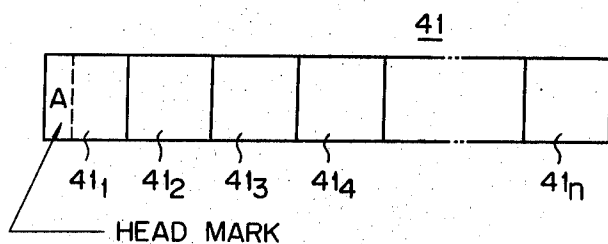


FIG. 1

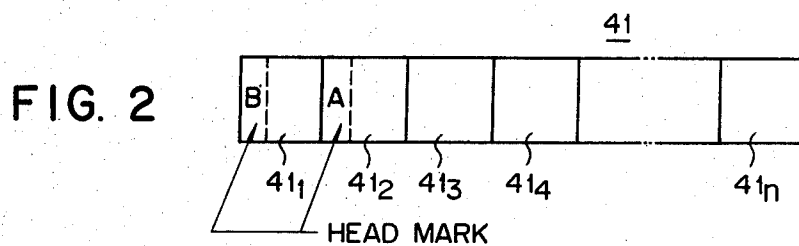


FIG. 2

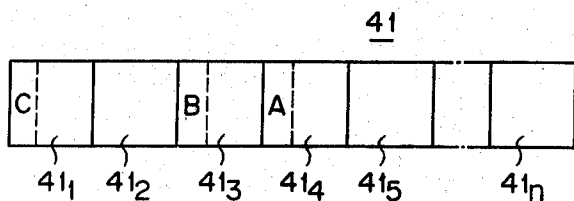
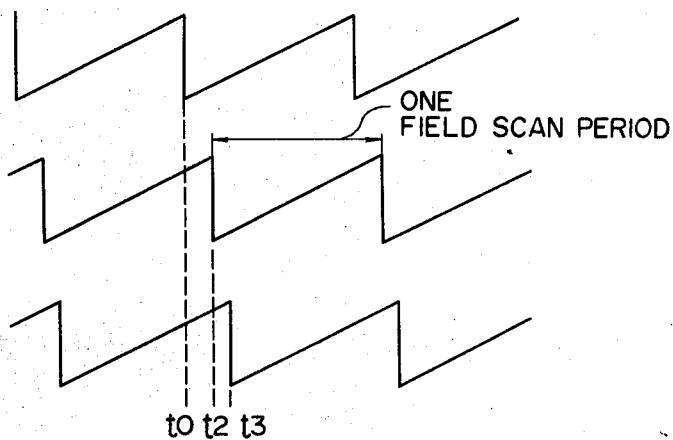


FIG. 3

FIG. 4A

FIG. 4B

FIG. 4C



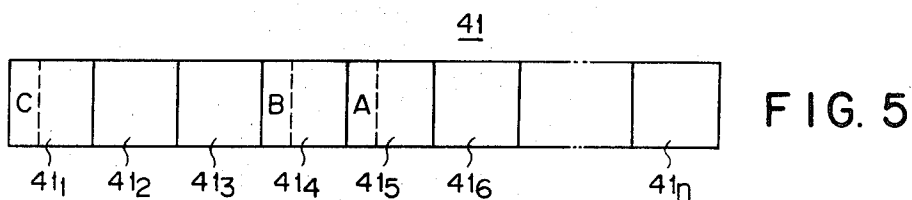


FIG. 6A

FIG. 6B

FIG. 6C

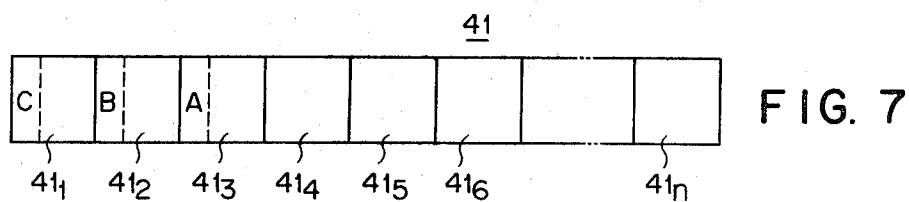
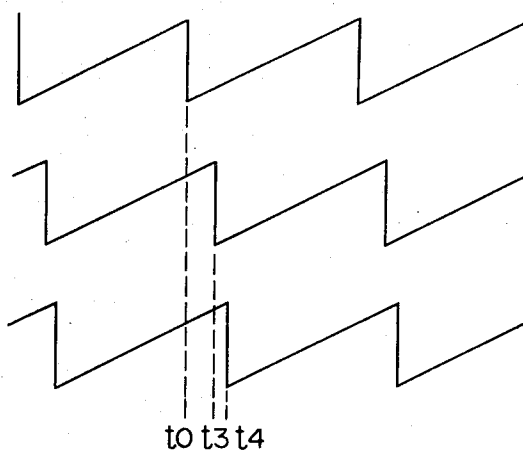


FIG. 8A

FIG. 8B

FIG. 8C

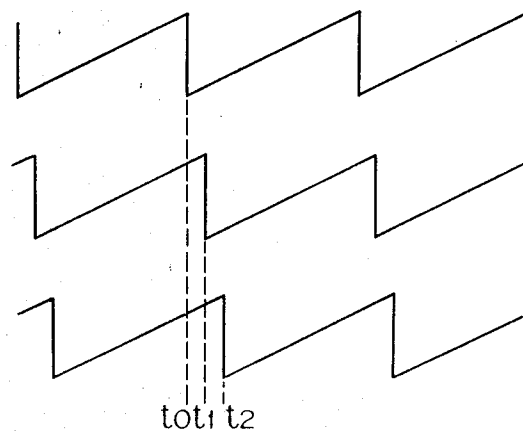


FIG. 9

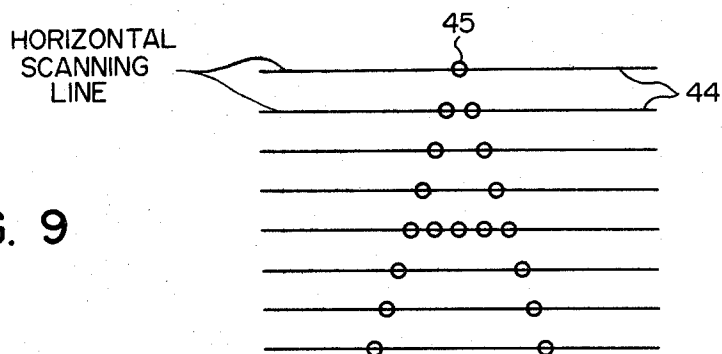


FIG. 12A

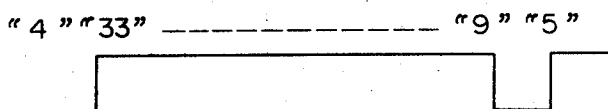


FIG. 12B



FIG. 13A

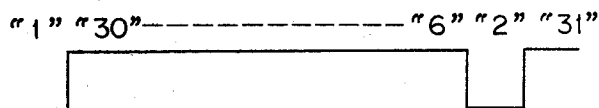


FIG. 13B



FIG. 10

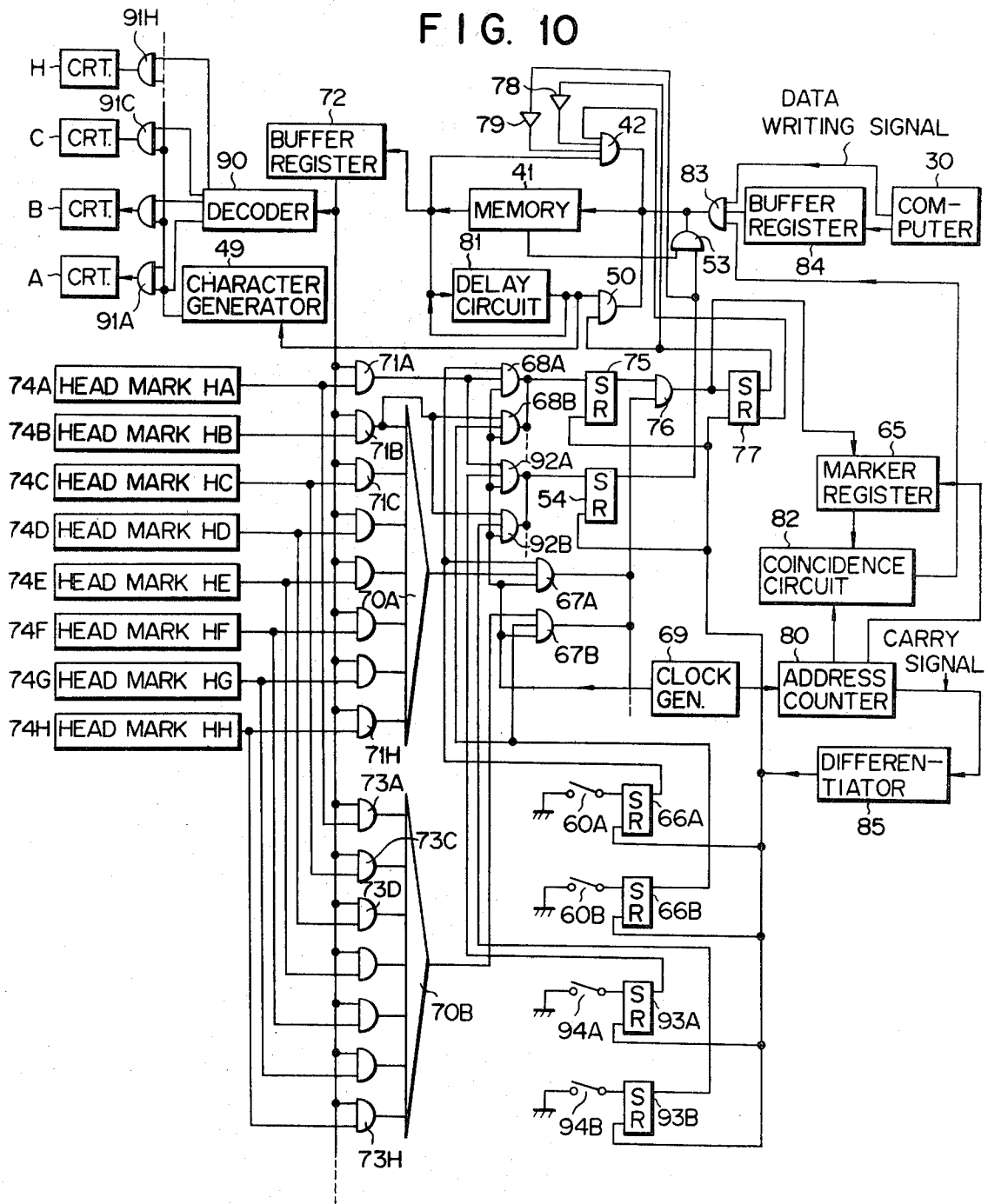
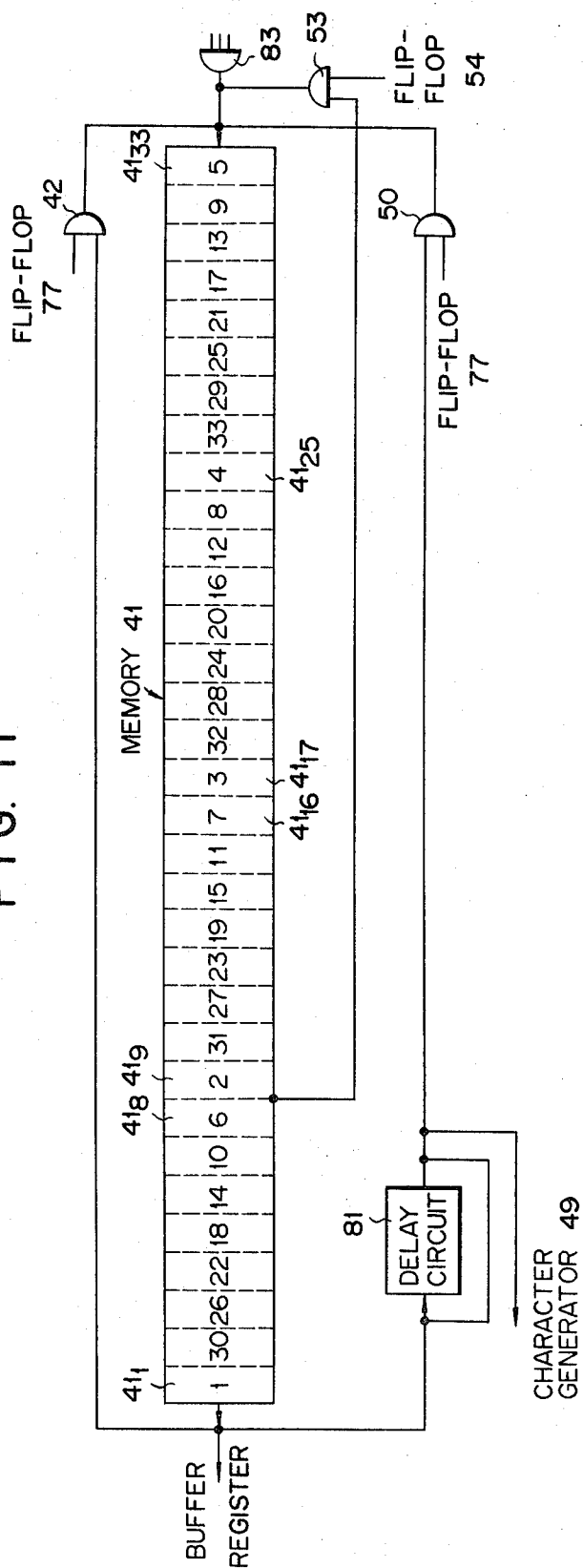


FIG. 11



CONTROL DEVICES FOR DISPLAY APPARATUS**CROSS-REFERENCE TO RELATED APPLICATION**

This is a Continuation-in-part of the U.S. Pat. application Ser. No. 724,558, filed on Apr. 26, 1968 now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to a control device for a display apparatus and more particularly to a control device for a terminal display apparatus such as a cathode ray tube utilized in an interlocked relation with an electronic computer.

Normally, such a display apparatus comprises a memory device, a control circuit, a display control device including a letter generating circuit, a cathode ray tube and a terminal display apparatus including a keyboard. The memory device functions to receive information directly or through a communication line and the like from the keyboard, a computer or the like and stores received information. Information corresponding to one line of the display surface of the cathode ray tube is sequentially read out from the memory device by the action of the control circuit and the read out information is converted into patterns such as letters or characters by a character generating circuit and the patterns are displayed on the indicating plane of the cathode ray tube as visible information. In this case it is usual to read out information stored in the memory device at a rate of several tens times per second and the read out information is then supplied to the cathode ray tube through the letter generating circuit so as to provide steadily and fixed display thereof on the display surface. Accordingly, the memory device is required to operate at a high speed commensurate with the read out speed thus requiring a complicated and expensive display control device. Accordingly, it has been proposed to connect a plurality of terminal display apparatuses to a common memory device whereby to decrease relative cost of the display control device per one terminal display apparatus. Where it is desired to display different information on different terminal display apparatus a memory device included in a display control device was divided into a plurality of memory blocks which are assigned and permanently connected to respective one of a plurality of terminal display apparatuses. For example where two terminal display apparatuses are to be connected to a memory device capable of storing 32 lines of information, memory blocks having a storing capacity of 16 lines are assigned and permanently connected to respective terminal display apparatuses. On the other hand where eight terminal display apparatuses are to be connected to the memory device, memory blocks of four line capacity are assigned and permanently connected to respective terminal display apparatuses to display information.

With such a conventional display apparatus, however, where some of the terminal display apparatus does not display information or displays lesser number of information than those assigned thereto there will be some not used or vacant memory blocks. As a consequence if it is desired to display long information on another terminal display apparatus, since memory blocks of the memory device are fixedly assigned to respective terminal display apparatuses information

more than fixedly assigned could not be displayed thus limiting the display capacity. If the arrangement were such that information more than fixedly assigned could be displayed on the terminal display apparatus, it would become necessary to fixedly assign to such display apparatus memory blocks capable of storing information of the number just enough to be displayed on the display surface or respective terminal display apparatuses, which requires a memory device of large capacity and high cost.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide a novel control device for a display apparatus whereby respective display apparatuses can display information of any number, thus improving their display ability.

According to this invention there is provided a control device for display apparatus for controlling the amount of information to be displayed on the display surfaces of at least first and second cathode ray tubes, which comprises a memory device consisting of a magneto-strictive delay line, transducers and write-in and read-out amplifiers; means for successively storing the memory device from its input terminal with first and second head marks representing the first and second cathode ray tubes and the following information to be displayed on the cathode ray tubes in the form of a block divided into a plurality of display lines; first feedback means for feeding back stored information directly from the output terminal to the input terminal of the memory device; second feedback means for feeding back stored information from the output terminal to the input terminal of the memory device by delaying said information for a length of time equal to that required for one display line to be presented on the display surface; third feedback means for drawing out stored information at a point displaced from the output terminal toward the input terminal of the memory device for a sufficient distance to store information corresponding to one display line to be indicated on the display surface and feeding back said information directly to the input terminal of the memory device; means for visibly displaying on one cathode ray tube a piece of information immediately following the head mark appearing at the output terminal of the memory device; first and second switch means corresponding to said first and second cathode ray tubes so as to generate information display-expanding signals; means for detecting upon the closure of the first or second switch means the head mark of a cathode ray tube expected to display information in succession to that which is already displaying information and rendering the first feedback means inoperable and the second feedback means operable according to the signals thus detected; third and fourth switch means corresponding to said first and second cathode ray tubes so as to generate information display-contracting signals; and means for rendering upon the closure of the third or fourth switch means the first feedback means inoperable and the third feedback means operable and the third feedback means operable when there appears at the output terminal of the memory device a piece of information representing a display line to be presented on the display surface of a prescribed cathode ray tube in succession to that which is already displayed thereon.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1,2,3,5 and 7 show information formats stored in a memory device including a magneto-strictive delay line used in a control device according to an embodiment of this invention;

FIGS. 4A,B,C; 6A,B,C; and 8A,B,C are wave form diagrams of vertical scanning signals used in indicating the contents of information of FIGS. 3,5 and 7 on the terminal display apparatuses, that is, cathode ray tubes;

FIG. 9 illustrates a letter included in a display line indicated according to this invention on the cathode ray tube;

FIG. 10 is a circuit diagram of a display control apparatus according to the invention;

FIG. 11 illustrates the operation of a memory device including a magneto-strictive delay line used in the display control device of FIG. 10;

FIGS. 12A, 12B, 13A and 13B indicate wave forms by way of illustrating the operation of the display control device of FIG. 10.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention will be outlined with reference to FIGS. 1 through 9. As shown in FIG. 1 a memory device 41 is divided into a plurality of memory blocks 41₁ to 41_n, in which content stored in each block corresponds to one line of characters to be displayed on the display surface of a terminal display apparatus or a cathode ray tube. Under the control of a control circuit (not shown), information to be displayed on respective display surfaces of the cathode ray tube together with information positioned at the leading end thereof and representing head marks inherent to respective terminal display apparatuses is sequentially written in the memory blocks as shown in FIG. 1. For example, where three cathode ray tubes A, B and C (shown in FIG. 10) are used, information representing a head mark HA inherent to the cathode ray tube A is attached to the leading end of information corresponding to two lines, and this information of the head mark HA and the information corresponding to the first one of said two lines is written in the first memory block 41₁, whereas information corresponding to the second line in the second memory block 41₂. Then, when it is desired to write in the memory device 41 information of one line, for example, to be displayed on the terminal display device B, information for the terminal display device A which is written in the first and second blocks 41₁, 41₂, is transferred to the second and third blocks 41₂ and 41₃, respectively and the information of one line is written in the first block 41₁ together with the information of the head mark HB inherent to the terminal display device B and attached to the leading end of said information of one line, as shown in FIG. 2.

Further where it is desired to write in the memory device 41 information of two lines, for example, to be displayed on the terminal display apparatus C, as shown in FIG. 3, information that is stored in the memory device 41 is shifted to blocks spaced backwardly by a number of blocks corresponding to two lines, that is information written in the first to third blocks, 41₁ to 41₃ is transferred to the third to fifth blocks 41₃ to 41₅ while at the same time information of the first line is written in the first block 41₁ together

with an information of the head mark HC inherent to the terminal display apparatus C and attached to the leading end of the information of two lines to be displayed on the terminal display device C, while information of the second line is written in the second block. In this manner, information to be displayed on respective terminal display apparatuses is sequentially written in memory blocks 41₁ to 41_n of the memory device 41 together with head marks inherent to respective terminal display apparatuses and attached to their leading ends. When a certain line of the information displayed on one of the terminal display apparatuses becomes unnecessary, information of that line is removed from a corresponding block and information stored in the memory block behind the block from which information is to be removed is sequentially transferred forwardly one block each to occupy the emptied block, thus leaving the last block unoccupied, as will be more fully described later.

Information stored in the memory device is repeatedly read out by sequentially scanning with the control circuit and read out information is converted into pattern signals such as characters by means of a character generating device. Each time a head mark is detected it is applied to a corresponding terminal display device. Concurrently therewith its vertical synchronizing signal is generated to provide scanning, and horizontal scanning is also provided to display read out information on the display surface. Utilization of a horizontal synchronizing signal common to all terminal display apparatuses enables to simultaneous display of different information sequentially on respective display surfaces starting from their upper end. Further, the interval of time required to read out information of one memory block is made equal to that required for scanning one line of the display surface of the terminal display apparatus. Detail of the vertical scanning is as follows: At an instant t_0 when the head mark HC for the terminal display apparatus C is detected, a vertical scanning signal as shown in FIG. 4A is generated for the terminal display apparatus C to begin its vertical scanning whereby to display information that has been stored in the first and second memory blocks 41₁ and 41₂ of the memory device 41 shown in FIG. 3 on the first and second lines from upper of the display surface of the terminal display apparatus C. When the head mark HB of the terminal display device B is detected at an instant t_2 later than the instant t_0 by an interval during which information of two lines can be read out from the memory device 41, a vertical scanning signal as shown in FIG. 4B is generated to begin the vertical scanning of the terminal display apparatus B thereby displaying information stored in the third memory block 41₃ of the memory device 41 on the first line from upper of the display surface of the terminal display device B. Likewise upon detection of a head mark HA of the terminal display apparatus A at an instant t_3 later than the instant t_2 by an interval during which information corresponding to one line can be read out from memory device 41, a vertical scanning signal as shown in FIG. 4C is generated to begin the vertical scanning of the terminal display apparatus A thereby displaying information that has been stored in the fourth and fifth memory blocks 41₄ and 41₅ of the memory device 41 on the first and second lines from

upper of the display surface of the terminal display apparatus A. In this manner, each time a head mark is detected the vertical scanning of the corresponding terminal display apparatus is initiated to display information. Where information to be displayed on the terminal display apparatus C is increased to three lines, as shown in FIG. 5, pieces of information to be stored on terminal display apparatuses A and B are respectively shifted one block backwardly, thus storing them in the fourth and following memory blocks, whereby information to be displayed on the third line of the terminal display apparatus C is stored in the third memory block 41₃.

In this case, vertical scanning of respective terminal display apparatuses is performed in the following manner. With regard to the terminal display apparatus C, a vertical scanning signal as shown in FIG. 6A is generated at an instant t_0 when its head mark HC is detected to begin vertical scanning and when the head mark HB of the terminal display apparatus B is detected at an instant t_3 later than t_0 by an interval during which information corresponding to three lines can be read out of the memory device 41 a vertical scanning as shown in FIG. 6B is generated to begin its vertical scanning. Similarly when the head mark HA of the terminal display apparatus A is detected at an instant t_4 later than t_3 by an interval during which information corresponding to one line can be read out from the memory device 41 a vertical scanning as shown in FIG. 6C is generated to begin its vertical scanning. By comparing FIG. 6 with FIG. 4, it can be noted that in the condition shown in FIG. 4 the vertical scanning signal for the terminal display apparatus B begins at instant t_2 but owing to the increase of one line in the display apparatus C the vertical scanning signal for the terminal display device B will come to begin at instant t_3 later than t_2 by an interval corresponding to one line. Thus, under this transient condition the vertical scanning signal is delayed for an interval corresponding to one line.

Also in the terminal display device A owing to the increase of one line in the terminal display apparatus C, the vertical scanning signal is delayed one line during the transient condition.

Regardless of the shift of the vertical scanning signal, it is possible to assure displayed information free from the effect of such shift as the vertical scanning of ordinary television receiver can follow such shift. Thus each time a head mark is detected the vertical scanning operation of a corresponding terminal display apparatus is initiated to display information. When information corresponding to one line is eliminated from information to be displayed on two lines of the terminal display apparatus C, information to be displayed on terminal display apparatuses A and B is shifted one block forward thus storing it in the second and following memory blocks as shown in FIG. 7. In this case the vertical scanning operation of respective terminal display apparatuses is performed in the following manner. The terminal display apparatus C generates a vertical scanning signal as shown in FIG. 8A at instant t_0 when the head mark HC is detected by the control device thereof. Whereas the terminal display apparatus B generates a vertical scanning as shown in FIG. 8B at the instant t_1 when its head mark HB is detected. The in-

stant t_1 is later than t_0 by an interval during which information corresponding to one line can be read out from the memory device 41. Likewise the terminal display apparatus A generates a vertical scanning signal as shown in FIG. 8C when its head mark HC is detected at the instant t_2 later than t_1 by an interval of reading out information corresponding to one line. In this case also, the vertical scanning signal of the terminal display apparatus B which begins at t_2 under the condition shown in FIG. 4 has changed to begin at the instant t_1 which is earlier than t_2 by the time interval to read out one line. Thus, under transient state the vertical scanning signal for the terminal display apparatus B is advanced one line. Similarly, under the transient state the vertical scanning signal for the terminal display apparatus A is also advanced one line. Thus, each time a head mark is detected the vertical scanning operation of the corresponding terminal display apparatus is commenced to display information thereon. During these procedures, increase or elimination of information to be displayed on respective terminal display apparatuses can be treated according to their sequence of arrival so that information can be shifted forward or backward by maximum one block in the memory device during the scanning time required to scan one display surface of a terminal display apparatus. Since with an ordinary television receiver the vertical scanning signal thereof can follow such shift there is no effect displayed information.

FIG. 9 shows a letter "A" included in a piece of information corresponding to one display line presented on the display surface of a terminal display apparatus, that is a cathode ray tube. The information representing one display line is, as described above, equal to the amount of information stored in one memory block of the memory device 41. Said information denoting one display line is designed, as shown in FIG. 9, to be displayed by eight horizontal scanning lines 44. As later described, the information stored in one memory block of the memory device 41 is conducted to the known character generator to be converted to, for example, television signals based on eight scanning lines to display under control by said character generator, for example, a letter "A" consisting of a plurality of bright spots 45 on a prescribed cathode ray tube.

There will now be described by reference to FIGS. 10 and 11 an embodiment of this invention. In the memory device 41 are stored in turn pieces of information bearing the head marks HA to HH of the cathode ray tubes A to H from the computer 30 through a buffer register 84 and AND gate 83. This write-in is effected by conducting display information from the buffer register 84 to the memory device 41 only when the AND gate 83 is supplied with a data writing signal from the computer 30 and signals from the coincidence circuit 82.

When the memory device 41 consists of a magnetostrictive delay line, an information is collected for each display line to be presented on a display surface and conducted to said delay line, then there are formed therein, as shown in FIGS. 1, 2, 3 and 5 or FIG. 7, a plurality of memory blocks in which there are apparently stored pieces of information each corresponding to one display line. FIG. 11 illustrates the condition in which there are formed 33 memory blocks 41₁ to 41₃₃ in the

memory device 41 consisting of a magneto-strictive delay line. Where the memory device 41 consists of a magneto-strictive delay line, the input terminal of said device 41 is fitted with a transducer and write-in amplifier and the output terminal with a transducer and read-out amplifier. Since this is a known technique, description thereof is omitted. The first block 41₁ is connected to the first input terminal of an AND gate 42 and the reset output of a flip-flop 77 generating circulating control pulses is connected to the second input terminal of the AND gate 42, the output terminal thereof being connected to the 33rd block 41₃₃ of the main circulating memory device 41. The main circulating memory device 41 is thus constructed to circulate information stored in its respective memory blocks 41₁ to 41₃₃.

Referring to FIG. 10, output from the memory device 41 is also supplied through a buffer register 72 to one input terminal of a decoder 90 and AND gates 71A to 71H respectively. The decoder 90 decodes those portions of information from the memory device 41 which represent the head marks of the respective display apparatuses or cathode ray tubes A to H, thereby selecting any of said cathode ray tubes according to the decoded head mark. Namely, output from the decoder 90 opens that of the AND gates 91A to 91H which is designated by the decoded head mark. Thus character information from the character generator 49 is conducted to the designated one of the cathode ray tubes A to H so as to be displayed. The character generator 49 may preferably consist of the type disclosed in, for example, the U.S. Pat. No. 3,426,344.

The other input terminal of the AND gates 71A to 71H is connected to the output terminals of the generators 74A to 74H for generating coded signals. Output from said generators excluding the generator 74B is supplied to one input terminal of each of the AND gates 73A, 73C to 73H. The other input terminal of said AND gates is connected to the output terminal of the buffer register 72. The embodiment of FIG. 10 can control the display of eight terminal display apparatuses A to H. Since, however, a circuit for full display control will be complicated, FIG. 10 only shows a circuit adapted to control the display of the terminal display apparatuses A and B. Output from the AND gate 71A is supplied to the AND gate 68A, which only produces output to set the flip-flop circuit 75 when simultaneously supplied with output from the clock pulse generator 69, set output from the flip-flop circuit 66A and output from the AND gate 71A. The flip-flop circuit 66A is set when the switch 60A is closed. Set output from the flip-flop circuit 75 is supplied to one input terminal of the AND gate 76, the other input terminal of which is impressed with output from the AND gate 67A. This AND gate 67A is further supplied with clock pulses, set output from the flip-flop circuit 66A and output from the OR gate 70A. This OR gate 70A is impressed with output from the AND gates 71B to 71H. When the head mark HA is already on display by the closure of the switch 60A and any of the succeeding head marks HB to HH has also just been displayed, the AND gate 76 produces output to set the flip-flop circuit 77, thereby causing the AND gate 40 to be closed and the AND gate 50 to produce output. The set output from the flip-flop circuit 77 is conducted to the AND

gate 42 through the inverter 72 to render said gate 42 operable.

The set input terminal of the flip-flop circuit 75 is connected to the output terminal of the AND gate 68B, which in turn is supplied with clock pulses, output from the AND gate 71B and set output from the flip-flop circuit 66B. This flip-flop circuit 66B is set when the switch B is closed. One input of the AND gate 76 is impressed with output from the AND gate 67B, the input terminal of which is supplied with clock pulses, and output from the OR gate 70B and flip-flop circuit 66B. The OR gate 70B is supplied with output from the AND gates 73A, 73C to 73H. When the head mark HB is already on display by the closure of the switch 60B and any of the succeeding head marks excluding HB has just been displayed, the AND gate 76 generates output to set the flip-flop circuit 77, thereby causing the AND gate 42 to be closed and the AND gate 50 to be opened.

The set input terminal of the flip-flop circuit 54 is connected in parallel to the output terminal of AND gates 92A and 92B. The input terminal of the AND gate 92A is supplied with clock pulses, output from the AND gate 71A and set output from a flip-flop circuit 93A. The input terminal of the AND gate 92B is impressed with clock pulses, output from the AND gate 71B and set output from the flip-flop circuit 93B. The flip-flop circuits 93A and 93B are so designed as to be set when the switches 94A and 94B are closed respectively.

Output from the clock pulse generator 69 is supplied to the address counter 80 to be counted. Said counter 80 generates a carry signal when there is counted a prescribed number of clock pulses corresponding to one circulation of information through the memory device 41, said carry signal being supplied to the differentiator 85, the differential output from which is conducted to the flip-flop circuits 54, 75, 77, 66A, 66B, 93A and 93B to cause these circuits to be reset. Namely, when information makes one circulation through the memory device 41, the control device of this invention never fails to be reset.

Output from the address counter 80 is supplied, together with output from the marker resistor 65, to the coincidence circuit 82. When there appears a coincidence output, it is conducted to one input terminal of the AND gate 83.

Referring now to FIG. 11, information is sequentially written in at an interval of eight blocks. For example, a head mark of a terminal display apparatus A and an information "1" corresponding to the first line thereof are written in the first block 41₁. Pieces of information "30" to "6" are those representing the head marks of, for example, the other cathode ray tubes B to H and that carried by the immediately following first display line. An information "2" corresponding to the second line of the display apparatus A is written in the ninth block 41₉, spaced from the first block 41₁ by eight blocks in the direction of circulation of information. In the same manner information corresponding to the third, fourth, fifth, sixth . . . lines is sequentially written in the 17th, 25th, 33rd, eighth . . . memory blocks respectively. Similarly with the other terminal display apparatuses, there are stored in turn the pieces of information representing the second, third and fourth dis-

play lines by being collected for every nine blocks. The reason that information is stored at an interval of eight blocks is to display information such as letter on the display surface of the cathode ray tube by eight horizontal scanning operations per line as shown in FIG. 9. The delay time of the delay circuit 81 is so defined as to be equal to that which is required for one horizontal scanning on the display surface. Output from said delay circuit 81 is fed back to its input terminal, causing the character generator 49 to be supplied with the same signal per horizontal scanning. The output of the AND gate 50 is connected to the 33rd memory block 41₃₃ of the memory circuit 41. The output of the ninth memory block 41₉ of the memory circuit 41 is connected to the first input terminal of an AND gate 53 while the second input terminal of the AND gate 53 is connected to the set output of a flip-flop 54 generating advance control pulses and an input terminal of the four input AND gate 42 via an inverter 79. The output of the AND gate circuit 53 is connected to the 33rd memory block 41₃₃ of the memory block 41.

To display information stored in the memory device 41 on the display surfaces of cathode ray tubes A, B, C, . . . H while the AND gate 42 is held opened or enabled by the reset output of the circulation control pulse generating circuit 77 and outputs of inverters 78 and 79, information stored in respective memory blocks 41₁ to 41₃₃ is advanced at a definite time interval to shift it to next blocks 41₃₃, 41₁, 41₂, . . . 41₃₂, thus causing it to circulate through memory blocks under control of the output of the flip-flop 77. The time interval for shifting information to next blocks is selected to be the same as the one horizontal scanning time of a cathode ray tube. When the information "1" corresponding to the first line is shifted to the 33rd memory block 41₃₃, the first information "1" is also stored in the image circulation memory device 81. During this displaying period, AND gate 50 and AND gate 53 are maintained in their closed state and AND gate 42 is maintained in its opened state. Thus the first information stored in the image circulating memory device 81 is caused to circulate eight times and applied to character generator 49 during circulation operation. At this time when the first head mark attached to the leading end of the first information "1" has been detected by the decoder 90, the first information will be applied to a corresponding cathode ray tube and displayed thereon. At the same time when the first information "1" completes its eight circulation through the image circulation memory device 81 the second information "2" has been shifted to the first memory block 41₁ and the second information "2" is stored in the image circulation memory device 81. Thereafter, the second information "2" stored in the image circulation memory device 81 is circulated eight times to apply it to character generator 49 during its circulation. As a result, character generator 49 generates a pattern signal of the second information "2" to apply it to a corresponding cathode ray tube, whereby a pattern such as characters on the second line is displayed by eight horizontal scanning lines. In this case, in the absence of a second head mark at its leading end, the second information "2" will be displayed on the second line of the same display plane selected by the first head mark whereas in the presence of the

second head mark the second information "2" will be displayed on the first line of the display surface of a corresponding cathode ray tube which is selected by the second head mark. In the same manner the third and following piece of information "3", "4" . . . are displayed on the predetermined positions of the predetermined cathode ray tubes and by repeating this operation for a predetermined number of cycles, the pattern of the information is displayed steadily on the display surface of the cathode ray tube.

Where the information to be displayed on a certain cathode ray tube, for example, the cathode ray tube A is increased one line, as above described, information stored in blocks following a particular memory block adapted to store the information corresponding to the increased one line is required to be shifted to provide a not occupied memory block to store said information of the increased line in the vacant block. More particularly, it is necessary to display the increased information on the last line, for example, between the third information "3" and the fourth information "4" displayed on the display surface of cathode ray tube A. Of course it is possible only when there is at least one vacant memory block in the memory device 41, and impossible to increase the information when all memory blocks are occupied. In such a case, it is necessary to sequentially shift the fourth information "4" and following information from their presently occupying memory blocks 41₂₅, 41₃₃, 41₁, . . . for example, to succeeding memory blocks 41₃₃, 41₁, 41₂, . . . , thus shifting at an interval of eight blocks to provide a vacant memory block 41₂₅. Thus the increased information can be written in this memory block 41₂₅ to be displayed on the display surface of said cathode ray tube A. Shift of the fourth and following pieces of information to succeeding blocks spaced therefrom eight blocks is accomplished in the following manner.

When expansion switch 60A is closed a display expansion signal is formed to set a flip-flop circuit 66A, thus supplying the output signal from the set terminal thereof to AND gate circuits 67A and 68A. These AND gate circuits 67A, 68A also receive the clock pulse signal from clock pulse generator 69 as well as the outputs from OR gate 70A and AND gate 71A. AND gate circuit 68A operates to the head mark "A" among information from the buffer register 72 to set the flip-flop circuit 75. Under this condition any one of AND gate circuits 71B to 71H operates to detect one head mark other than the head mark "A" to provide a logical product thereof by the action of the AND gate circuit 67A. The output of AND gate circuit 67A is supplied to the AND gate circuit 76 to provide the output from the set terminal of the flip-flop circuit 75. The logical product provided by the AND gate circuit 76 means that there is left a vacant space on the display surface of cathode ray tube A after display thereon of all information from the memory device 41 has completed. Then the output from AND gate circuit 76 is sent to flip-flop circuit 77 to set it to enable the AND gate circuit 50. Concurrently therewith the output from the circuit 76 is sent to set terminal of marker register 65.

Counting output from address counter 80 which counts the clock pulse from a clock pulse generator 69 is also supplied to marker register 65 as the address

signal which is set in register 65 by said set signal. Since at that time AND gate circuit 42 is disenabled or closed and since the information is lagged one block through a delay memory device 81, memory block 41₃₃ at the input end of the magneto-strictive delay line memory device 41 is vacant so that by enabling AND gate 83 by the output from a coincidence detection circuit 82, information from the electronic computer 30 can be written in the vacant memory block 41₃₃ through a data writing buffer 84. At this time the carry signal from the address counter 80 functions to reset flip-flop circuits 75 and 77 and 66A through a build-up differentiation circuit 85. Accordingly when the expansion switch 60A is operated one time, one expansion operation is effected and continuous depression of switch 60A enables continuous expansion operation.

The marker register 65 is set by output generated by the AND gate 76 when the switch 60A or 60B is closed, thereby storing the number of counts indicated at that time on the address counter 80, that is, the address or memory number on the memory device 41 of the corresponding display line of the terminal display device, whose information display has been expanded by the closure of the switch 60A or 60B. When the number of counts indicated on the address counter 80 coincides with output from the marker register 65, then the input terminal of the memory device 41 is made blank by being subjected to the display line increasing operation, thereby enabling fresh information from the computer 30 to be written in said memory device 41 according to output from the coincidence circuit 82. Thus, at an instant when the fourth information "4" is shifted from the first block 41₁ to the 33rd block 41₃₃, as shown in FIG. 12A, the output flip-flop 77 is interrupted to disenable the circulating AND gate 42 to intercept the fourth information "4" whereby to empty the 33rd memory block 41₃₃ to write therein said increased information. Thereafter, at an instant where the information stored in the memory device 41 has shifted eight blocks, the circulation AND gate 42 is again disenabled to intercept the fifth information "5", while at the same time a pulse signal as shown in FIG. 12B is applied to the lag output AND gate 50 from flip-flop 77 to enable the AND gate 50 thus writing the fourth information "4" which has circulated eight times through the image circulation memory device 81. In the same manner the fifth and following pieces of information "5", "6", "7" ... are sequentially shifted.

To erase a particular information displayed on a cathode ray tube A, said information is eliminated from the memory device 41 and succeeding information is shifted forwardly. For example, in order to eliminate the first information "1" at an instant when the first information "1" is shifted from the first memory block 41₁ to the 33rd memory block 41₃₃, as shown in FIG. 13A, the reset output signal from flip-flop 77 is interrupted to disenable the circulation AND gate 42 thus removing the first information "1". At the same time the advance control flip-flop 54 supplies a pulse signal as shown in FIG. 13B to the advance AND gate 53 to enable the same whereby second information "2" which is being shifted to the eighth block 41₈ from the ninth block 41₉, spaced eight blocks from the first block 41₁, is written in the 33rd block 41₃₃ instead of the first information "1". In the same manner the third and fol-

lowing pieces of information are shifted eight blocks in the forward direction. As has been pointed out hereinbefore, shift of information in the forward or backward direction for the purpose of increasing or decreasing the information does not affect the display on the cathode ray tube.

The closure of the advance control switch 94A leads to the closure of the AND gate 42 to eliminate information supplied from the block 41₁ to the block 41₃₃ and set the flip-flop circuit 93A, the set output from which is conducted to the AND gate 92A. Since, at this time, there is already displayed information on the cathode ray tube, output from the AND gate 71A is supplied to said AND gate 92A, output from which in turn sets the flip-flop circuit 54. Output from said flip-flop circuit 54 actuates the AND gate 53 to cause information "2" to be stored instead of the eliminated information "1" in the memory block 41₃₃ which was previously made blank by rendering the AND gate 42 inoperable. Thus the operation of advancing one display line is conducted on the terminal display apparatus A. Said display line-advancing operation is brought to an end when it is carried out with all pieces of information to be displayed on said terminal display apparatus A. At this time, the flip-flop circuits 54 and 77 are reset, causing fresh information to make a normal circulation through the memory device 41.

There will now be described the operations of expanding, eliminating and advancing information on the display surface of the terminal display apparatus, that is, cathode ray tube B. When the switch 60B is closed while there is displayed information on the cathode ray tube B, the flip-flop circuit 66B is set to have its output supplied to the AND gates 67B and 68B. The AND gate 68B is supplied with output from the AND gate 71B to set the flip-flop circuit 75. If, at this time, there is produced output from any of the AND gates 73A, 73C to 73H, said output is conducted through the OR gate 70B to the AND gate 67B to actuate the AND gate 76, output from which sets the flip-flop circuit 77 to render the AND gate 42 inoperable and the AND gate 50 operable. Thus there is performed an information display-expanding operation on the terminal display apparatus B as in the case of the terminal display apparatus A.

There will now be described the information display advancing operation. When the advance control switch 94B is closed, the AND gate 42 is rendered inoperable to eliminate information to be supplied from the memory block 41₁ to the memory block 41₃₃, causing the flip-flop circuit 54 to be set by output from the AND gate 92B. Set output from the flip-flop circuit actuates the AND gate 53 to advance information display in the same manner as in the terminal display apparatus A.

What we claim is:

1. A control device for display apparatus for controlling the amount of information to be displayed on the display surfaces of at least first and second cathode ray tubes, which comprises a memory device consisting of a magneto-strictive delay line, transducers and write-in and read-out amplifiers; means for successively storing information from its input terminal with first and second head marks representing the first and second cathode ray tubes and the following information to be

displayed on the cathode ray tubes in the form of a block divided into a plurality of display lines; first feedback means for feeding back stored information directly from the output terminal to the input terminal of the memory device; second feedback means for feeding back stored information from the output terminal to the input terminal of the memory device by delaying said information for a length of time equal to that required for one display line to be presented on the display surface; third feedback means for drawing out stored information at a point displaced from the output terminal toward the input terminal of the memory device for a sufficient interval to store information corresponding to one display line to be indicated on the display surface and feeding back said information directly to the input terminal of the memory device; means for visibly displaying on one cathode ray tube a piece of information immediately following the head mark appearing at the output terminal of the memory device; first and second switch means corresponding to

said first and second cathode ray tubes so as to generate information display-expanding signals; means for detecting upon the closure of the first or second switch means the head mark of a cathode ray tube expected to display information in succession to that which is already displaying information and rendering the first feedback means inoperable and the second feedback means operable according to the signals thus detected; third and fourth switch means corresponding to said first and second cathode ray tubes so as to generate information display-containing signals; and means for rendering upon the closure of the third or fourth switch means the first feedback means inoperable and the third feedback means operable when there appears at the output terminal of the memory device a piece of information representing a display line to be presented on the display surface of a prescribed cathode ray tube in succession to that which is already displayed thereon.

* * * * *

25

30

35

40

45

50

55

60

65