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MULTI-SERIES INVERTER ARRANGEMENT

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(56) Prior Art Documents
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(57) Claim

1. A multi-series inverter arrangement comprising, a DC circuit (11, 12, 13) including a neutral point output terminal and a multi-series inverter including three arms (S1U~ S4U, S1V~ S4V, S1W~ S4W) each for U, V and W phases connected in parallel with said DC circuit, each arm including :

first, second, third and fourth switching elements (S1 ~ S4) connected in series, the mutual juncture point of said first and second switching elements (S1, S2) and the mutual juncture point of said third and fourth switching elements (S3, S4) are connected to the neutral point output terminal of said DC circuit via respective clamping diodes (CD1, CD2), and said first and third switching elements (S1, S3) and said second and fourth switching elements (S2, S4) are on and off controlled

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each other in a conjugate relationship ;

flywheel diodes (D1~ D4), each connected in parallel with said first, second, third and fourth switching elements (S1~ S4) ;

snubber circuits (20, 20a, 20b) having a capacitor (25a, 25b) therein, each connected in parallel with said first, second, third and fourth switching elements (S1~ S4) ; and

individual gate driving circuits (E1, R1, R2, C, SW1, E1H, R2, SW1H, E1W, R1, SW1W, E2, SW2) for said first, second, third and fourth switching elements (S1~ S4) for providing a gate current (IFG1, IFG2) thereto,

characterized in that,

the gate current provided by said individual gate driving circuits for said second and third switching elements (S2, S3) is determined larger than that provided by said individual gate driving circuits for said first and fourth switching elements (S1, S4).

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COMPLETE SPECIFICATION

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INVENTION TITLE:

Multi-series inverter arrangement

The following statement is a full description of this invention, including the best method of performing it known to me/us:-

Background of the Invention

1. Field of the Invention

The present invention relates to a multi-series inverter arrangement and, in particular, relates an improvement in a gate driving circuit in a multi-series inverter arrangement which controls turn on and turn off of switching elements such as gate turn-off thyristers (hereinafter abbreviated as GTO) for a multi-series inverter.

2. Description of Related Art

An example of conventional multi-series inverters is disclosed such as in JP-A-56-74088(1981). Fig.1 is a diagram illustrating a main circuit of the multi-series inverter. In the drawing, numeral 11 is a DC power source, smoothing capacitors 12 and 13 connected in series are connected to the DC power source 11 in parallel. The mutural juncture point of these two smoothing capacitors 12 and 13 is used as a neutral point of the DC power source 11. A switching circuit thereof is constituted by GTOs S1U through S4W, flywheel diodes D1U through D4W and clamping diodes CD1U through CD2W for clamping respective output terminals U, V and W at a neutral potential.

The GTOs S1U through S4W constituting the multi-series inverter are controlled turned on and turned off by on and off signals provided from a control circuit (not shown) and the GTOs S1 and S3, and the GTOs S2 and S4 are designed to operate respectively as a set of inverter and are controlled to turn on and turn off in a conjugate relationship each other. As a result, the output voltage at the output terminals of the multi-series inverter is controlled depending upon the on condition of the respective switching elements as illustrated in Fig.2. For example, noting U phase, when the switching elements S1U and S2U are turned on (and the switching elements S3U and S4U are turned off), the potential at the output terminal U is rendered at +E. Contrary thereto, when the switching elements S3U and S4U are turned on (and the switching elements S1U and S2U are turned off), the potential at the output terminal U is rendered at -E. Further, when the switching elements S2U and S3U are turned on (and the switching elements S1U and S4U are turned off), the output terminal U is connected to the juncture point of the smoothing capacitors 12 and 13 via the switching elements S2U and S3U and the clamping diodes CD1U and CD2U, and is fixed at zero potential of the power source neutral point. Simultaneous turn on of the switching elements S1U and S4U is inhibited. As a result of the above explained operation of the switching circuit, potential at the

output terminal U varies between +E, 0 and -E.

Fig.3 shows a waveform diagram of a gate current supplied to GTOs from a gate driving circuit for turning on the GTOs which is illustrated, for example, on page 24 in "Semiconductor Power Converter Circuit" (edited by Special Committee for Investigating Semiconductor Power Conversion System for the Institute of Electrical Engineers of Japan, 1987). When an on signal is applied to a GTO from a control circuit, at first a high gate drive forward current IFG1 is provided thereto and subsequently a wide width gate forward current IFG2 is provided thereto. Based upon "Characteristics of GTO of 4.5kV and 2000A", a reference papar SPC-83-29 prepared by Semiconductor Power Conversion Study Committee for the Institute of Electrical Engineers of Japan, 1983, in case of a GTO of 4.5kV and 2000A, for example, IFG1=25A and IFG2=2A are proposed. Accordingly, a gate driving circuit is constituted in such a manner that when an on signal is applied thereto the gate driving circuit causes to flow a high gate drive forward current IFG1 until the GTO is turned on and thereafter a wide width gate forward current IFG2 is caused to flow until the signal from the control circuit is changed into an off signal.

Fig.4 shows an example of gate driving circuits which causes to flow the gate current as illustrated in Fig.3. When an on signal is applied thereto, a switch SW1 is closed. As a result, electric charges stored in

the capacitor C via a resistor R1 is discharged via a resistor R2 and is provided to the GTO as a high gate drive forward current IFG1 and subsequently a wide width gate forward current IFG2 is provided thereto from an on power source E1. When turning off the GTO, the switch SW1 is opened and a switch SW2 is closed to reversely biasing the GTO with an off power source E2. As will be apparent from Fig.3, the high gate drive forward current IFG1 can not be caused to flow except for the moment when an on signal is applied. Further, switching elements such as transistors and FETs are used for the switches SW1 and SW2.

A reason, which necessitates a large gate current such as the high gate drive forward current when a GTO is required to be turned on, is that if the gate current is small at the moment when a current suddenly begins to flow through the GTO, areas of an on condition do not easily expand over the GTO and a current concentration therein is induced which likely causes a break-down of the GTO.

Accordingly, for a GTO through which no current flows although an on signal is applied thereto, a high gate drive forward current has to be theoretically provided at the moment when a current begins to flow suddenly depending upon the circuit condition. However, in the conventional gate driving circuit no current except for the wide width gate forward current can be

caused to flow at the moment. For this reason, under these conditions even if a current tends to flow suddenly, the GTO likely turns off once due to insufficient on condition thereof and there arises a problem that a voltage between the anode and cathode of the GTO is induced. Such problem is in particular remarkable with regard to a high speed GTO having a short turn off time. Hereinbelow, this phenomenon is explained in detail with reference to drawings.

Fig.5 is a circuit diagram showing only a portion for one phase of the multi-series inverter illustrated in Fig.1. In the multi-series inverter, the GTOs S1 and S3 and the GTOs S2 and S4 are respectively operated to turn on and turn off in a conjugate relationship each other as a set of inverter, therefore as illustrated in Fig.6 there exists three kinds of switching conditions (1)~(3) of the GTOs S1 through S4 and four kinds of changes in switching conditions ① through ④. Among these changes in switching conditions a phenomenon, wherein the GTO tends to turn off, in other words, a phenomenon that a voltage is induced at the GTO (hereinafter called as "incomplete on phenomenon) because the GTO is not sufficiently moved into an on condition when a current having a high di/dt (which will be explained later in detail) flows through the GTO, is caused under the following two conditions, in that one is caused under a condition that the GTOs S1 and S2 in Fig.5 are in an on

condition (the condition (2) in Fig.6) and a load current is flowing through the flywheel diodes D1 and D2 in the direction of an arrow 15 in Fig.5 when the GTO S1 is turned off and the GTO S3 is turned on (the change in switching condition ② in Fig.6), and the other is caused under a condition that the GTOs S3 and S4 are in an on condition (the condition (3) in Fig.6) and a load current is flowing through the flywheel diodes D3 and D4 in the direction of an arrow 16 in Fig.5 when the GTO S4 is turned off and the GTO S2 is turned on (the change in switching condition ④). These two changes in switching conditions are hereinafter called respectively as mode 1 and mode 2.

Current flows during the mode 1 are illustrated in Fig.7. When the GTO S1 is turned off and the GTO S3 is turned on, the load current flowing through the flywheel diodes D1 and D2 is commutated toward the GTO S3 and the clamping diode CD2 in the direction of an arrow 21 and a current from the smoothing capacitor 12 flowing through the flywheel diode D1 for recovering the same and a snubber circuit 20 for the GTO S1 as shown by arrow 22 flows through the GTO S2. This current as indicated by arrow 22 is one which bulids up suddenly at a di/dt of about 100A/μs and is caused to flow through the GTO S2 through which no current has been flown until that moment although an on signal has been provided thereto. Fig.8 shows a voltage waveform induced between the anode and

gate of the GTO S2 and the current waveform thereof at that moment. As seen from the drawing a voltage is induced at the GTO S2 and the induced voltage $\triangle V$ when di/dt is 100A /μs reaches upto 200V. Such voltage induction leads to an increase of switching element damaging and, in some cases, leads to a breakdown of the switching elements which is undesirable.

Current flows during the mode 2 are illustrated in Fig.9. When the GTO S4 is turned off and the GTO S2 is turned on, a load current flowing through the flywheel diodes D3 and D4 is commutated toward the clamping diode CD1 and the GTO S2 in the direction of an arrow 23 and a current from the smoothing capacitor 13 flowing through the flywheel diode D4 for recovering the same and a snubber circuit 20 for the GTO S4 as shown by an arrow 24 flows through the GTO S3. This current as indicated by arrow 24 is one which, like in the mode 1, builds up suddenly at a di/dt of about 100A/μs and a voltage as illustrated in Fig.8 is also induced at the GTO S3. In this instance like in the mode 1, such voltage induction leads to an increase of switching element damaging and, in some cases, leads to a breakdown of the switching elements which is undesirable.

Although there was a similar mode in a conventional two level inverter wherein a current begins to flow a GTO through which no current has been flown until then nevertheless an on signal is applied thereto, the current

variation was a slow one (di/dt of about 1A/μ s) which is determined by a load and there arises no such problems.

Fig. 10 shows a relationship between voltage Δ V induced at GTO due to incomplete on phenomenon and gate current provided thereto using di/dt of a current flowing through the GTO as a parameter. For a gate current 7A which is flown as a wide width gate forward current in a conventional gate driving circuit, no voltage is induced at the GTO with di/dt=1A/μ s as seen from Fig. 10, contrary thereto, with di/dt=100A/μ s a voltage of about 200V is induced at the GTO.

Summary of the Invention

According to the present invention there is provided a multi-series inverter arrangement comprising, a DC circuit (11, 12, 13) including a neutral point output terminal and a multi-series inverter including three arms (S1U~ S4U, S1V~ S4V, S1W~ S4W) each for U, V and W phases connected in parallel with said DC circuit, each arm including:

AUSTRALIA PATENT OFFICE

first, second, third and fourth switching elements (S1 ~ S4) connected in series, the mutual juncture point of said first and second switching elements (S1, S2) and the mutual juncture point of said third and fourth switching elements (S3, S4) are connected to the neutral point output terminal of said DC circuit via respective clamping diodes (CD1, CD2), and said first and third switching elements (S1, S3) and said second and fourth switching elements (S2, S4) are on and off controlled each other in a conjugate relationship;

flywheel diodes (D1~D4), each connected in parallel with said first, second, third and fourth switching elements (S1~S4);

snubber circuits (20, 20a, 20b) having a capacitor (25a, 25b) therein, each connected in parallel with said first, second, third and fourth switching elements (S1~S4); and

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individual gate driving circuits (E1, R1, R2, C, SW1, E1H, R2, SW1H, E1W, R1, SW1W, E2, SW2) for said first, second, third and fourth switching elements (S1~S4) for providing a gate current (IFG1, IFG2) thereto, characterized in that,

the gate current provided by said individual gate driving circuits for said second and third switching elements (S2, S3) is determined larger than that provided by said individual gate driving circuits for said first and fourth switching elements (S1, S4).

The invention also provides a multi-series inverter arrangement comprising, a DC circuit including serially connected n DC power sources (12, 13, 14) wherein said DC power source located at the most positive side is designated as a first DC power source (12) and (n+1) output terminals, and a multi-series inverter including a plurality of series connections of 2n switching elements (S1~S6) each connected in parallel with said DC circuit wherein the switching element located at the most positive side is designated as the first switching element (S1), a positive side terminal for said first DC power source (12) connected to the first switching element (S1), a negative side terminal for said nth DC power source (14) connected to the 2nth switching element (S6), an inverter output terminal connected

AUSTRALIA PATENT OFFICE

to a mutual juncture point of said nth and (n+1)th switching elements (S3, S4), (i+l)th output terminal for said DC circuit being connected to the mutual juncture point of the ith and (i+1)th switching elements (S1, S2; S2, S3) and the juncture point of the (n+i)th and (n+i+1)th switching elements (S4, S5; S5, S6) via respective clamping diodes (CD1, CD2; CD3, CD4) wherein i is from 1 to n−1, and said ith and (n+i)th switching elements (S1, S4; S2, S5; S3, S6) are on and off controlled in a conjugate relationship wherein i is from 1 to n characterized in that, among said 2n switching elements magnitude of the gate current (IFG1, IFG2) which is provided for said second switching element (S2) through said (2n−1)th switching element (S5) is determined larger than that of the gate current provided for said first and 2nth switching elements(S1, S6).

In the multi−series inverter arrangement according to the present invention having the constitution as shown in Fig. 1, magnitude of gate current to flow to the gates of GTOs to which an on signal is applied is selected larger for the GTOs S2 and S3 located inside than for the GTOs S1 and S4 located outside.

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In this instance, among the high gate drive forward current and the wide width gate forward current which flow through the gate of the GTO when an on signal is applied thereto from the gate driving circuit, the conventional magnitude of the wide width gate forward current of about 7A is increased, for example, up to about 20A and the increased wide width gate forward current is provided to the gate of the GTO to thereby prevent generation of an incomplete on phenomenon of the GTO.

Further, the GTO gate driving circuit is adapted to output the high gate drive forward current and the wide width gate forward current independently when an on signal is applied thereto, and every time when an incomplete on phenomenon is caused at a GTO, a high gate drive forward current is always provided to the GTO. A signal which causes the high gate drive forward current is formed based upon an output from means detecting the GTO voltage, means detecting gate current flowing through the GTO anode or means detecting the GTO main circuit current, or a logical combination of on signals applied to the respective GTOs.

PATENT OFFICE

Embodiments of the invention provide a wide width gate forward current or a high gate drive forward current which is large enough to turn on the GTOs as a GTO gate current a spreading of an on area within the GTO is hastened even when a current begins to flow suddenly through the GTO such that no high voltage is induced between the anode and the cathode of the GTO. Accordingly breakdown of the GTO is prevented.

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Brief Description of the Drawings

Fig. 1 is a constitutional diagram showing a main circuit of a multi-series inverter to which the present invention is applied;

Fig. 2 is a table indicating output voltages of the multi-series inverter depending upon on conditions of switching elements therein;

Fig. 3 is a gate current waveform of GTO in the multi-series inverter;

Fig. 4 is a diagram showing a conventional gate driving circuit for the multi-series inverter;

Fig. 5 is a constitutional diagram showing one phase

AUSTRALIA PATENT OFFICE

portion in the main circuit of the multi-series inverter ;

Fig.6 is a table indicating conditions of the multi-series inverter depending upon switching conditions of respective GTOs therein and changes of the conditions ;

Fig.7 is a diagram showing a load current flow in mode 1 in which an incomplete on phenomenon may be caused at GTO S2 ;

Fig.8 is voltage and current waveforms induced at GTO S2 when an incomplete on phenomenon is caused ;

Fig.9 is a diagram showing a load current flow in mode 2 in which an incomplete on phenomenon may be caused at GTO S3 ;

Fig.10 is a diagram showing a relationship between voltage induced at GTO due to an incomplete on phenomenon and gate current provided thereto ;

Fig.11 is gate current waveforms when an on signal is applied to respective GTOs according to one embodiment of the present invention ;

Fig.12 is a schematic diagram of an embodiment of gate driving circuits in the multi-series inverter arrangement according to the present invention which causes to flow a high gate drive forward current and a wide width gate forward current independently ;

Fig.13 is a schematic diagram of another embodiment of gate driving circuits in the multi-series inverter arrangement according to the present invention ;

Fig.14 is a schematic diagram of a still another

embodiment of gate driving circuits in the multi-series inverter arrangement according to the present invention ;

Fig.15 is a schematic diagram of a further embodiment of gate driving circuits in the multi-series inverter arrangement according to the present invention ;

Fig.16 is a schematic diagram of a still further embodiment of gate driving circuits in the multi-series inverter arrangement according to the present invention ;

Fig.17 is a constitutional diagram showing one phase portion in a main circuit of a multi-series inverter wherein six GTOs are connected in series in one arm to which the present invention is applied ; and

Fig.18 is a schematic diagram of an embodiment of multi-series inverter arrangement according to the present invention.

Detailed Description of the Embodiments

Hereinbelow, embodiments of the present invention is explained.

A first embodiment according to the present invention is explained with reference to Fig.5. In Fig.5, a GTO gate driving circuit having the same configuration as the conventional one as shown in Fig.4 is used. However, in the conventional gate driving circuit a wide width gate forward current IFG2, for example, of about 7A is usually provided for the GTOs S2 and S3 as well as the GTOs S1 and S4, contrary thereto,

the gate driving circuit of the present embodiment uses a large wide width gate forward current IFG2 of about 20A. In the gate driving circuit according to the present embodiment, the resistance of the resistor R1 shown in Fig.4 is selected small in comparison with the conventional one. As a result, a large wide width gate forward current IFG2 is provided for the GTOs S2 and S3. On the other hand, the conventional gate driving circuit is used for the GTOs S1 and S4. Fig.11 shows a difference of gate current waveforms for the GTOs S2 and S3 and for the GTOs S1 and S4. In the drawing, the solid line shows the gate current waveform for the GTOs S2 and S3, and the dotted line shows the gate current waveform for the GTOs S1 and S4. In the present embodiment, a gate current close to the high gate drive forward current is always flown through the GTOs S2 and S3 during the time when an on signal is applied to the GTOs as illustrated in Fig.11, therefore even if a current begins to flow suddenly through the GTOs, generation of an incomplete on phenomenon at the GTOs is prevented to maintain a normal operation of the GTOs.

In the present embodiment, an electrical power loss generated in the gate driving circuits is increased in association with the current increase flowing through the gates of the GTOs S2 and S3, however the present embodiment has a feature that a circuit having the same configuration as the conventional gate driving circuit

as shown in Fig.4 can be used.

Nextly, Fig.12 shows a second embodiment according to the present invention. The gate driving circuit shown in Fig.12 is adapted to provide the high gate drive forward current and the wide width gate forward current indenpendently. In Fig.12, R1 and R2 are resistors having the same functions as those in Fig.4, E1H is a power source for the high gate drive forward current, E1W is a power source for the wide width gate forward current, and E2 is a power source for turning off. In the present embodiment, a gate driving circuit which provideds the high gate drive forward current and the wide width gate forward current independently is used as the gate driving circuits for the GTOs S2 and S3 in the multi-series inverter. This gate driving circuit provides a wide width gate forward current when an on signal is applied and a switch SW1W is closed, and when a switch SW1H is closed a high gate drive forward current is provided. Accordingly, during the time when the switch SW1H is closed the high gate drive forward current can be always flown. The circuit as shown in Fig.4 is used for the GTOs S1 and S4.

In the present embodiment, it is necessary to separate the signal which causes the high gate drive forward current from the signal which causes the wide width gate forward current so that the gate driving circuit becomes complex in comparison with the circuit

shown in Fig.4, on one hand the large gate current can be flown only when it is required such that the present embodiment has a feature that an electrical power loss generated in the gate driving circuit can be decreased.

Now, as methods of preparing the high gate drive forward current signal which is caused only when a large gate current is necessitated, such methods are conceived as a method of obtaining a signal by detecting a voltage caused by the incomplete on phenomenon of the GTOs, a method of obtaining a signal by detecting a gate current flowing through the anode of the GTOs, a method of obtaining a signal by detecting initiation of current flow through the GTOs and a method of obtaining a signal from a logical combination of on signals provided for the respective GTOs. Hereinafter embodiments of these methods are explained.

Fig.13 shows a third embodiment according to the present invention. The circuit shown in Fig.13 is a gate driving circuit wherein a circuit for detecting a voltage at the GTO and a circuit for providing a signal to the switch SW1H are added to the circuit illustrated in Fig.12. The same on signal as that of the conventional one is applied as it is to the switch SW1W as the wide width gate forward current signal. For preparing a high gate drive forward current signal a voltage detector 31 and an AND operator 30 are introduced. The voltage detector 31 detects a voltage between the anode and

cathode of the GTO and generates a signal of "1" when a voltage is induced therebetween. The AND operator 30 generates a signal based upon AND operation of the signal of "1" from the voltage detector 31 and an on signal, and applies the same to the switch SW1H. As a result, the switch SW1H is closed and a high gate drive forward current is caused to flow through the GTO at an instance when an on signal is already applied and an incomplete on phenomenon is caused at the GTO as well as at an instance when the GTO is in an off condition and an on signal is applied thereto. Further, when the GTO is required to be turned off, an off signal is applied to the switch SW2.

With the present embodiment, even if an incomplete on phenomenon tends to be caused at the GTO, the phenomenon is eliminated to thereby prevent breakdown of the GTO.

Fig.14 shows a fourth embodiment according to the present invention. The circuit shown in Fig.14 is a gate driving circuit wherein a circuit composed of a resistor 32 and a diode 33 connected between the anode and gate of the GTO and a current detector 34 are provided for detecting an incomplete on phenomenon of the GTO, namely generation of a voltage thereat. Through the circuit to which the current detector 34 is provided a gate current flows during the time when the GTO is turned on, however when an incomplete on phenomenon is caused at the GTO,

the GTO is turned off, a voltage is generated between the anode and gate thereof and the flow of the gate current is suppressed. The current detector 34 detects the moment when the gate current is reduced to zero and outputs a signal of "1". The AND operator 30 performs AND operation of the signal of "1" from the current detector 34 and an on signal, and causes to close the switch SW1H. As a result, a high gate drive forward current is provided to the GTO. The other operations of the present embodiment are the same as those explained in connection with the third embodiment.

Fig.15 shows a fifth embodiment according to the present invention. The circuit shown in Fig.15 is a gate driving circuit wherein a current detector 35 is provided for detecting an anode current of the GTO. When an incomplete on phenomenon is caused at the GTO under a condition that an on signal is applied to the GTO and a wide width gate forward current is provided thereto via the switch SW1W, the current detector 35 detects that an anode current begins to flow and outputs a signal of "1". The AND operator 30 performs AND operation of the signal of "1" from the current detector 35 and an on signal and causes to close the switch SW1H. As a result, a high gate drive forward current is provided to the GTO. The other operations of the present embodiment are the same as those explained in connection with the third embodiment.

Fig.16 shows a sixth embodiment according to the present invention. The circuit shown in Fig.16 is a gate driving circuit wherein a high gate drive forward current is caused to flow when an on signal is applied both the GTOs S2 and S3 in view of the fact that an incomplete on phenomenon at the GTOs may be caused at the moment when both the GTOs S2 and S3 are turned on. In Fig.16, two gate driving circuits for the GTOs S2 and S3 are illustrated. A high gate drive forward current signal applied to the switch SW1H for causing a high gate drive forward current is provided at the moment when an on signal is applied to both the GTOs S2 and S3, which is detected by an AND operator 41 and an AND operator 45 respectively, by one shot multi-vibrators 43 and 46 via OR operators 44 and 45 until both the GTOs S2 and S3 are turned on. Further, in the circuit shown in Fig.16 at the moment when an on signal is applied only to the GTO S2 a high gate drive forward current signal is provided by the one shot multi-vibrator 42 via the OR operator 44 until the GTO S2 is turned on. The same is true with regard to the gate driving circuit for the GTO S3 through the members 47 and 48.

In the present embodiment, a high gate drive forward current may be provided even when no incomplete on phenomenon is caused, however no voltage or current detector for a main circuit is necessitated, the present embodiment is realized with a logic circuit using a low

voltage, it is a feature of the present embodiment that the circuit is easily realized in comparison with those of the third through fifth embodiments.

Hereinabove, examples of multi-series inverters wherein four GTOs are connected in series are explained, however in multi-series inverters wherein GTOs more than six are connected in series an incomplete on phenomenon is also caused. Fig.17 shows one phase portion in a main circuit of a multi-series inverter wherein six GTOs connected in series. The operation of the circuit illustrated in Fig.17 is explained in detail in JP-A-2-131370(1990), therefore explanation thereof is omitted here. Like in the circuit shown in Fig.5, in the circuit shown in Fig.17 an incomplete on phenomenon of the GTOs is caused under the following two instances, in that one is caused under a condition that the GTOs S1, S2 and S3 are in an on condition and a load current is flowing through the flywheel diodes D1, D2 and D3 when the GTO S1 is turned off and the GTO S4 is turned on, and the other is caused under a condition that the GTOs S4, S5 and S6 are in an on condition and a load current is flowing through the flywheel diodes D4, D5 and D6 when the GTO S6 is turned off and the GTO S3 is turned on. In case of the former instance an incomplete on phenomenon may be caused at the GTOs S2 and S3, and in the latter instance such phenomenon may be caused at the GTOs S4 and S5. Accordingly, by selecting a larger gate current for

the GTOs S2 through S5 than for the GTOs S1 and S6 such phenomenon is eliminated.

Further, in a multi-series inverter having more than eight serially connected GTOs for one arm such incomplete on phenomenon is likely eliminated by selecting a larger gate current for the GTOs other than the outer two GTOs.

Fig.18 shows seventh embodiment according to the present invention. In the circuit shown in Fig.18, the capacitance of snubber capacitors 25a and 25b in snubber circuits 20a and 20b which are respectively connected with the GTOs S2 and S3 is selected larger than that in a conventional circuit. Now, when an incomplete on phenomenon is caused at the GTO S2 or S3 a current is bypassed toward a snubber capacitor 25a in the snubber circuit 20a or a snubber capacitor 25b in the snubber circuit 20b and a voltage induced at the GTOs is suppressed. Herein the capacitance of the snubber capacitors 25a and 25b is determined at such a magnitude that the voltage induced at the GTOs is suppressed below a voltage which never breaks-down the GTOs.

By increasing the capacitance of the snubber capacitor in such a manner that the voltage induced at the GTOs is reduced sufficiently small, breakdown of GTOs due to the incomplete on phenomenon is prevented without any modification of the conventional gate signal and gate driving current.

In the above embodiments, multi-series inverters

using GTOs are exemplified, however in multi-series inverters using other switching elements such as transistors in place of the GTOs, substantially the same advantages can be obtained by increasing the gate current (in case of transistors the base current) in the same manner as explained. Further, when voltage drive type elements such as MOSFETs and IGBTs are used for the multi-series inverters, substantially the same advantages can be also obtained by increasing the gate voltage in the same manner as explained.

As explained above, in the multi-series inverter according to the present invention, even if a current begins to flow suddenly through a GTO to which an on signal is already applied but through which no current flows until then, no incomplete on phenomenon is caused at the GTO and the GTO continues to operate normally. Further, since the incomplete on phenomenon of the GTO is eliminated, breakdown of the GTO is prevented.

The reference numerals in the following claims do not in any way limit the scope of the respective claims.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A multi-series inverter arrangement comprising, a DC circuit (11, 12, 13) including a neutral point output terminal and a multi-series inverter including three arms (S1U~S4U, S1V~S4V, S1W~S4W) each for U, V and W phases connected in parallel with said DC circuit, each arm including :

first, second, third and fourth switching elements (S1 ~S4) connected in series, the mutual juncture point of said first and second switching elements (S1, S2) and the mutual juncture point of said third and fourth switching elements (S3, S4) are connected to the neutral point output terminal of said DC circuit via respective clamping diodes (CD1, CD2), and said first and third switching elements (S1, S3) and said second and fourth switching elements (S2, S4) are on and off controlled each other in a conjugate relationship ;

flywheel diodes (D1~D4), each connected in parallel with said first, second, third and fourth switching elements (S1~S4) ;

snubber circuits (20, 20a, 20b) having a capacitor (25a, 25b) therein, each connected in parallel with said first, second, third and fourth switching elements (S1~S4) ; and

individual gate driving circuits (E1, R1, R2, C, SW1, E1H, R2, SW1H, E1W, R1, SW1W, E2, SW2) for said first, second, third and fourth switching elements (S1~

S4) for providing a gate current (IFG1, IFG2) thereto,

characterized in that,

the gate current provided by said individual gate driving circuits for said second and third switching elements (S2, S3) is determined larger than that provided by said individual gate driving circuits for said first and fourth switching elements (S1, S4).

2. A multi-series inverter arrangement according to claim 1, wherein among the gate current including a high gate drive forward current (IFG1) and a wide width gate forward current (IFG2) the magnitude of the wide width gate forward current (IFG2) provided by said individual gate driving circuits for said second and third switching elements (S2, S3) is determined larger than that provided by said individual gate driving circuit for said first and fourth switching elements (S1, S4).

3. A multi-series inverter arrangement according to claim 1, wherein the gate current includes a high gate drive forward current (IFG1) and a wide width gate forward current (IFG2) following thereto, and said individual gate driving circuits for said second and third switching elements (S2, S3), each includes a first gate driving circuit (E1H, R2, SW1H) for providing the high gate drive forward current (IFG1), a second gate driving circuit (E1W, R1, SW1W) for providing the wide

width gate forward current (IFG2) and means (30, 31, 32, 33, 34, 35, 41～48) for detecting tendency of an incomplete on phenomenon at the corresponding switching element, said first gate driving circuit (E1H, R2, SW1H) is activated when a turn on signal for the corresponding switching element is received or when said detecting means detects the tendency of an incomplete on phenomenon at the corresponding switching element and said second gate driving circuit (E1W, R1, SW1W) is activated when the turn on signal for the corresponding switching element is received.

4. A multi-series inverter arrangement according to claim 3, wherein said detecting means (30, 31) determines a tendency of an incomplete on phenomenon at the corresponding switching element when a predetermined voltage between the anode and gate of the corresponding switching element is detected.

5. A multi-series inverter arrangement according to claim 3, wherein said detecting means (30, 32 ～34) determines a tendency of an incomplete on phenomenon at the corresponding switching element when a current between the anode and gate of the corresponding switching element is reduced to zero.

6. A multi-series inverter arrangement according to

claim 3, wherein said detecting means (30, 35) determines a tendency of an incomplete on phenomenon at the corresponding switching element when a predetermined current begins to flow through the corresponding switching element.

7. A multi-series inverter arrangement according to claim 3, wherein said detecting means (41 ~ 48) determines a tendency of an incomplete on phenomenon at the corresponding switching element when both turn on signals for second and third switching elements are received.

8. A multi-series inverter arrangement comprising, a DC circuit (11, 12, 13) including a neutral point output terminal and a multi-series inverter including three arms (S1U~ S4U, S1V~ S4V, S1W~ S4W) each for U, V and W phases connected in parallel with said DC circuit, each arm including :

first, second, third and fourth switching elements (S1 ~ S4) connected in series, the mutual juncture point of said first and second switching elements (S1, S2) and the mutual juncture point of said third and fourth switching elements (S3, S4) are connected to the neutral point output terminal of said DC circuit via respective clamping diodes (CD1, CD2), and said first and third switching elements (S1, S3) and said second and fourth

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switching elements (S2, S4) are on and off controlled each other in a conjugate relationship ;

flywheel diodes (D1~ D4), each connected in parallel with said first, second, third and fourth switching elements (S1~ S4) ;

snubber circuits (20, 20a, 20b) having a capacitor (25a, 25b) therein, each connected in parallel with said first, second, third and fourth switching elements (S1~ S4) ; and

individual gate driving circuits (E1, R1, R2, C, SW1, E1H, R2, SW1H, E1W, R1, SW1W, E2, SW2) for said first, second, third and fourth switching elements (S1~ S4) for providing a gate current (IFG1, IFG2) thereto,

characterized in that,

the capacitance of the capacitor (25a, 25b) in said snubber circuit (20a, 20b) for each of said second and third switching elements (S2, S3) is determined at such an amount that a voltage induced across said corresponding switching element when an incomplete on phenomenon is caused thereat is limited below a predetermined voltage which never breaks down the corresponding switching element.

8 8. A multi-series inverter arrangement comprising, a DC circuit including serially connected n DC power sources (12, 13, 14) wherein said DC power source located at the most positive side is designated as a first DC

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power source (12) and (n+1) output terminals, and a multi-series inverter including a plurality of series connections of 2n switching elements (S1～S6) each connected in parallel with said DC circuit wherein the switching element located at the most positive side is desgnated as the first switching element (S1), a positive side terminal for said first DC power source (12) connected to the first switching element (S1), a negative side terminal for said nth DC power source (14) connected to the 2nth switching element (S6), an inverter output terminal connected to a mutual juncture point of said nth and (n+1)th switching elements (S3, S4), (i+1)th output terminal for said DC circuit being connected to the mutual juncture point of the ith and (i+1)th switching elements (S1, S2 ; S2, S3) and the juncture point of the (n+i)th and (n+i+1)th switching elements (S4, S5 ; S5, S6) via respective clamping diodes (CD1, CD2 ; CD3, CD4) wherein i is from 1 to n-1, and said ith and (n+i)th switching elements (S1, S4 ; S2, S5 ; S3, S6) are on and off controlled in a conjugate relationship wherein i is from 1 to n characterized in that, among said 2n switching elements magnitude of the gate current (IFG1, IFG2) which is provided for said second switching element (S2) through said (2n-1)th switching element (S5) is determined larger than that of the gate current provided for said first and 2nth switching elements (S1, S6).

9

~~10.~~ A multi-series inverter arrangement substantially as hereinbefore described with reference to the drawings.

~~11. The steps, features, compositions and compounds disclosed herein or referred to or indicated in the specification and/or claims of this application, individually or collectively, and any and all combinations of any two or more of said steps or features.~~

DATED this ELEVENTH day of FEBRUARY 1993

Hitachi, Ltd.

by DAVIES COLLISON CAVE
Patent Attorneys for the applicant(s)

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Abstract

A multi-series inverter arrangement

In a multi-series inverter arrangement comprising a DC circuit (11, 12, 13) including a neutral point output terminal and a multi-series inverter including three series connections of first through fourth GTOs (S1, S2, S3, S4), each connected in parallel with the DC circuit, the juncture of the first and second GTOs (S1, S2) and the juncture of the third and fourth (S3, S4) GTOs being connected to the neutral point output terminal via respective clamping diodes (CD1, CD2) and the first and third GTOs (S1, S3) and the second and fourth GTOs (S2, S4) being on and off controlled each other in a conjugate relationship, individual gate driving circuits (E1H, R2, SW1H, E1W, R1, SW1W) for the second and third GTOs (S2, S3) being designed to provide a larger gate current (IFG1, IFG2), in particular, a larger wide width gate forward current (IFG2) to the corresponding GTOs (S2, S3) than that provided by individual gate driving circuits (E1, R1, R2, C, SW1) for the first and fourth GTOs (S1, S4) to the corresponding GTOs (S1, S4).

Fig. 11

11 02 93 32995

FIG. 1

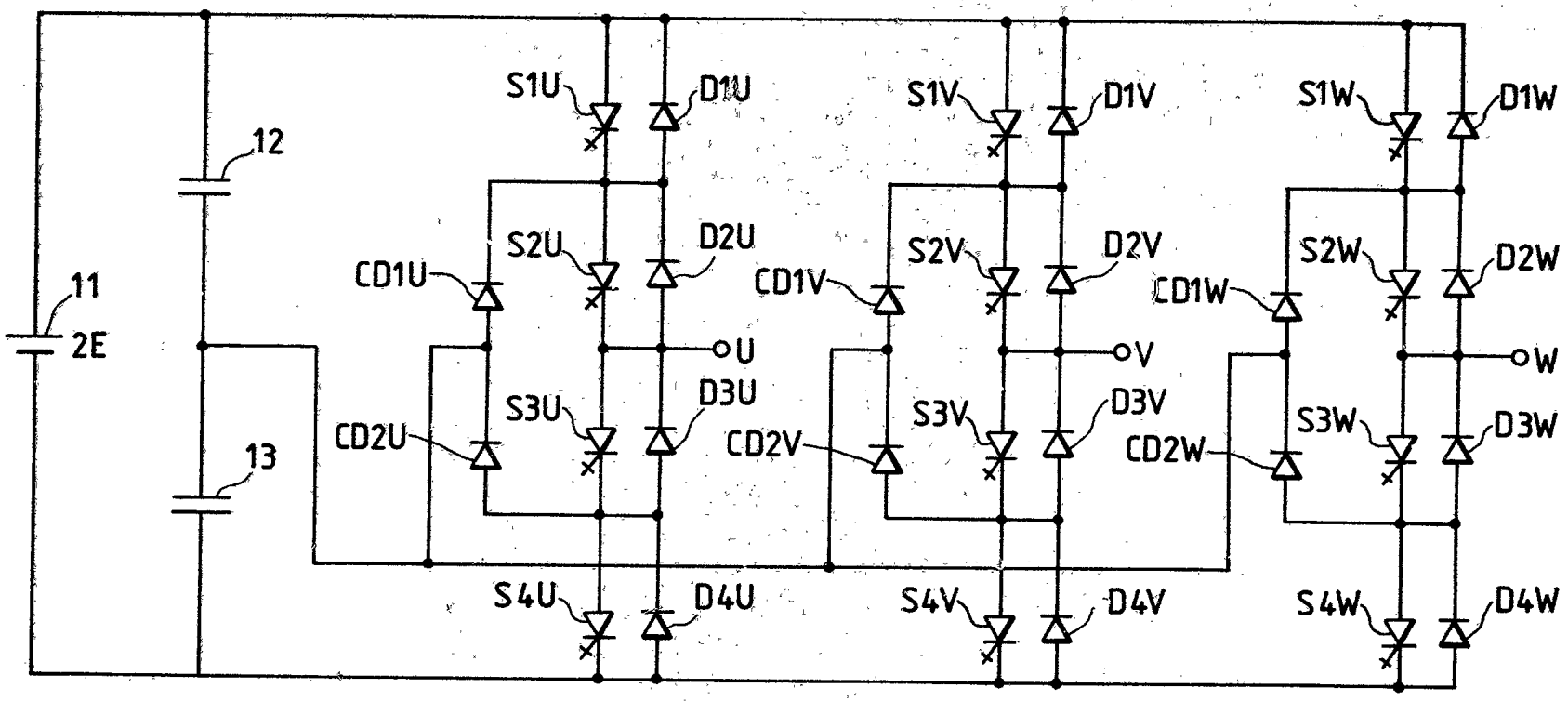


FIG. 2

	S1 ON	S3 ON
S2 ON	+E	0
S4 ON	INHIBITED	-E

FIG. 3

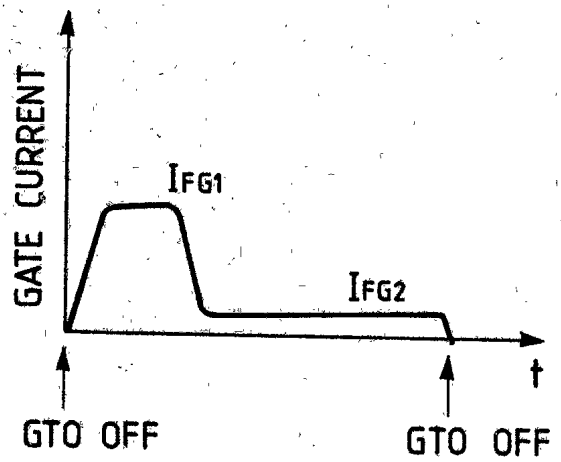


FIG. 4

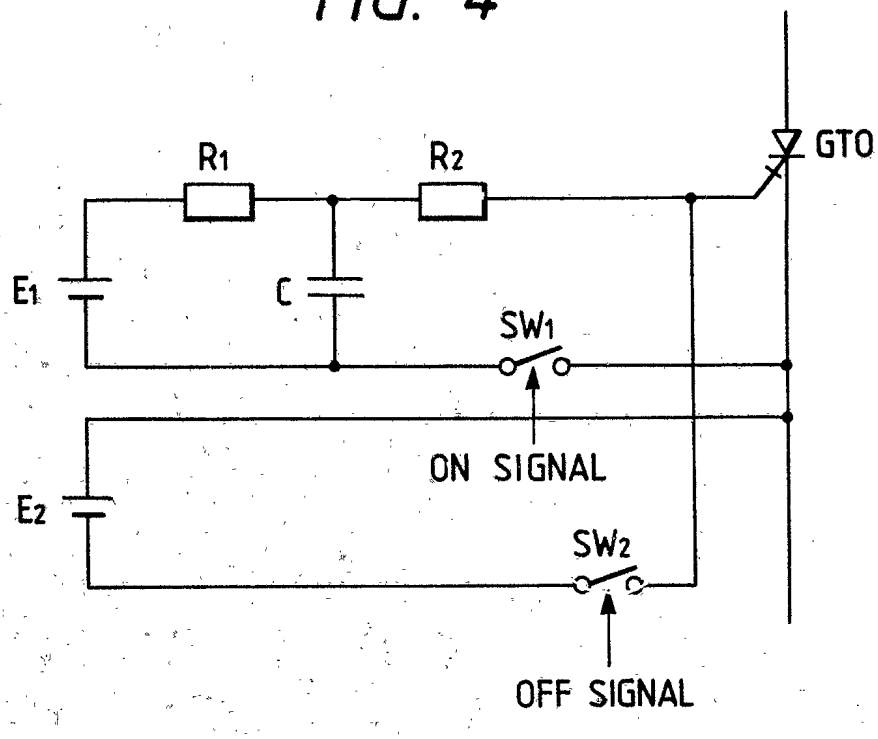

R1
R2
GTO
E1
C
SW1
ON SIGNAL
E2
SW2
OFF SIGNAL

FIG. 5

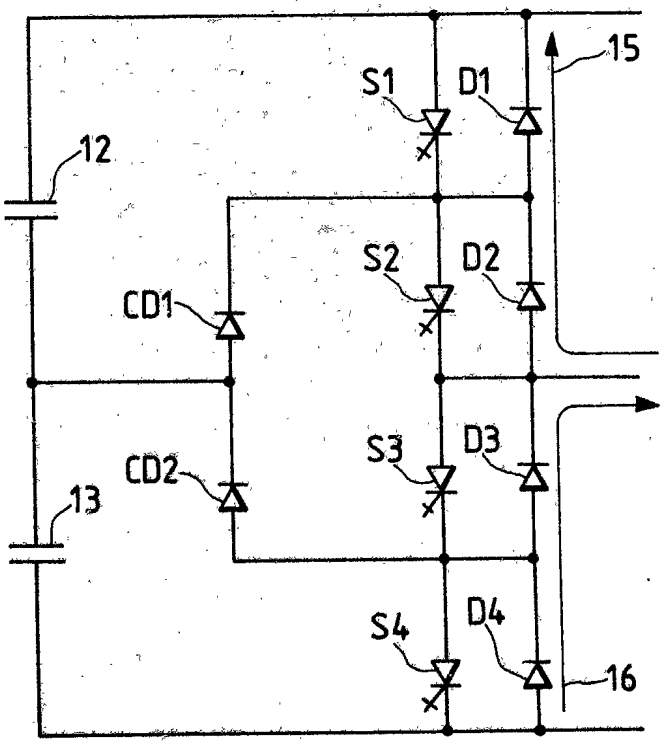

15
S1
D1
12
S2
D2
CD1
S3
D3
CD2
13
S4
D4
16

FIG. 6

S1	OFF	ON	OFF	OFF	OFF
S2	ON	ON	ON	OFF	ON
S3	ON	OFF	ON	ON	ON
S4	OFF	OFF	OFF	ON	OFF
OUTPUT VOLTAGE	0	E	0	-E	0
SWITCHING CONDITION	(1)	(2)	(1)	(3)	(1)
CHANGE OF SWITCHING CONDITION	①	②	③	④	

FIG. 7

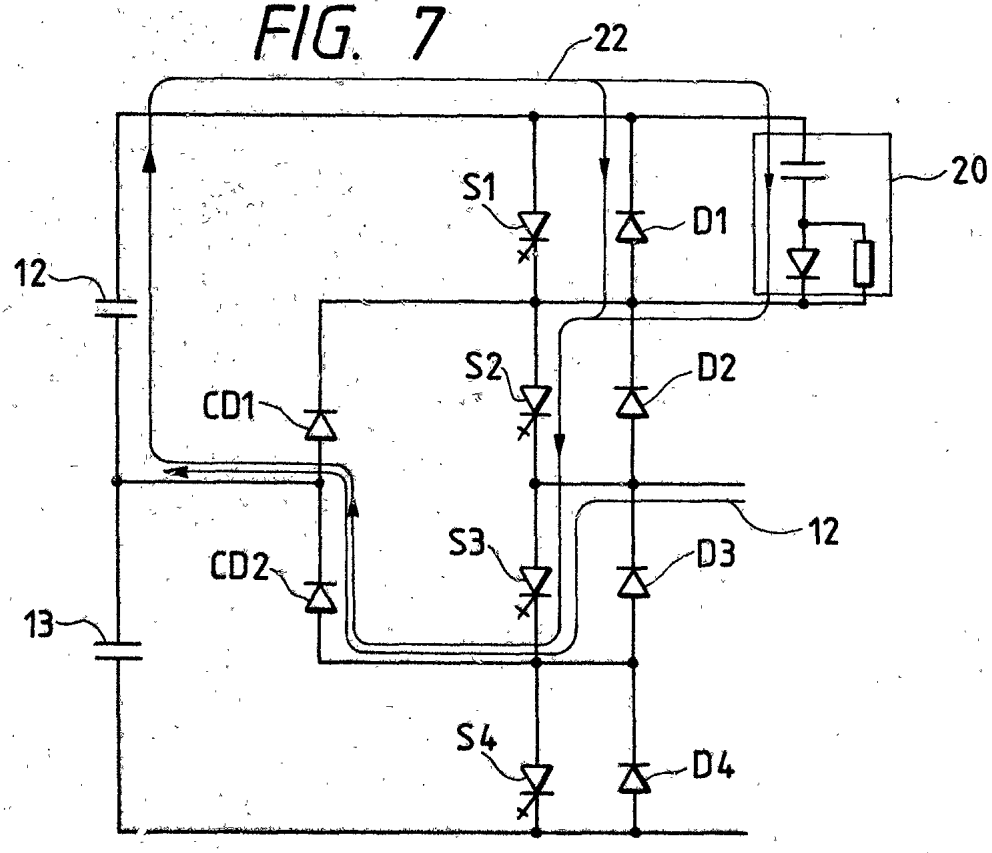


FIG. 8

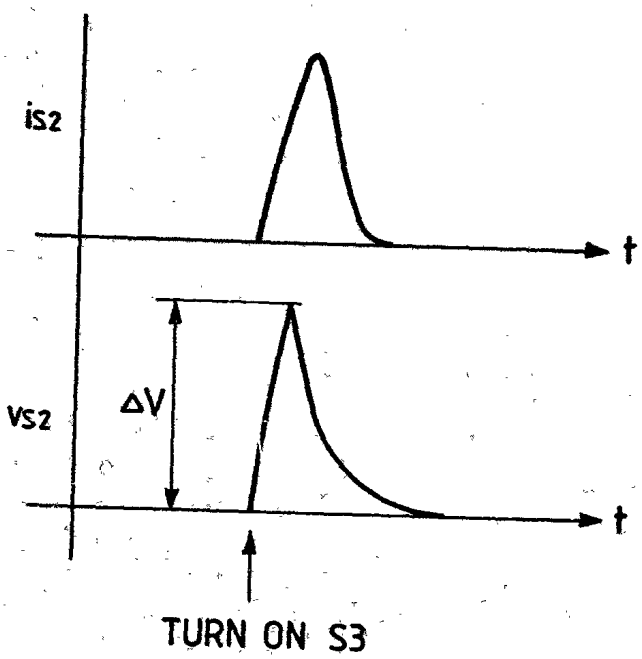

iS2
t
VS2
ΔV
t
TURN ON S3

FIG. 9

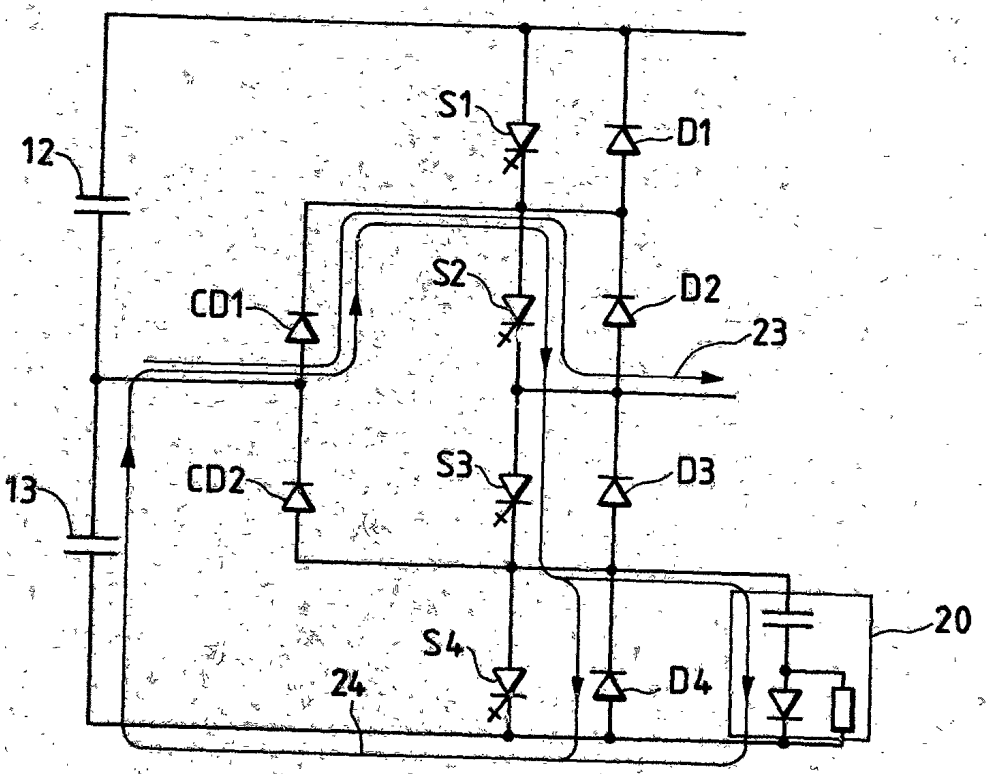

S1
D1
12
CD1
S2
D2
23
13
CD2
S3
D3
20
S4
24
D4

FIG. 10

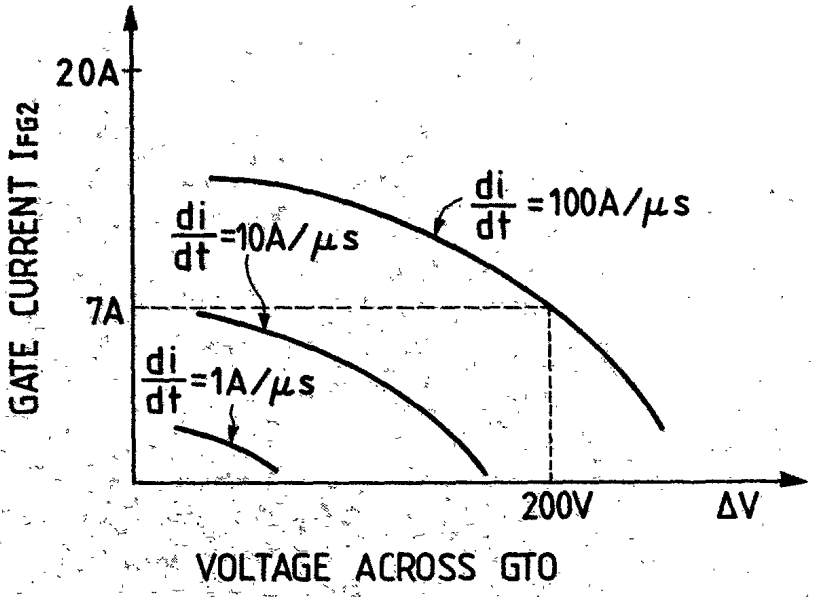

20A
GATE CURRENT IFG2
di/dt =100A/μs
di/dt =10A/μs
7A
di/dt =1A/μs
200V
ΔV
VOLTAGE ACROSS GTO

FIG. 11

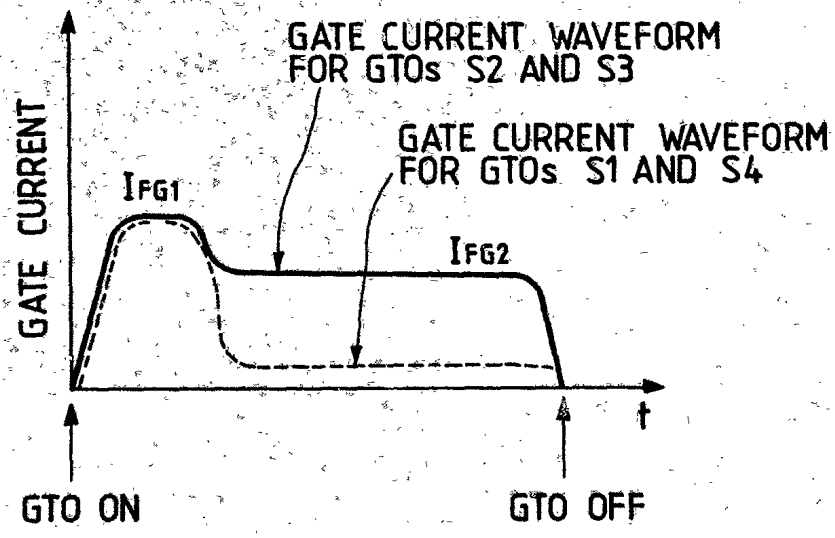

GATE CURRENT WAVEFORM
FOR GTOs S2 AND S3
GATE CURRENT WAVEFORM
FOR GTOs S1 AND S4
GATE CURRENT
IFG1
IFG2
t
GTO ON
GTO OFF

FIG. 12

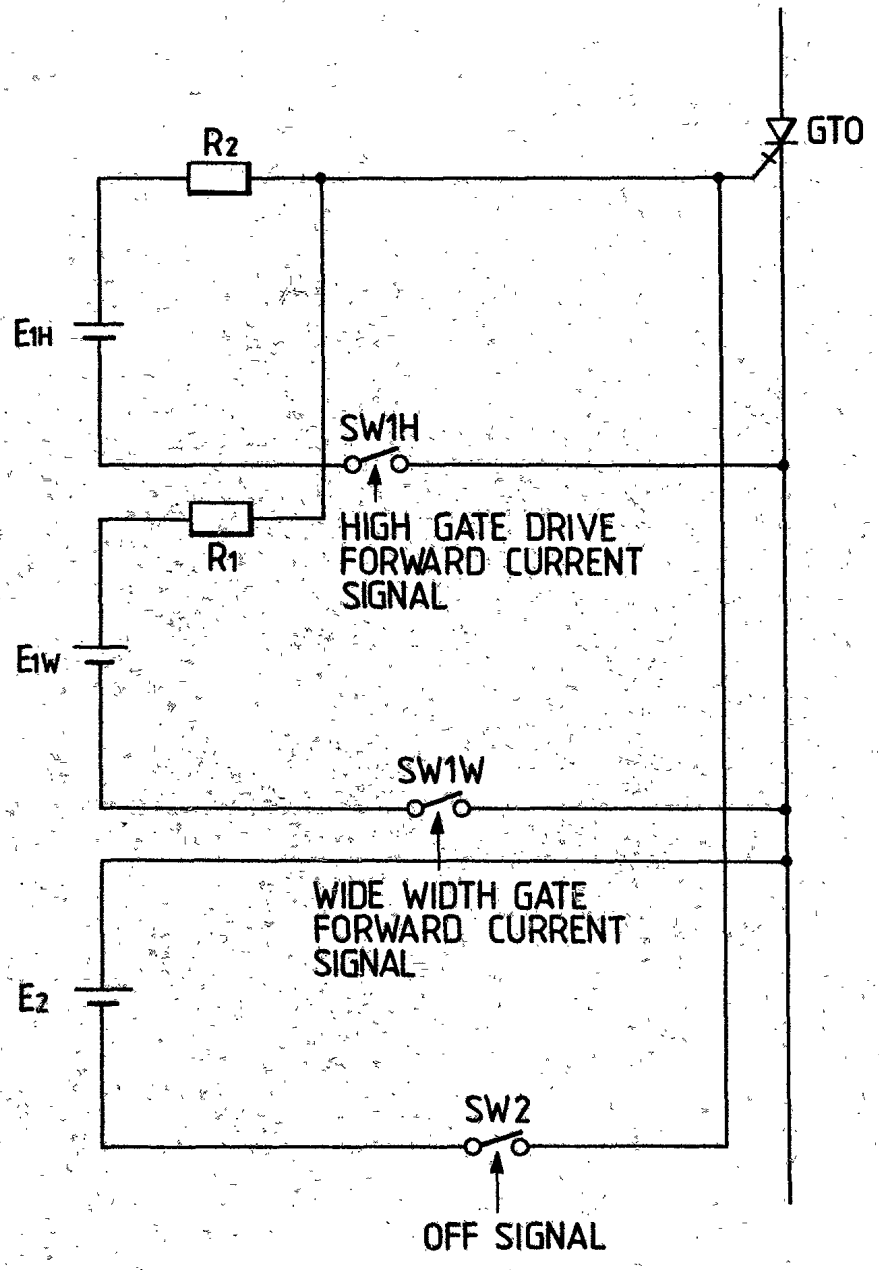

GTO
R2
E1H
SW1H
HIGH GATE DRIVE
FORWARD CURRENT
SIGNAL
R1
E1W
SW1W
WIDE WIDTH GATE
FORWARD CURRENT
SIGNAL
E2
SW2
OFF SIGNAL

FIG. 13

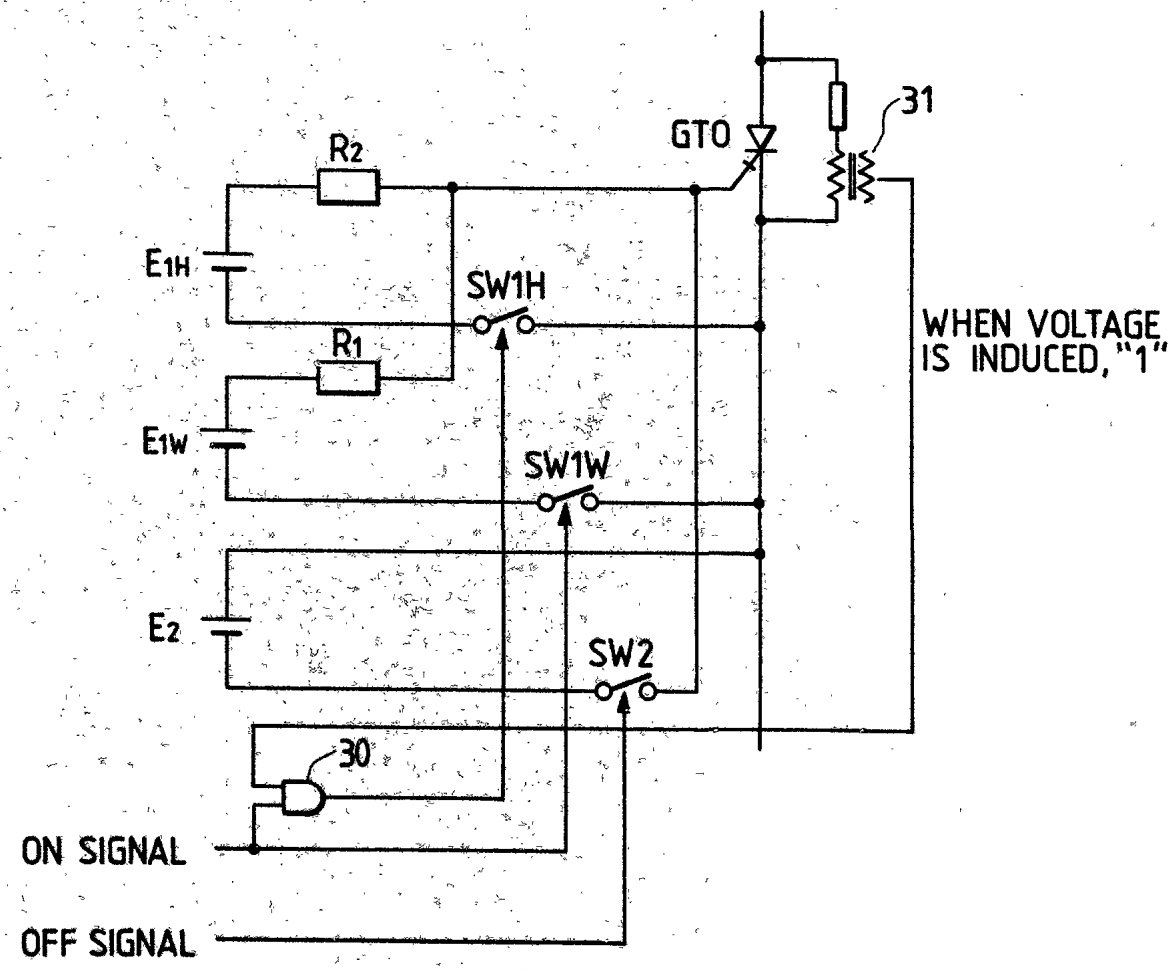

R2
E1H
SW1H
R1
E1W
SW1W
E2
SW2
30
ON SIGNAL
OFF SIGNAL
GTO
31
WHEN VOLTAGE IS INDUCED, "1"

FIG. 14

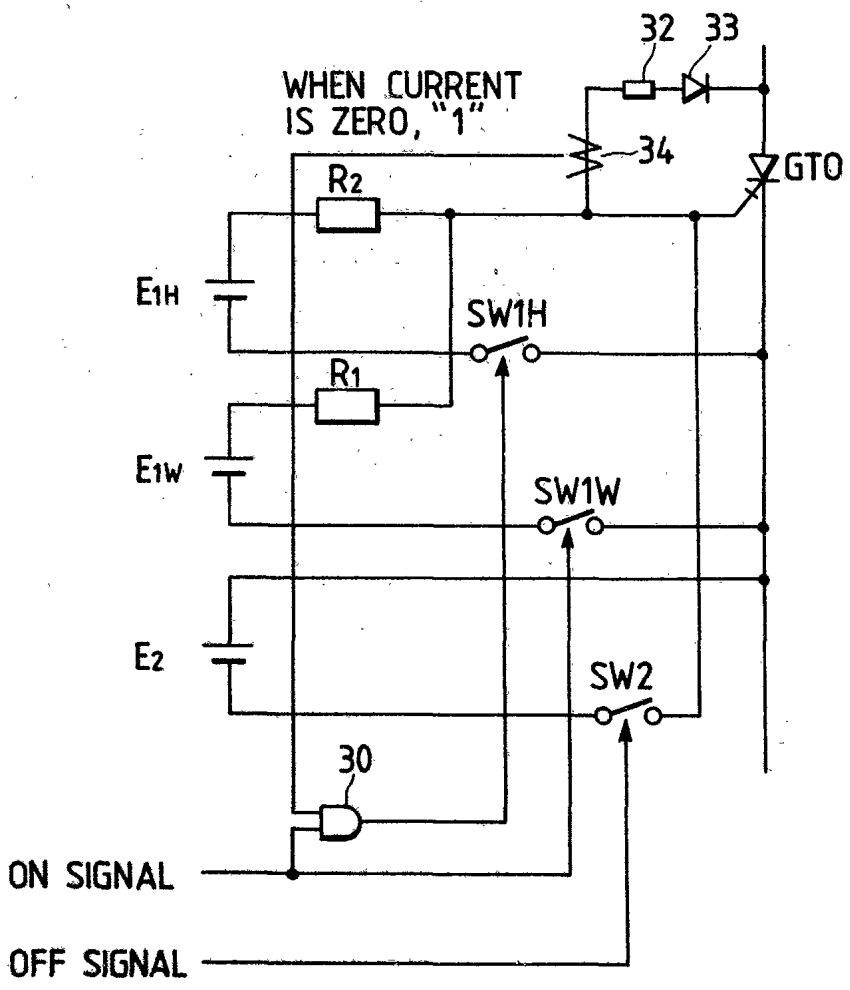

32
33
WHEN CURRENT
IS ZERO, "1"
34
GTO
R2
E1H
SW1H
R1
E1W
SW1W
E2
SW2
30
ON SIGNAL
OFF SIGNAL

FIG. 15

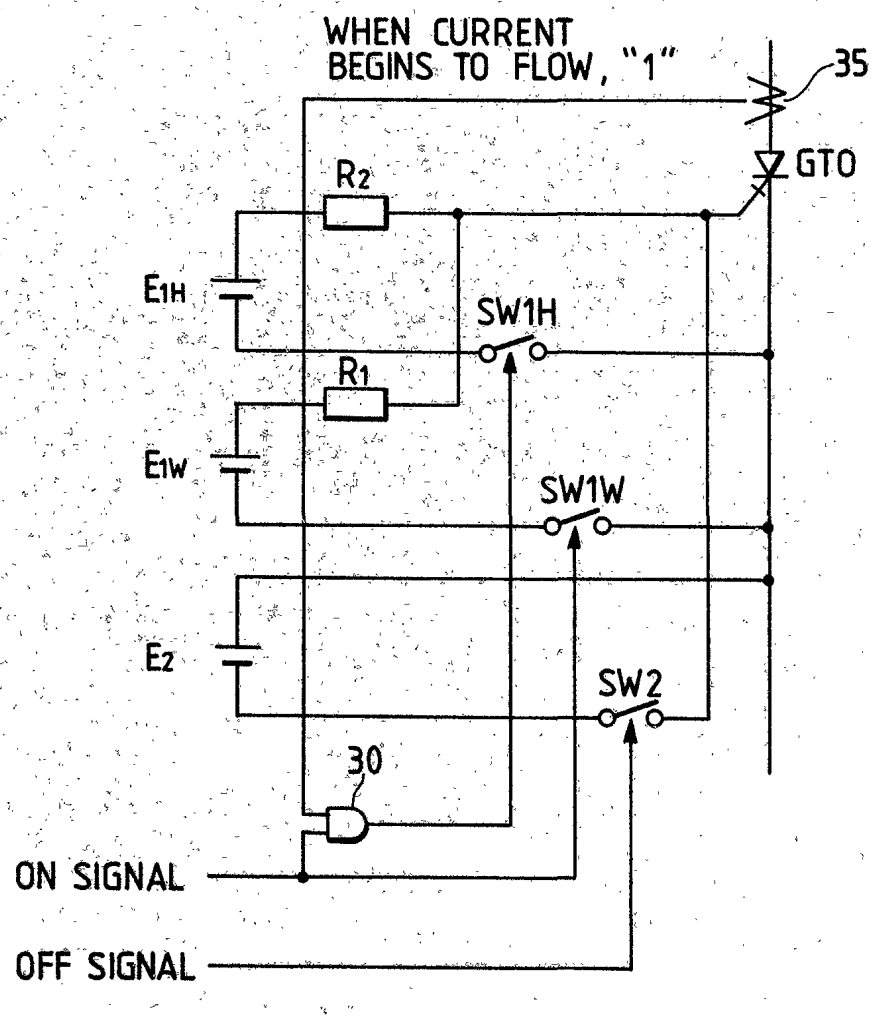

WHEN CURRENT
BEGINS TO FLOW, "1"
35
GTO
R2
E1H
SW1H
R1
E1W
SW1W
E2
SW2
30
ON SIGNAL
OFF SIGNAL

FIG. 16

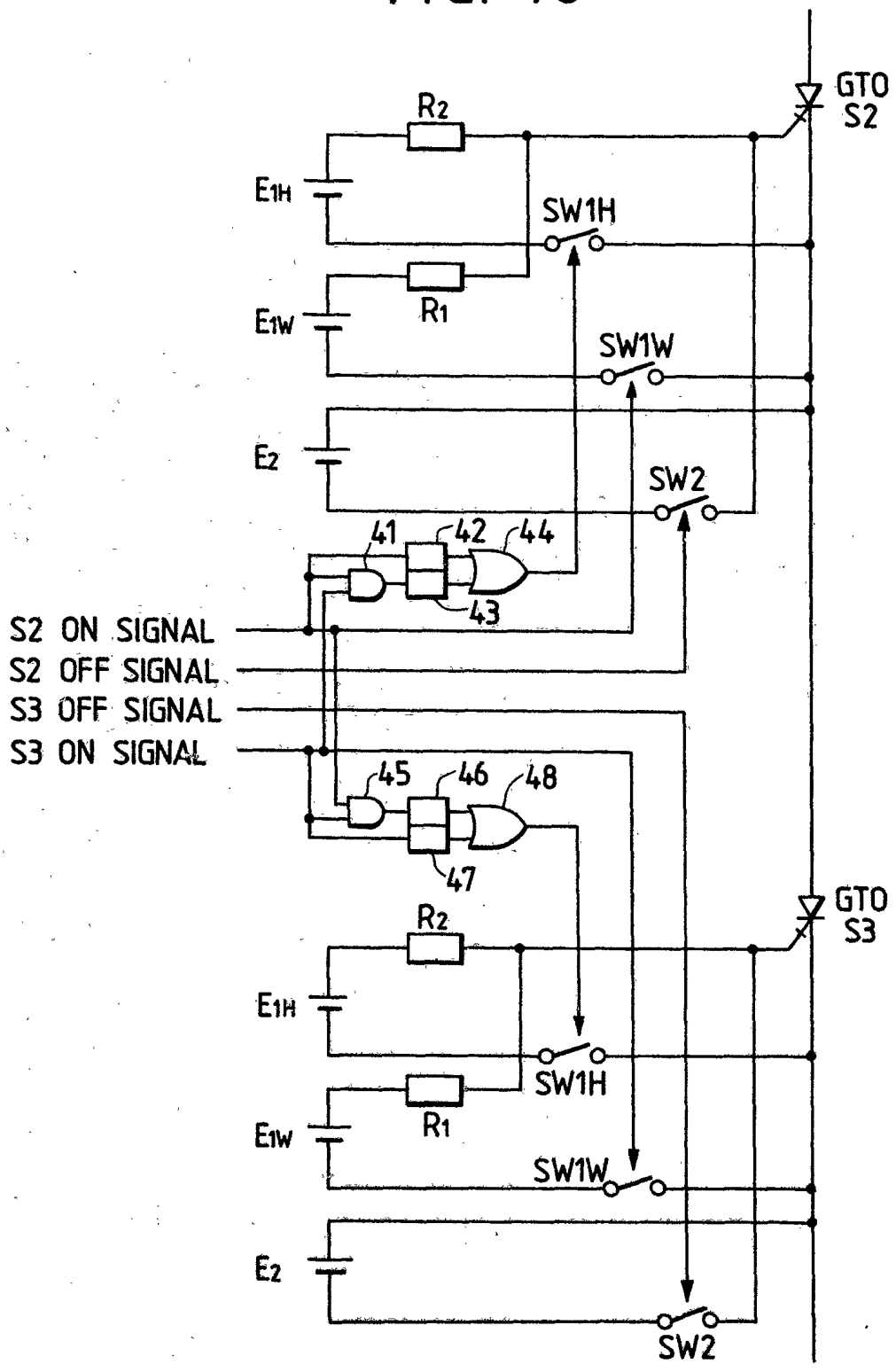

GTO
S2
R2
E1H
SW1H
R1
E1W
SW1W
E2
SW2
41
42
44
43
S2 ON SIGNAL
S2 OFF SIGNAL
S3 OFF SIGNAL
S3 ON SIGNAL
45
46
48
47
GTO
S3
R2
E1H
SW1H
R1
E1W
SW1W
E2
SW2

FIG. 17

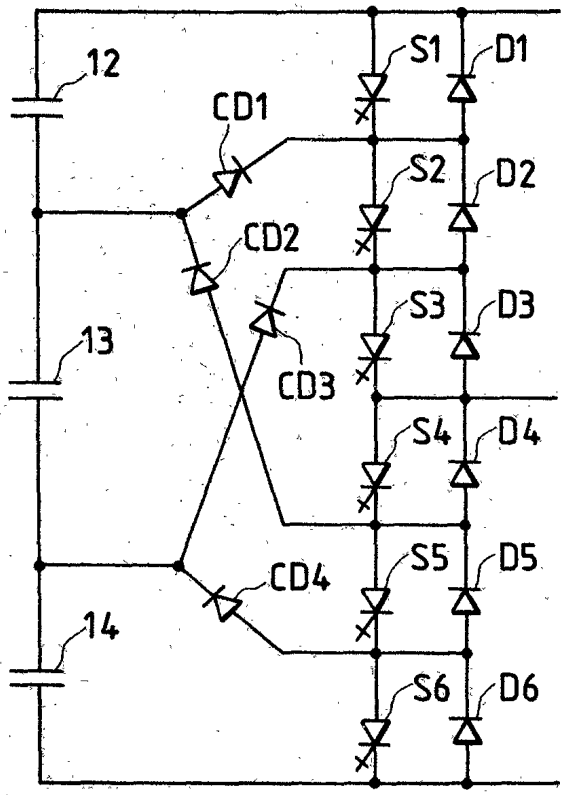
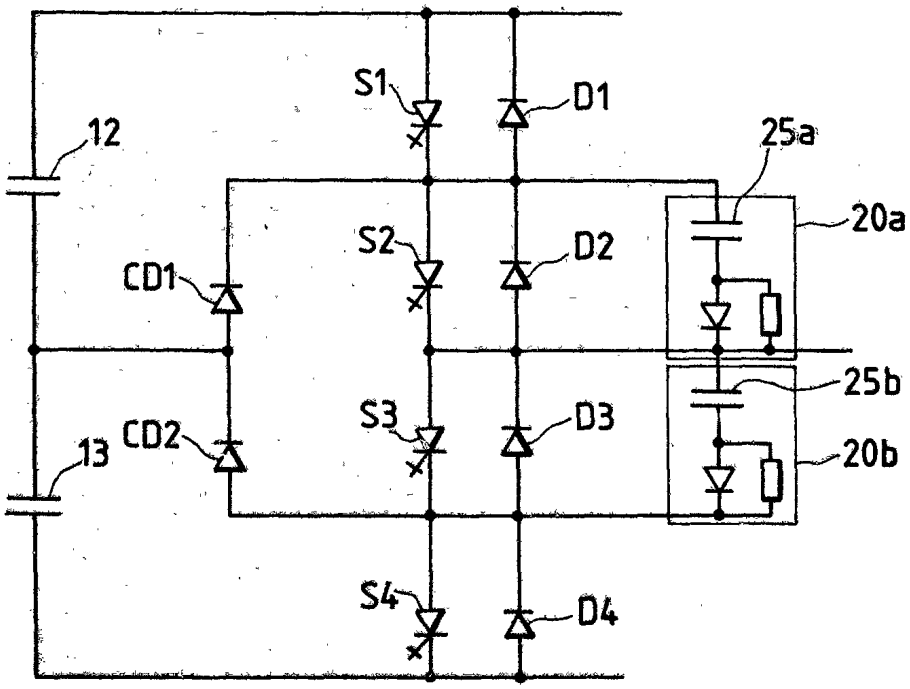

12
13
14
CD1
CD2
CD3
CD4
S1
S2
S3
S4
S5
S6
D1
D2
D3
D4
D5
D6

FIG. 18


12
13
CD1
CD2
S1
S2
S3
S4
D1
D2
D3
D4
25a
20a
25b
20b