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(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) Inventors: **THEN, Han Wui**; 4191 N.W. 127th Avenue, Portland, Oregon 97229 (US). **DASGUPTA, Sansaptak**; 132 N.E. Greenridge Terrace, Hillsboro, Oregon 97124 (US). **RADOSAVLJEVIC, Marko**; 3684 N.W. Loriann, Portland, Oregon 97229 (US).

(74) Agent: **NOEL, Samuel J.** et al.; LOWENSTEIN SANDLER LLP, 65 Livingston Avenue, Roseland, New Jersey 07068 (US).

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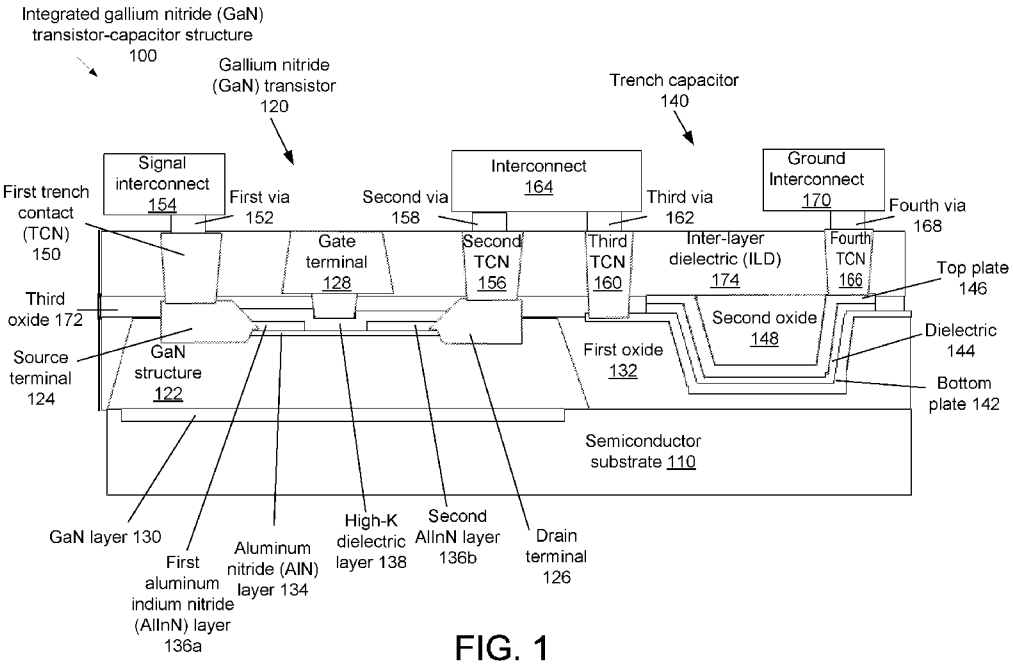

FIG. 1

(57) Abstract: A switch capacitor bank structure, an integrated circuit die, and a method of fabricating the switch capacitor bank are disclosed. The switch capacitor bank structure includes a plurality of gallium nitride (GaN) transistors on a semiconductor substrate and one or more trench capacitors above the semiconductor substrate. Each of the trench capacitors is located between and is coupled to at least a first corresponding GaN transistor and a second corresponding GaN transistor of the plurality of GaN transistors. The first corresponding GaN transistor and a first trench capacitor of the one or more trench capacitors are coupled to a first interconnect. The second corresponding GaN transistor and the first trench capacitor are coupled to a second interconnect. The first interconnect and the second interconnect are coupled.

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INTEGRATED GALLIUM NITRIDE CAPACITOR-TRANSISTOR STRUCTURES

Background

[0001] User devices may include components such as an antenna and a transistor. The transistor (e.g., a power amplifier) transmits a signal to the antenna and the antenna transmits the signal to another user device. The antenna is designed to transmit signals that are within an impedance range (e.g., 30-50 Ohms). If the transistor transmits a signal to the antenna within the impedance range of the antenna (i.e., matched condition), the radio frequency (RF) power of the signal is radiated to air via the antenna. If the transistor transmits a signal to the antenna at a value outside of the impedance range (e.g., lower than the impedance range, 1-2 Ohms), the antenna does not radiate and does not transmit the signal to the other user device. Instead, the RF power for transmission of the signal returns to the transistor (e.g., signal reflection) as wasted power (e.g., 0.5-2 Watts) and is discharged as heat. Such a scenario may also result in the degradation of the transistor and impairment of reliability. The user device may continue attempting to transmit the signal to the other user device (and discharging heat) until the impedance of the signal is within the impedance range of the antenna, resulting is wasting much power as heat and quickly draining the battery.

Brief Description of the Drawings

[0002] The present disclosure described herein is illustrated by way of example and not by way of limitation in the accompanying figures. For simplicity and clarity of illustration, features illustrated in the figures are not necessarily drawn to scale. For example, the dimensions of some features may be exaggerated relative to other features for clarity. Further, where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements.

[0003] FIG. 1 illustrates an integrated gallium nitride (GaN) transistor-capacitor structure, according to an implementation of the present disclosure.

[0004] FIG. 2 illustrates a switch capacitor bank including integrated GaN transistor-capacitor structures, according to an implementation of the present disclosure.

[0005] FIG. 3 illustrates a process flow for fabricating a switch capacitor bank, according to an implementation of the present disclosure.

[0006] FIG. 4 is a computing device built in accordance with an implementation of the present disclosure.

Detailed Description

[0007] In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present disclosure may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0008] Electrical impedance is the measure of the opposition that a circuit presents to a current when a voltage is applied (e.g., voltage divided by current). Impedance of a user device may vary according to the instantaneous voltage, the instant current, and placement of the user device. For example, a user device in a clothes pocket (e.g., pants pocket, jacket pocket) will have different impedance than a user device placed on a metal surface of an automobile. In another example, when there is a current surge, the resulting impedance can be outside of an impedance range of a component (e.g., antenna) of a user device; a situation also referred to as an unmatched condition.

[0009] One or more capacitors can be used for impedance tuning and matching. One or more capacitors can draw away current during a current surge and transmit a lower current to a component (e.g., the antenna) so that the impedance (e.g., instant voltage over instant current) at the component is within the impedance range of the component. In another example, an antenna may attempt to transmit a signal until the signal is transmitted and each attempt may occur over part of a duration of a cycle of signal oscillation. In the first part of the cycle, the RF power for signal transmission may be transmitted to the one or more capacitors and the energy may be temporarily stored in the capacitor (e.g., instead of returning to the transistor). During the ensuing part of the cycle, the capacitor may then release the stored energy and send the stored energy to the antenna instead of returning the stored energy to the transistor (e.g., so that the signal can be transmitted by an antenna). By doing so, the capacitor effectively tunes and matches the impedance of the antenna to the transistor, hence preventing energy from being returned to the transistor and being dissipated as heat.

[0010] Fixed impedance matching strategy in monolithic microwave integrated circuits results in losses in RF power (e.g., as much as 50-60%, 3-4 decibels (dB)) under unmatched conditions. Because the impedance of the antenna varies depending on its surroundings (e.g., impedance of a smartphone in a pocket differs from impedance of the smartphone on a car), the antenna may only

be matched to the transistor only under a small number of scenarios. Impedance tuning techniques using silicon (Si) n-type metal-oxide-semiconductor (nMOS) or gallium arsenide (GaAs) high-electron-mobility transistor (HEMT) incur a large footprint and high capacitance which results in parasitic losses that negate any gain (e.g., zero sum gain).

[0011] The present disclosure addresses the above-mentioned and other deficiencies by using integrated GaN transistor-capacitor structures to form a switch capacitor bank. GaN transistors are much smaller (e.g., five times smaller than GaAs HEMT, 12 times smaller than Si MOSFET) which causes GaN transistor capacitance to be small and parasitic losses to be small which allows low loss impedance tuning. The integrated GaN transistor-capacitor structures may be integrated high voltage GaN capacitor-transistor structures that can be used to dynamically vary the amount of capacitance required for impedance tuning and matching in varying use scenarios.

[0012] In one implementation, a switch capacitor bank structure includes gallium nitride (GaN) transistors on a semiconductor substrate and one or more trench capacitors above the semiconductor substrate, where each of the trench capacitors is electrically coupled to at least one GaN transistor on one end and electrically coupled to a ground node on the other end. The source of the GaN transistor is electrically coupled to the signal interconnect, the drain terminal of the GaN transistor is electrically coupled to the trench capacitor, and the gate terminal of the GaN transistor is electrically coupled to a switch interconnect. Depending on the amount of capacitance required to achieve a matched condition in each varying use scenario, the GaN transistors, acting as switches, may be turned on (i.e., switch interconnect is biased supplying a gate voltage above transistor threshold voltage) to electrically couple more capacitors to the signal (e.g., via one or more interconnects), or may be turned off (i.e., switch interconnect is supplying a gate voltage below transistor threshold voltage) to electrically decouple more capacitors from the signal (e.g., via one or more interconnects).

[0013] **FIG. 1** illustrates an integrated GaN transistor-capacitor structure 100 (e.g., an integrated circuit die), according to an implementation. The integrated GaN transistor-capacitor structure 100 includes a GaN transistor 120 and trench capacitor 140 above a semiconductor substrate 110 (e.g., substrate 110). The semiconductor substrate 110 may include silicon.

[0014] The GaN transistor 120 may include a GaN structure 122 (e.g., GaN island 122, GaN discrete structure 122, each GaN structure 122 is a separate structure on a semiconductor substrate 110 (e.g., the same semiconductor substrate 110)), a source terminal 124, a drain terminal 126, and a gate terminal 128. The source terminal 124 may include indium gallium nitride (InGaN) and n-type doping. The drain terminal 126 may include InGaN and n-type doping. In one

implementation, the source terminal 124 and drain terminal 126 may each contain 0-20% indium (In).

[0015] A GaN layer 130 may be disposed in trench in the semiconductor substrate 110. A GaN structure 122 may be on the GaN layer 130. The GaN structure 122 may have sloped sidewalls. A first oxide 132 may be disposed on the semiconductor substrate 110 and on the sloped sidewalls of the GaN structure 122.

[0016] The source terminal 124 and drain terminal 126 are on the GaN structure 122. An aluminum nitride (AlN) layer 134 is on the GaN structure 122 between the source terminal 124 and the drain terminal 126. A first aluminum indium nitride (AlInN) layer 136a is on a first portion of the AlN layer 134 proximate the source terminal 124 and a second AlInN layer 136b is on a second portion of the AlN layer 134 proximate the drain terminal 126. A high-k dielectric layer 138 is disposed on the first AlInN layer 136a, the second AlInN layer 136b, and on a third portion of the AlN layer 134 between the first AlInN layer 136a and the second AlInN layer 136b. The high-k dielectric layer 138 may be a material with a high dielectric constant k (κ) as compared to silicon dioxide (e.g., high-k dielectric layer 138 may have a dielectric constant greater than 3.9 (the dielectric constant of silicon dioxide)).

[0017] The gate terminal 128 is above the GaN structure 122 (e.g., above the third portion of the AlN layer 134 between the first AlInN layer 136a and the second AlInN layer 136b). The gate terminal 128 may be a t-shape including a top portion that is wider than a bottom portion. A bottom surface of the gate terminal 128 may be disposed in the high-k dielectric layer 138.

[0018] The trench capacitor 140 is above the semiconductor substrate 110 (e.g., above the first oxide 132). The trench capacitor 140 may include a bottom plate 142 above the semiconductor substrate 110, a top plate 146 above the bottom plate 142, and a dielectric material 144 between the bottom plate 142 and the top plate 146. The top plate 146 may have an upper surface including a first sidewall, a second sidewall, and a bottom surface between the first sidewall and the second sidewall. The first sidewall, second sidewall, and bottom surface may form a trench and a second oxide 148 may be in the trench. The dielectric material 144 may include silicon dioxide (SiO_2), aluminum dioxide (AlO_2), or another oxide. The bottom plate 142 and top plate 146 may include tungsten. The second oxide 148 may include an inter-layer dielectric.

[0019] A first trench contact (TCN) 150 may be on the source terminal 124, a first via 152 may be on the first TCN 150, and a signal interconnect 154 may be on the first via 152. A second TCN 156 may be on the drain terminal 126 and a second via 158 may be on the second TCN 156. A third TCN 160 may be on the bottom plate 142 and a third via 162 may be on the third TCN 160. An interconnect 164 may be on the second via 158 and the third via 162. The interconnect 164

couples the GaN transistor 120 and the trench capacitor 140. A fourth TCN 166 may be on the top plate 146, a fourth via 168 may be on the fourth TCN 166, and a ground interconnect 170 may be on the fourth via 168. The interconnect 164 may include one or more of tungsten (W), copper (Cu), and/or gold (Au). One or more of the TCNs 150, 156, 160, and 166 may include one or more of W, Cu, and/or Au.

[0020] The signal interconnect 154 may be coupled to a signal node 208 (see **FIG. 2**). The interconnect 164 may be coupled to one or more other interconnects 164 corresponding to other GaN transistors 120 that are coupled to the same trench capacitor 140 (see **FIG. 2**). The ground interconnect 170 may be coupled to a ground node 206 (see **FIG. 2**). The gate terminal 128 may be coupled to a switch interconnect (e.g., external control circuitry 204, see **FIG. 2**).

[0021] A third oxide 172 may be on the first oxide 132, the GaN structure 122, the source terminal 124, the high-k dielectric layer 138, the gate terminal 128 (sidewalls of the bottom portion of the gate terminal 128), the drain terminal 126, and the bottom plate 142. The third oxide 172 may also be on the sidewalls of the first TCN 150, the second TCN 156, and the third TCN 160.

[0022] An inter-layer dielectric (ILD) 174 may be on the third oxide 172, the gate terminal 128, the top plate 146, the second oxide 148, the first TCN 150, the second TCN 156, the third TCN 160, and the fourth TCN 166.

[0023] **FIG. 2** illustrates a switch capacitor bank structure 200 including integrated GaN transistor-capacitor structures 100 on a semiconductor substrate 110, according to an implementation. Each integrated GaN transistor-capacitor structure 100 is a discrete structure (e.g., separate structures, islands) on the semiconductor substrate 110. In one implementation, the integrated GaN transistor-capacitor structures 100 are surrounded by a shallow trench isolation (STI) 210. In another implementation, the integrated GaN transistor-capacitor structures 100 are surrounded by first oxide 132 (see **FIG. 1**). The STI 210 or first oxide 132 may be on the semiconductor substrate 110 between the integrated GaN transistor-capacitor structures 100.

[0024] Each integrated GaN transistor-capacitor structure 100 may include two or more GaN transistors 120 (e.g., four GaN transistors 120 as shown in **FIG. 2**) and one trench capacitor 140. An integrated GaN transistor-capacitor structure 100 including multiple GaN transistors 120 coupled with the same trench capacitor 140 provides area efficiencies. Each GaN transistor 120 includes a source terminal 124, a drain terminal 126, a gate terminal 128, and an interconnect 164. Each of the interconnects 164 of the GaN transistors 120 of the same integrated GaN transistor-capacitor structure 100 are coupled to the bottom plate 142 of the trench capacitor 140 of the integrated GaN transistor-capacitor structure 100. In one implementation, the interconnects 164 of

the two or more GaN transistors 120 in an integrated GaN transistor-capacitor structure 100 are coupled. The gate terminals 128 of the two or more GaN transistors 120 in an integrated GaN transistor-capacitor structure 100 are coupled to a switch interconnect 202 and the switch interconnect 202 is coupled to an external control circuitry 204 that generates and supplies a suitable level of gate voltage to turn on or turn off the GaN transistors. Each of the trench capacitors 140 (e.g., each of the top plates 146 of the trench capacitors 140) in the switch capacitor bank structure 200 are coupled to the ground interconnect 170 and the ground interconnect 170 is coupled to the ground node 206. Each of the source terminals 124 of the GaN transistors 120 are coupled to the signal interconnect 154 and the signal interconnect 154 is coupled to the signal node 208.

[0025] The switch capacitor bank structure 200 includes a plurality of GaN transistors 120 on a semiconductor substrate 110 and one or more trench capacitors 140 above the semiconductor substrate 110. Each of the trench capacitors 140 is located between and is coupled to at least a first corresponding GaN transistor 120 and a second corresponding GaN transistor 120 of the plurality of GaN transistors (e.g., trench capacitor 140 is located between a first GaN transistor 120 and a second GaN transistor 120 and the trench capacitor 140 is coupled to the first GaN transistor 120 and the second GaN transistor 120). The first corresponding GaN transistor 120 and a first trench capacitor 140 of the one or more trench capacitors 140 are coupled to a first interconnect 164. The second corresponding GaN transistor 120 and the first trench capacitor 140 are coupled to a second interconnect 164. The first interconnect and the second interconnect are coupled.

[0026] **FIG. 3** illustrates a process flow for fabricating a switch capacitor bank, according to another implementation. Method 300 may be performed as operations. It may be noted that method 300 may be performed in any order and may include the same, more, or fewer operations. It may be noted that method 300 may be performed by one or more pieces of semiconductor fabrication equipment or fabrication tools.

[0027] Method 300 begins at operation 310 that forms a GaN structure 122 (e.g., GaN structure 122) on a semiconductor substrate 110 (e.g., substrate 110). Operation 310 may include forming a substrate trench in the semiconductor substrate 110, disposing GaN layer 130 (e.g., a first layer of GaN) in the substrate trench, and disposing the GaN structure 122 on GaN layer 130. Forming the GaN layer 130 and GaN structure 122 may be one process of depositing the GaN and growing the GaN structure 122. The GaN layer 130 and GaN structure 122 may have a wurtzite crystal structure. In one implementation, the GaN structure 122 has sloped sidewalls (e.g., tapered sidewalls) and method 300 further includes disposing a first oxide 132 on the semiconductor

substrate 110 and on the sloped sidewalls of the GaN structure 122. In one implementation, forming the GaN structure 122 on the semiconductor substrate 110 may include growing a GaN structure 122 directly on a semiconductor substrate 110 in a reactor.

[0028] At operation 320, a source terminal and a drain terminal are formed on the GaN structure 122. The region where one or more of the first AlInN layer 136a, AlN layer 134, high-k dielectric layer 138, and/or second AlInN layer 136b will be disposed is a gate region (e.g., active region). The gate region may be masked while the source terminal 124 and the drain terminal 126 are grown.

[0029] At operation 330, a gate terminal 128 is formed on the GaN structure 122 between the source terminal 124 and the drain terminal 126. Operation 330 may include removing the mask (after the source terminal 124 and the drain terminal 126 are grown), disposing an AlN layer 134 on the GaN structure 122 between the source terminal 124 and the drain terminal 126, disposing a first AlInN layer 136a on the AlN layer 134 proximate the source terminal 124, and disposing a second AlInN layer 136b on the AlN layer 134 proximate the drain terminal 126. Operation 330 may further include disposing a high-k dielectric layer 138 on the first AlInN layer 136a, the second AlInN layer 136b and a portion of the AlN layer 134 between the first AlInN layer 136a and the second AlInN layer 136b. The gate terminal 128 may be formed on the high-k dielectric layer 138 above the portion of the AlN layer 134 between the first AlInN layer 136a and the second AlInN layer 136b.

[0030] At operation 340, a bottom plate 142 of the trench capacitor 140 is formed above the semiconductor substrate 110. The bottom plate 142 may be formed above the first oxide 132.

[0031] At operation 350, a dielectric material 144 is formed on the bottom plate.

[0032] At operation 360, a top plate 146 is formed on the dielectric material. The top plate 146 may have an upper surface that includes sidewalls and a bottom surface that form a trench. A second oxide 148 may be disposed in the trench of the upper surface of the top plate 146.

[0033] At operation 370, the drain terminal 126 and the bottom plate 142 are coupled to an interconnect 164. Operation 370 may include forming a second trench contact 156 on the drain terminal 126, forming a second via 158 on the second trench contact 156, forming a third trench contact 160 on the bottom plate 142, and forming a third via 162 on the third trench contact 160, and disposing the interconnect 164 on the second via 158 and the third via 162.

[0034] In one implementation, method 300 may further include forming a first trench contact 150 on the source terminal 124, forming a first via 152 on the first trench contact 150, and disposing a signal interconnect 154 on the first via 152. The source terminal 124 is coupled to a signal node 208 via the signal interconnect 154.

[0035] Method 300 may further include forming a fourth trench contact 166 on the top plate 146, forming a fourth via 168 on the fourth trench contact 166, and disposing a ground interconnect 170 on the fourth via 168. The top plate 146 is coupled to the ground node 206 via the ground interconnect 170.

[0036] In one implementation, method 300 may further include disposing a third oxide 172 on the GaN structure 122, the source terminal 124, the gate terminal 128, the drain terminal 126, and the bottom plate 142. The method 300 may further include disposing an inter-layer dielectric 174 on the third oxide 172, the gate terminal 128, the top plate 146, and the second oxide 148.

[0037] FIG. 4 is a computing device built in accordance with an implementation of the present disclosure. The computing device 400 may include a number of components. In one implementation, the components are attached to one or more motherboards. In an alternate implementation, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die, such as an SoC used for mobile devices. The components in the computing device 400 include, but are not limited to, an integrated circuit die 402 and at least one communications logic unit 408. In some implementations the communications logic unit 408 is fabricated within the integrated circuit die 402 while in other implementations the communications logic unit 408 is fabricated in a separate integrated circuit chip that may be bonded to a semiconductor substrate or motherboard that is shared with or electronically coupled to the integrated circuit die 402. The integrated circuit die 402 may include a CPU 404 as well as on-die memory 406, often used as cache memory that can be provided by technologies such as embedded DRAM (eDRAM), SRAM, or spin-transfer torque memory (STT-MRAM). It may be noted that in implementations integrated circuit die 402 may include fewer elements (e.g., without processor 404 and/or on-die memory 406) or additional elements other than processor 404 and on-die memory 406. In one example, integrated circuit die 402 may be an LED, such as a monolithic multi-color LED pixel 405A or non-monolithic LED 405B, with or without processor 404 and/or on-die memory 406. In another example, integrated circuit die 402 may be LED display with multiple monolithic multi-color LED pixels 405A (or multiple LEDs 405B) and a TFT backplane, with or without processor 404 and/or on-die memory 406. In another example, integrated circuit die 402 may include some or all the elements described herein, as well as include additional elements.

[0038] Computing device 400 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 410 (e.g., DRAM), non-volatile memory 412 (e.g., ROM or flash memory), a graphics processing unit 414 (GPU), a digital signal processor 416, a crypto processor 442 (e.g., a specialized processor that executes cryptographic

algorithms within hardware), a chipset 420, at least one antenna 422 (in some implementations two or more antenna may be used), a display or a touchscreen display 424 (e.g., that may include integrated circuit die 402) , a touchscreen controller 426, a battery 428 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 427, a compass (not shown), a motion coprocessor or sensors 432 (that may include an accelerometer, a gyroscope, and a compass), a microphone (not shown), a speaker 434, a camera 436, user input devices 438 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 440 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). The computing device 400 may incorporate further transmission, telecommunication, or radio functionality not already described herein. In some implementations, the computing device 400 includes a radio that is used to communicate over a distance by modulating and radiating electromagnetic waves in air or space. In further implementations, the computing device 400 includes a transmitter and a receiver (or a transceiver) that is used to communicate over a distance by modulating and radiating electromagnetic waves in air or space.

[0039] The communications logic unit 408 enables wireless communications for the transfer of data to and from the computing device 400. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some implementations they might not. The communications logic unit 408 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Infrared (IR), Near Field Communication (NFC), Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 400 may include a plurality of communications logic units 408. For instance, a first communications logic unit 408 may be dedicated to shorter range wireless communications such as Wi-Fi, NFC, and Bluetooth and a second communications logic unit 408 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0040] The processor 404 (also referred to "processing device" herein) of the computing device 400 includes one or more devices, such as transistors, RF filters, or LEDs, that are formed in accordance with implementations of the present disclosure. The term "processor" or "processing device" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in

registers and/or memory. Processor 404 represents one or more general-purpose processing devices such as a microprocessor, a central processing unit, or the like. More particularly, the processor 404 may be complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, or processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 404 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like.

[0041] The communications logic unit 408 may also include one or more devices, such as transistors (e.g., power amplifiers, switches, low noise amplifiers, etc.), RF filters, or LEDs, that are formed in accordance with implementations of the present disclosure.

[0042] In some implementations, antenna 422 is coupled to the communications logic unit 408 (e.g., communications chip(s)). In some implementations the antenna 422 and communications logic unit 408 are coupled to a motherboard.

[0043] In further implementations, another component housed within the computing device 400 may contain one or more devices, such as transistors, RF filters, or LEDs, that are formed in accordance with implementations of the present disclosure.

[0044] In various implementations, the computing device 400 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a dumbphone, a tablet, a tablet/laptop hybrid, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, self-driving (autonomous) automobile, or a digital video recorder. In further implementations, the computing device 400 may be any other electronic device that processes data.

[0045] The following examples pertain to further embodiments.

[0046] Example 1 is a switch capacitor bank structure comprising: a plurality of gallium nitride (GaN) transistors on a semiconductor substrate; and one or more trench capacitors above the semiconductor substrate, wherein each of the trench capacitors is located between and is coupled to at least a first corresponding GaN transistor and a second corresponding GaN transistor of the plurality of GaN transistors.

[0047] In Example 2, the switch capacitor bank structure of Example 1, wherein: each of the one or more trench capacitors comprises: a bottom plate; a top plate coupled to a ground node; and a dielectric between the bottom plate and the top plate; and each of the plurality of GaN transistors comprises: a GaN structure on the semiconductor substrate; a source terminal on the

GaN structure; a gate terminal on the GaN structure, the gate terminal being coupled to a switch interconnect; and a drain terminal on the GaN structure, the drain terminal and a corresponding bottom plate of a corresponding trench capacitor of the one or more trench capacitors being coupled together via an interconnect.

[0048] In Example 3, the switch capacitor bank structure of any one of Examples 1-2, wherein: an aluminum nitride (AlN) layer is on the GaN structure between the source terminal and the drain terminal; a first aluminum indium nitride (AlInN) layer is on a first portion of the AlN layer proximate the source terminal; a second AlInN layer is on a second portion of the AlN layer proximate the source terminal; a high-k dielectric layer is on the first AlInN layer, the second AlInN layer, and a third portion of the AlN layer between the first portion and the second portion; and the gate terminal is on the high-k dielectric layer above the third portion of the AlN layer.

[0049] In Example 4, the switch capacitor bank structure of any one of Examples 1-3, wherein: a first trench contact is on the source terminal, a first via is on the first trench contact, and a signal interconnect is on the first via; the source terminal is coupled to a signal node via the signal interconnect to receive a signal; a second trench contact is on the drain terminal and a second via is on the second trench contact; a third trench contact is on the bottom plate, a third via is on the third trench contact, and the interconnect is on the second via and the third via; a plurality of interconnects comprising the interconnect are coupled, the plurality of interconnects corresponding to a subset of the plurality of integrated GaN transistor-capacitor structures that comprise a common trench capacitor; a fourth trench contact is on the top plate, a fourth via is on the fourth trench contact, and a ground interconnect on the fourth via; and the top plate is coupled to the ground node via the ground interconnect.

[0050] In Example 5, the switch capacitor bank structure of any one of Examples 1-4, wherein: the top plate has an upper surface comprising a first sidewall, a second sidewall, and a bottom surface between the first sidewall and the second sidewall; the first sidewall, second sidewall, and bottom surface form a trench; and a second oxide is in the trench.

[0051] In Example 6, the switch capacitor bank structure of any one of Examples 1-5, wherein: the source terminal comprises indium gallium nitride (InGaN) and n-type doping; and the drain terminal comprises InGaN and n-type doping.

[0052] In Example 7, the switch capacitor bank structure of any one of Examples 1-6, wherein: a third oxide is on the GaN structure, the source terminal, the gate terminal, the drain terminal, and the bottom plate; and an inter-layer dielectric is on the third oxide, the gate terminal, and the top plate.

[0053] In Example 8, the switch capacitor bank structure of any one of Examples 1-7, wherein the semiconductor substrate comprises silicon.

[0054] In Example 9, the switch capacitor bank structure of any one of Examples 1-8, wherein each GaN structure is grown directly on the semiconductor substrate, wherein the GaN structures are separated by one or more shallow trench isolations (STI).

[0055] Example 10 is an integrated circuit die comprising: a semiconductor substrate; a trench capacitor above the semiconductor substrate, the trench capacitor comprising a bottom plate; a gallium nitride (GaN) transistor comprising a drain terminal; and an interconnect above the trench capacitor and the GaN transistor, the interconnect coupling the drain terminal and bottom plate.

[0056] In Example 11, the integrated circuit die of Example 10, wherein: the trench capacitor further comprises a top plate coupled to a ground node and a dielectric between the bottom plate and the top plate; and the GaN transistor further comprises: a GaN structure on the semiconductor substrate; a source terminal on the GaN structure; and a gate terminal on the GaN structure, the gate terminal being coupled to a switch interconnect, wherein the drain terminal is on the GaN structure.

[0057] In Example 12, the integrated circuit die of any one of Examples 10-11, wherein: an aluminum nitride (AlN) layer is on the GaN structure between the source terminal and the drain terminal; a first aluminum indium nitride (AlInN) layer is on a first portion of the AlN layer proximate the source terminal; a second AlInN layer is on a second portion of the AlN layer proximate the source terminal; a high-k dielectric layer is on the first AlInN layer, the second AlInN layer, and a third portion of the AlN layer between the first portion and the second portion; and the gate terminal is on the high-k dielectric layer above the third portion of the AlN layer.

[0058] In Example 13, the integrated circuit die of any one of Examples 10-12, wherein: a first trench contact is on the source terminal, a first via is on the first trench contact, and a signal interconnect is on the first via; the source terminal is coupled to a signal node via the signal interconnect to receive a signal; a second trench contact is on the drain terminal and a second via is on the second trench contact; a third trench contact is on the bottom plate, a third via is on the third trench contact, and the interconnect is on the second via and the third via; and a fourth trench contact is on the top plate, a fourth via is on the fourth trench contact, and a ground interconnect on the fourth via; and the top plate is coupled to the ground node via the ground interconnect.

[0059] In Example 14, the integrated circuit die of any one of Examples 10-13, wherein: the top plate has an upper surface comprising a first sidewall, a second sidewall, and a bottom surface

between the first sidewall and the second sidewall; the first sidewall, second sidewall, and bottom surface form a trench; and a second oxide is in the trench.

[0060] In Example 15, the integrated circuit die of Example 11, wherein: the source terminal comprises indium gallium nitride (InGaN) and n-type doping; and the drain terminal comprises InGaN and n-type doping.

[0061] In Example 16, the integrated circuit die of Example 11, wherein: a third oxide is on the GaN structure, the source terminal, the gate terminal, the drain terminal, and the bottom plate; and an inter-layer dielectric is on the third oxide, the gate terminal, and the top plate.

[0062] Example 17 is a method of fabricating a switch capacitor bank structure, the method comprising: forming a gallium nitride (GaN) structure on a semiconductor substrate; forming a source terminal and a drain terminal on the GaN structure; forming a gate terminal on the GaN structure between the source terminal and the drain terminal; forming a bottom plate above the semiconductor substrate; forming a dielectric material on the bottom plate; forming a top plate on the dielectric material; and coupling the drain terminal and the bottom plate to an interconnect.

[0063] In Example 18, the method of Example 17 further comprising: forming a first trench contact on the source terminal, forming a first via on the first trench contact, and disposing a signal interconnect on the first via; and forming a fourth trench contact on the top plate, forming a fourth via on the fourth trench contact, and disposing a ground interconnect on the fourth via, wherein: the source terminal is coupled to a signal node via the signal interconnect; the top plate is coupled to a ground node via the ground interconnect; and coupling the drain terminal and the bottom plate to the interconnect comprises forming a second trench contact on the drain terminal and a third trench contact on the bottom plate, forming a second via on the second trench contact and a third via on the third trench contact, and disposing the interconnect on the second via and the third via.

[0064] In Example 19, the method of any one of Examples 17-18, wherein forming the GaN structure on the semiconductor substrate comprises: forming a substrate trench in the semiconductor substrate; disposing a first layer of GaN in the substrate trench; and disposing the GaN structure on the first layer of GaN.

[0065] In Example 20, the method of any one of Examples 17-19, wherein forming the gate terminal on the GaN structure comprises: disposing an aluminum nitride (AlN) layer on the GaN structure between the source terminal and the drain terminal; disposing a first aluminum indium nitride (AlInN) layer on the AlN layer proximate the source terminal and a second AlInN layer on the AlN layer proximate the drain terminal; disposing a high-k dielectric layer on the first AlInN layer, the second AlInN layer, and a portion of the AlN layer between the first AlInN layer and

the second AlInN; and forming the gate terminal on the high-k dielectric layer above the portion of the AlN layer between the first AlInN layer and the second AlInN.

[0066] In Example 21, the method of any one of Examples 17-20 further comprising: disposing a second oxide on the top plate; disposing a third oxide on the GaN structure, the source terminal, the gate terminal, the drain terminal, and the bottom plate; and disposing an inter-layer dielectric on the third oxide, the gate terminal, the top plate, and the second oxide.

[0067] In Example 22, the method of any one of Examples 17-21, wherein the GaN structure has sloped sidewalls and the method further comprises disposing a first oxide on the semiconductor substrate and on the sloped sidewalls of the GaN structure.

[0068] Example 23 is an apparatus comprising means to perform a method of any one of Examples 17-22.

[0069] Example 24 is an apparatus comprising means for performing the method of any one of Examples 17-22.

[0070] The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

[0071] Various operations are described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0072] The terms “over,” “above” “under,” “between,” and “on” as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed above or over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer “on” a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0073] Implementations of the disclosure may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other

implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to Germanium, Indium Antimonide, Lead Telluride, Indium Arsenide, Indium Phosphide, Gallium Arsenide, Indium Gallium Arsenide, Gallium Antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the semiconductor substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

[0074] A plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the semiconductor substrate. In various implementations of the disclosure, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein may illustrate only planar transistors, it should be noted that the disclosure may also be carried out using nonplanar transistors.

[0075] Each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO_2) and/or a high-k dielectric material. The high-k dielectric material may include elements such as Hafnium, Silicon, Oxygen, Titanium, Tantalum, Lanthanum, Aluminum, Zirconium, Barium, Strontium, Yttrium, Lead, Scandium, Niobium, and Zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, Hafnium Oxide, Hafnium Silicon Oxide, Lanthanum Oxide, Lanthanum Aluminum Oxide, Zirconium Oxide, Zirconium Silicon Oxide, Tantalum Oxide, Titanium Oxide, Barium Strontium Titanium Oxide, Barium Titanium Oxide, Strontium Titanium Oxide, Yttrium Oxide, Aluminum Oxide, Lead Scandium Tantalum Oxide, and Lead Zinc Niobate. In some implementations, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

[0076] The gate electrode layer is formed on the gate dielectric layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer.

[0077] For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, Ruthenium, Palladium, Platinum, Cobalt, Nickel, and conductive metal oxides, e.g., Ruthenium Oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, Hafnium, Zirconium, Titanium, Tantalum, Aluminum, alloys of these metals, and carbides of these metals such as Hafnium Carbide, Zirconium Carbide, Titanium Carbide, Tantalum Carbide, and Aluminum Carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

[0078] In some implementations, when viewed as a cross-section of the transistor along the source-channel-drain direction, the gate electrode may consist of a "U"-shaped structure that includes a bottom portion substantially parallel to the surface of the semiconductor substrate and two sidewall portions that are substantially perpendicular to the top surface of the semiconductor substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the semiconductor substrate and does not include sidewall portions substantially perpendicular to the top surface of the semiconductor substrate. In further implementations of the disclosure, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0079] In some implementations of the disclosure, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as Silicon Nitride, Silicon Oxide, Silicon Carbide, Silicon Nitride doped with Carbon, and Silicon Oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process operations. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0080] In implementations, source and drain regions are formed within the semiconductor substrate adjacent to the gate stack of each MOS transistor. The source and drain regions may be formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as Boron, Aluminum, Antimony, Phosphorous, or Arsenic may be ion-implanted into the semiconductor substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the semiconductor substrate typically follows the ion implantation process. In the latter process, the

semiconductor substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a Silicon alloy such as Silicon Germanium or Silicon Carbide. In some implementations, the epitaxially deposited silicon alloy may be doped in situ with dopants such as Boron, Arsenic, or Phosphorous. In further implementations, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. In further implementations, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[0081] In other implementations, one or more interlayer dielectrics (ILD) are deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, Silicon Dioxide (SiO_2), Carbon doped oxide (CDO), Silicon Nitride, organic polymers such as Perfluorocyclobutane or Polytetrafluoroethylene, Fluorosilicate glass (FSG), and organosilicates such as Silsesquioxane, Siloxane, or Organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

CLAIMS

What is claimed is:

1. A switch capacitor bank structure comprising:

a plurality of gallium nitride (GaN) transistors on a semiconductor substrate; and

one or more trench capacitors above the semiconductor substrate, wherein each of the trench capacitors is located between and is coupled to at least a first corresponding GaN transistor and a second corresponding GaN transistor of the plurality of GaN transistors.

2. The switch capacitor bank structure of claim 1, wherein:

each of the one or more trench capacitors comprises:

a bottom plate;

a top plate coupled to a ground node; and

a dielectric between the bottom plate and the top plate; and

each of the plurality of GaN transistors comprises:

a GaN structure on the semiconductor substrate;

a source terminal on the GaN structure;

a gate terminal on the GaN structure, the gate terminal being coupled to a switch interconnect; and

a drain terminal on the GaN structure, the drain terminal and a corresponding bottom plate of a corresponding trench capacitor of the one or more trench capacitors being coupled together via an interconnect.

3. The switch capacitor bank structure of claim 2, wherein:

an aluminum nitride (AlN) layer is on the GaN structure between the source terminal and the drain terminal;

a first aluminum indium nitride (AlInN) layer is on a first portion of the AlN layer proximate the source terminal;

a second AlInN layer is on a second portion of the AlN layer proximate the source terminal;

a high-k dielectric layer is on the first AlInN layer, the second AlInN layer, and a third portion of the AlN layer between the first portion and the second portion; and

the gate terminal is on the high-k dielectric layer above the third portion of the AlN layer.

4. The switch capacitor bank structure of claim 2, wherein:

a first trench contact is on the source terminal, a first via is on the first trench contact, and a signal interconnect is on the first via;

the source terminal is coupled to a signal node via the signal interconnect to receive a signal;

a second trench contact is on the drain terminal and a second via is on the second trench contact;

a third trench contact is on the bottom plate, a third via is on the third trench contact, and the interconnect is on the second via and the third via;

a plurality of interconnects comprising the interconnect are coupled, the plurality of interconnects corresponding to a subset of the plurality of integrated GaN transistor-capacitor structures that comprise a common trench capacitor;

a fourth trench contact is on the top plate, a fourth via is on the fourth trench contact, and a ground interconnect on the fourth via; and

the top plate is coupled to the ground node via the ground interconnect.

5. The switch capacitor bank structure of claim 2, wherein:

the top plate has an upper surface comprising a first sidewall, a second sidewall, and a bottom surface between the first sidewall and the second sidewall;

the first sidewall, second sidewall, and bottom surface form a trench; and

a second oxide is in the trench.

6. The switch capacitor bank structure of claim 2, wherein:

the source terminal comprises indium gallium nitride (InGaN) and n-type doping; and

the drain terminal comprises InGaN and n-type doping.

7. The switch capacitor bank structure of claim 2, wherein:

a third oxide is on the GaN structure, the source terminal, the gate terminal, the drain terminal, and the bottom plate; and

an inter-layer dielectric is on the third oxide, the gate terminal, and the top plate.

8. The switch capacitor bank structure of claim 1, wherein the semiconductor substrate comprises silicon.

9. The switch capacitor bank structure of claim 2, wherein each GaN structure is grown directly on the semiconductor substrate, wherein the GaN structures are separated by one or more shallow trench isolations (STI).

10. An integrated circuit die comprising:

a semiconductor substrate;

a trench capacitor above the semiconductor substrate, the trench capacitor comprising a bottom plate;

a gallium nitride (GaN) transistor comprising a drain terminal; and

an interconnect above the trench capacitor and the GaN transistor, the interconnect coupling the drain terminal and bottom plate.

11. The integrated circuit die of claim 10, wherein:

the trench capacitor further comprises a top plate coupled to a ground node and a dielectric between the bottom plate and the top plate; and

the GaN transistor further comprises:

a GaN structure on the semiconductor substrate;

a source terminal on the GaN structure; and

a gate terminal on the GaN structure, the gate terminal being coupled to a switch interconnect, wherein the drain terminal is on the GaN structure.

12. The integrated circuit die of claim 11, wherein:

an aluminum nitride (AlN) layer is on the GaN structure between the source terminal and the drain terminal;

a first aluminum indium nitride (AlInN) layer is on a first portion of the AlN layer proximate the source terminal;

a second AlInN layer is on a second portion of the AlN layer proximate the source terminal;

a high-k dielectric layer is on the first AlInN layer, the second AlInN layer, and a third portion of the AlN layer between the first portion and the second portion; and

the gate terminal is on the high-k dielectric layer above the third portion of the AlN layer.

13. The integrated circuit die of claim 11, wherein:

a first trench contact is on the source terminal, a first via is on the first trench contact, and a signal interconnect is on the first via;

the source terminal is coupled to a signal node via the signal interconnect to receive a signal;

a second trench contact is on the drain terminal and a second via is on the second trench contact;

a third trench contact is on the bottom plate, a third via is on the third trench contact, and the interconnect is on the second via and the third via; and

a fourth trench contact is on the top plate, a fourth via is on the fourth trench contact, and a ground interconnect on the fourth via; and

the top plate is coupled to the ground node via the ground interconnect.

14. The integrated circuit die of claim 11, wherein:

the top plate has an upper surface comprising a first sidewall, a second sidewall, and a bottom surface between the first sidewall and the second sidewall;

the first sidewall, second sidewall, and bottom surface form a trench; and

a second oxide is in the trench.

15. The integrated circuit die of claim 11, wherein:

the source terminal comprises indium gallium nitride (InGaN) and n-type doping; and

the drain terminal comprises InGaN and n-type doping.

16. The integrated circuit die of claim 11, wherein:

a third oxide is on the GaN structure, the source terminal, the gate terminal, the drain terminal, and the bottom plate; and

an inter-layer dielectric is on the third oxide, the gate terminal, and the top plate.

17. A method of fabricating a switch capacitor bank structure, the method comprising:

forming a gallium nitride (GaN) structure on a semiconductor substrate;

forming a source terminal and a drain terminal on the GaN structure;

forming a gate terminal on the GaN structure between the source terminal and the drain terminal;

forming a bottom plate above the semiconductor substrate;

forming a dielectric material on the bottom plate;

forming a top plate on the dielectric material; and

coupling the drain terminal and the bottom plate to an interconnect.

18. The method of claim 17 further comprising:

forming a first trench contact on the source terminal, forming a first via on the first trench contact, and disposing a signal interconnect on the first via; and

forming a fourth trench contact on the top plate, forming a fourth via on the fourth trench contact, and disposing a ground interconnect on the fourth via, wherein:

the source terminal is coupled to a signal node via the signal interconnect;

the top plate is coupled to a ground node via the ground interconnect; and

coupling the drain terminal and the bottom plate to the interconnect comprises forming a second trench contact on the drain terminal and a third trench contact on the bottom plate, forming a second via on the second trench contact and a third via on the third trench contact, and disposing the interconnect on the second via and the third via.

19. The method of claim 17, wherein forming the GaN structure on the semiconductor substrate comprises:

forming a substrate trench in the semiconductor substrate;

disposing a first layer of GaN in the substrate trench; and

disposing the GaN structure on the first layer of GaN.

20. The method of claim 17, wherein forming the gate terminal on the GaN structure comprises:

disposing an aluminum nitride (AlN) layer on the GaN structure between the source terminal and the drain terminal;

disposing a first aluminum indium nitride (AlInN) layer on the AlN layer proximate the source terminal and a second AlInN layer on the AlN layer proximate the drain terminal;

disposing a high-k dielectric layer on the first AlInN layer, the second AlInN layer, and a portion of the AlN layer between the first AlInN layer and the second AlInN; and

forming the gate terminal on the high-k dielectric layer above the portion of the AlN layer between the first AlInN layer and the second AlInN.

21. The method of claim 17 further comprising:

disposing a second oxide on the top plate;

disposing a third oxide on the GaN structure, the source terminal, the gate terminal, the drain terminal, and the bottom plate; and

disposing an inter-layer dielectric on the third oxide, the gate terminal, the top plate, and the second oxide.

22. The method of claim 17, wherein the GaN structure has sloped sidewalls and the method further comprises disposing a first oxide on the semiconductor substrate and on the sloped sidewalls of the GaN structure.

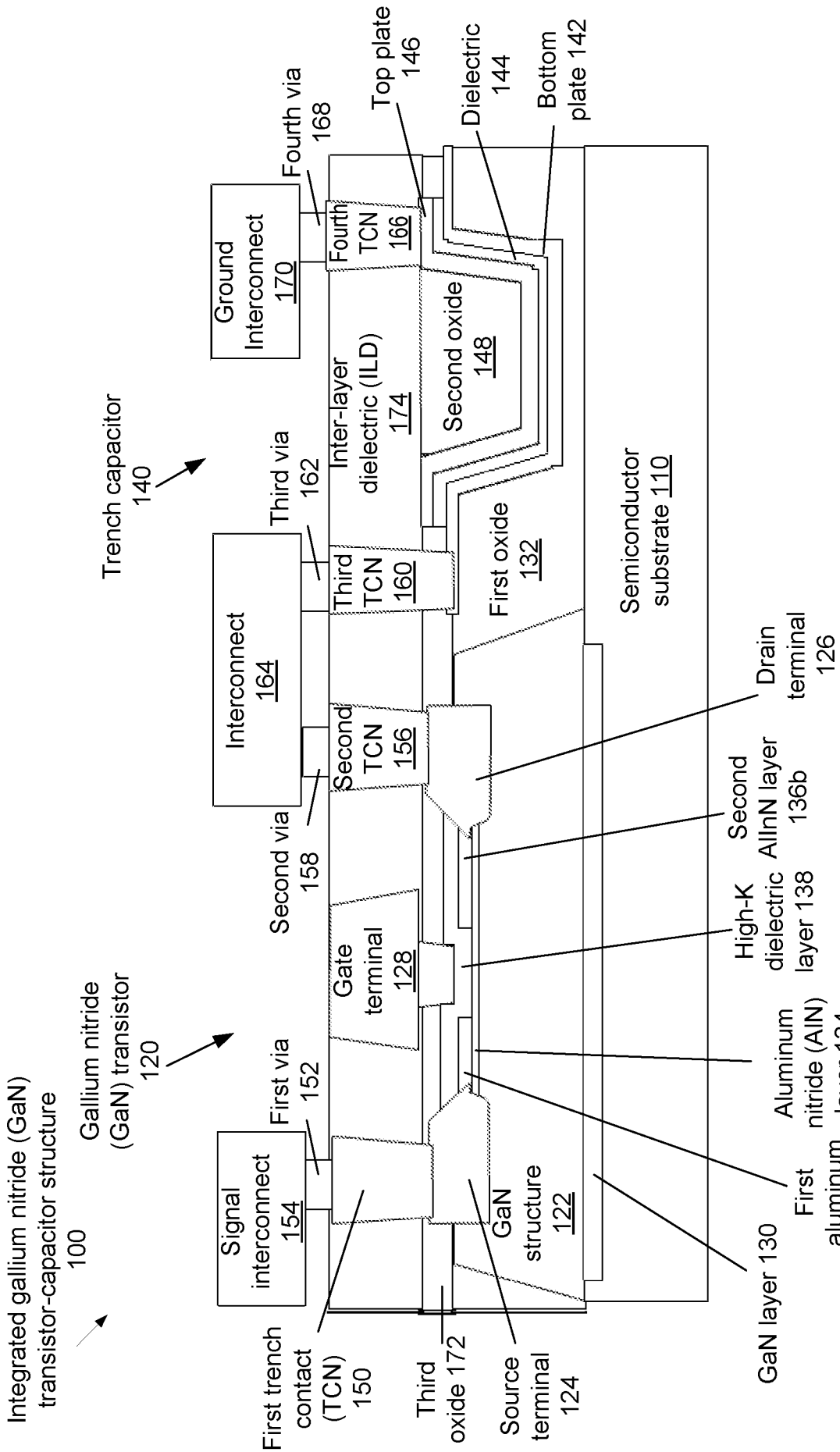
Integrated gallium nitride (GaN) transistor-capacitor structure 100
Gallium nitride (GaN) transistor 120
Trench capacitor 140
Signal interconnect 154
First via 152
Gate terminal 128
Second via 158
Interconnect 164
Second TCN 156
Third via 162
Third TCN 160
Inter-layer dielectric (ILD) 174
Ground Interconnect 170
Fourth via 168
Fourth TCN 166
Top plate 146
Dielectric 144
Bottom plate 142
Second oxide 148
First oxide 132
Semiconductor substrate 110
Drain terminal 126
Second AlInN layer 136b
High-K dielectric layer 138
Aluminum nitride (AlN) layer 134
First aluminum indium nitride (AlInN) layer 136a
GaN layer 130
GaN structure 122
Source terminal 124
Third oxide 172
First trench contact (TCN) 150

FIG. 1

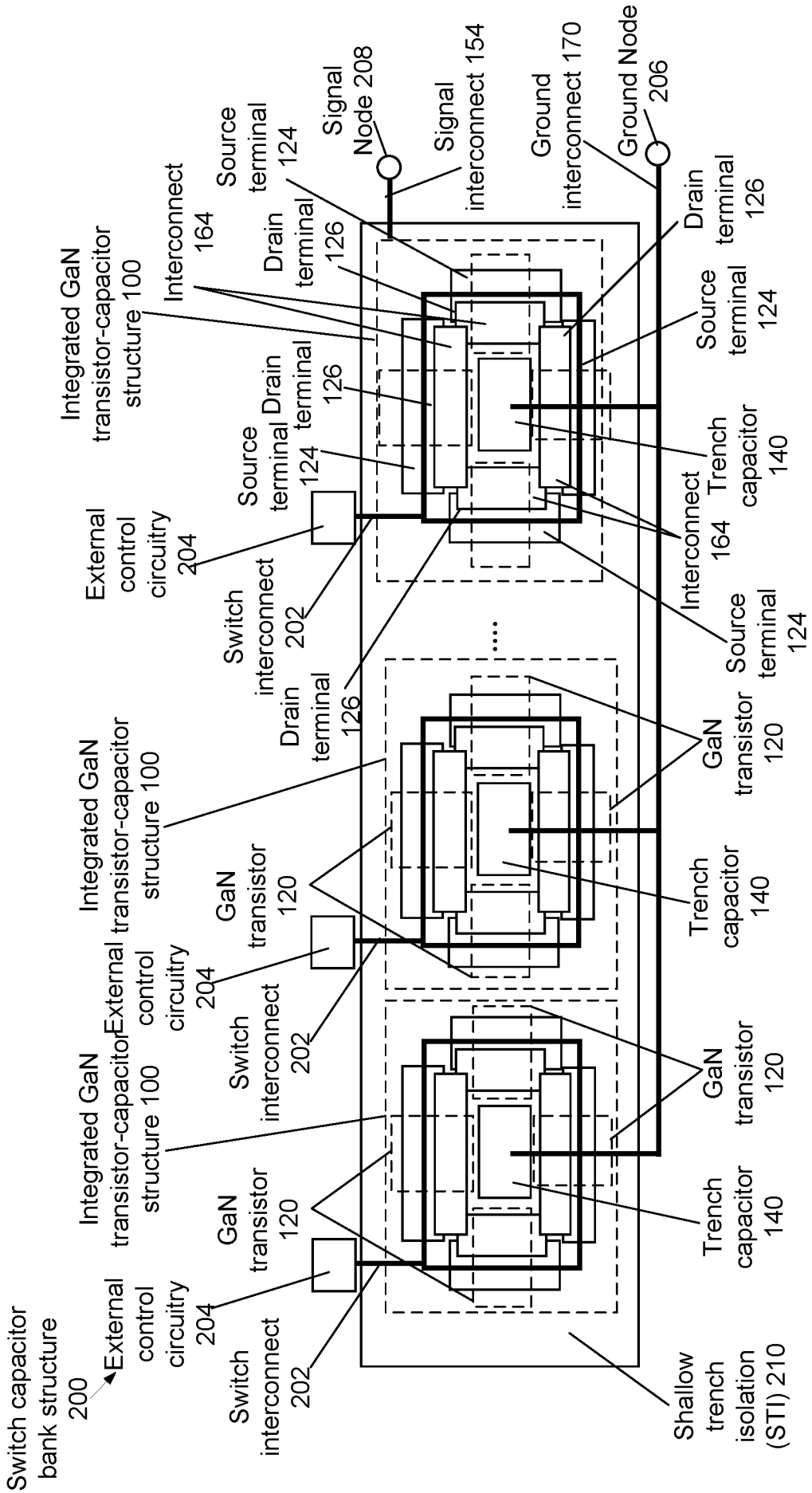
Switch capacitor bank structure 200
External control circuitry 204
Switch interconnect 202
GaN transistor 120
Integrated GaN transistor-capacitor structure 100
Trench capacitor 140
Shallow trench isolation (STI) 210
Drain terminal 126
Source terminal 124
Interconnect 164
Signal Node 208
Signal interconnect 154
Ground interconnect 170
Ground Node 206

FIG. 2

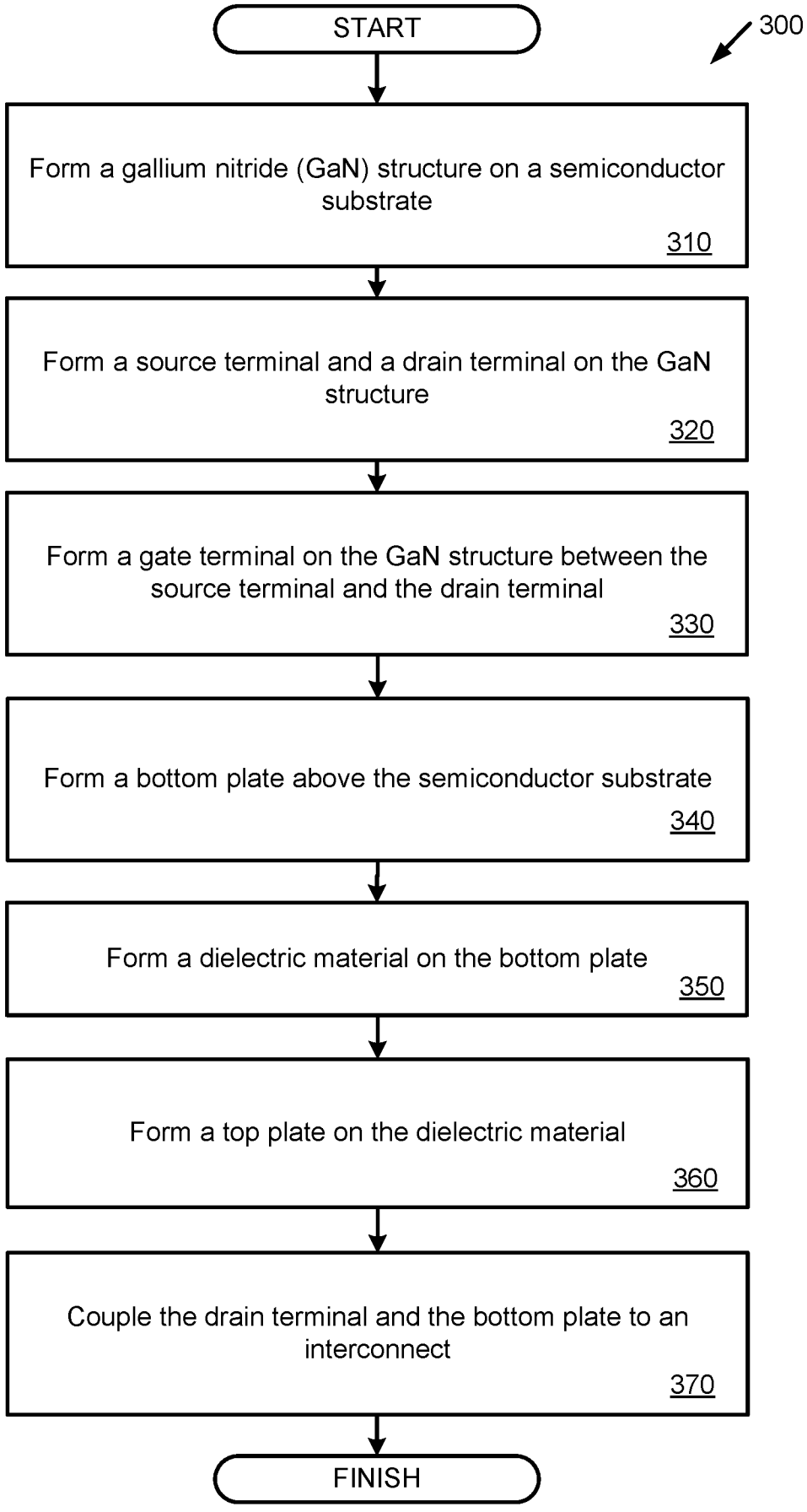
START
300
Form a gallium nitride (GaN) structure on a semiconductor substrate
310
Form a source terminal and a drain terminal on the GaN structure
320
Form a gate terminal on the GaN structure between the source terminal and the drain terminal
330
Form a bottom plate above the semiconductor substrate
340
Form a dielectric material on the bottom plate
350
Form a top plate on the dielectric material
360
Couple the drain terminal and the bottom plate to an interconnect
370
FINISH

FIG. 3

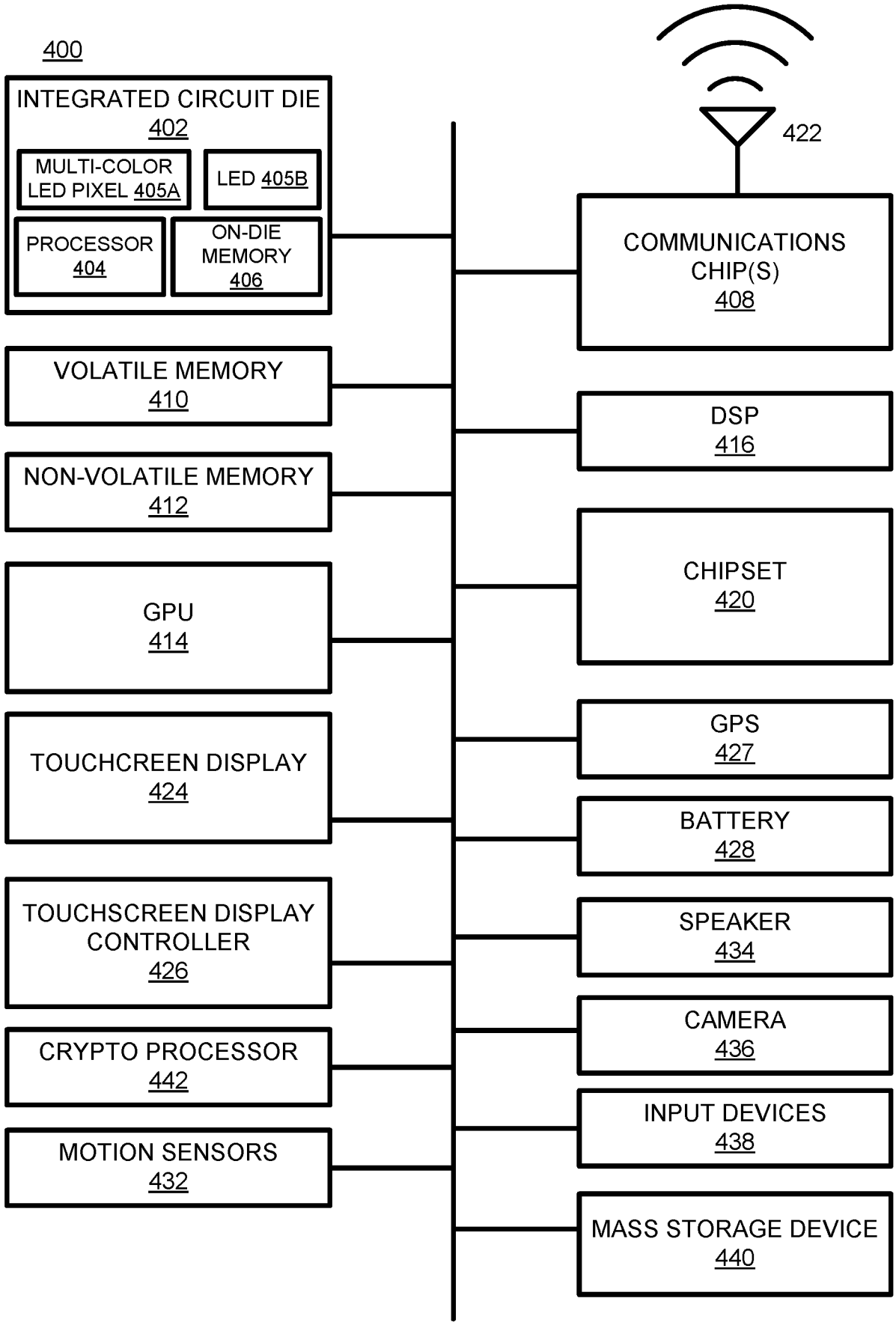
400
INTEGRATED CIRCUIT DIE
402
MULTI-COLOR LED PIXEL 405A
LED 405B
PROCESSOR 404
ON-DIE MEMORY 406
VOLATILE MEMORY 410
NON-VOLATILE MEMORY 412
GPU 414
TOUCHCREEN DISPLAY 424
TOUCHSCREEN DISPLAY CONTROLLER 426
CRYPTO PROCESSOR 442
MOTION SENSORS 432
422
COMMUNICATIONS CHIP(S) 408
DSP 416
CHIPSET 420
GPS 427
BATTERY 428
SPEAKER 434
CAMERA 436
INPUT DEVICES 438
MASS STORAGE DEVICE 440

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/023646

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/06(2006.01)i, H01L 49/02(2006.01)i, H01L 29/778(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 27/06; H01L 31/112; H01L 29/778; H01L 29/47; H01L 27/108; H01L 29/40; H01L 21/8234; H01L 21/31; H01L 49/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: switch capacitor bank structure, gallium nitride (GaN) transistor, trench capacitor, drain terminal, bottom plate, interconnect

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007-0181884 A1 (ERIC BLOMILEY et al.) 09 August 2007 See paragraphs [0029]-[0061] and figures 1, 6-7.	1-22
A	US 2008-0214015 A1 (TIM BOESCKE) 04 September 2008 See paragraphs [0050]-[0060] and figures 9-11.	1-22
A	US 2016-0086938 A1 (NAVITAS SEMICONDUCTOR INC.) 24 March 2016 See paragraphs [0022]-[0033] and figure 1.	1-22
A	US 2015-0295075 A1 (FREESCALE SEMICONDUCTOR, INC.) 15 October 2015 See paragraphs [0033]-[0051] and figures 1-13.	1-22
A	US 2016-0043072 A1 (INFINEON TECHNOLOGIES AUSTRIA AG) 11 February 2016 See paragraphs [0061]-[0062] and figure 7B.	1-22

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 December 2017 (15.12.2017)	**18 December 2017 (18.12.2017)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
KIM, Sung Gon
Telephone No. +82-42-481-8746

INTERNATIONAL SEARCH REPORT

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