APPLICATION ACCEPTED AND AMENDMENTS ALLOWED

CONVENTION

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598253

APPLICATION FOR A STANDARD PATENT

~~I~~/We Digital Equipment Corporation

of 146 Main Street,
Maynard,
Massachusetts,
UNITED STATES OF AMERICA.

hereby apply for the grant of a standard patent for an invention entitled:

SYSTEM FOR DETACHABLY MOUNTING SEMI-CONDUCTORS ON CONDUCTOR SUBSTRATES

which is described in the accompanying complete specification.

Details of basic application

Number of basic application: 860,725

Convention country in which basic application was filed: UNITED STATES OF AMERICA

Date of basic application : 7 May 1986

Address for Service:

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APPLICATION ACCEPTED AND AMENDMENTS

Dated: 23 April 1987

ALLOWED 30-3-90

PHILLIPS ORMONDE and FITZPATRICK
Attorneys for:
Digital Equipment Corporation,

By: David B Fitzpatrick

FEE STAMP TO VALUE OF ATTACHED MAIL OFFICER

Our Ref : 53249
POF Code: 775/1038

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LODGED AT SUB-OFFICE
28 APR 1987
Melbourne

6012q/1

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DECLARATION FOR A PATENT APPLICATION

▼ INSTRUCTIONS

(a) Insert "Convention" if applicable

(b) Insert FULL name(s) of applicant(s)

In support of the (a) Convention application made by (b) Digital Equipment Corporation, 146 Main Street, Maynard, Massachusetts, 01754, United States of America,

(c) Insert "of addition" if applicable

(d) Insert TITLE of invention

(hereinafter called "applicant(s)" for a patent (c) for an invention entitled (d)

SYSTEM FOR DETACHABLY MOUNTING SEMICONDUCTORS ON CONDUCTOR SUBSTRATES

(e) Insert FULL name(s) AND address(es) of declarant(s) (See headnote*)

I/We (e)

Marietta M. Ethier, Assistant Secretary of Digital Equipment Corporation

do solemnly and sincerely declare as follows:

~~I am/We are the applicant(s).~~

~~The invention is the application by a body corporate.~~

1. I am/~~We are~~ authorized to make this declaration on behalf of the applicant(s).

~~The name(s) of the inventor(s) of the invention is/are~~

(f) Insert FULL name(AND address(es) of actual inventor(s)

James C. K. Lee, 28446 Christopher Lane, Los Altos Hills, California, 94022, U.S.A.; Gene M. Amdahl, 165 Patricia Avenue, Atherton, California, 94025, U.S.A.; Richard Beck, 10182 Parish Place, Cupertino, California, 95014, U.S.A.; Chune Lee, 1836 Cabrillo Street, San Francisco, California, 94121, U.S.A.; Edward Hu, 648 Kodiak Court, #4, Sunnyvale, California, U.S.A.

(g) Delete how applicant(s) derive(s) title from actual inventor(s) (See headnote**)

~~The~~/are the actual inventor(s) of the invention and the facts upon which the applicant(s) ~~is~~/are entitled to make the application are as follows:

(g)

Applicant is the Assignee of the Inventors.

(Note: *Paragraphs 3 and 4 apply* only *to Convention applications)*

(h) Insert country, filing date, and basic applicant(s) for the/or EACH basic application

3. The basic application(s) for patent or similar protection on which the application is based is/~~are~~ identified by country, filing date, and basic applicant(s) as follows:

(h) United States of America
07 May 1986
James C. K. Lee, Gene M. Amdahl, Richard, Beck, Chune Lee, and Edward Hu

4. The basic application(s) referred to in paragraph 3 hereof was/~~were~~ the first application(s) made in a Convention country in respect of the invention the subject of the application.

(k) Insert PLACE of signing

(l) Insert DATE of signing

(m) Signature(s) of declarant(s)

Note: No legalization or other witness required

Declared at (k) Maynard, Massachusetts

Dated (l) May 11, , 1987

(m) Digital Equipment Corporation

Marietta M. Ethier

Marietta M. Ethier,
Assistant Secretary

To: The Commissioner of Patents

P18/7/78

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(12) PATENT ABRIDGMENT (11) Document No. AU-B-72165/87
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 598253

(54) Title
DETACHABLE MOUNTING OF SEMICONDUCTORS

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(56) Prior Art Documents
AU 590514 42598/85 H01L 23/04, 23/08, 23/12
AU 559141 79709/82 H01L 21/96, 23/14
US 4597617

(57) Claim

1. A semiconductor die mounting system comprising:

a) a conductor substrate having an array of substrate contacts on a substrate face thereof;

b) at least one semiconductor die having first and second opposed die faces and a plurality of die contacts on the first die face thereof disposed in alignment with corresponding substrate contacts on the conductor substrate;

c) a conductor pad disposed between the substrate and the die having first and second opposed pad surfaces in contact with the substrate face and first die face, respectively the conductor pad including a plurality of electrically conductive elements mutually electrically isolated within the pad and extending between the first and second surfaces thereof in the direction of alignment between the substrate and die contacts so as to provide electrical conduction between the pad surfaces, adjacent conductive elements being spaced apart by less than the

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minimum width of the contacts; and

d) means for holding the semiconductor die and the conductor substrate in contact with the conductor pad so that the corresponding die and substrate contacts are in alignment.

2. A semiconductor die mounting system as claimed in claim 1 wherein the means for holding the semiconductor die and the conductor pad includes:

a) a nest plate mounted over the conductor substrate for aligning the contacts on the conductor substrate with the contacts on the semiconductor die; and

b) a cover mounted on the nest plate.

3. A semiconductor die mounting system as claimed in claim 2 wherein:

a) the cover includes a cover face; and

b) the semiconductor mounting system further includes a second conductor pad disposed between the semiconductor die and the cover, the second conductor pad having first and second opposed surfaces in contact with a cover face and the second die face, respectively, and including a plurality of thermally conductive elements extending between the first and second surfaces so as to provide thermal conduction between the die and the cover.

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COMPLETE SPECIFICATION
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This document contains the amendments made under Section 49 and is correct for printing.

APPLICANT'S REFERENCE: 83-432AU

Name(s) of Applicant(s):

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UNITED STATES OF AMERICA.

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Complete Specification for the invention entitled:

SYSTEM FOR DETACHABLY MOUNTING SEMI-CONDUCTORS ON CONDUCTOR SUBSTRATES

Our Ref : 53249
POF Code: 775/1038

The following statement is a full description of this invention, including the best method of performing it known to applicant(s):

SYSTEM FOR DETACHABLY MOUNTING SEMICONDUCTORS ON CONDUCTOR SUBSTRATE

~~The present application is a continuation~~ in-part of application serial no. 757,~~600~~, filed on July 22, 1985.

BACKGROUND OF THE INVENTION

~~1. Field of the Invention~~

The present invention relates generally to systems for mounting semiconductor dies on conductor substrates, and more particularly to a system which provides for detachably mounting such semiconductor dies without soldering by interposing a resilient anisotropic conductor pad between the semiconductor die and the conductor substrate.

Integrated circuits are typically fabricated on relatively large silicon wafers which are then divided into a plurality of individual circuits, referred to as dies or chips. The individual dies may then be packaged in a variety of ways, including the familiar dual-in-line package, referred to as the DIP, where the die is encapsulated in plastic or ceramic. The individual DIPs may then be mounted and interconnected on printed circuit boards in order to build up the desired circuitry. Although workable, the use of discrete packages, such as DIPs, can result in unacceptable signal propagation delay time between the separated integrated circuits.

An approach which has been developed in order to reduce such signal propagation delay time involves mounting a plurality of discrete dies in a common enclosure on a single conductor substrate, typically a multilayer ceramic substrate. The dies are usually soldered directly to the conductor substrate and may be spaced together very closely in order to reduce the propagation delay time. The use of a common enclosure

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avoids the necessity of individually packaging the chips for protection.

The use of such multichip modules, however, suffers from a number of problems. It is desirable to have the module as small as possible in order to reduce the signal propagation delay as much as possible. The small module size makes it very difficult to locate and attach the individual dies. Moreover, the large number of dies in a single module greatly increases the likelihood of failure of the module since the chance of at least one die failing is greatly increased. Since the modules must be tested after assembly, the failure of a single die necessitates either discarding the entire module, which can be prohibitively expensive, or detaching and replacing the die or dies which have failed. Detaching the die can be very difficult since in most cases it will have been soldered to the conductor substrate. The problem is exacerbated if, as is frequently the case, the die has also been soldered to a heat sink to enhance heat dissipation.

For the above reasons, it would be desirable to provide alternate systems for the high density mounting of a plurality of semiconductor dies on a single conductor substrate. It would be particularly desirable to provide such systems which allow for detachably mounting the dies on the substrate without solder so that the dies may be easily removed from the substrate in the event of failure. The system should also provide for adequate heat dissipation without the need to solder or otherwise attach the dies to a heat sink, and should additionally provide for a minimum signal propagation delay time between the dies and the conductor substrate. Also, the electrical connections between the dies and the substrate should have a low resistance, and allow for differential thermal expansion between the dies and the substrate which is a particular problem with larger semiconductor dies.

Modules for mounting a plurality of semiconductor dies on a common conductor substrate are described in IBM Technical Disclosure Bulletin Vol. 13, Page 58; Vol. 19, pages 1270-1272; and Vol. 20, pages 3919-3920.

IBM Technical Disclosure Bulletin Vol. 25, pages 1801-1802, discloses an elastomeric layer having widely spaced, discrete spring elements embedded therein. The elastomeric layer is interposed between a chip carrier and a pin carrier to provide for electrical connection.

Elastomeric, anisotropic conductors are described in U.S. Patent Nos. 4,003,621; 3,982,320, and 3,862,790. None of these patents suggests the use of such conductors for directly mounting a semiconductor die on a conductor substrate.

US Patent Nos. 4667219 and 4667220 assigned to the assignee of the present application, disclose the use of soldered, flexible connectors mounted in a connector board for surface mounting of semiconductor dies.

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The present invention is a system for the detachable surface mounting of semiconductor dies on conductor substrates. The system may allow high density packing of a plurality of individual dies on a common conductor substrate in order to reduce the package size and minimize the signal propagation delay time between the dies. The system may eliminate the need for solder connecting the dies to the substrate, and may thus allow for disassembly and replacement of defective chips within the system and minimize damage to the chips from the soldering operation. The system may provide for low resistance contacts between the dies and the conductor board, and can provide for enhanced heat dissipation when desired.

The system of the present invention may be useful for mounting semiconductor dies of the type having a plurality of signal, power, and/or ground contacts formed on one face thereof. Such contacts are usually arranged in a two-dimensional array extending across the face, but may be arranged peripherally. The conductor substrate, which may be any conventional conductor board, including ceramic substrates and printed circuit boards, will have a plurality of surface contacts arranged in a pattern corresponding at least partly to the pattern of contacts on the semiconductor dies. Interconnection between the dies and the conductor substrate may be effected by a resilient, anisotropic conductor pad comprising a plurality of discrete conductive elements embedded in an elastomeric matrix. By spacing the conductors sufficiently closely, electrical conduction between contacts located on opposite sides of the pad may be assured. In this way, alignment of the conductor pad may not be necessary, so long as the semiconductor die and the conductor substrate are themselves in proper alignment.

In the preferred embodiment, alignment between the dies and the conductor substrate may be achieved using a nest plate having a plurality of apertures. The nest plate may be mounted on the conductor substrate, and the conductor pads and semiconductor dies may be placed in the

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apertures which are located to assure proper alignment. A cover may then be placed over the nest plate to compress the semiconductor die against the resilient conductor pad in order to establish low resistance electrical conduction. Preferably, the cover comprises a heat sink, and a second resilient conductor pad may be interposed between the upper face of the semiconductor die and the heat sink. The resilient pad helps evenly distribute downward force on the semiconductor die, and the metal conductors in the pad provide for enhanced thermal dissipation from the die to the heat sink.

According to one aspect of the present invention there is provided a semiconductor die mounting system comprising:

a) a conductor substrate having an array of substrate contacts on a substrate face thereof;

b) at least one semiconductor die having first and second opposed die faces and a plurality of die contacts on the first die face thereof disposed in alignment with corresponding substrate contacts on the conductor substrate;

c) a conductor pad disposed between the substrate and the die having first and second opposed pad surfaces in contact with the substrate face and first die face, respectively, the conductor pad including a plurality of electrically conductive elements mutually electrically isolated within the pad and extending between the first and second surfaces thereof in the direction of alignment between the substrate and die contacts so as to provide electrical conduction between the pad surfaces, adjacent conductive elements being spaced apart by less than the minimum width of the contacts; and

d) means for holding the semiconductor die and the conductor substrate in contact with the conductor pad so that the corresponding die and substrate contacts are in alignment.

According to a further aspect of the present invention there is provided a semiconductor die mounting system comprising:

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a) a conductor substrate having an array of substrate contacts on a substrate face thereof;

b) at least one semiconductor die having first and second opposed die faces and a plurality of die contacts on the first die face thereof disposed in alignment with corresponding substrate contacts on the conductor substrate;

c) a first conductor pad disposed between the substrate and the die having first and second opposed pad surfaces in contact with the substrate surface and first die face, respectively, the first conductor pad including a plurality of electrically conductive elements mutually electrically isolated within the pad and extending between the first and second surfaces thereof in the direction of alignment between the substrate and die contacts so as to provide electrical conduction between the pad surfaces, adjacent conductive elements being spaced apart by less than the minimum width of the contacts;

d) means for holding the semiconductor die and the conductor substrate in contact with the first conductor pad so that the corresponding die and substrate contacts are in alignment;

e) a cover mounted on the means for holding the semiconductor die and the conductor substrate, the cover including a cover face; and

f) a second conductor pad disposed between the semiconductor die and the cover, the second conductor pad having first and second opposed surfaces in contact with a cover face and the second die face, respectively, and including a plurality of thermally conductive elements extending between the first and second surfaces so as to provide thermal conduction between the die and the cover.

According to a still further aspect of the present invention there is provided a semiconductor die mounting system comprising:

a) a conductor substrate having an array of substrate contacts on a substrate face thereof;

b) at least one semiconductor die having first and second opposed die faces and a plurality of die contacts

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on the first die face thereof disposed in alignment with corresponding substrate contacts on the conductor substrate;

c) a first conductor pad disposed between the substrate and the die having first and second opposed pad surfaces in contact with the substrate face and first die face, respectively, the first conductor pad including a plurality of electrically conductive elements mutually electrically isolated within the pad and extending between the first and second surfaces thereof in the direction of alignment between the substrate and die contacts so as to provide electrical conduction between the pad surfaces, adjacent conductive elements being spaced apart by less than the minimum width of the contacts;

d) a nest plate mounted over the conductor substrate for aligning the contacts on the conductor substrate with the contacts on the semiconductor die;

e) a cover having a cover face mounted on the nest plate; and

f) a second conductor pad disposed between the semiconductor die and the cover, the second conductor pad having first and second opposed surfaces in contact with a cover face and the second die face, respectively, and including a plurality of thermally conductive elements extending between the first and second surfaces so as to provide thermal conduction between the die and the cover.

Preferred embodiments of the present invention will now be described with reference to the accompanying drawings wherein:-

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~~conductors in the pad provide for enhanced thermal~~ dissipation from the die to the heat sink.

~~BRIEF DESCRIPTION OF THE DRAWINGS~~

Fig. 1 illustrates a resilient anisotropic conductor pad useful in the mounting system of the present invention.

Fig. 2 is a detailed cross-sectional view illustrating the resilient anisotropic conductor pad of the present invention interposed between a semiconductor die and a conductor substrate.

Fig. 3 is an exploded view of the multiple die mounting system of the present invention, with portions broken away.

Fig. 4 illustrates the assembled mounting system of Fig. 3.

Fig. 5 is an alternate embodiment of the mounting system of the present invention adapted for surface mounting on a printed circuit board.

Fig. 6 is a second alternate embodiment of the mounting system of the present invention where semiconductor dies are mounted directly on opposite sides of a printed circuit board.

~~DESCRIPTION OF THE PREFERRED EMBODIMENTS~~

According to the present invention, semiconductor dies are detachably surface mounted on conductor substrates by interposing resilient, anisotropic conductor pads therebetween. The conductor pads provide for electrical conduction between contacts formed on one face of the chip and corresponding contacts formed on one face of the substrate. The mounting system is particularly useful for mounting a plurality of chips on a common substrate, although it will also find use in mounting single dies on a substrate.

Semiconductor dies are normally formed in multiples on a single silicon wafer on the order of several inches in diameter. The wafer is then divided

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into individual dies, usually on the order of 50 square millimeters or smaller, and each die will include thousands of individual transistors and other circuit elements. The die may provide memory, logic, or a variety of other useful functions. Of particular interest to the present invention are dies having electrical signal contacts formed on one face thereof. Such contacts will provide for power and ground connections, as well as signal connections. Typically, the contacts will be formed as metal contact pads in a predetermined two-dimensional array extending across the surface of the die. Alternatively, the contact pads may be formed linearly along the periphery of the face. The present invention provides a system for interconnecting such contact pads, including signal, power, and ground contact pads, to corresponding contact pads formed on a connector substrate.

The connector substrate may be any conventional connector substrate, including ceramic substrates, plastic substrates, printed circuit boards, and the like. The connector substrate will normally include internal metal traces defining appropriate conductive pads between preselected locations on the conductor board. For example, a contact pad connected to a semiconductor die may be interconnected with a contact pad on the same semiconductor die, with a contact pad on a different semiconductor die, or with an external contact on the conductor substrate. Such external contacts may be in the form of pins, solder pads, spring connectors, or the like.

The present invention employs a resilient, anisotropic conductor pad as the conductive interface between the semiconductor die and the conductive substrate. Such conductor pads must provide for anisotropic electrical conduction in one direction only, while providing very high resistivity, on the order of 10^{15} ohm-cm, in the other two orthogonal

directions. In this way, electrical conduction is provided between electrical contacts which are located directly across from each other on opposite sides of the conductor pad, while the contacts are electrically isolated from all other contacts which are not so aligned.

Referring now to Figs. 1 and 2, a resilient, anisotropic conductor pad 10 suitable for use in the present invention will typically comprise an elastomeric matrix 12 having a plurality of discrete conductive elements 14 embedded therein. The conductive elements 14 will be oriented parallel to one another so that contact between any two elements 14 is avoided. In this way, an electrical signal which is introduced to one of the elements 14 will be conducted through the pad 10 by that element only. The elastomeric matrix may be formed from a variety of electrically-insulating elastomers, such as silicone rubbers, including dimethyl, methyl-phenyl, methyl-vinyl, and halogenated siloxanes; butadiene-styrene, butadiene-acrylonitrile, butadiene-isobutylene, and the like.

The conductive elements 14 will usually be conductive metals, such as copper, aluminum, silver, gold, or alloys thereof, although conductive carbon fibers and the like may also find use.

The dimensions of the resilient, anisotropic conductive pad 10 will vary depending on the particular mounting system being constructed. Usually, the thickness T will be made as small as possible consistent with the need to maintain a resilient interface between the semiconductor die and the ceramic substrate. The thickness T will usually be in the range from about 0.01 to 0.30 inches, more usually in the range from 0.03 to 0.15 inches. The peripheral dimensions will frequently correspond to those of the

semiconductor die being mounted, although the dimensions may be greater.

Referring now to Fig. 2, the conductor pad 10 is interposed between a semiconductor die 20 and a conductor substrate 22. The semiconductor die 20 includes a plurality of surface contact pads 24 (only two of which are illustrated in Fig. 2) which are disposed directly against contact pad 10, while substrate 22 includes a plurality of corresponding contact pads 26 which are disposed against the opposite face of the conductive pad 10. The spacing S between adjacent conductors 14 will be selected to be less than the width W_c of the contact pad 24 or 26. In this way, contact between at least one element 14 and each contact pad 24 or 26 is assured. Usually, the spacing S will be selected to be less than half the width W_c of the contact pads 24 and 26 in order to assure that at least 2, and usually 4, conductors 14 will be in contact with each contact pad. In this way, electrical conduction between contact pads 24 on the die 20 and contact pads 26 on the substrate 22 is accomplished so long as the die and the substrate are properly aligned. The alignment of the conductive pad 10 is not critical so long as the spacing of the conductive elements 14 is uniform and sufficiently close.

Suitable anisotropic conductors may be fabricated by a variety of techniques. Suitable techniques are disclosed in U.S. Patent Nos. 4,003,621 and 4,729,166, ~~co-pending application serial no. 757,600~~, the latter of which is assigned to the assignee of the present invention. The relevant disclosures of both of these references are incorporated herein by reference.

Referring now to Figs. 3 and 4, a specific multiple semiconductor die mounting system constructed in accordance with the principles of the present invention will be described. A ceramic substrate 30

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includes a plurality of conductor regions 32 formed on one face thereof. Each conductor region 32 includes a multiplicity of individual contact pads 34. The ceramic substrate 30 further includes internal metallic traces 36 which interconnect the contacts 34 with other contacts 34 and connector pins 38. Connector pins 38 provide for connecting the module with external circuitry by means of a conventional pin receptacle (not shown) which may be mounted on a printed circuit board or other mounting surface.

A nest plate 44 includes a plurality of apertures 46 which are arranged in a pattern corresponding to the pattern of contact regions 32 on the substrate 30. By placing the nest plate over the ceramic substrate 30, the apertures 46 will be aligned with the contact regions 32 and will define receptacles for receiving the resilient conductor pads 10 and semiconductor dies 20. The apertures 46 will be aligned so that the individual contacts 24 (Fig. 2) on the semiconductor die 20 are aligned with corresponding contacts 32 on the substrate 30.

A second anisotropic conductor pad 50 will usually be mounted directly over the semiconductor pad 20. The pad 50 serves two purposes. First, the semiconductor 20 will be interposed between two resilient pads 10 and 50 which will protect the die during the module assembly procedure. Second, by providing the metallic conductors within the pad 50, thermal conduction from the die to a heat sink 52 is facilitated. The heat sink 52 acts as a cover when it is placed over the nest plate 44, compressing the layered structure of the resilient pads 10 and 50 and the semiconductor die 20.

The fully assembled module, with a portion broken away, is illustrated in Fig. 4.

Referring now to Fig. 5, an alternate embodiment of the multisemiconductor module of the present

invention is illustrated. The module 60 is identical to the module 30 of Figs. 3 and 4, except that the connector pins 38 are replaced by peripheral solder connectors 62. The solder connectors 62 are conventional and adapted for surface mounting on a printed circuit board or other suitable surface.

Referring now to Fig. 6, the mounting system of the present invention may be used to surface mount semiconductor dies directly on printed circuit boards or ceramic boards without use of discrete mounting modules. A printed circuit board 70 is a multilayer conductive substrate having a plurality of contact regions formed on both surfaces thereof. Contact pads are mounted directly over the contact regions, while semiconductor dies 20 are mounted over the conductor pads 10. Second conductor pads 50 are mounted over the semiconductor dies 20, and the layered structures are aligned in nest plates 44, as described previously. The nest plates 44, in turn, are covered by heat sinks 52 which are detachably secured directly to the printed circuit board 70 by bolts 72.

It will be appreciated that each of the mounting systems described hereinabove may be disassembled without the need to break any solder contacts or other permanent connections made between the semiconductor dies and the conductor substrates. This is a particular advantage since it allows the entire mounting system to be assembled, and fully tested and burned in. If any of the individual semiconductor dies are found to be defective, the mounting system may be disassembled, the defective die removed and replaced. This eliminates the need to dispose of the expensive mounting systems because of the failure of a single component.

Although the foregoing invention has been described in some detail by way of illustration and example for purposes of clarity of understanding, it

will be obvious that certain changes and modifications may be practiced within the scope of the appended claims.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A semiconductor die mounting system comprising:

a) a conductor substrate having an array of substrate contacts on a substrate face thereof;

b) at least one semiconductor die having first and second opposed die faces and a plurality of die contacts on the first die face thereof disposed in alignment with corresponding substrate contacts on the conductor substrate;

c) a conductor pad disposed between the substrate and the die having first and second opposed pad surfaces in contact with the substrate face and first die face, respectively, the conductor pad including a plurality of electrically conductive elements mutually electrically isolated within the pad and extending between the first and second surfaces thereof in the direction of alignment between the substrate and die contacts so as to provide electrical conduction between the pad surfaces, adjacent conductive elements being spaced apart by less than the minimum width of the contacts; and

d) means for holding the semiconductor die and the conductor substrate in contact with the conductor pad so that the corresponding die and substrate contacts are in alignment.

2. A semiconductor die mounting system as claimed in claim 1 wherein the means for holding the semiconductor die and the conductor pad includes:

a) a nest plate mounted over the conductor substrate for aligning the contacts on the conductor substrate with the contacts on the semiconductor die; and

b) a cover mounted on the nest plate.

3. A semiconductor die mounting system as claimed in claim 2 wherein:

a) the cover includes a cover face; and

b) the semiconductor mounting system further includes a second conductor pad disposed between the semiconductor die and the cover, the second conductor pad having first and second opposed surfaces in contact with a

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cover face and the second die face, respectively, and including a plurality of thermally conductive elements extending between the first and second surfaces so as to provide thermal conduction between the die and the cover.

4. A semiconductor die mounting system as claimed in claim 3 further comprising means for sealing the periphery of the cover to the periphery of the conductor substrate so that the semiconductor die and the conductor pads are compressed against the conductor substrate.

5. A semiconductor die mounting system as claimed in claim 3 or 4 wherein the first and second conductor pads are resilient.

6. A semiconductor die mounting system as claimed in any one of claims 2-5 wherein the cover comprises a heat sink.

7. A semiconductor die mounting system as claimed in claim 1 or 2 wherein the conductor pad is resilient.

8. A semiconductor die mounting system as claimed in any one of the preceding claims wherein the conductor substrate comprises ceramic.

9. A semiconductor die mounting system as claimed in any one of the preceding claims wherein the substrate includes a pin grid on a face opposite the array of contacts.

10. A semiconductor die mounting system as in any one of claims 1-7 wherein the substrate includes edge connectors formed about its periphery.

11. A semiconductor die mounting system as claimed in any one of the preceding claims wherein the substrate includes a plurality of arrays of contacts formed on the substrate face and wherein a separate conductor pad is mounted on each array of contacts.

12. A semiconductor die mounting system comprising:

a) a conductor substrate having an array of substrate contacts on a substrate face thereof;

b) at least one semiconductor die having first and second opposed die faces and a plurality of die contacts on the first die face thereof disposed in alignment with corresponding substrate contacts on the conductor

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substrate;

c) a first conductor pad disposed between the substrate and the die having first and second opposed pad surfaces in contact with the substrate surface and first die face, respectively, the first conductor pad including a plurality of electrically conductive elements mutually electrically isolated within the pad and extending between the first and second surfaces thereof in the direction of alignment between the substrate and die contacts so as to provide electrical conduction between the pad surfaces, adjacent conductive elements being spaced apart by less than the minimum width of the contacts;

d) means for holding the semiconductor die and the conductor substrate in contact with the first conductor pad so that the corresponding die and substrate contacts are in alignment;

e) a cover mounted on the means for holding the semiconductor die and the conductor substrate, the cover including a cover face; and

f) a second conductor pad disposed between the semiconductor die and the cover, the second conductor pad having first and second opposed surfaces in contact with a cover face and the second die face, respectively, and including a plurality of thermally conductive elements extending between the first and second surfaces so as to provide thermal conduction between the die and the cover.

13. A semiconductor die mounting system as claimed in claim 12 wherein the means for holding the semiconductor die and the conductor pad includes a nest plate mounted over the conductor substrate for aligning the contacts on the conductor substrate with the contacts on the semiconductor die.

14. A semiconductor die mounting system as claimed in claim 12 or 13 further comprising means for sealing the periphery of the cover to the periphery of the conductor substrate so that the semiconductor die and the conductor pads are compressed against the conductor substrate.

15. A semiconductor die mounting system as claimed in any one of claims 12-14 wherein the first and second

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conductor pads are resilient.

16. A semiconductor die mounting system as claimed in any one of claims 12-15 wherein the cover comprises a heat sink.

17. A semiconductor die mounting system comprising:

a) a conductor substrate having an array of substrate contacts on a substrate face thereof;

b) at least one semiconductor die having first and second opposed die faces and a plurality of die contacts on the first die face thereof disposed in alignment with corresponding substrate contacts on the conductor substrate;

c) a first conductor pad disposed between the substrate and the die having first and second opposed pad surfaces in contact with the substrate face and first die face,respectively, the first conductor pad including a plurality of electrically conductive elements mutually electrically isolated within the pad and extending between the first and second surfaces thereof in the direction of alignment between the substrate and die contacts so as to provide electrical conduction between the pad surfaces, adjacent conductive elements being spaced apart by less than the minimum width of the contacts;

d) a nest plate mounted over the conductor substrate for aligning the contacts on the conductor substrate with the contacts on the semiconductor die;

e) a cover having a cover face mounted on the nest plate; and

f) a second conductor pad disposed between the semiconductor die and the cover, the second conductor pad having first and second opposed surfaces in contact with a cover face and the second die face, respectively, and including a plurality of thermally conductive elements extending between the first and second surfaces so as to provide thermal conduction between the die and the cover.

18. A semiconductor die mounting system as claimed in claim 17 further comprising means for sealing the periphery of the cover to the periphery of the conductor substrate so that the semiconductor die and the conductor

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pads are compressed against the conductor substrate.

19. A semiconductor die mounting system as claimed in claim 17 or 18 wherein the first and second conductor pads are resilient.

20. A semiconductor die mounting system as claimed in any one of claims 17-19 wherein the cover comprises a heat sink.

21. A semiconductor die mounting system substantially as herein described with reference to figures 1-4 or figure 5 or figure 6 of the accompanying drawings.

DATED: 20 February 1990.

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AUSTRALIAN PATENT OFFICE LS

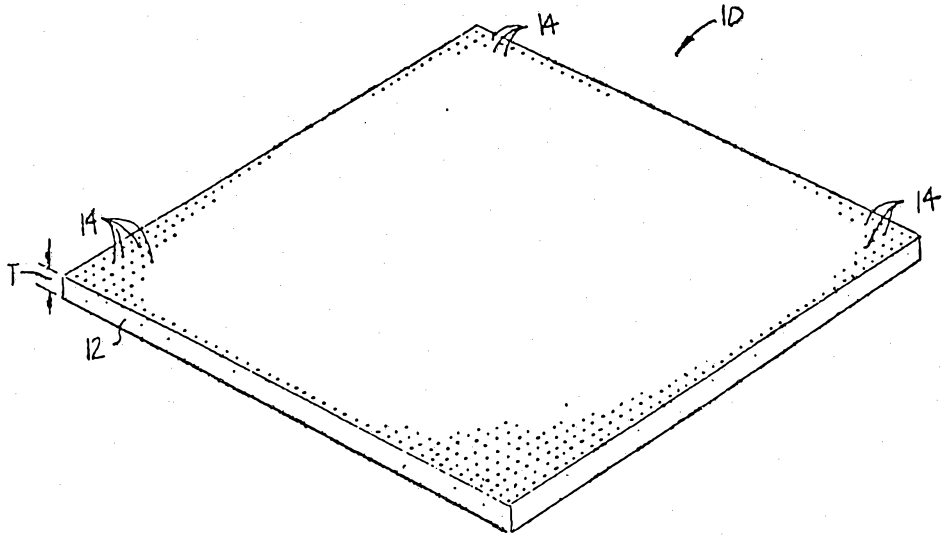


FIG. 1.

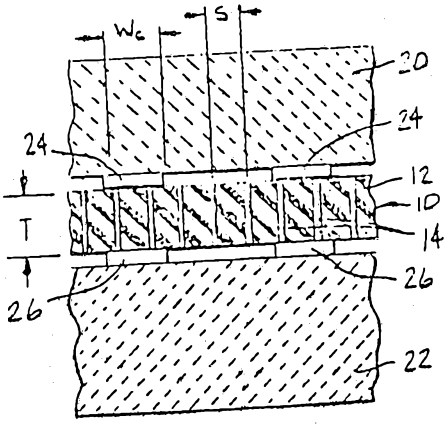
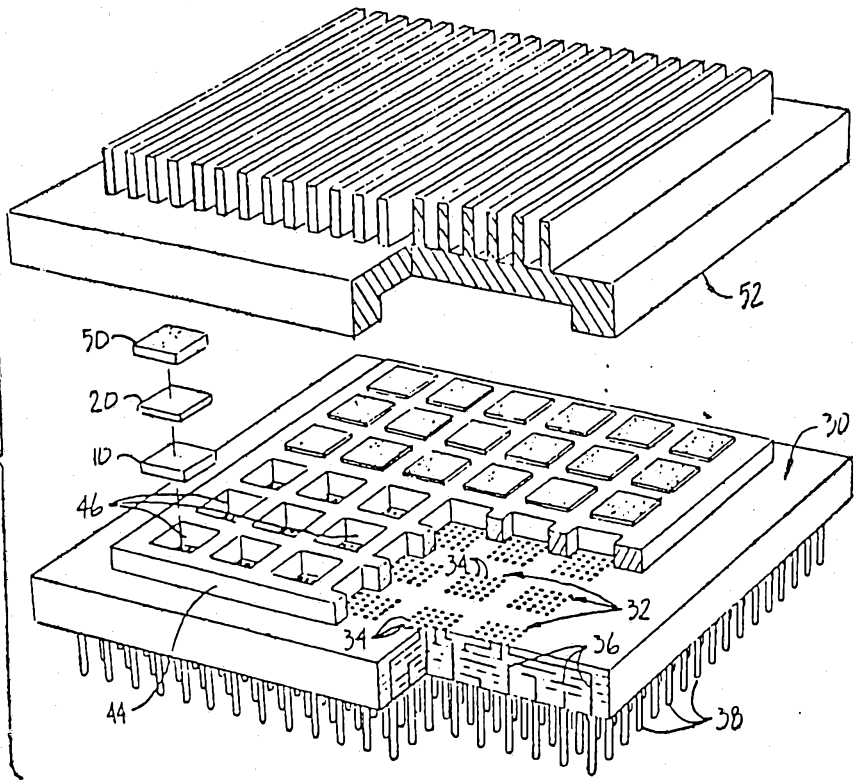


FIG. 2.

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FIG_3.



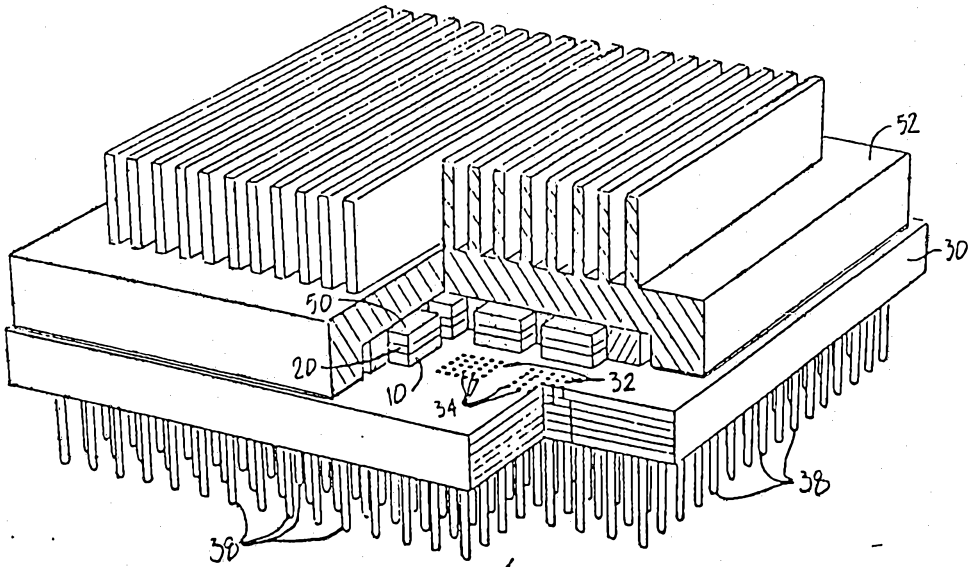


FIG_4.

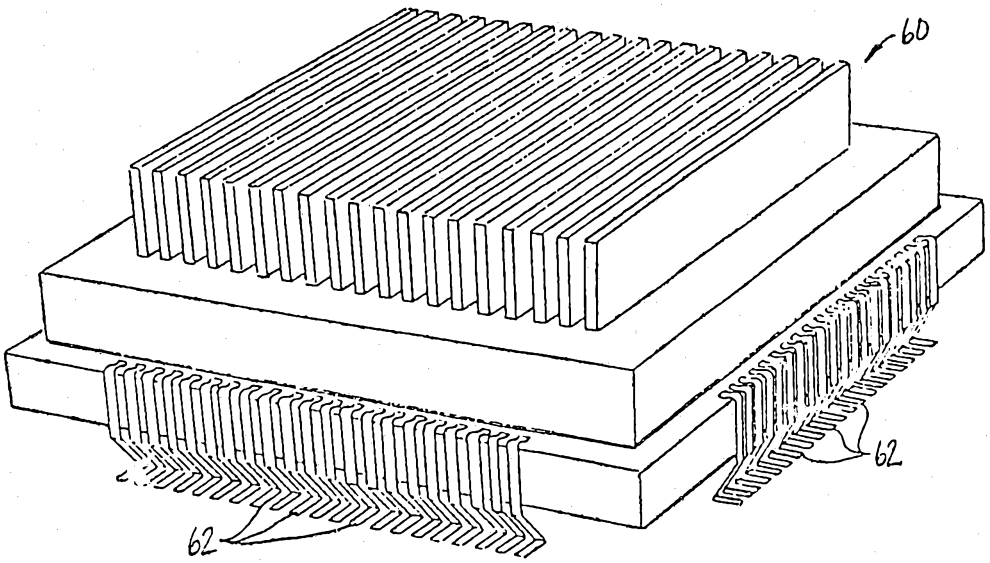


FIG._5.

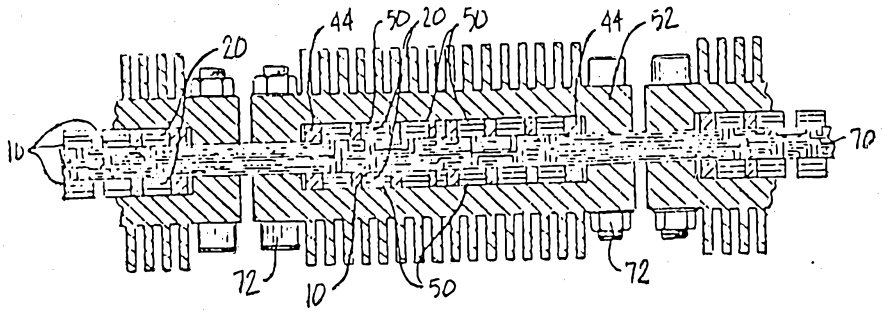


FIG._6.