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(54) Title: A DYNAMIC VOLTAGE SCALING SCHEME FOR AN ON-DIE VOLTAGE DIFFERENTIATOR DESIGN

(57) Abstract: According to one embodiment, an integrated circuit is disclosed. The integrated circuit includes a plurality of circuit blocks. Each circuit block includes a voltage differentiator that generates a local supply for the circuit block.

A DYNAMIC VOLTAGE SCALING SCHEME FOR AN ON-DIE VOLTAGE DIFFERENTIATOR DESIGN

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FIELD OF THE INVENTION

[0002] The present invention relates to integrated circuits; more particularly, the present invention relates to generating multiple power supply voltages on an integrated circuit.

BACKGROUND

[0003] Recently, power consumption has become an important concern for high performance computer systems. Consequently, low power designs have become significant for present-day very large scale integration (VLSI) systems. The most effective way to reduce power dissipation in an integrated circuit (IC) is by decreasing the power supply voltage (V_{CC}) at the IC.

[0004] In order to simultaneously achieve high performance and low power, multi-V_{CC} design, various techniques have been developed. However, due to the high cost of packaging and routing, it is typically difficult to generate multi-V_{CC} designs using traditional off-chip voltage regulators.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present invention will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the invention. The drawings, however, should not be taken to limit the invention to the specific embodiments, but are for explanation and understanding only.

[0006] **Figure 1** is a block diagram of one embodiment of an integrated circuit;

[0007] **Figure 2** is a block diagram of one embodiment of a circuit block;

[0008] **Figure 3** illustrates one embodiment of a voltage differentiator;

[0009] **Figure 4** illustrates one embodiment of a reference voltage selector; and

[0010] **Figure 5** illustrates one embodiment of a linear voltage regulator.

DETAILED DESCRIPTION

[0011] A mechanism to dynamically scale voltage at one or more circuit blocks on an integrated circuit (IC) using on-die voltage differentiators is described. In the following description, numerous details are set forth. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention.

[0012] Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the

invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

[0013] **Figure 1** is a block diagram of one embodiment of an IC 100. According to one embodiment, IC 100 is partitioned into twenty-five circuit blocks 110. In a further embodiment, each circuit block 110 includes a voltage differentiator 120. Each voltage differentiator 120 generates a local power supply (V_{CC}_local) from an external power supply (V_{CC}_global).

[0014] In one embodiment, differentiator 120 dynamically changes V_{CC}_local based upon the operation status of the particular circuit block 110 in which the differentiator 120 is included. One of ordinary skill in the art will appreciate that other quantities of circuit blocks 110 may be implemented within IC 100.

[0015] **Figure 2** is a block diagram of one embodiment of a circuit block 110. Circuit block 110 includes voltage differentiator 120, a functional unit block (FUB) 230 and a control module 250. FUB 230 is coupled to voltage differentiator 120. In one embodiment, FUB 230 is logic circuitry that may encompass various components within IC 100 (e.g., microprocessor logic, microcontroller logic, memory logic, etc.). FUB 230 is powered by V_{CC}_local received from voltage differentiator 120.

[0016] Control module 250 is coupled to voltage differentiator 120 and FUB 230. According to one embodiment, control module 250 transmits a binary encoded signal to voltage differentiator 120 that is used to scale the local operating voltage generated at voltage differentiator 120. In a further embodiment, control module 250 transmits either a local control signal or a global

control signal. In yet another embodiment, the global control signal overrides the local control signal.

[0017] **Figure 3** illustrates one embodiment of voltage differentiator 120 coupled to control module 250. Voltage differentiator 120 includes bandgap reference circuit 310, reference voltage selector 320 and linear voltage regulator 330. Bandgap reference circuit 310 generates a bandgap reference voltage V_{BG}. In one embodiment, V_{BG} is a stable voltage source that is insensitive to temperature and process variations.

[0018] Reference voltage selector 320 is coupled to bandgap reference circuit 310 and control module 250. Reference voltage selector 320 generates a reference voltage (V_{REF}) for linear voltage regulator 330. **Figure 4** illustrates one embodiment of reference voltage selector 320. Reference voltage selector 320 includes PMOS voltage divider transistors P1-Pn, PMOS pass transistors P11-Pn-1 and a NMOS transistor N. According to one embodiment, up to n-1 voltage levels can be selected. For instance, if four voltage levels are needed, four PMOS pass transistors P11-P14 are used.

[0019] In one embodiment, voltage divider transistors P1-Pn are series connected transistors that provide a variable resistance to V_{BG} received from bandgap reference circuit 310 in order to generate V_{REF}. For instance, if the number of transistors in the voltage divider is n, the granularity of V_{REF} is V_{BG}/n.

[0020] In one embodiment, V_{REF} is determined by the encoded control signal received at transistors P11-P14 from control module 250. The received signal is determined by the operation status of FUB 230. For example, if a relatively high V_{REF} is needed, the binary control signal 01110 is received at transistors P11-P14 and transistor N, respectively. As a result, only transistor P11

is activated and V_{REF} is equal to V_{BG} * (1-1/n), where n is the number of transistors in the voltage divider. Similarly, V_{REF} is equal to V_{BG} * (1-2/n), V_{BG} * (1-3/n) and V_{BG} * (1-4/n) when the control signal is 10110, 11010, 11100, respectively.

[0021] According to one embodiment, the value of V_{CC}_local changes dynamically based upon the activity of the corresponding FUB 230. For instance, if a FUB 230 requires a relatively high voltage, a higher V_{REF} is generated by reference voltage selector 320. Consequently, a higher V_{CC}_local is generated by line voltage regulator 330. Conversely, if a FUB 230 requires a relatively low voltage, lower V_{REF} and V_{CC}_local voltages are generated.

[0022] In a further embodiment, a higher V_{REF} may be needed to satisfy performance requirements for circuit blocks 110 that are in a critical path. However, for other circuit blocks 110 that are not in a critical path, a lower V_{REF} can be selected to reduce power dissipation. In a further embodiment, control module 250 may cause circuit block 110 to enter a standby mode by transmitting 11111 as the control signal. In such an instance, only transistor N is activated, and a V_{REF} of 0V is transmitted to linear voltage regulator 330.

[0023] Referring back to **Figure 3**, linear voltage regulator 330 generates V_{CC}_local for circuit block 110. **Figure 5** illustrates one embodiment of linear voltage regulator 330. Linear voltage regulator 330 includes a comparator 530, a PMOS transistor (P), resistors R1 and R2 and a capacitor. Comparator compares the V_{REF} received from reference voltage selector 320 with a feedback voltage (V_{FB}) received from transistor P through resistors R1 and R2.

[0024] If V_{FB} falls below V_{REF}, the output of comparator 530 is activated at a low logic level (e.g., logic 0). Otherwise, the output of comparator 530 remains at high logic level (e.g., logic 1). According to one embodiment, comparator 530 is

an operational amplifier. However, one of ordinary skill in the art will recognize that other comparison logic circuitry may be used to implement comparator 530.

[0025] The output of comparator 530 is coupled to the gate of transistor P. The source of transistor P is coupled to V_{CC}_global, while the drain is coupled to resistor R1, the capacitor and FUB 230 through V_{CC}_local. Transistor P is activated whenever comparator 530 is activated to logic 0.

[0026] Resistor R1 is coupled to resistor R2 and comparator 530. Resistors R1 and R2 are used to generate V_{FB} for comparator 530. Resistors R1 and R2, and the generation of V_{FB}, help to control the output of linear voltage regulator 330 by providing a larger voltage range. However, one of ordinary skill in the art will appreciate that resistors R1 and R2 are not necessary to implement linear voltage regulator 330.

[0027] As described above, the value of V_{CC}_local changes dynamically based upon the activity of the corresponding FUB 230. During the active mode, transistor P is activated whenever V_{FB} falls below V_{REF}. In particular, comparator 530 senses such a condition and is activated to logic 0. Consequently, the gate of transistor P is activated to logic 0. Transistor P charges the decouple capacitor, thus increasing V_{CC}_local. In the active mode, linear voltage regulator 330 generates V_{CC}_local = V_{REF} * (1 + R1/R2).

[0028] During the standby mode, V_{REF} is 0. Accordingly, V_{FB} is always greater than or equal to V_{REF}, and the output of the comparator is logic 1 and transistor P is turned off. As a result, V_{CC}_local is floating to reduce the leakage power at circuit block 110.

[0029] The use of on-die voltage differentiators enables the generation of a local power supply voltage for each circuit block within an IC. The local power

supply voltage changes dynamically based on the activity of the corresponding circuit block. This reduces the power dissipation while maintaining performance. Moreover, the dynamic voltage scaling mechanism using on-die voltage differentiator has a standby control capability, which can drastically reduce leakage power during idle time for a circuit block.

[0030] Whereas many alterations and modifications of the present invention will no doubt become apparent to a person of ordinary skill in the art after having read the foregoing description, it is to be understood that any particular embodiment shown and described by way of illustration is in no way intended to be considered limiting. Therefore, references to details of various embodiments are not intended to limit the scope of the claims which in themselves recite only those features regarded as the invention.

CLAIMS

What is claimed is:

1. An integrated circuit comprising a plurality of circuit blocks, each circuit block having a voltage differentiator that generates a local power supply for the circuit block.

2. The integrated circuit of claim 1 wherein each voltage differentiator dynamically modifies the local power supply based upon the operation status of the corresponding circuit block.

3. The integrated circuit of claim 2 wherein each of the plurality of circuit blocks operates in a standby mode whenever the voltage differentiator switches off the local power supply.

4. The integrated circuit of claim 2 further comprising a first circuit block comprising:

a first voltage differentiator;

a first functional unit block (FUB) coupled to the first voltage differentiator; and

a first control module, coupled to the first voltage differentiator and the first FUB, that determines the operation mode for the first circuit block.

5. The integrated circuit of claim 4 wherein the control module generates a binary encoded signal that is transmitted to the first voltage differentiator to indicate the voltage magnitude of the local power supply.

6. The integrated circuit of claim 5 wherein the first voltage differentiator comprises:

a bandgap reference circuit that generates a bandgap voltage;

a reference voltage selector, coupled to the bandgap reference circuit and the control module, that generates a reference voltage based upon the received bandgap voltage; and

a linear voltage regulator, coupled to the reference voltage selector, that generates the local power supply based upon the received reference voltage.

7. The integrated circuit of claim 6 wherein the reference voltage selector comprises:

a plurality of voltage divider transistors that divide the bandgap voltage to generate the reference voltage; and

a plurality of pass transistors, coupled to the control module, that select a reference voltage based upon the received signal received from the control module.

8. The integrated circuit of claim 6 wherein the linear voltage regulator comprises:

a comparator, coupled to the reference voltage selector, that compares the reference voltage to the local power supply voltage;

a PMOS transistor having a gate coupled to the output of the comparator and a drain coupled to the FUB; and

a capacitor coupled to the drain of the PMOS transistor.

9. The integrated circuit of claim 8 wherein the linear voltage regulator

comprises:

a first resistor coupled to the drain of the PMOS transistor; and

a second resistor coupled to the first resistor, the comparator and ground.

10. The integrated circuit of claim 8 wherein the comparator comprises an operational amplifier.

11. The integrated circuit of claim 4 further comprising a second circuit block, the second circuit block comprising:

a second voltage differentiator;

a second FUB coupled to the second voltage differentiator; and

a second control module, coupled to the second voltage differentiator and the second FUB, that determines the operation mode for the second circuit block.

12. A circuit block within an integrated circuit, the circuit block comprising:

a control module;

a functional unit block (FUB) coupled to the control module; and

a voltage differentiator, coupled to the control module and the FUB, that dynamically modifies the local power supply for the circuit block based upon the operation status of the FUB.

13. The circuit block of claim 12 wherein the circuit block operates in a standby mode whenever the voltage differentiator switches off the local power supply.

14. The circuit block of claim 12 wherein the control module generates a binary encoded signal that is transmitted to the voltage differentiator to indicate the voltage magnitude of the local power supply.

15. The circuit block of claim 14 wherein the voltage differentiator comprises:

a bandgap reference circuit that generates a bandgap voltage;

a reference voltage selector, coupled to the bandgap reference circuit and the control module, that generates a reference voltage based upon the received bandgap voltage; and

a linear voltage regulator, coupled to the reference voltage selector, that generates the local power supply based upon the received reference voltage.

16. The circuit block of claim 15 wherein the reference voltage selector comprises:

a plurality of voltage divider transistors that divide the bandgap voltage to generate the reference voltage; and

a plurality of pass transistors, coupled to the control module, that select a reference voltage based upon the received signal received from the control module.

17. The circuit block of claim 15 wherein the linear voltage regulator comprises:

a comparator, coupled to the reference voltage selector, that compares the reference voltage to the local power supply voltage;

a PMOS transistor having a gate coupled to the output of the comparator and a drain coupled to the FUB; and

a capacitor coupled to the drain of the PMOS transistor.

18. The circuit block of claim 17 wherein the linear voltage regulator comprises:

a first resistor coupled to the drain of the PMOS transistor; and

a second resistor coupled to the first resistor, the comparator and ground.

19. The circuit block of claim 18 wherein the comparator comprises an operational amplifier.

20. A voltage differentiator comprising:

a bandgap reference circuit that generates a bandgap voltage;

a reference voltage selector, coupled to the bandgap reference circuit and the control module, that generates a reference voltage based upon the received bandgap voltage; and

a linear voltage regulator, coupled to the reference voltage selector, that generates a local power supply based upon the received reference voltage.

21. The voltage differentiator of claim 20 wherein the reference voltage selector comprises:

a plurality of voltage divider transistors that divide the bandgap voltage to generate the reference voltage; and

a plurality of pass transistors, coupled to the control module, that select a reference voltage based upon the received signal received from the control module.

22. The voltage differentiator of claim 20 wherein the linear voltage regulator comprises:

a comparator, coupled to the reference voltage selector, that compares the reference voltage to the local power supply voltage;

a PMOS transistor having a gate coupled to the output of the comparator and a drain coupled to the FUB; and

a capacitor coupled to the drain of the PMOS transistor.

23. The voltage differentiator of claim 22 wherein the linear voltage regulator comprises:

a first resistor coupled to the drain of the PMOS transistor; and

a second resistor coupled to the first resistor, the comparator and ground.

5

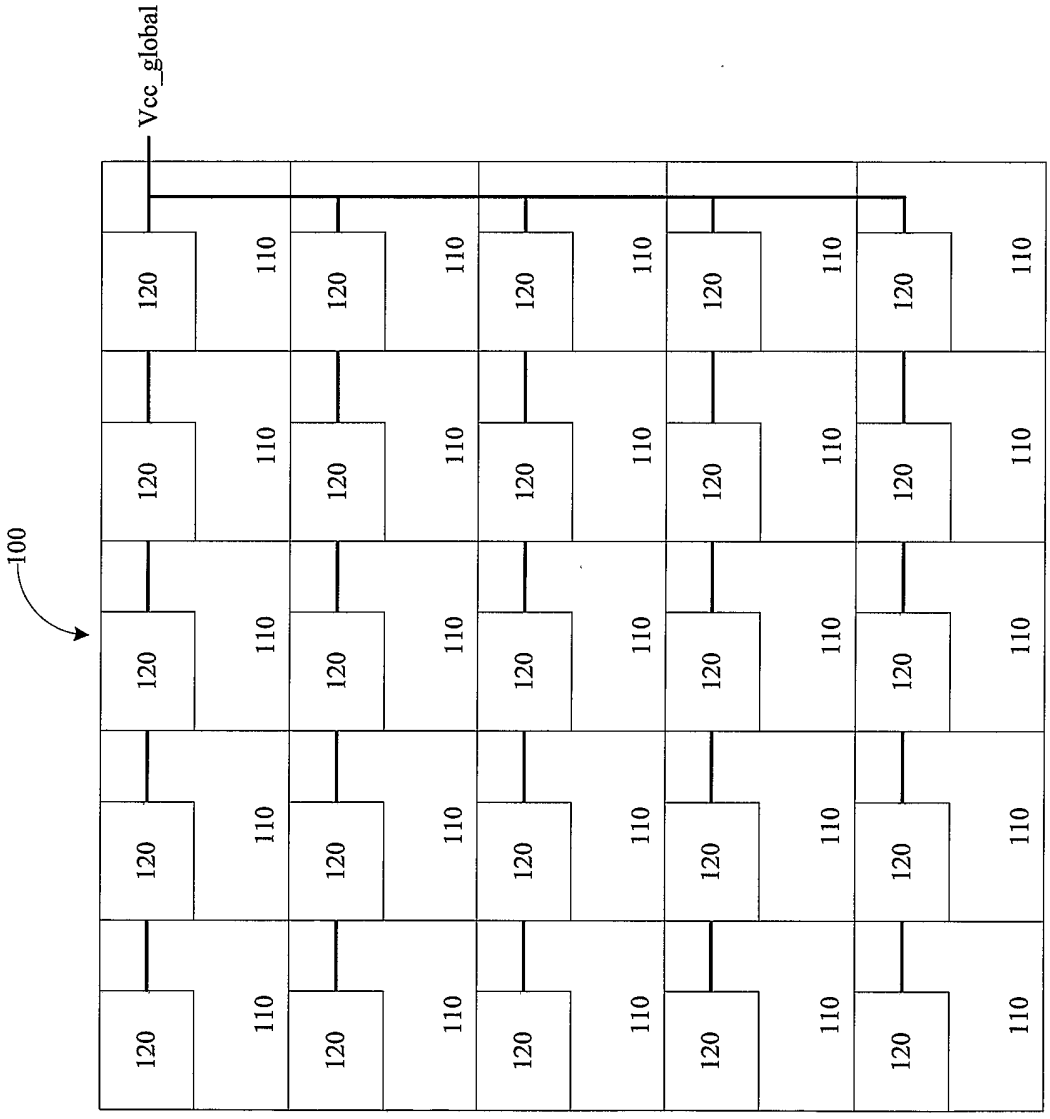

FIG. 1

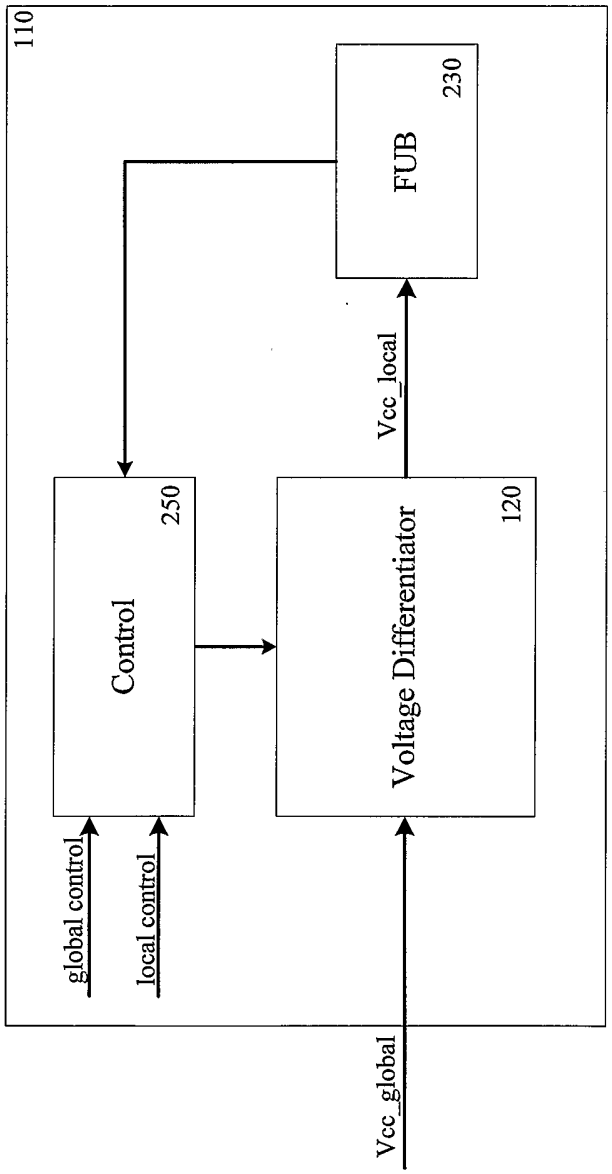
110
FUB
230
Vcc_local
Control
250
Voltage Differentiator
120
global control
local control
Vcc_global

FIG. 2

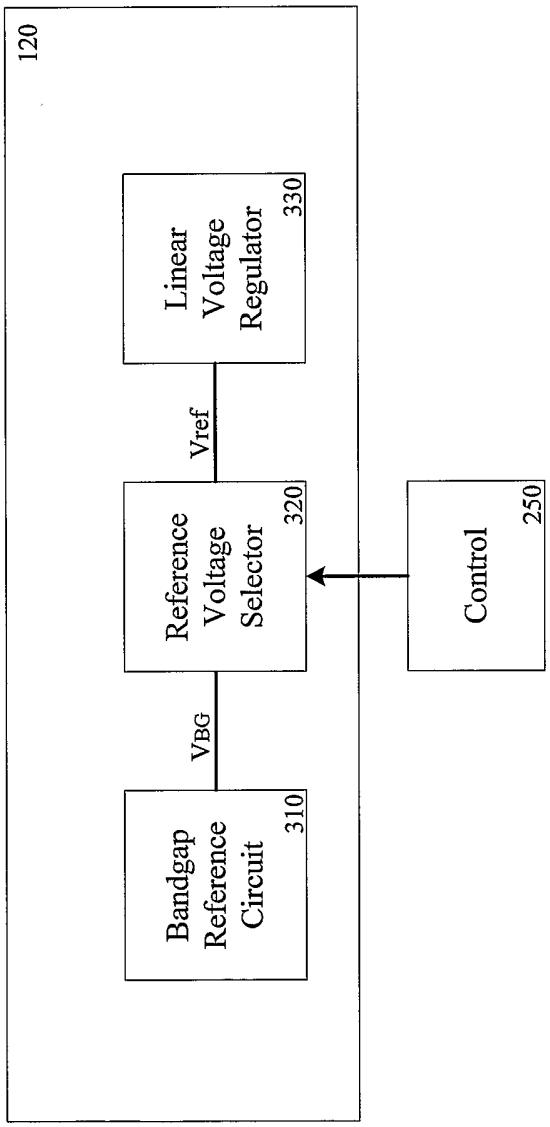
120
Linear Voltage Regulator
330
Vref
Reference Voltage Selector
320
Control
250
VBG
Bandgap Reference Circuit
310

FIG. 3

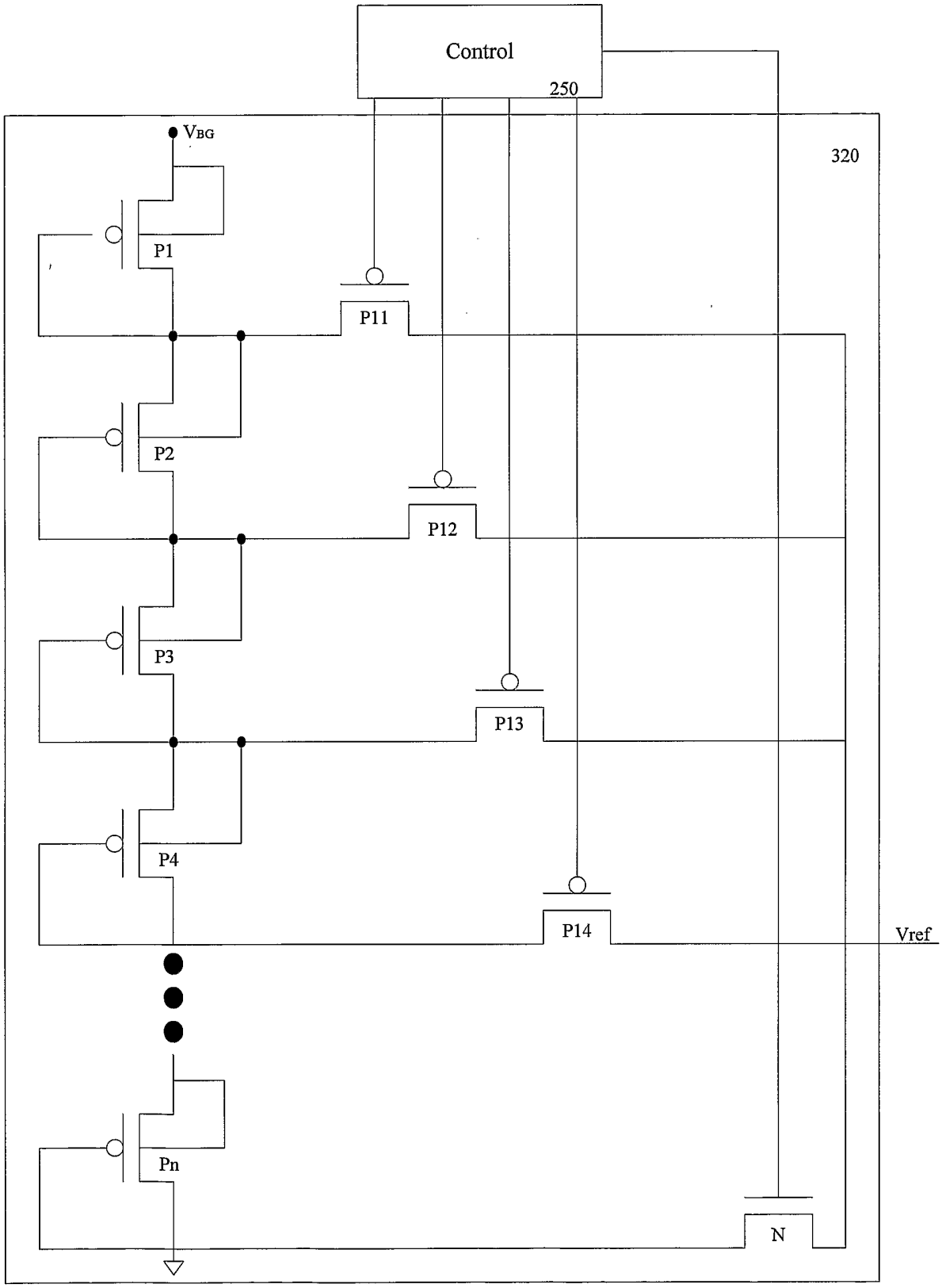

FIG. 4

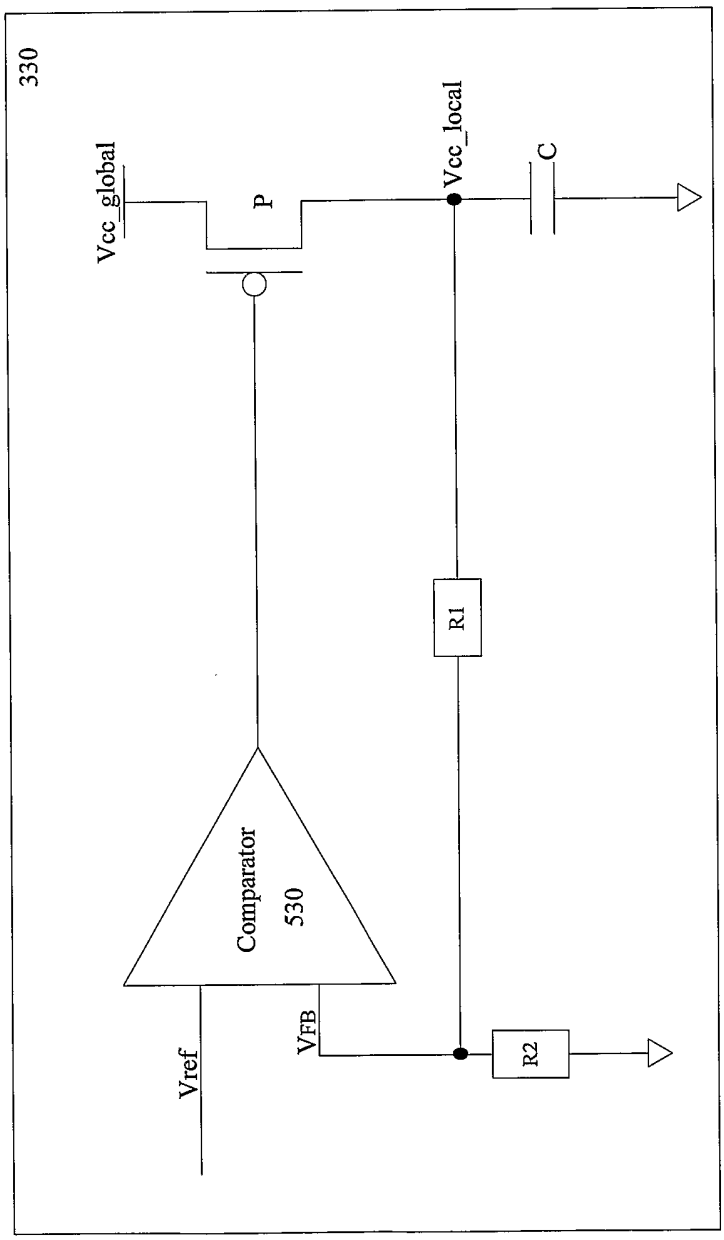

FIG. 5