

- [54] **BULK ERASE SYSTEM FOR GAS
DISCHARGE DISPLAY PANELS**
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- [73] **Assignee: Owens-Illinois, Inc., Toledo, Ohio**
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[58] Field of Search 340/324 R, 324 M,
340/166 R, 166 EL, 173 PL; 315/169 R, 169
TV: 313/108 B: 178/7.3 D

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|------------------------------|--------|--------------------------------|
| [56] References Cited | | |
| UNITED STATES PATENTS | | |
| 3,609,658 | 9/1971 | Soltan 340/166 R |
| 3,644,925 | 2/1972 | Kupsky 315/169 TV X |
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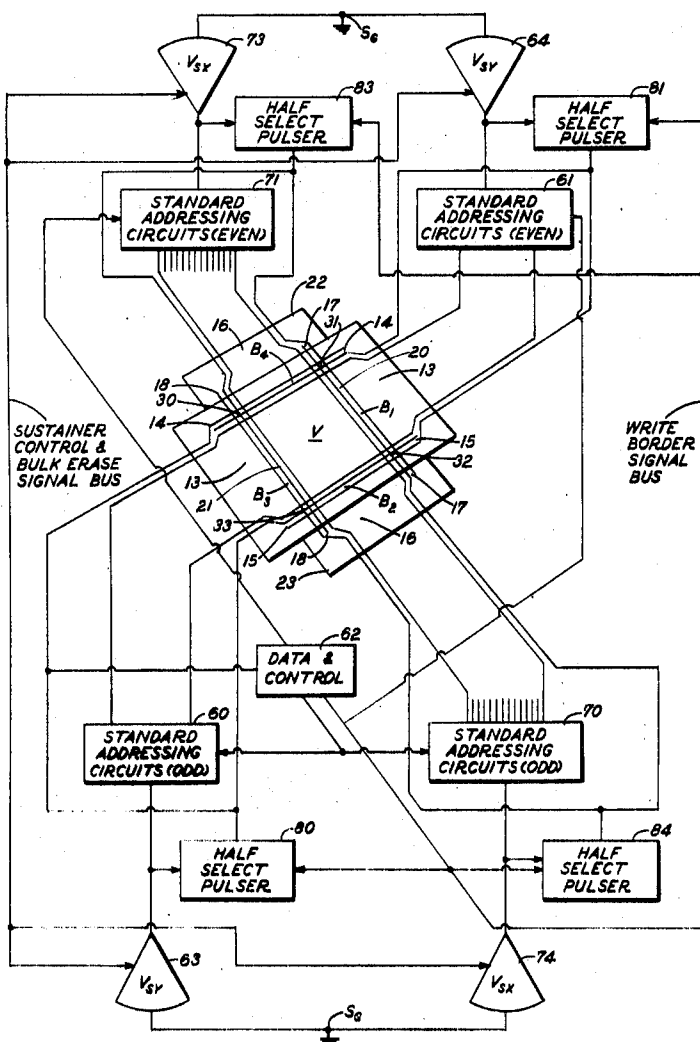
3,654,508 4/1972 Caras..... 315/169 TV X

Primary Examiner—David L. Trafton
Attorney—Donald Keith Wedding et al.

[57] **ABSTRACT**

In gaseous discharge display panels of the crossed conductor matrix type wherein the conductors are non-conductively coupled to the gas border discharge sites are normally maintained on for information or data display site conditioning purposes. According to the invention, rather than maintaining the border sites on while bulk erasing the entire panel, in the process of this invention, the border sites as well as the panel display areas are erased and then the border is rewritten. Circuitry is provided for inserting in the border conductors locating the border sites a voltage with the sustainer signal voltage following a bulk erase of all the signals due to sustainer control.

6 Claims, 7 Drawing Figures



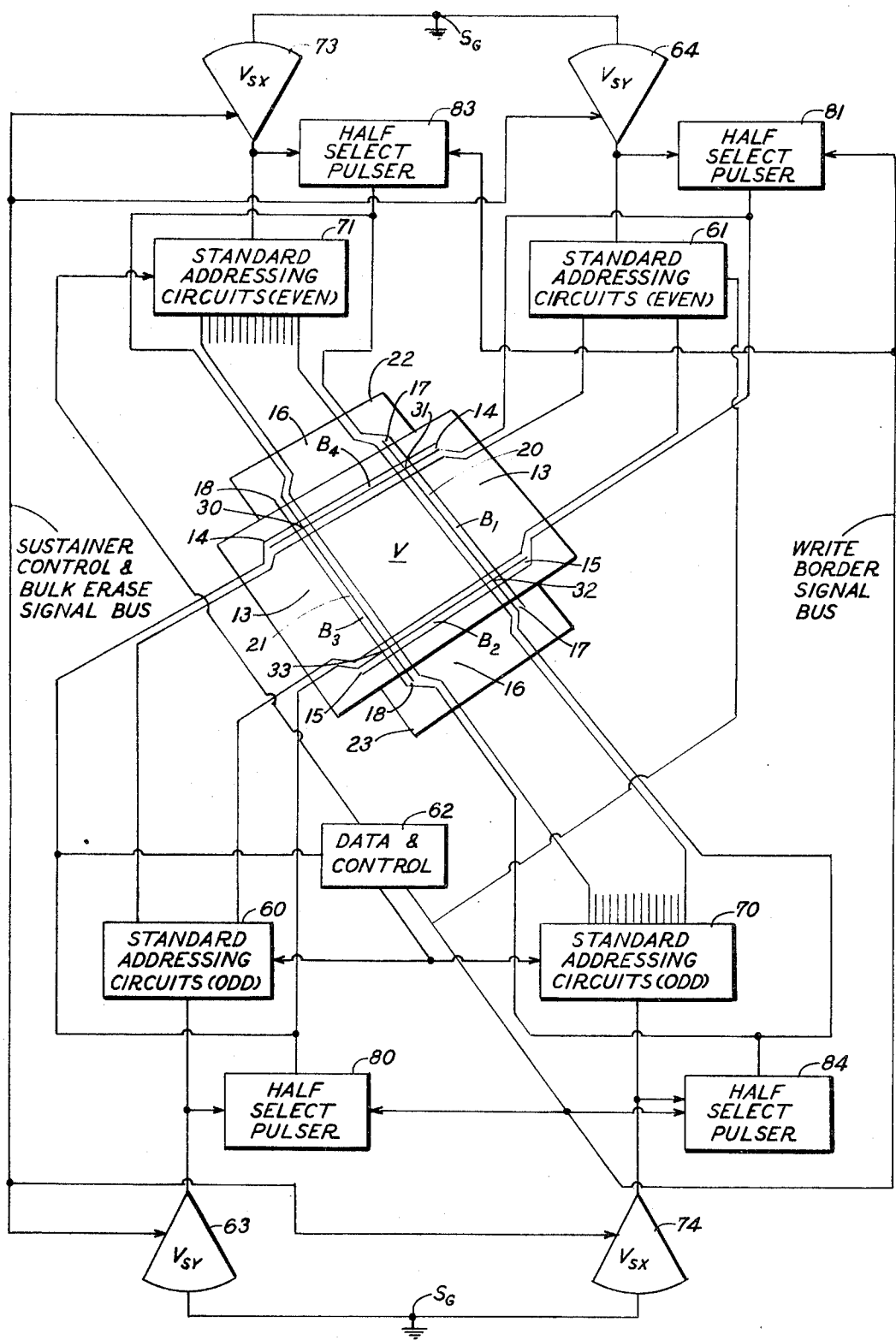


FIG.1

SHEET 2 OF 2

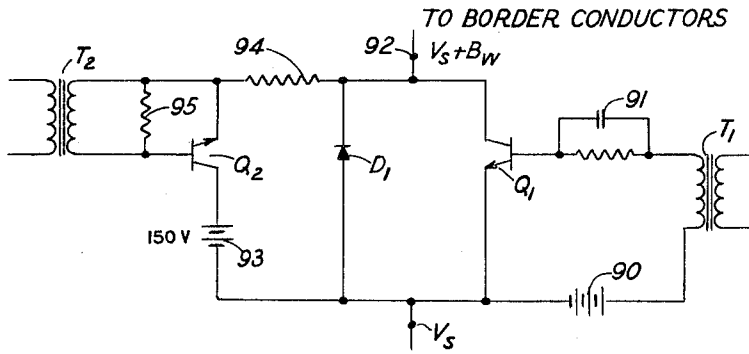


FIG. 2

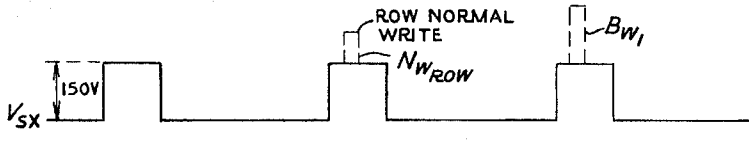


FIG. 3A

ROW (V_{SX})

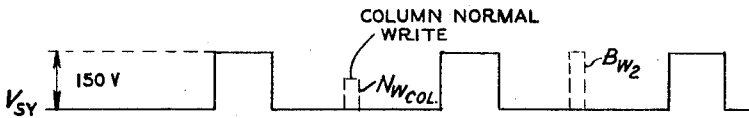


FIG. 3B

COLUMN (V_{SY})

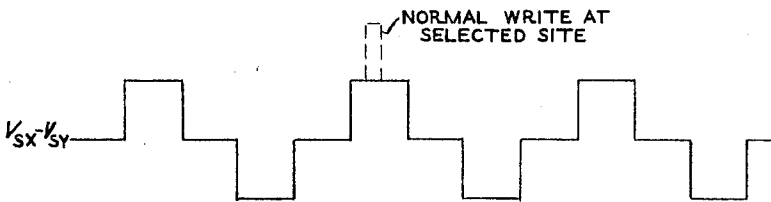


FIG. 3C

NORMAL
SUSTAINED
($V_{SX} - V_{SY}$)

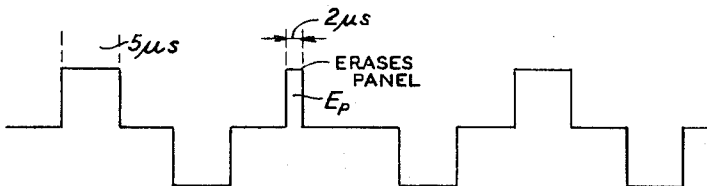


FIG. 3D

DATA AREA "V"
SITES OF PANEL

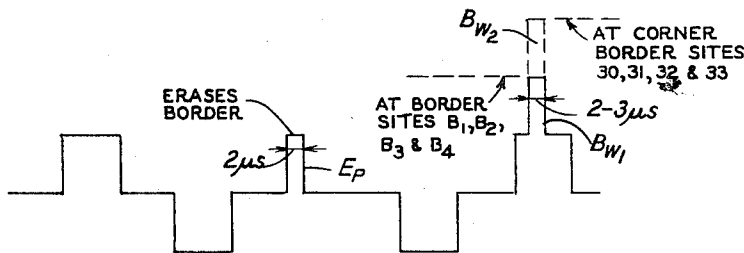


FIG. 3E

BORDER AREA
SITES

BULK ERASE SYSTEM FOR GAS DISCHARGE DISPLAY PANELS

The present invention is directed to a novel method and circuitry for bulk erasing a gaseous discharge display panel having inherent memory of the type as disclosed in, for example, Baker et al. U.S. Pat. No. 3,499,167.

As disclosed in the above-mentioned Baker et al. patent, there are a number of ways for conditioning the discrete information display discharge sites in such panels for operating at substantially uniform potentials. In a preferred case and one that is currently being used, photon conditioning as is described in the Baker et al. patent, an entire row or column of the sites on the border are maintained in a fired or on condition during normal operation of the panel with the light produced being masked or blocked off from the normal viewing area or otherwise not used for display purposes. In the past, these border sites were turned on and supplied with sustainer potential from the same sustainer sources as the normal viewing or display area of the panel. Thus, when it was desired to erase a "page" of data or information that was being displayed in the viewing area of the panel, simultaneously, by control of the sustainer voltages, the border sites were also erased. This is called "bulk erase" and as used herein means the turning off of all the information or data display sites on the panel while the border is turned on at the end of the erase cycle for conditioning of these sites for discharge an entry of new information to the panel. IN the past, effort has been made to avoid "half-selection" pulses. In accordance with this invention, while the border sites which are to be maintained on for conditioning purposes, are driven from the same sustainer, the circuitry according to the present invention operates by inserting a voltage in series with the sustainer signal voltage to the border conduction, following a bulk erase of all sites and panels due to sustainer control. This signal may be used to initially fire the panel on startup and fired periodically in case of a power failure or transient. Corner border sites therefore see as their applied voltages the sustainer and each of the half select voltages on the border conductors and this magnitude of voltage is sufficient to assure reliable turn on of at least the corner border sites.

The method and circuitry of the present invention provides a simplified bulk erase process and is a simplification from circuitry standpoint and provides certain characteristics and flexibility to the system at no additional expense.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, advantages and feature of the invention will become more apparent in light of the following specification taken in conjunction with the accompanying drawings wherein:

FIG. 1 is a stylized block diagram of the circuitry in accordance with the invention with a isometric showing of a gas discharge panel to which the invention has been applied (several circuitry blocks being duplicated for clarity of illustration only), FIG. 2 is one schematic drawing of the "half select pulsers" for the purposes of adding a half select voltage pulse onto the sustainer to the border sites on the panel, and

FIG. 3 (A, B, C, B and E) are wave form diagrams which are provided to supply explanation of the operation of the invention.

Referring now to FIG. 1, gaseous discharge display panel 10 is preferably of the type disclosed in Baker et al. U.S. Pat. No. 3,499,167, filled with a neon-argon gas mixture (99.9% neon and 0.1% argon) as is disclosed in Nolan application Ser. No. 764,577 filed Oct. 2, 1968, and as further modified by a dielectric or insulating overcoating (not shown) on the dielectric coatings of the aforementioned Baker et al. patent of a lead oxide. Typically, the discharge gap distance in such panels selected to be between 4 and 6 mils. The panel 10 is constituted by a row conductor plate 11 and a column conductor plate 12 joined in spaced apart relation by a spacer sealant (not shown) so as to provide the aforementioned discharge gap distances and a thin gas discharge chamber.

The row conductor plate 11 carries a row conductor array 13 in the writing or data display area "V" and a row border array 14 and 15 at the sides thereof. The column conductor plate 12 is identical, having a column conductor array 16 in the writing or viewing area of data display area "V" and border or side conductors 17 and 18 respectively. Alternate ones of the conductors in array 13 are grouped and extended towards the opposite ends 20 and 21 of panel 12 and in a similar fashion, alternate ones of the conductors in array 16 are extended to the opposite ends 22 and 23 respectively, of column conductor plate 12. In like manner, alternate ones of the border conductors are extended to the edges of their respective plates and adapted for connection to supply potentials. It will be appreciated that instead of extending the conductors of an array to opposite edges they may all be extended towards the same edge and receive operating potentials from the same side or edge. Thus, instead of extending the row conductors (writing conductors 13 and border conductors 14 and 15) towards the edge 22, these may all be extended towards edge 23 of row plate 12 and be served with operating potentials from the same side or edge. In like manner, the conductors on column plate 12 may be arranged and energized in the same fashion. Thus, the illustration in FIG. 1 of separate circuitry for addressing for the sustainer voltages and the border half select pulsers is for the purpose of illustration only, it being understood that they may be, and preferably are, driven from the same supply. Since the border or side conductors in an array will be supplied with the same potential, all those on one side may be connected together. Thus, if there are several conductors constituting border conductors 17, for example, they may be connected together at their ends in the forming of these conductors.

The viewing area of the panel is labeled "V" in FIG. 1, and the border areas are labeled "B". In a rectangularly shaped panel there will be four border areas. The border conductors in each array while crossing each other in the corners (as at 30, 31, 32 and 33) are normally lit along the entire border areas B1, B2, B3 and B4 to provide sufficient photon conditioning for the entire data display or viewing area "V" of the panel. It will be appreciated therefore that each of the border conductors in the areas B1, B2, B3, B4 which cross a row conductor 13 or a column conductor 16, respectively (and extend into and across the viewing area "V" to form the light emitting display matrix), will cooperate with the border conductors to provide the necessary operating potentials to the border sites in the border areas B1, B2, B3 and B4. However, the half select

pulsers to be described later herein are only applied to the border conductors in conjunction with the sustainer potentials so as to write the border conductors only. (The term "write" means the initiation of a sequence of discharges at selected sites, and the term "erase" means the termination of a discharge; and, the term "discharge" means the momentary or pulsing discharge nature of the sites as described in said Baker et al. patent). The "half select voltages" are not applied to the row and column conductors because such voltages would tend to turn on all of the sites along the conductor to which they are applied, which, however, satisfies the objective of turning on the border sites.

The panel 10, per se, as well as the sustainer generators and addressing circuits is conventional insofar as this invention is concerned. The row conductor array 13 is supplied with discharge condition manipulating pulse potentials from standard addressing circuits 60 and 61 which receive information and control signals from a data and control source 62. The sustainer sources have a common ground or reference point S_G so the addressing circuits 60 and 61 float upon sustainer potentials from row sustainer generator sources 63 and 64, respectively. The addressing circuits 60 and 61 may be of the type disclosed in D. L. Leuck application Ser. No. 135,621 filed Apr. 19, 1971 and the sustainer generators may be of the type disclosed in D. S. Wojcik application Ser. No. 135,022 filed Apr. 19, 1971. In a similar manner, the column conductors in array 16 are driven by addressing circuits 70 and 71 which float on column sustainer generators 73 and 74.

THE PRESENT INVENTION

As described above, the border sites in corner areas 30 and 31, 32 and 33 and border areas B1, B2, B3, B4 are driven or supplied by sustainer potential from sources 63, 64 for the border row conductors 14 and 15 and 73, 74 for the border column conductors 17 and 18. It is possible to turn off a site and remove information at random information sites in the panel by applying an erase pulse to selected conductors crossing each other at the site and thereby selectively remove information from the panel at any selected discrete site. However, it frequently is an advantage to erase the entire panel, which means to eliminate the memory or wall voltage due to stored charges at all information display sites in the panel. In the bulk erase process described herein, this is done by modifying the sustainer potential as applied to all the sites for one or more cycles or periods and then reapplying the sustainer potential in the normal fashion. As shown in FIG. 3(D) bulk erase is achieved by simply narrowing the width of the sustainer for at least one half cycle. Thus, when the sustainer voltage pulses are normally 150 volts and 5 microseconds in width (and at 30-50 kHz) the erase pulse E_p can be the same magnitude and rate sustainer but having a 2 microsecond width. The normal sustainer voltage applied to the gas at a site shown in FIG. 3(C), is constituted by the sustainer voltages applied to the row and column conductor arrays as illustrated in FIG. 3(A) and FIG. 3(B).

The mechanism of discharge at substantially uniform potential requires, among other things, the existence or presence of some charged particles at each discrete discharge site, which implies some conditioning processes. These conditioning processes have involved, in the past, the use of radiation by ultraviolet energy on the

panel, use of radioactive sources in the panel, conditioning pulse voltages applied to the conductor arrays and, as in the aforementioned Baker et al. U.S. Pat. No. 3,499,167, the elimination of the discharge isolation structures permits photon conditioning of the sites by turning on the border sites and maintaining the border sites on during the addressing of selected sites in the viewing or writing area of the panel.

In the past it was sought to maintain the border sites on while erasing the whole information or data display of the panel. According to the present invention, simultaneously with the bulk erasing of the data from the entire panel, the border sites are also erased and then the border sites are immediately rewritten by application of the normal sustainer potential along with a border write signal potential. Moreover, this border write signal potential (B_W) is applied to only the border conductors of the conductor arrays and, when algebraically added to the sustainer potential on the border conductors, is of sufficient magnitude to initiate the discharges at the border sites without a corresponding pulse on the opposite conductor in the areas B1, B2, B3, B4. Thus, on bulk erase, the sustainer voltages V_{SX} from sources 63 and 64 are controlled by data and control source 62 to cause a relatively short time duration (about 2 microsecond duration as compared to a normal sustainer of about 5 microsecond duration) voltage pulse E_p to be substituted in place of the normal sustainer pulse at the selected time interval or period. In FIG. 3A a normal write pulse N_W row as applied to a selected row conductor is approximately one-fourth the voltage needed to initiate a discharge. A further one-fourth is simultaneously supplied by a normal write pulse N_W col. (FIG. 3(B)) is applied to a column conductor locating the selected site in data viewing or display area V. The sum of these two voltages with the sustainer voltage at the selected site (FIG. 3(C)) is sufficient to turn on any selected site. It will be noted that the memory or wall voltage of the panel will maintain the sites in an on state. However, since any voltage applied to a conductor of an array is also applied to all other discharge sites located by that conductor, the voltage applied thereto cannot be of a magnitude to turn on unselected sites. However, in the case of the border sites, the objective is to turn on all sites and hence the voltage applied to the border conductors must be of a magnitude which, when added to the sustainer, will turn on the sites in border area B1, B2, B3 and B4 without adversely affecting the sites in the data display or viewing areas V of the panel.

A simplified circuit for use as a border site writer is shown in FIG. 2. The circuit includes transistor Q1 which is biased on or conductive by a voltage from a source such as battery 90 and controlled or turned off by a control signal from data and control circuit 62 applied via transformer T1 and resistor-capacitor coupling circuit 91. With transistor Q1 being normally conductive, the sustainer voltage V_S (which may be for the row or column conductor arrays) appears at the output terminal 92. A second, normally non-conductive, transistor switch Q2 has its collector-emitter connected in series with a 150 volt source, such as battery 93, and coupling resistor 94 and in shunt with the collector emitter circuit of transistor Q1. Transistor Q2 is controlled by a signal coupled from data and control circuit 62 by way of transformer T2 and shunt resistor 95. When transistor Q1 is rendered non-conductive or a

high impedance, transistor Q2 is rendered conductive so that the 150 volt source 93 is added to the sustainer voltage as a short pulse B_w. This action occurs simultaneously at all half select pulsers 80, 81, 83, 84 so that the border write pulses B_{w1} and B_{w2} (FIGS. 3A, 3B and 3E) are applied to the border conductors (14-15 and 17-18) in each array. As shown in FIG. 3E the corner border sites 30, 31, 32 and 33 will have a much larger amplitude voltage applied thereto so that the initial discharges at these sites can be more reliably initiated.

Shunt diode D1 is a bypass for sustainer displacement currents as disclosed in the aforementioned Leuck patent application and Johnson application Ser. No. 60,402 filed Aug. 5, 1970.

It will be noted that in the areas B1, B2, B3, B4, the normal writing circuits 60, 61, 70, 71 are not energized during the writing of the border sites in those areas. Thus, as discussed above, the row conductors in the areas B1 only are provided with the "half select pulses" which cooperate with the sustainer voltages applied via the standard addressing circuits. However, in the border areas 30, 31, 32 and 33 the sustainer voltage coacts with the sustainer voltages and the half select pulser circuits.

It will be appreciated that various modifications and changes obvious to those skilled in the art may be incorporated in the practice of this invention without departing from the spirit or scope of the claims appended hereto.

What is claimed is:

1. A method of operating a gas discharge data display panel of the type having a dielectrically coated row-conductor array on a first support plate, a dielectrically coated column conductor array on a second support plate, means joining said plates in spaced apart relation with a gaseous discharge medium between said dielectrically coated conductor arrays, a selected number of conductors in each said array locating border discharge sites which are used as non-data display areas, and wherein the operating potentials to said conductor arrays includes a periodic voltage for sustaining discharges once initiated, said periodic sustainer voltage being of a magnitude insufficient to initiate a discharge at any site but of sufficient magnitude to maintain discharges once initiated at any site, and a data entering discharge initiating signal voltage for algebraic addition to said sustainer voltage potential, said method including the step of bulk erasing data displayed on said panel by modifying sustainer voltages from conductors of at least one of said arrays,

the improvement comprising,

simultaneously with the bulk erasing of data from the entire panel, erasing said border sites and then re-writing said border sites by application of said sustainer voltage thereto along with a border write signal voltage.

2. The invention defined in claim 1 wherein said border write signal voltage for said border conductors is applied to at least one of said conductor arrays and, when algebraically added to said sustainer potential on said border conductor, is of sufficient magnitude to initiate discharges at said border sites.

3. The invention defined in claim 2 wherein said border write signal voltage is applied to all said border conductors in each array so that the corner border sites are turned on by a voltage comprised of the algebraic sum of said sustainer voltage and twice the magnitude of said border write signal voltage.

4. In a gaseous discharge display panel having row-column conductor arrays, non-conductively coupled to a gas discharge medium in the chamber space between said row and said column conductor array and a border conductor array cooperating with the ends of the conductors in the row-column conductor arrays which, for the purpose of photon conditioning of information display sites in the panel, are on during the entry of information to be displayed on said panel, the improvement in the bulk erasing of said panel which comprises,

means for modifying the sustainer voltage on at least one of said arrays for at least one period thereof, and

means for turning said border sites on prior to the entry of information to said panel.

5. The invention defined in claim 4 wherein said means for turning on said border sites prior to entry of new information to said panel includes a source of border pulse potential selectively connectable only to at least one of said border conductors which, border pulse potential algebraically added to the sustainer voltage to said at least one border conductor is sufficient to cause a discharge at any border site only on the panel located by said at least one border conductor.

6. The invention defined in claim 4 wherein the border conductors in each array are supplied with said border pulse potential so that the corner border sites have applied thereto said sustainer potential and algebraically added thereto twice the magnitude of said border pulse potential.

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