

[54] NUMBER GUESSING GAME DEVICE

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[58] Field of Search..... **273/1 E, 138 A, 139, 85 R**

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[57] **ABSTRACT**

A game device or apparatus of the electronic type where the concept of the game is to find a hidden and random number generated automatically by the electronic apparatus. The game includes a keyboard entry unit by means of which players may select a number in search of the hidden random number and the number

so selected will be displayed on a numerical readout display. Once the number has been selected, a test command will compare the selected number with the hidden random number to determine the relationship of the same relative thereto. The selection can either be higher than, lower than, or equal to the hidden random number. If the selection is equal to the hidden random number, the game is completed with a win indication displayed on the display modules on the face of the apparatus. Should the number be higher or lower than the hidden random number, an indication will be provided on the display apparatus of this relationship and the number transferred from its initial position to a higher or lower register wherein it will be displayed. As the game progresses, and after initial selections, the selected number, when found to be higher or lower than the hidden random number will be compared with the next previous selection of a higher or lower number so that its relationship relative to the previous numbers which are stored and displayed on the display modules must be closer to the hidden random number than the previous number or an error situation exists and no transfer of the selected number as a new high or low selection takes place. The keyboard entry unit provides for a clear command to clear the error in the selected number by removing the same from the main keyboard register in the display modules and permits a new try or selection by the player in the search for the random number. The keyboard selection entries together with the logic control operating the display modules are all in binary coded decimal form. The hidden random number is generated by a continuously running clock apparatus whenever the game is energized but not in operation and is determined by initial operation of a keyboard entry unit at the start of a game.

17 Claims, 9 Drawing Figures

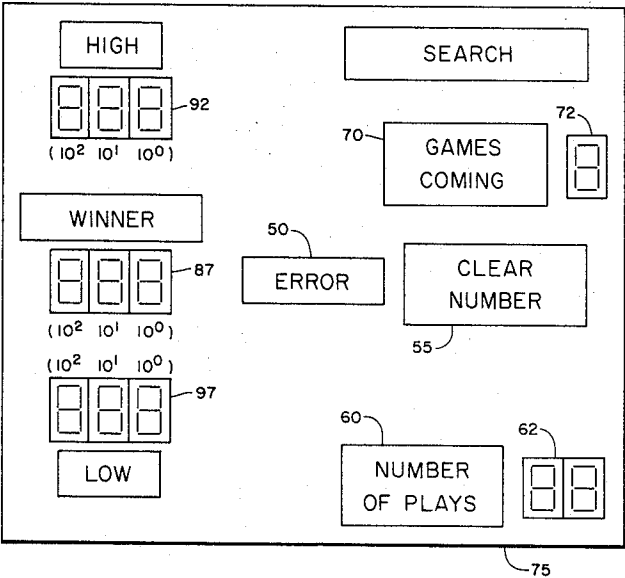


Fig. 1

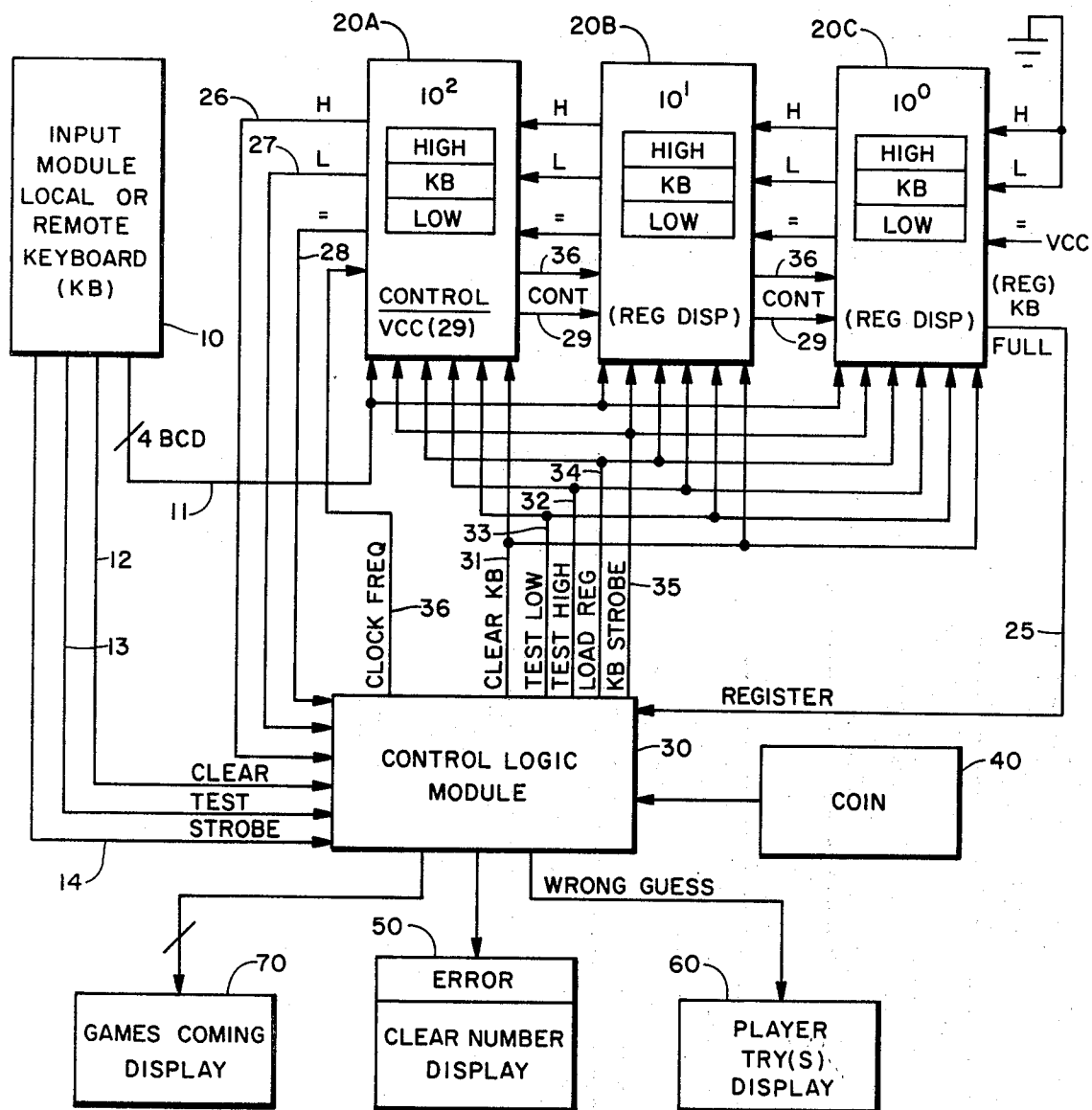


Fig. 2

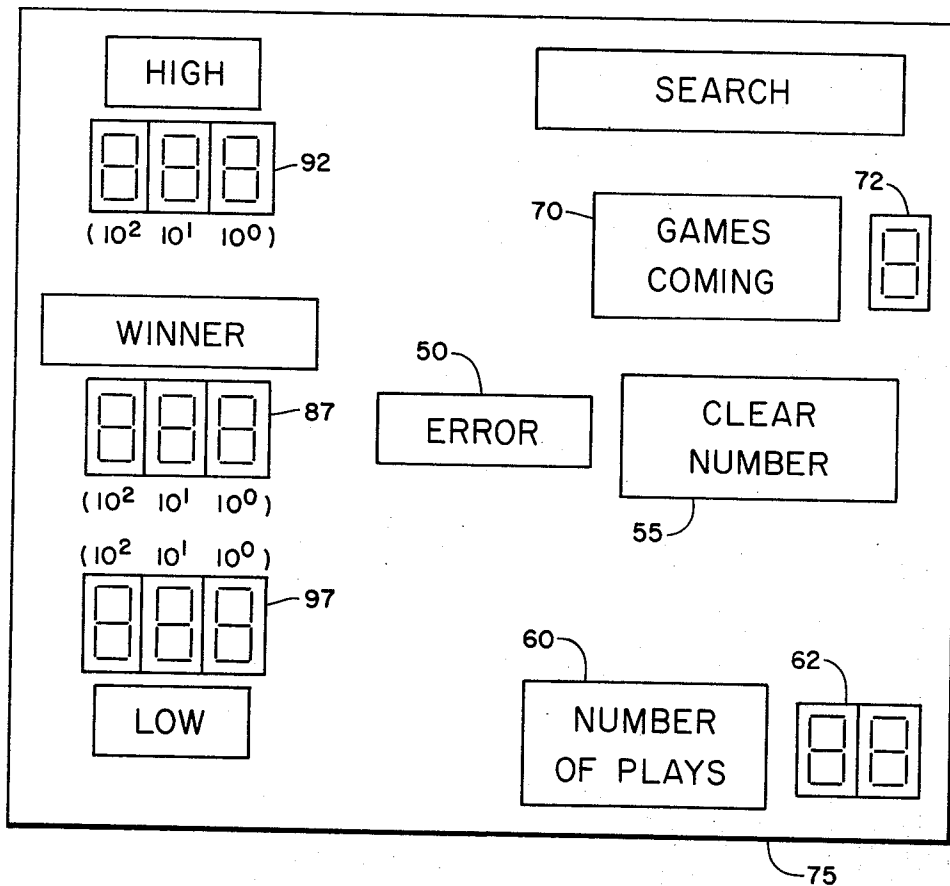
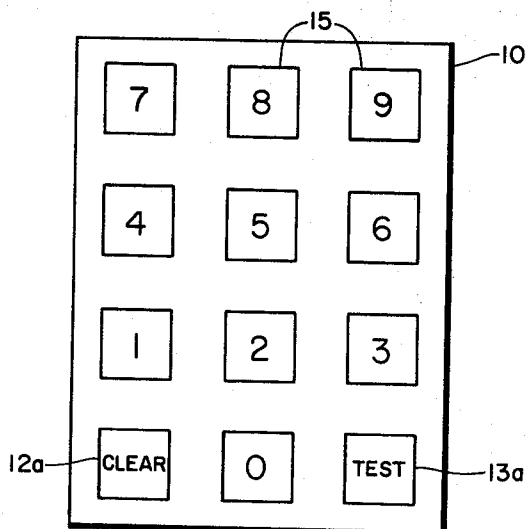


Fig. 3



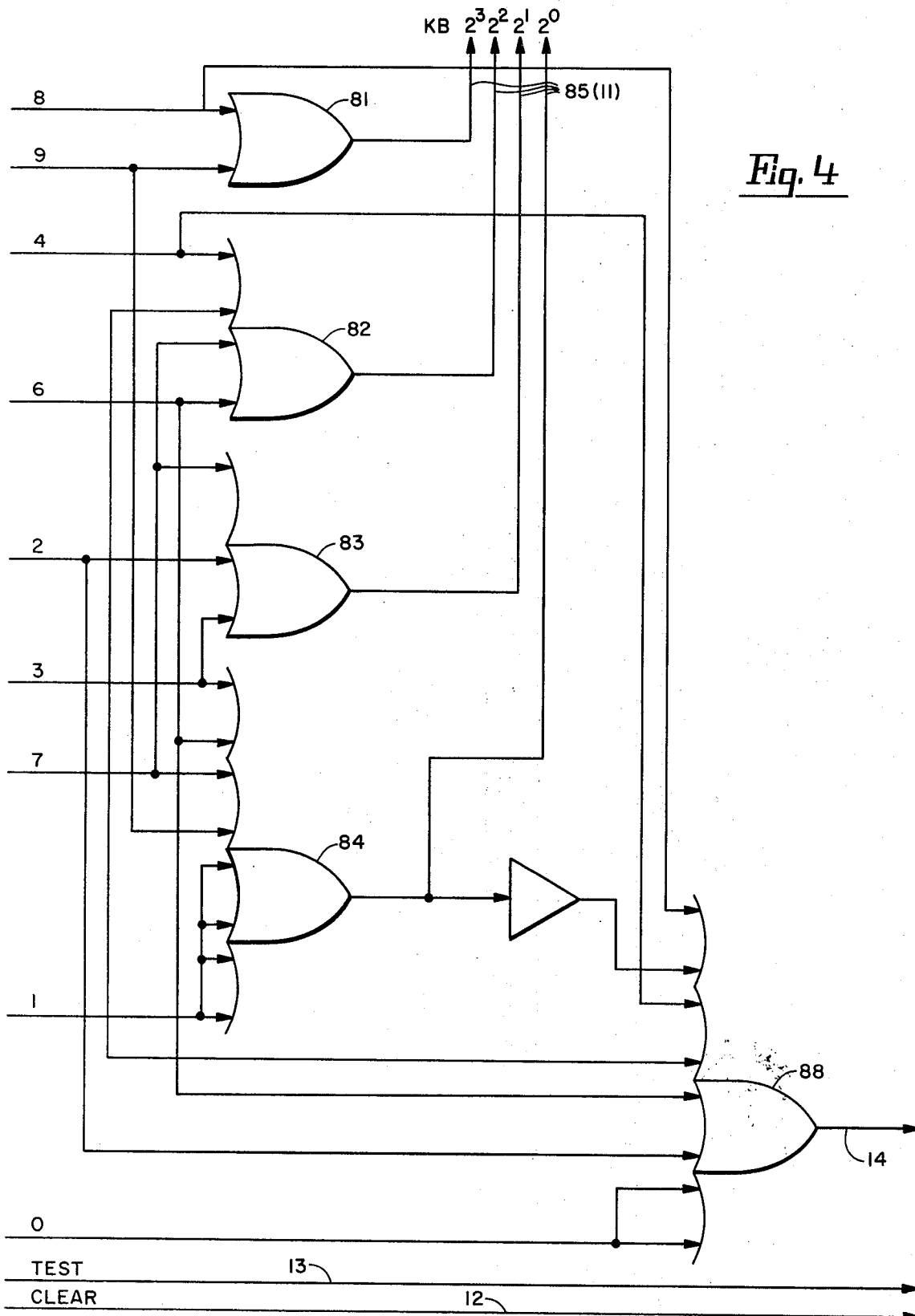


Fig. 4

Fig. 5

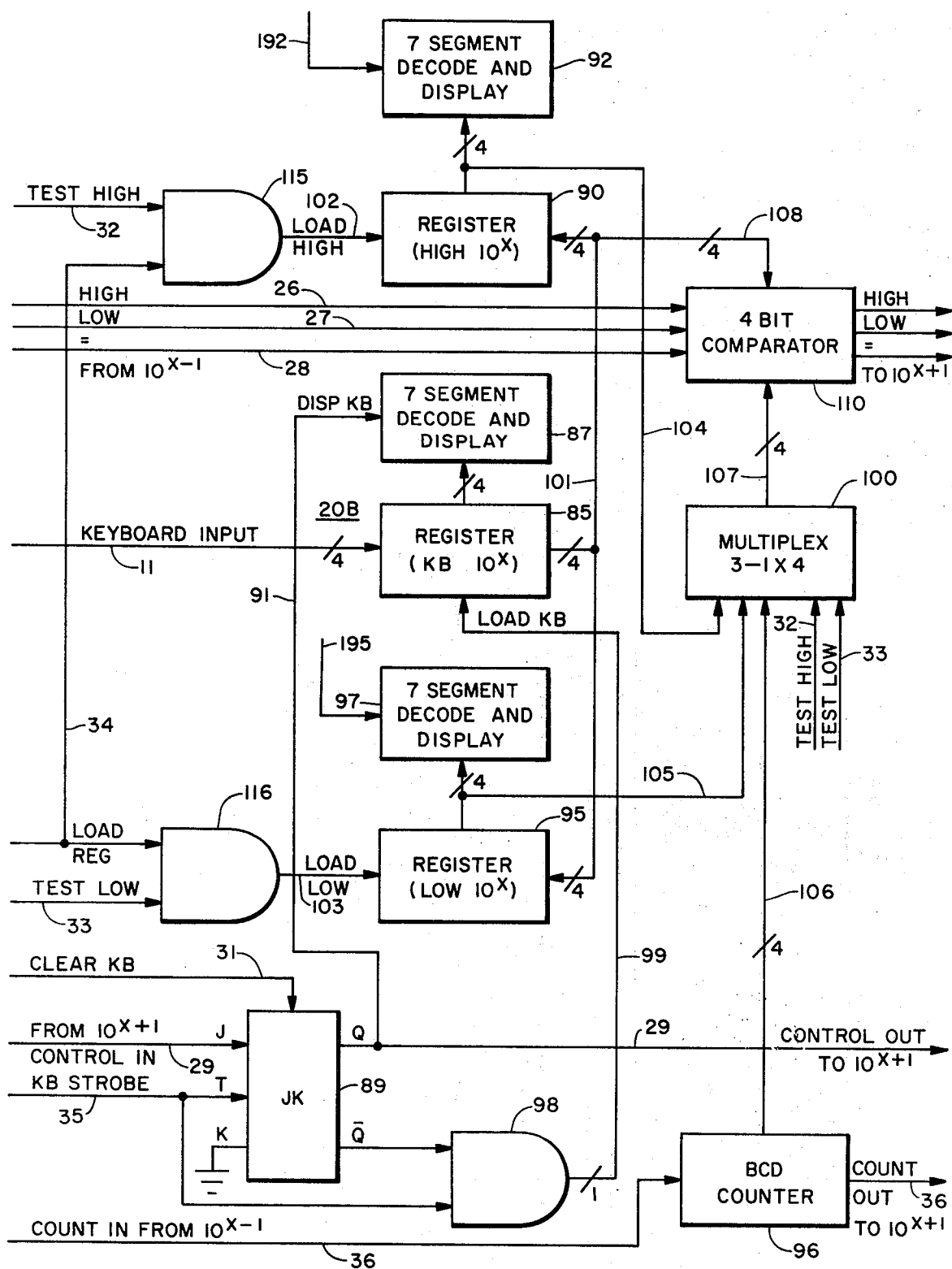


Fig. 6

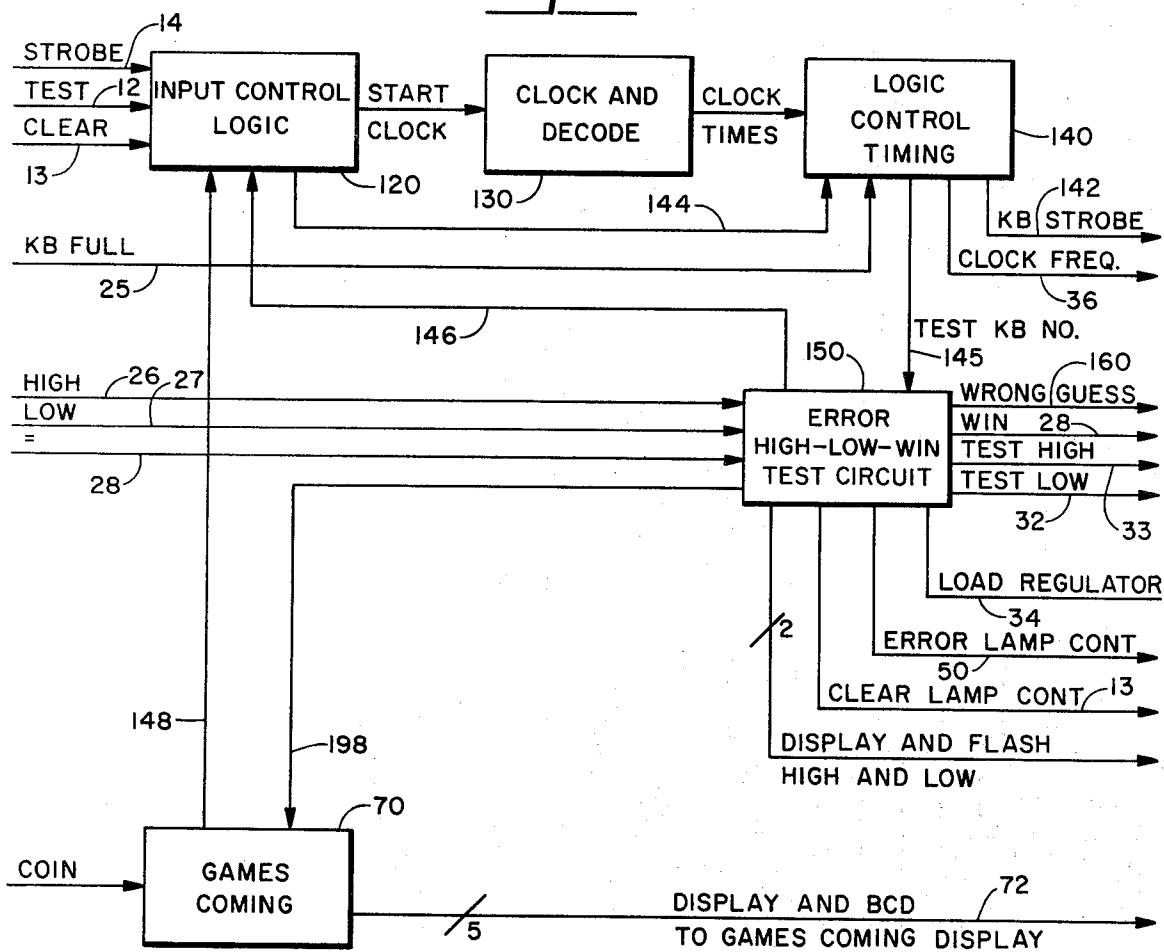


Fig. 7

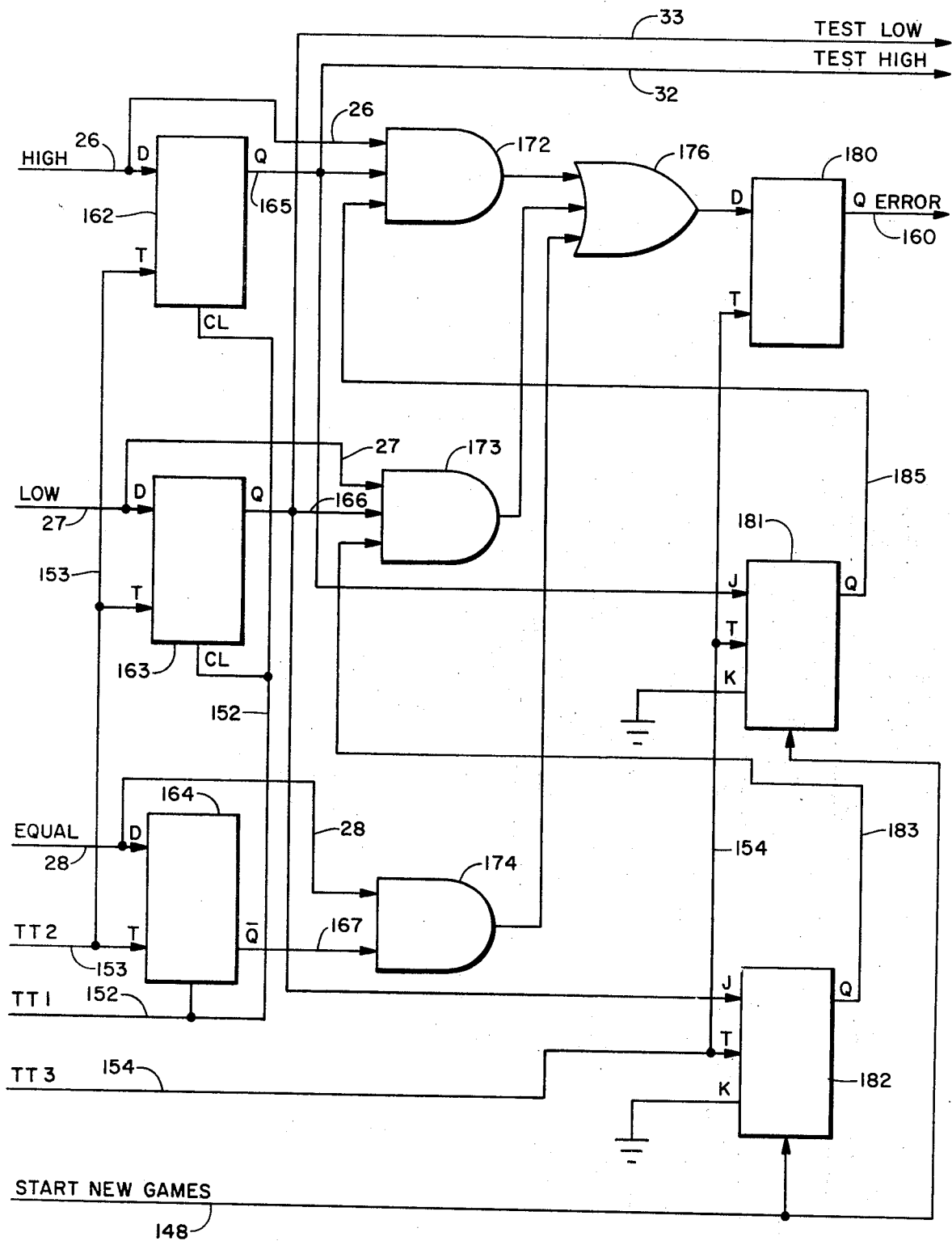
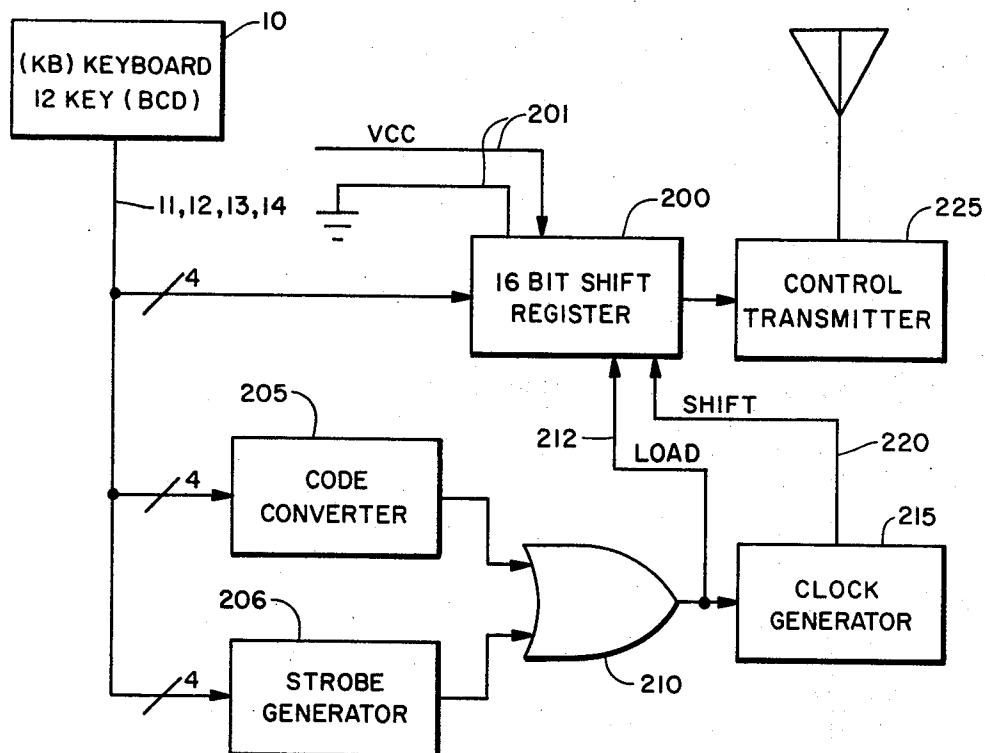
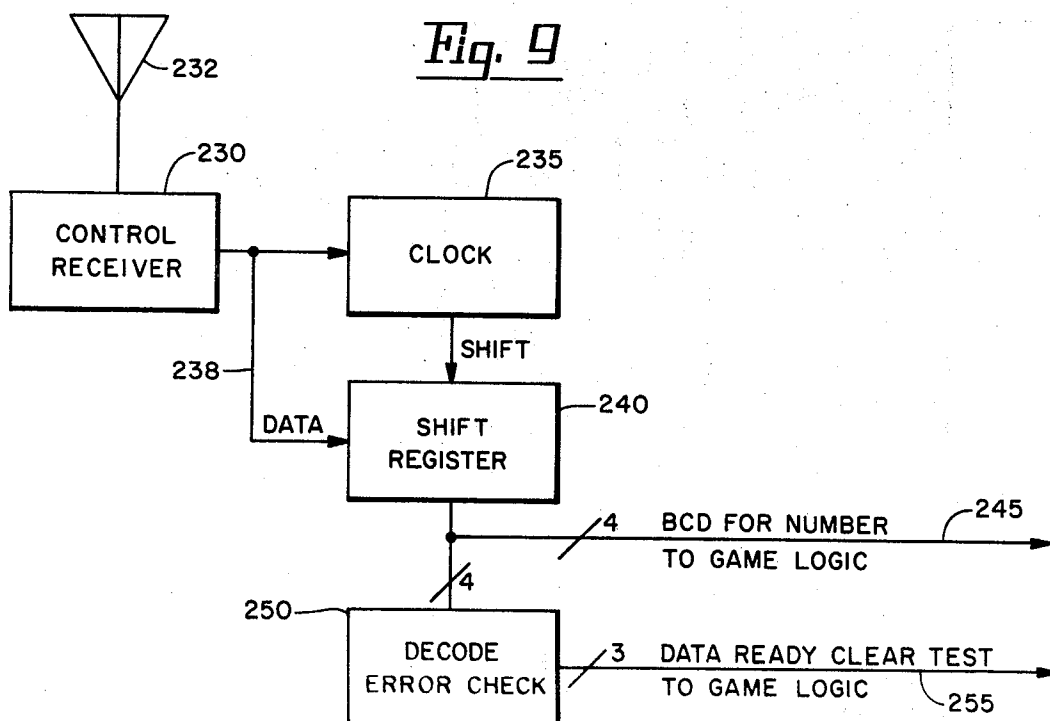


Fig. 8Fig. 9

NUMBER GUESSING GAME DEVICE

Our invention relates to a game device and more particularly to an electronic game apparatus of the type in which a hidden random number is selected by a player with operation of an input module in the selection of a plural digit number which will be compared with an unknown random number in the apparatus to determine the relationship relative thereto.

Game apparatus of this general type is generally known and is evidenced by prior issued patents, such as for example the patent Adam Becker et al, U.S. Pat. No. 3,483,628 entitled ELECTRIC GAME APPARATUS, dated Apr. 5, 1969. This patent and other prior structures all utilize previously programed records which may take the form of magnetic tape, punched tapes, photographic strips, or equivalent structures as the random number storage. Thus in the prior structures, the random number, which is to be found in the operation of the game, is previously selected and stored. Prior apparatus include provisions for player selecting a plural digit number or a sequence of numbers and characters which are to be compared with the preselected numbers to determine whether correspondence exists either between the number or the combination of numbers or letters that is randomly selected from the previously programed record as a game of skill. Such prior structures shows correspondence and non-correspondence but fail to include positive relationships between the selections and the random number and do not provide a truly unknown random number in the selection.

In the present invention, the improved game apparatus provides for a truly unknown random number which is not prerecorded but is generated by a continuously running clock whenever the apparatus is energized, even though not in playing condition. The clock will generate a sequence of numbers from zero to the maximum of the plural digit selection for which the apparatus is capable and will continue the sequence until initial operation of the apparatus by a player will stop the clock and load in the apparatus a truly random number. In the game device, a remotely positioned input module includes a plurality of manually operated selection means or keys each representing integers or digits from zero through nine and with certain operation command keys in the input module. Depressing a number of these keys in sequence, each operation representing a digit to a total number of operation indicative of the total number of digits in the unknown number, is required for a player operation. As the digits are selected they are displayed on a register and an operational command sequence initiated by operation of one of the operational keys at the input module will compare the hidden random number with the selected number. The input module converts operation of the digital keys into binary coded decimal signals with the input commands which are supplied to a logic system and registers wherein the random number has similarly been converted for binary decimal form and will be compared with the selected number. These numbers are compared digit by digit and the relationship of the selected number to the random number, will be displayed as either higher or lower than the random number as the selected number is selectively transferred to registers representing this relationship, should the selected number not be equal to the hidden random num-

ber. Prior to the transfer from the main display register the selected number will be compared with a previously selected higher or lower number stored in and displayed in the high or low display registers and should the selected number not be closer to the hidden number than the previous high or low selection, a transfer of the selected number to the higher or lower registers will not be effected. Such a selected number will then have to be cleared from the main display register wherein it is displayed and a new selection made which will be closer to the random number than the previous selection. The apparatus includes display of the selected number, display of the relationship of the selected number to the random by transfer and display in the higher or lower register, counting of the number of tries or operations of a player, an error indication should the number not be closer to the random number than of a previous selection, and a true conformance or an exact comparison of the selected number with the random number should they be equal with a win indication. The improved game device also includes provision for a radio control from the input module to a receiver on the remotely positioned display to provide a connectionless coupling therebetween. The apparatus further includes provisions for coin operation and display indication of the game coming from the coins inserted to permit operation of the same. Thus, the improved game device does not require any precoded records which will require changing or selection to change the random number and therefore may be continuously operated without alteration of the apparatus.

It is therefore a principal object of this invention to provide an improved game apparatus which employs a truly random number selection and which makes possible a comparison between operator selected numbers and that randomly established and stored in the apparatus to determine a comparison between the numbers.

Another object of this invention is to provide in an improved game device of this type an improved logic register apparatus which keeps track of previously selections so that a new selection does not depart from the random number greater than the previous selections.

A further object of this selection is to provide an improved apparatus of this type utilizing binary coded decimal signals from the input to the logic and registers with appropriate decoding and displaying in numerical form of the number selections.

A still further object of this invention is to provide an improved apparatus of this type which is suitable for radio control through the use of the radio transmitter at the input module and a receiver at the display apparatus with the registers and logic control therein which does not require electrical connection therebetween.

A still further object of this invention is to provide an improved apparatus of this type which is relatively easy to use and relatively maintenance free. These and other objects of the invention will become apparent from a reading of the attached description together with the drawings therein:

FIG. 1 is a block diagram of the improved game apparatus;

FIG. 2 is a schematic diagram of the face of the display unit of the improved game device;

FIG. 3 is a schematic diagram of the face of the input module for the improved game device;

FIG. 4 is a circuit diagram of the input module for the improved game device;

FIG. 5 is a block diagram of one of the display modules for the improved game device;

FIG. 6 is a block diagram of the logic control portion for the improved game device;

FIG. 7 is a logic circuit diagram of the error detection circuit portion to the improved game device;

FIG. 8 is a functional logic diagram of an alternate embodiment of the game device showing radio transmitter control; and;

FIG. 9 is the function logic diagram of the receiver circuit control for the alternate embodiment of the improved game device.

As shown in FIG. 1, the game device includes an input module, indicated in block at 10 which may be either local or remote. Thus it may employ radio control or be directly connected to the remaining apparatus as will be hereinafter defined. The module has a keyboard with a plurality of manually operable selection means representing digits or integers and operative commands positioned thereon. In FIG. 1, the input module 10 is connected to a plurality of display modules so that the output from the input module is directed to the plurality of display modules, indicated generally at 20A, 20B and 20C. Each of the display modules is identical in form and has three sets of registers and converters to display digits so that the displays form a plural digit number. The input module output also has command output signals, such as is indicated by the clear 12, test 13 and strobe 14 lines which are connected to a control logic module 30 for the purpose of providing input commands thereto. The control logic module 30 in addition is controlled by the operation of a coin device, indicated generally at 40, which provides input to the control logic module to permit initiation of the inputs from the input module 10 to the display modules 20A, 20B and 20C. The control logic module 30 also provides a number of output signals through output conductors such as is indicated in lines 31, 32, 33, 34, and 35 respectively, these being commands to clear the keyboard, test low, test high, load the registers and the keyboard strobe signal. The number selection from the input module 10 is fed through the conductors 11 to feed all of the display modules 20A - C. Each number selection is converted in the input module to a binary coded decimal form and is fed to all three registers in this form. However, as will be later noted, the logic module or control permits loading of the highest digit register indicated as the hundreds unit 20A, disabling the remaining two registers from displaying the same. On the next digit selection from the input module, the tens and units are loaded with the tens module 20B receiving and displaying the selected digit and with the units module being disabled to display the selection. On the third selection, the signal is loaded only into the units module 20C, and at this time the keyboard is listed as full with a signal back to the logic control 30 as indicated by conductor 25. Prior to the loading of the registers, a suitable clock in the logic module 30 is running and generating a random number in terms of units, tens and hundreds between zero and 999 which numbers are converted to binary decimal form and loaded into the respective registers 20A - C. The numbers are generated through the maximum

three digit number and restarted again for continuous generation and conversion whenever the equipment is energized. The generation of the random number will stop and the actual random number will be established upon the first input signal from the input module 10 through the strobe line, indicated at 14. Thus, the line indicated at 36 indicates the clock frequency feed to the display modules which contain a portion of the control logic as well as the random number selection and storage units, the multiplexers, comparison registers, high, low and keyboard registers and the display decoders, all of which will be hereinafter identified. After a plural digit number has been selected, a signal originating in the input module 10 and as produced on conductor 13 will be fed through the logic control 30 to test the plural digit number displayed in the keyboard register of the display modules against the random number. This comparison will be by digit and equality or any disparity high, low for a particular digit will generate a signal in the conductors, indicated at 26, 27, and 28 which will indicate whether a digit is higher, lower or equal to that stored in the registers representing the random number. After the first digit is compared, the tens unit digit will be compared and finally the unit digit compared as long as correspondence exists between the random number and the selected number. Whenever disparity exists in any of the digits compared with a random number, one or the other of the lines 26, 27 will be energized, feeding a signal back to the control logic module 30. Should the random number equal the selected number, line 28 will be energized, feeding a signal back to the logic module. Under circumstances of disparity, the logic control will test the selected number against the previously selected number which could be high or low, assuming one exists. In each instance, the selected number should be lower than the previously high number or higher than the previous low number already displayed in the high and low registers before the present selected number can be shifted from the keyboard or center register for all three digits or all three modules to the upper and lower registers depending upon whether the selection is high or low. In the event that this condition does not exist, that is that the selected number is higher than the previous high number selected or lower than the previous low number selection or equal to the previous number selected, an error indication will exist and the line or block 50 connected to the logic control will show this error. In other words, the selections consecutively have to be closer to the random number than the previous selections on the high or low side in order for a transfer to take place. Thus the control logic will display an error under such conditions in the indicator 50 and it will be necessary to generate the clear signal from the input module, as indicated by module conductor 12, to the logic to clear the keyboard as indicated by the control conductors 31 leading to all three blocks. The keyboard strobe signal, as evidenced by conductor 35, facilitates transfer of information at a particular time in a clock sequence and will be hereinafter identified. The clock frequency signal 36 is stopped randomly by the first entry of the games, hence, and the random number is established under control of the strobe signal 14. The registers are loaded in sequence indicated by the arrows 29 extending therein with the last unit digit display module providing the full signal back to the logic control as indicated by conductor 25. Whenever a selected number

fails to correspond with the hidden random number, and the same has been transferred to the display modules, either in the high or low registers, the logic control will supply a signal to the block counter in block 60, indicating an additional try. Similarly, as seen in FIG. 1, deposit of a coin to initiate or enable operation of the input module to transfer information to the registers will also count and display a number of games coming as indicated by the logic block 70 where the coin provides for more than one set of games. The games coming to the display will also be the source of additional initiation or energization of the logic controls to permit transfer of input information from the module to the registers and the control logic with games coming display and logic being accordingly adjusted with each game or group of selections when the winner is picked and thus allows the start of a new game.

The display modules 20A, 20B, and 20C which are typical modules are housed in a suitable display structure or container having a face with a plurality of indicating lights thereon. Thus, in FIG. 2, the face 75 of the box-like container will include the coded display lights for the various registers, and the additional displays of the blocks indicating game operation. It will be understood, although not specifically disclosed, that all of the registers, multiplexers, control logic, and like circuitry will generally be housed in the container upon which the indicator face shown in FIG. 3 is positioned for simplicity. Thus, as is indicated in FIG. 3, three sets of control lights indicating high, low and keyboard or winner are positioned in a side-by-side spaced relationship across the face of the indicator. Thus, the display on the face of the container and on the left hand side thereof represent the selected digits and the logic comparison thereof. Each of the displays are controlled by seven segment decoders operating from the four bit binary code intelligence to form the integer from zero to nine. Each row includes the decoders associated with the registers 20A, 20B and 20C shown in block in FIG. 1 with the upper row being the display for the high register and including a high light indication above the same, the keyboard or center register displaying the hundreds, tens, and units bit in numeric form with the winner light above the same and the lower grouping representing the lower register with the low indicating light and the numeric digits representing the display of the selected number in the low register. Thus, whenever a selected number employing three digits in selected on the input module, it will appear in the center register up to the time a comparison is made. Should it test high or low with respect to the random number included in the logic and should no error appear from the standpoint of being high than or lower than a previous high or low number, it will be transferred to the respective high or low register above or below the center keyboard register to be displayed thereon with the appropriate light being also lighted and blinking. In the event that the selected number corresponds with the random number, no transfer will be made and it will be continued to be displayed on the center register with the winner light illuminated. In the event that an error appears due to selection of a number higher or equal to a previous high, or lower than or equal to a previous low, the error indicating light, as indicated by block 50 will be lighted along with the light in block 55 identifying the player to clear the number by operation of a clear key 12a to be later defined. The remaining indicia on the

face of the display includes the games coming illumination block corresponding to block 70 in the block diagram which will be illuminated in accord with the amount of money deposited in the coin slot for initiating operation. A seven segment decoder similar to that employed in the high, low, and keyboard registers is employed to define the number indicating the games coming. Similarly, on the lower face of the display, the block 60 is illuminated to indicate the number of plays or complete selections made by the player in the search for the random number, with block 62 having two seven segment decoders and attached to an appropriate counter included in block 60 which will count and display the total number of player selections in a game before a winner is determined. The block indication shown herein indicates that the total of the number of plays would be a two digit number as high as the number 99.

In FIG. 3, the face of the input module is displayed with the general number 10 to indicate the switching and encoder unit being included in the container where the face is displayed. Suitable keys or manual selection means cover nine digits from zero to nine as indicated at 15 with a clear and a test button 12a and 13a corresponding to the signal outputs from the input module. This input module may be directly coupled by cabling to the control logic and registers included in the container shown in FIG. 2 with the decoders and lights upon the face of the same or may be radio coupled through the radio transmitter to operate a receiver included in the display container as will be hereinafter identified. In such instances, the transmitter will be self-contained and will include a battery powered supply so that no connections will be required thereto.

FIG. 4 shows the input module in circuit form without regard to remote control to indicate the encoding of numeric integers into binary coded decimal signals to be fed to the register which will be hereinafter defined. This portion of the circuit identified generally as 10 includes a plurality of "or" gates 81, 82, 83 and 84 which are connected to the conductors, indicated generally at 85 representing various integers from 1 - 9. The zero integer is evidenced by a binary zero so that only a strobe signal is taken therefrom. Thus, as indicated in FIG. 4, the lines 85 taken from the "or" gates represent the binary coded decimal signals from the integers between zero and nine for any selection on the input module fed on the input conductor 11 in FIG. 1. Each of the integers is also connected to a second or gate 88 which provides a strobe signal output, as indicated at 14, which provided an initial signal to the logic controls as will be hereinafter identified for varying purposes, one of which is to set the random number in the logic control. The input module also provides for operate or clear commands as evidenced by the conductors 12 and 13 as in the block diagram of FIG. 1.

FIG. 5 shows a portion of the display modules shown in block at 20A - C in FIG. 1 to indicate the high, low and keyboard registers together with the decoders and display elements associated therewith, the multiplex system and the four bit comparer which controls and compares a random number with a selected number. For simplicity only one display module is shown and the decoder displays, registers, counters, multiplex units, comparator, and flip-flops therein are shown in block since such units are conventional and their detail is omitted for simplicity. The display block shown is

that labeled 20B in FIG. 1 or the tens unit or digit. It will be understood, as indicated in FIG. 1 that three such display modules including counters, multiplex units, and comparers together with a high, low and keyboard registers will be employed, one for each digit. As will be seen in FIG. 5, the output of the keyboard in terms of the selected digits and in binary coded decimal will be applied through the cable 11 to the tens register 85. In actual operation, the output of the keyboard will be applied to the hundreds keyboard register first with simultaneous application of the same digit to the keyboard registers for the tens and units digits. Through the logic system, only the hundredth digit will be enabled from the clock to load the register and display the particular digit thereon. Thus in FIG. 5, the register 85 has associated therewith a seven segment decode and display register 87. The display command for this register to display the digit and decode the same from binary coded decimal form to numeric form is controlled by display command indicated by conductor 91 which is provided from the output of the flip-flop 89 the input of which is a power control signal, as indicated by the conductor 29, and the keyboard strobe signal 35. The flip-flop is reset by the clear command from the logic control as indicated by the conductor 31 and the output of the flip-flop will provide loading of the register 85 and the display of the digit on the decode and display module 87 of a time set by the keyboard strobe which initiates a clock timing signal in the logic control. Once the hundredth keyboard is set, a second digit will be applied in binary coded decimal form to the tens and units keyboard registers which will be identical to that shown in FIG. 5 with the tens units being loaded and displayed through the operation of a similar flip-flop logic control at a particular time and with the hundred unit digit being disabled after operation so that it retains the first digit selected. The third digit selected on the keyboard will similarly be loaded into the keyboard register for the units module which will be similar to register 85 and displayed on a display module 87 through operation of a similar flip-flop control at a timing signal originating from the keyboard strobe. Once the units digit is applied to the register, a signal indicated by the conductor or cabling 25 will be sent back to the logic system to indicate a full keyboard. During the period of time that the logic and registers are energized, even though they may not be conditioned through coin operation to receive signals from the input module, a clock in the logic control is running and counting in binary coded decimal from the integer zero through the integer 999 to select a random number. This random number is determined only upon the presence of an initial signal which is determined by the initial operation of a keyboard module assuming that the control aspects are activated through operation of a coin or the presence of a win signal in the control logic circuit. Thus, the random number will be selected by operation of the first manual digit selection at the input module and the keyboard strobe signal 14 will condition appropriate logic to stop the clock which has associated therewith a binary coded decimal counter for each digit that is counted. Thus, as will be seen in FIGS. 1 and 5, the signals from the logic control, indicated as clock frequency 36, is fed to all three display modules 20A, 20B and 20C, and in FIG. 5, is applied to the binary coded decimal counter 96 to establish the random number, it being understood that the termina-

tion of this signal will establish the number in all three binary coded decimal counters, one for each display module, only one of which is shown in FIG. 5. Thus all of the binary coded decimal counters will be set with initial operation from the control module. The keyboard register is controlled by the logic clock signal from the strobe indicated at 35 which will actually be a pulsed timed sequence which is initiated with each operation of the manual operation of the input module, independent of the clock frequency generated, as shown in 36. This signal at a particular period of time will be applied to the "and" gate 98 along with a logic 1 output from the flip-flop 89 to provide the load register signal 99 to the keyboard register. Thus, the keyboard will be loaded from all three display modules and displayed in accord with the operation of the flip-flop 89, the loading taking place first. It will be noted that associated with the keyboard register are high and low registers indicated at 90 and 97 with display modules at 92, 97 associated therewith. The output of the register 85 is fed to the registers 90 and 95 but is not displayed thereon. Thus as will be seen by the conductor 101, the output from the keyboard register 85 is similarly applied to the high and low registers 90 and 95 which are loaded only by input command indicated by conductors 102, and 103 respectively. Similarly, the output from these registers from the display on the output side thereof, as indicated by conductors 104, 105 respectively, are connected to a multiplex unit 100 as inputs to the same. Similarly, the binary coded decimal counter as indicated by the conductor 106 is supplied to the multiplex unit together with command signals 32, 33 which direct the application of either the outputs of the higher or lower registers to the output side thereof as indicated at 107 and to the input of a four bit comparator 110. This comparator also is fed from the output of the register 85 as evidenced by the conductor 101 and 108 so that the output multiplex unit can be compared against the content of the register 85 in a particular time sequence. Thus, whenever the keyboard has been filled, and the test button has been applied at the input module, the multiplexer is conditioned to transfer the binary coded decimal on the counter 96 through the multiplexer to the comparator 110 wherein it will be compared with the content of the register 85. The conductors 26, 27 and 28 will indicate the result of that comparison with a plus signal on the high conductor and zeros on the low and equal if the selected number should be higher in that of the random number on the multiplexer.

Assuming that the comparison between the selected digit and the digit from the binary decimal counter are the same, a check will be made in the next lower order digit utilizing the same procedure. Thus, in the operation of the display modules, the higher order digit or the hundredth digit in binary coded decimal form is compared from the keyboard register with the same digits of the random number and if the comparison exists or is equal, the circuit is enabled to continue a check in the 10 order digit following the same procedure and subsequently into the units digit or the third register 20C. At any point in the comparison of digits, a discrepancy between the random number and the digit in the keyboard will stop the comparison and an indication of high or low will prevail on the conductors 26 or 27. At this point, and before the selected number can be moved to the higher or lower register, a check

will be made of the previous number in the high or low register to insure that the selected number is not equal to, higher or lower, as the case may be, than the number in the respective register. Thus, the test command from the keyboard applied to the logic control 30 will initiate a series of steps which first checks the selected number in the keyboard or module registers and then assuming no exact comparison condition exists permits the logic control to apply a signal on either of the conductors 32, 33 to the multiplexer 100 depending upon whether the selected number was high or low so that the contents of the high or low display register will be fed through the multiplexer 100 to the comparator 110. In steps, the three display modules representing the hundredth unit and tens and units digits will be compared in the selected sequence, the higher order being compared first. Thus, assuming the selected number was higher than the random number, the content of the high register 90 will be fed through the conductor 104 to the multiplexer 100 and upon an input command on conductor 33 past to the comparator. The comparator still retains the keyboard register number and a comparison of the digits in binary coded decimal form takes place. Assuming that the particular digit being tested from the high register is higher than the selected number, the high line will again be energized indicating an error as previously described. The same would be true if the number would be equal and the equality would exist in all three registers. Assuming that the number is lower than the previous high in the comparison in the three registers, the conductors 27 would be energized and through the logic would enable the loading of the new information from the keyboard register into the high register 90 to be displayed on the display 92 eliminating the previous number. This will be accomplished by the test high and load signals 32 and 33 applied to an "and" gate 115 whose output indicated by the conductor 102 loads the keyboard number through conductors 101 into the high register for the display on the decoder 92. The opposite would take place in case the selected number were lower than the random number and yet higher than the previous number in the register 95 with the gate 116 being enabled to provide a signal through conductor 103 to register 95 to load the keyboard information into register 95 and display the information or digits, therein with the decoder 97 therein. Thus, the comparison effected between the keyboard number and the random number takes place in sequence for all three digits starting from the highest order and going down to the units display. Where there is a difference, that is absent a "win," the keyboard number is then checked against the previous high or low number included in a high or low register and being displayed therein as a previous selection. The check and "error" indication would result if the selected number were equal to that shown in the high or low register displays, as well as if the present selection was further from the random number than that previously recorded and displayed. The time sequence in which the above operations take place, as well as the loading of the high and low registers, is determined by the keyboard strobe which with the test operation from the input module starts a timing clock function in binary coded decimal form and which runs through a given number of counts performing these functions at different clock times. The strobe timing operation, when

completed, is restarted only by a subsequent command from the input module.

With reference to FIG. 6, the control logic block is shown as it relates to the basic timing and signal outputs therefrom. Thus the block 120 receives inputs from the keyboard module in the form of signals on the strobe 14, the test and the clear conductors. Within the logic block 120 is a gate to start the clock and decode unit 130 which initiates a particular timing sequence for each selection and command. Thus the clock decode is fed to a clock logic control timing block 140 out of which is provided the various keyboard strobe or time signals indicated by the conductor 142. In addition, the clock frequency 36 which runs continuously from a separate clock in the logic control timing unit and not started by the strobe control or test clear commands. It is a continuously running clock which runs when power is applied to the game device but which is stopped by the strobe control to set the random number in the binary coded form as indicated by the counters 96 in the modules. The logic timing block also receives an output from the input control logic, as indicated by the conductor 144, which is basically the test command 12 at a particular time sequence, this being applied to the block 150 through the conductor 145 which includes the error flip-flops, the high and low flip-flops, and the win test circuit, as will be explained in FIG. 7. The schematic block diagram, a control line 146 extends back from the logic block 150 to the input control logic to indicate an error which disables gate therein (not shown) so no further input by way of strobe or clock signals can be made until the clear button is set on the input module clearing information from the registers and inhibiting further transfer of data. The output of the control logic block 150 provides the error indication along with load register command, the test high and low signals, the win signal and controls for the error lamp, clear lamp and display and flash on the high and low registers. The details of the lamp indication are omitted for simplicity. The inputs to the logic block 150 are basically signals from the conductors 26, 27, 28 from the comparison circuit indicating high, low or win. It is the signal inputs plus the timing commands which enables the test high or test low signals and provides the error indication in the event that the error exists in the present selection as compared to the previous selection, namely, that the present guess is not closer to the random number than the previous selected number. The logic control circuit also shows a game coming block 70 which is initiated by coins and displays as to the number of game paid for but not used. The output of the block 150 reduces the amount with each win and when games are stored on the games coming display, the conductor 148 enables initiation of the control logic without the use of a coin to start another game. Similarly, the "win" signal reduces the "games coming" display count as indicated by the conductor 198.

FIG. 7 is the error detection circuit basically found in block 150 in FIG. 6 and in which the high, low, and equal signals from the comparison circuit as indicated by the conductors 26, 27 and 28 are fed as inputs. Three different timed sequences are provided with this error detection circuit which are controlled by the test signal 13 but spaced in timing so that the check and operation is performed in a given timed sequence between selections and commands. Thus, the conductors

TT1, TT2 and TT3 as evidenced by conductors 152, 153 and 154 enable the error detection circuit to be initially conditioned to receive commands, to make the comparisons and to provide the output for the test high, test low commands and which brings back into the comparator 110 the numbers from the high or low registers 90, 97 and provide the error indication output as indicated by the conductor 160. The error circuit includes flip-flops 162, 163 and 164, which are energized from the high, low or equal conductors 26 - 28, depending upon the results of the test of the selected number with the random number. If the tests were high or low one or the other of the flip-flops 183, 185, will have been energized and set, as will be hereinafter noted. Before the comparison with the random number and with a prior discrepancy indicated, the strobe at time TT1 provides that a clearing signal is applied to these flip-flops simultaneously from the conductor 152 which clears all of the flip-flops 162 - 164 at the start of a test cycle. Clearing of these flip-flops removes the test high 32 or test low 33 signal from the multiplexer 100, thus allowing the hidden random number as shown in line 106 to go through the multiplexer 100 and be compared in the comparator 110 with the selected number. At time TT2, or the energization of the timing signal on conductor 153, all of the flip-flops will be enabled and only the one having the proper signal thereon such as high, low or equal as a result of the test of the hidden number with the high or low register number will be energized. The energization of one of the flip-flops 162 or 163 will have set the test high or test low signal on conductors 32 or 33 which will pass the content of the high or low registers through the multiplexer to the comparator so that this information may be compared with the selected number. Thus at time TT2, as indicated by conductor 153, one of the flip-flops 162 - 164 will be energized to provide an output therefrom. The one of the flip-flops 162 - 164 energized at time TT2 will depend upon which signal, namely, high, low or equal, is present on the conductors 26 - 28. This will set the particular flip-flop for a condition of operation as indicated by the outputs 165, 166 or 167. In the event that the signals from the initial test, that is the selected number with the random number, was high or low, one or the other of the flip-flops 162 - 163 will be energized providing a test high or test low command on the conductors 32, 33 connected respectively to the output conductors 165, 166. This will have conditioned the apparatus to seek the previous high or low number included on the display modules or registers in the high or low registers to compare the same with the selected number as previously described. The output of the flip-flops 162 - 164 are fed through "and" gates 172, 173 and 174, respectively. In addition, these gates receive the second high, or low or equal signals from the comparator 110. The output of the gates 172 - 174 are all fed as inputs to the "or" gate 176 whose output feeds one of the input of a flip-flop 180 providing the error indication 160 output therefrom. The opposite input for the flip-flop 180 is the time signal 154. Flip-flops 181 and 182 are also conditioned with the operation of the flip-flops 162 and 163. Flip-flops 181 and 182 are cleared by the starting of a new game sequence 148. The flip-flops 181 and 182 may be set following TT3 shown as lines 154 to determine that a high or low transfer did occur. They will thus be conditioned for future tests which are to be

conducted against the high or low register. Therefore, the output of the flip-flops 181 and 182, as indicated by the conductors 183, 185 will have conditioned the gates 172 and 173 with the information of the previous test conditions of the selected number with the random number. When the high or low test signals 32 or 33 have been applied to the multiplexer, they pass the contents of the high or low registers to the comparator to compare the previous high or low register numbers with the selected numbers. In the test or comparison of all three digits or of the content of the high or low registers indicating the previous high or low selections, a new high, low or equal signal will be obtained on the conductors 26 - 28. With the operation of the logic system to conduct the high or low test error check, the sub sequence or timing continues to operate the error detection system. Certain conditions of input to the gates 172, 173 or 174 may be such as to energize the "or" gate 176 and turn on the flip-flop 180 to indicate the error. Thus, for example, if the test of the selected number had indicated a low signal when compared to the random number, line 27 would have been energized, while lines 26 and 28 would have been de-energized. Thus, the flip-flop 162 would have been set and the conductor 33 would have been energized to indicate a conducting of the test of the low register. As the content of the low register is loaded into the multiplexer, the lines 26 - 28 are conditioned or reset so that no signal appears thereon. The sub sequence timing clears the flip-flops 162 - 164 at the start of the test of the selected number with the hidden number so that only the flip-flop energized by the results of the test will remain enabled or set. If in the next comparison or the comparison of the selected number with the content of the low register, should either the lines 27 or 28 that is either lower to the previous low or equal to it be energized, then either of the gates 173 or 174 will be energized with the presence or such a signal to operate the "or" gate 176 and display an error on the conductor 160. Gate 173 will have been conditioned by flip flop 182 to gate a low signal to the or gate 176 and flip-flop 180. This will prevent further input information and transfer of the selected number to a register at the end of the time signal. Should the selected number be higher than the previous low, conductor 26 will have been energized, but since the flip-flop 162 was not set in the initial test, the absence of its output will be such as to not operate the gate 172 without an input signal from flip-flop 162. This will be true even though the high register has a number therein and flip-flop 181 is energized with an output or conductor 185. Consequently, no error will appear since the gate 176 will not become energized. The same will be true at the start of a game when either or both of the high or low registers have no numbers displaced therein and the flip-flops have not been conditioned with output. Further, where there is no number in a high or low register, an equal test signal is not possible on a high or low test of a selected number. Thus, at the end of the time sequence, the load register command from the block 150 will be applied to the display modules as indicated by FIG. 5 to transfer the content of the keyboard register 85 to the high or low register depending upon which of the conductors 32 or 33 had been energized, that is the test high or test low signal. Thus the load register signal will remove the previous number and display on the respective decoder elements 92 or 97 should one be present

and the new selected number will be loaded into the high or low register and displayed. In the event that the error signal had persisted, turning on the error indicating light and preventing transfer of information to the registers from the keyboard register, a further operation of the digital keys in the input modules would be ineffective in loading the keyboard register since it would remain as indicated full. Only the operation of the clear button 31a would be effective and this would clear or reset the setting of the flip-flop 89 unloading the keyboard register and conditioning the logic system for a new sequence of operation or a new selection of numbers.

In the event that the selected number was equal to the random number, the condition on the logic or comparison line 26, 27 and 28 would be such that only the conductor 28 would be energized. This would provide the output on the conductor 28 from the logic block 150 to display the win signal at the keyboard register with the flashing light. Under these conditions, the keyboard, high and low registers and the logic will be cleared for the start of another game by operation of the clear controls. Inter-connection of the clear command line with the high and low registers is indicated by the conductors 192, 195 connected to the display decoders 92, 97 respectively as well as conductor 148 in the logic error block. Similarly, the win signal turns on the game coming display 70 as indicated by the conductor 198 which reduces the count of any indication therein, to indicate a completed game. Unless there are additional games coming or unless additional coins have been inserted to increase the number in the block 70, the conductor 148 to the input control logic 120 will not be energized so that a new game will not be started until these conditions have been satisfied. At this point, the clear number command from the input module is necessary to clear the content of the keyboard register which is now displayed so that with the win indication and the clear indication the input logic is again conditioned for selection of numbers to be fed to the keyboard register. With the win indication, the logic timing starts the clock timing frequency signal to establish a new random number.

The operation of a clear key at any time prior to the operation of the test key upon the selection of a three digit number or less than all of the necessary digits for a number will enable a player to change his mind and clear out the content of the keyboard register regardless of whether it is filled or not and without penalty to a player in the counting of tries of operations.

FIGS. 8 and 9 show structure for the remote control of the input module to the display module in the form of a block diagram for a transmitter and receiver respectively. The block 10 in FIG. 8 contains the digits from zero to nine and the test and clear commands for a 12 key keyboard with the output from the same being in binary coded decimal. The output therefrom is fed through a shift register 200 powered from a battery supply indicated by the conductors 201. The keyboard also is connected to a code converter 205 and a clock generator 206 which combines with gate 210 to provide a load signal 212 to the shift register. The block 206 and the code converter 205 energize and control the operation of a timing clock 215 which operates through a signal indicated at 220 to shift the register coding the input therefrom to the transmitter indicated in block 225. Information from the keyboard is trans-

mitted with operation of any of the keys and is not stored in the register 200. Thus individual digit selections for the selected number will be transmitted in serial form as clocked out by the generator and controlled by the strobe 206 which starts the clock to the transmitter so that a series of transmissions will take place, one representative of each keyboard operation. A code command for the test and clear signals similarly are transmitted in binary code from the transmitter to operate a receiver to be hereinafter described.

FIG. 9 shows the simplified receiver for remote control purposes as including a conventional receiver 230 receiving transmissions through the antenna 232 from the radiating transmitter 225. This starts a clock 235 which operates to control a shift register 240 gating the received data from the receiver as indicated by the conductor 238 and controlled by the clock to parallel form. The output from the register 240 in binary coded decimal form and in parallel form as distinguished from series form is impressed on the conductor 245 as game logic to feed the input of the keyboard register with a number selection made therefrom. The block 250 decodes command data such as test or clear and submits the same to the control logic and display modules through conductor 255 in the same manner as the direct connection shown in the embodiment as previously described. The remainder of the game device including the error detection circuit, the logic control, the display modules remain unchanged and only the transmitter and receiver are added between the keyboard module and the display modules and the keyboard logic as a connectionless type of coupling. The improved transmitter will be battery powered with the transmitter ready for transmission at all times. Similarly, the receiver will be powered to a point where it will receive input signals radiating from a transmitter and decode the same from serial to parallel form in a binary coded decimal and coded signals transmitting the operating commands from the input module.

Thus, in the improved game device, a simplified electronic display and logic with an input module is provided by means of which a hidden random number generated automatically in the apparatus can be searched for and found by players. The players will search for this number via the keyboard entry unit which will translate the operation of several manual selection means such as keys representing digits of a plural digit number into binary coded information which will be transmitted and displayed on the display board or numerical read-out units as the selected number. At the same time and upon the test command from the keyboard entry unit or input module, a comparison with these selected numbers will be made with the random number to indicate whether the same is high, low or equal to the same. In the present disclosure, the random number is any number between zero and a three digit number 999 and three rows of numerical digits zero to nine are displayed on the face of the display modules to represent the selected number in the search for the random number. The random number is selected from a continuous clock operation translated in binary coded decimal form determined only by the initial operation of the machine with the clock running continuously whenever the apparatus is energized but not operating in the selection or comparison of numbers. The improved game device is made in module form so that any number of digital units may be em-

ployed without necessitating a change in a control logic or the like. The improved game device not only checks the selected number with a hidden random number which was determined by the start of the game, but also checks the same against previous selections should there had been one which was higher or lower than the random number and is displayed on the board. Unless the newly selected number is closer to the random number than a previous selection, an error will exist and the new number will not be loaded into the registers and displayed as a selection and a player try. At this point, the apparatus will be cleared from the input module or the keyboard entry removing the error in the form of a selected number so that a new selection may be made in the search for the random number.

Thus in considering this invention, it should be remembered that the present disclosure is intended to be illustrative only, and the scope of the invention should be determined by the appended claims.

What is claimed is:

1. In the game device, in combination, an input module having a plurality of manually operable selection means the majority of which are integers representing numbers between zero and nine, additional selection means providing an operation command means included on the module, means included in the module for providing signal outputs from the manually operable selection means in binary coded decimal outputs therefrom representative of the integers of a plural digit number, a plurality of main display register means connected to and set by said input module and displaying the digits selected at the manually operable selection means in plural digit form, logic control means including means for generating a random number in binary coded decimal form having a plurality of integers equal to the number of integers selectable on the input module, said logic control means including clock generating means for generating a timing sequence signal and transfer commands, means included in the logic control means and responsive to an operation command from the input module to compare the selected integers from the manually operable selection means with the random number upon operation of the operation command in the manual selection means, additional register means representing high and low registers controlled by the logic control means for transferring the selected digits forming the number to a high or a low register depending on the comparison in the logic control with the random number, and means included in said high or low registers for displaying the selected number.

2. The game device of claim 1 and including in the logic control means, a circuit responsive to an exact comparison of a random number with a selected number to display the selected number in the main display registers with a win indication without transfer to a high or lower register and to prevent further input from the input module.

3. The game device of claim 2 including means in the logic control and connected to the main display register means for preventing further transfer of digits by the manually operable selection means after a number of digits have been selected equal to the number of digits to the random number.

4. The game device of claim 2 in which numbers displayed in the main register are displayed in the lighted display in digit form and including means upon transfer

of said number to a high or low register for displaying the number in the high or low register in a flashing lighting form.

5. The game device of claim 1 in which the main display register means and the additional register means each include separate registers for each digit in binary coded decimal form with each of the registers simultaneously receiving input signals from the input module with operation of the manually operable selection means and with the selected number being displayed in the main display register means prior to the comparison with the random number upon operation of the operation command.

6. The game device of claim 5 in which the main display register means and the additional register means include decoders and lighted displays operatively connected to the logic control and decoding and displaying the selected integers in numeric form from the binary coded decimal forms in the respective registers.

7. The game device of claim 6 in which previously selected numbers which are higher or lower than the random number are continuously displayed on the additional registers with the current selection of the of the selected number on the main display register means, and including means in the logic control after comparison of the random number with the selected number and before transfer of the selected number to a high or lower register depending upon the direction of comparison in the logic control for comparing the selected number with a previously selected high or low selection and determining whether the selected number is closer to the random number than the previously selected number.

8. The game device of claim 7 in which the logic control includes further means responsive to the comparison between the selected number and the previously selected number permitting transfer of the selected number to a high or lower register only if the selected number is closer to the random number than the previously selected number and including means for displaying an error in the selection if the selected number is not closer to the random than the previously selected number.

9. The game device of claim 8 in which the input module includes an additional operation command means in the selection means operative to clear the selected number from the registers with operation of the same.

10. The game device of claim 9 and including lighted counter means counting the number of complete operations of the manually operable selected means in a selection of a plural digit number which is compared with the random number and selectively displayed in the high or low register and the main display registers.

11. The game device of claim 1 and including energizing circuit control means for said register means and said logic control means including coin operated switch preventing operation of said register means and said logic control means until operation of the coin operated switch.

12. The game device of claim 11 in which said logic control means and said register means with said indicating and coding displays are mounted in a common structure and including a counter means displaying operation of the coin operated switch and energization of the logic control means and register means.

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13. The game device of claim 1 in which said input module is a self-contained portable unit and including a power supply and a radio transmitter for transmitting radio signals in binary coded decimal form and the operation commands in binary coded decimal form, and including the receiver means associated with the logic control means and said register means for receiving the radio signals from the input module and decoding the same for operation of said logic control means and said register means.

14. The game device of claim 13 in which the radio transmitter and the receiver means send and receive transmission in a bit form with the transmitter including a clock generator means, controlling operation of the clock generating means in said logic control means.

15. The game device of claim 1 in which the means for generating the random number in the logic control means includes separate clock generating means continuously counting between zero and the maximum of the plural digit number and converting said count to binary coded decimal form with said clock generation means being stopped and the random number established with initial operation of a manually operable selection means in the input module and with the random number retained in the logic control means for comparison with selected numbers through operation of the manually operated selection means.

16. A game device comprising, an input module, a plurality of registers connected to the input module, means included in the input module for providing the selection of a plural digit integer and converting said

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plural integer in to binary coded decimal form and transferring the same selectively to the plurality of registers, a logic control connected to said input module and said registers and operative in response to an initial operation of the input module to select a plural digit random number in binary coded decimal form and to store the same in the logic control, means included in the logic control and responsive in an operative command after selection of the plural digit integer in the input module to compare the random number with the selected number in said register in binary coded decimal form, means indicative of the comparison and operative upon a lack of comparison to transfer the selected digits to additional registers and display the same with respect to their relationship to their random number, and means included in the logic system operative upon a like comparison of the integers of the random number with the selected integers to indicate the like comparison and to prevent further operation of the input module in the selection of plural digit integers.

17. The game device of claim 16 in which the logic control includes clock generator means continuously counting between zero and the maximum of the plural digit number and converting the same count to binary coded decimal form with said counting sequence being continuous until initial operation of the input module to set the plural digit random number in binary coded decimal form in the logic control for comparison with selected numbers from the input module.

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