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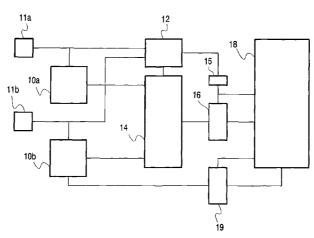
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[Continued on next page]

(54) Title: DATA PROCESSING CIRCUIT WITH MULTIPLEXED MEMORY



(57) Abstract: A data processing apparatus contains several processing circuits each operating under control of its own periodic clock signal, so that the clock signals may have different frequencies and/or can be autonomous. The several processing circuits each have an output for outputting memory access requests, which remain at the output for a validity duration interval defined by the clock signal of the particular processor. A multiplexing circuit multiplexes the access requests to a memory. The memory needs a minimum memory repetition period before it can accept an access request following acceptance of a preceding access request. The clock periods of the processing circuits are longer than the minimum memory repetition period. A timing circuit selects acceptance time points at which each particular access request from a first data processing circuit is accepted. The time point at which the particular request is accepted is always within the validity duration interval in which the particular access request is made. The timing circuit varies the position of the acceptance time points within the validity duration intervals, so that the position is delayed to make room for previously accepting an access request from another processor. The position is subsequently moved back toward a start of the validity duration interval in successive steps during application of successive access requests from the first data processing circuit.



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A. CLASSIFICATION OF SUBJECT MATTER IPC 7 G06F13/16

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B. FIELDS SEARCHED

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Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Х	US 6 412 049 B1 (PAWLOWSKI STEPHEN S ET AL) 25 June 2002 (2002-06-25) abstract column 1, line 6 - column 2, line 37	1-12
X	US 5 202 973 A (HO STEVEN ET AL) 13 April 1993 (1993-04-13) abstract; figures 1,4 column 3, line 7 - line 20 column 5, line 66 - column 6, line 9 claim 1	1-12
Α	EP 1 253 518 A (MATSUSHITA ELECTRIC IND CO LTD) 30 October 2002 (2002-10-30) abstract; figure 6	1-12

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Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Authorized officer Juenger, B

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