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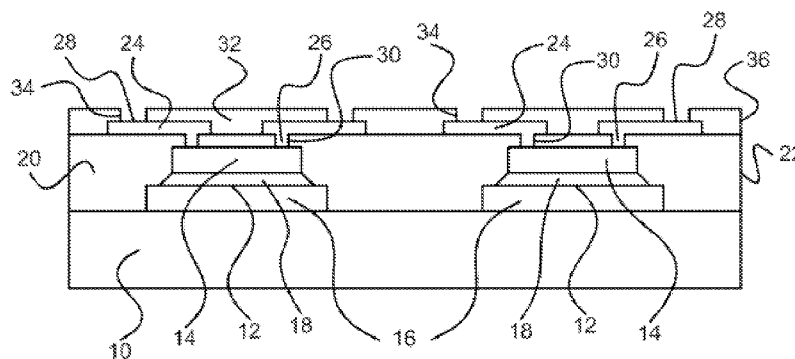


FIG. 3

(57) Abstract: A semiconductor packaging method, a semiconductor package and stacked semiconductor packages are provided. The method includes providing a carrier (10) having a plurality of semiconductor chip receiving areas (12) and attaching a plurality of first semiconductor chips (14) to the semiconductor chip receiving areas (12). The first semiconductor chips (14) are encapsulated with a first encapsulant (20) and a plurality of electrical connections (24) is formed to the first semiconductor chips (14). At least a portion of the carrier (10) is removed to provide a heat release area (38).



SEMICONDUCTOR PACKAGING METHOD, SEMICONDUCTOR PACKAGE AND STACKED SEMICONDUCTOR PACKAGES

Field of the Invention

The present invention relates to semiconductor packaging and more particularly to a semiconductor packaging method, a semiconductor package
5 and stacked semiconductor packages.

Background of the Invention

Manufacturability, thermal considerations and package dimensions are important considerations in semiconductor packaging as these affect
10 packaging cost, package applications and/or reliability. It would therefore be desirable to have a semiconductor packaging method and a semiconductor package that meets one or more of these needs.

Summary of the Invention

Accordingly, in a first aspect, the present invention provides a
15 semiconductor packaging method. The semiconductor packaging method includes providing a carrier having a plurality of semiconductor chip receiving areas and attaching a plurality of first semiconductor chips to the semiconductor chip receiving areas. The first semiconductor chips are encapsulated with a first encapsulant and a plurality of electrical connections
20 is formed to the first semiconductor chips. At least a portion of the carrier is removed to provide a heat release area.

In a second aspect, the present invention provides a semiconductor package including a first semiconductor chip, a first encapsulant encapsulating the first semiconductor chip, and a plurality of electrical
25 connections to the first semiconductor chip. A heat release area is arranged to release heat generated by the first semiconductor chip. The heat release area includes one of: a surface of a die pad to which the first semiconductor

chip is attached; a non-active surface of the first semiconductor chip; a surface of a conductive layer to which a die pad is attached, the first semiconductor chip being attached to the die pad; a surface of a conductive layer to which the first semiconductor chip is attached; a surface area of a heat sink attached to a conductive layer, the first semiconductor chip being attached to the conductive layer; a surface area of an array of heat sinks attached to a conductive layer, the first semiconductor chip being attached to the conductive layer; a surface area of a plurality of fins attached to a conductive layer, the first semiconductor chip being attached to the conductive layer; and a surface area of a heat sink attached to a conductive layer to which a die pad is attached, the first semiconductor chip being attached to the die pad.

In a third aspect, the present invention provides a stacked semiconductor package. The stacked semiconductor package includes a first semiconductor package in accordance with the second aspect and further including a plurality of vias extending through the first encapsulant to the first semiconductor chip, a plurality of first traces on a surface of the first encapsulant, the first traces being electrically connected by the vias to the first semiconductor chip, a second encapsulant encapsulating the first traces and a plurality of openings extending through the second encapsulant to expose a surface of the first traces. A plurality of solder bumps is attached to the exposed surface of the first traces. The stacked semiconductor package also includes a second semiconductor package in accordance with the second aspect and further including at least one of a plurality of pads, a plurality of connectors, a plurality of passive components, at least one strengthening element, an electromagnetic shielding structure and an inductor coil encapsulated by the first encapsulant. The solder bumps are electrically coupled to the pads of the second semiconductor package.

In a fourth aspect, the present invention provides a stacked semiconductor package. The stacked semiconductor package includes first and second semiconductor packages in accordance with the second aspect

and further including at least one of a plurality of pads, a plurality of connectors, a plurality of passive components, at least one strengthening element, an electromagnetic shielding structure and an inductor coil encapsulated by the first encapsulant. A solder material electrically couples a first die pad of the first semiconductor package to a second die pad of the second semiconductor package and a plurality of first pads of the first semiconductor package to a plurality of second pads of the second semiconductor package.

In a fifth aspect, the present invention provides a stacked semiconductor package. The stacked semiconductor package includes a first semiconductor package in accordance with the second aspect and further including a plurality of vias extending through the first encapsulant to the first semiconductor chip, a plurality of first traces on a surface of the first encapsulant, the first traces being electrically connected by the vias to the first semiconductor chip, a second encapsulant encapsulating the first traces and a plurality of openings extending through the second encapsulant to expose a surface of the first traces. A plurality of solder bumps is attached to the exposed surface of the first traces. The stacked semiconductor package also includes a second semiconductor package in accordance with the second aspect and further including at least one of a plurality of pads, a plurality of connectors, a plurality of passive components, at least one strengthening element, an electromagnetic shielding structure and an inductor coil encapsulated by the first encapsulant, and a plurality of openings formed in the conductive layer, the openings exposing a surface of the connectors. The solder bumps are electrically coupled to the exposed surface of the connectors of the second semiconductor package.

In a sixth aspect, the present invention provides a stacked semiconductor package. The stacked semiconductor package includes a first semiconductor package in accordance with the second aspect and further including at least one of a plurality of pads, a plurality of connectors, a plurality of passive components, at least one strengthening element, an

electromagnetic shielding structure and an inductor coil encapsulated by the first encapsulant, and a plurality of openings formed in the conductive layer, the openings exposing a surface of the connectors. The stacked semiconductor package also includes a second semiconductor package, the second semiconductor package being a wafer-level package having a plurality of solder bumps. The solder bumps are electrically coupled to the exposed surface of the connectors of the first semiconductor package.

In a seventh aspect, the present invention provides a semiconductor package including a first semiconductor chip, a plurality of connectors, a first encapsulant encapsulating the first semiconductor chip and the connectors, and a plurality of electrical connections to the first semiconductor chip and the connectors. A heat release area is arranged to release heat generated by the first semiconductor chip. The heat release area includes one of: a surface of a die pad to which the first semiconductor chip is attached; a surface of a conductive layer to which a die pad is attached, the first semiconductor chip being attached to the die pad; a surface of a conductive layer to which the first semiconductor chip is attached; and a surface area of a heat sink attached to a conductive layer, the first semiconductor chip being attached to the conductive layer.

In an eighth aspect, the present invention provides a stacked semiconductor package including a first semiconductor package in accordance with the seventh aspect and further including a plurality of vias extending through the first encapsulant to the first semiconductor chip, a plurality of first traces on a surface of the first encapsulant, the first traces being electrically connected by the vias to the first semiconductor chip and the connectors being electrically connected to the first traces, a second encapsulant encapsulating the first traces and a plurality of openings extending through the second encapsulant to expose a surface of the first traces. A plurality of solder bumps is attached to the exposed surface of the first traces. The stacked semiconductor package also includes a second semiconductor package in accordance with the seventh aspect and further

including a plurality of pads encapsulated by the first encapsulant, the connectors being provided on the pads. The solder bumps are electrically coupled to the pads of the second semiconductor package.

5 In a ninth aspect, the present invention provides a stacked semiconductor package including first and second semiconductor packages in accordance with the seventh aspect and further including a plurality of pads encapsulated by the first encapsulant, the connectors being provided on the pads. A solder material electrically couples a first die pad of the first semiconductor package to a second die pad of the second semiconductor
10 package and a plurality of first pads of the first semiconductor package to a plurality of second pads of the second semiconductor package.

In a tenth aspect, the present invention provides a stacked semiconductor package including a first semiconductor package in accordance with the seventh aspect and further including a plurality of vias
15 extending through the first encapsulant to the first semiconductor chip, a plurality of first traces on a surface of the first encapsulant, the first traces being electrically connected by the vias to the first semiconductor chip and the connectors being electrically connected to the first traces, a second encapsulant encapsulating the first traces and a plurality of openings
20 extending through the second encapsulant to expose a surface of the first traces. A plurality of solder bumps is attached to the exposed surface of the first traces. The stacked semiconductor package also includes a second semiconductor package in accordance with the seventh aspect and further including a plurality of pads encapsulated by the first encapsulant, the
25 connectors being provided on the pads, and a plurality of openings formed in the conductive layer, the openings exposing a surface of the connectors. The solder bumps are electrically coupled to the exposed surface of the connectors of the second semiconductor package.

In an eleventh aspect, the present invention provides a stacked
30 semiconductor package including a first semiconductor package in

accordance with the seventh aspect and further including a plurality of pads encapsulated by the first encapsulant, the connectors being provided on the pads, and a plurality of openings formed in the conductive layer, the openings exposing a surface of the connectors. The stacked semiconductor package
5 also includes a second semiconductor package, the second semiconductor package being a wafer-level package having a plurality of solder bumps. The solder bumps are electrically coupled to the exposed surface of the connectors of the first semiconductor package.

In a twelfth aspect, the present invention provides a semiconductor
10 package including a first semiconductor chip, a plurality of connectors, a first encapsulant encapsulating the first semiconductor chip and the connectors, and a plurality of electrical connections to the first semiconductor chip and the connectors. A heat release area is arranged to release heat generated by the first semiconductor chip. The heat release area includes one of: a surface
15 area of an array of heat sinks attached to a conductive layer, the first semiconductor chip being attached to the conductive layer; a surface area of a plurality of fins attached to a conductive layer, the first semiconductor chip being attached to the conductive layer; and a surface area of a heat sink attached to a conductive layer to which a die pad is attached, the first
20 semiconductor chip being attached to the die pad.

In a thirteenth aspect, the present invention provides a semiconductor package including a first semiconductor chip, an electromagnetic shielding structure, a first encapsulant encapsulating the first semiconductor chip and the electromagnetic shielding structure, and a plurality of electrical
25 connections to the first semiconductor chip and the electromagnetic shielding structure. A heat release area is arranged to release heat generated by the first semiconductor chip. The heat release area includes one of: a surface of a die pad to which the first semiconductor chip is attached; a surface of a conductive layer to which a die pad is attached, the first semiconductor chip
30 being attached to the die pad; a surface of a conductive layer to which the first semiconductor chip is attached; a surface area of a heat sink attached to a

conductive layer, the first semiconductor chip being attached to the conductive layer; a surface area of an array of heat sinks attached to a conductive layer, the first semiconductor chip being attached to the conductive layer; a surface area of a plurality of fins attached to a conductive layer, the first semiconductor chip being attached to the conductive layer; and a surface area of a heat sink attached to a conductive layer to which a die pad is attached, the first semiconductor chip being attached to the die pad.

In a fourteenth aspect, the present invention provides a semiconductor package including: a first semiconductor chip, at least one strengthening element, a first encapsulant encapsulating the first semiconductor chip and the at least one strengthening element, and a plurality of electrical connections to the first semiconductor chip. A heat release area is arranged to release heat generated by the first semiconductor chip, the heat release area including one of: a surface of a die pad to which the first semiconductor chip is attached; a surface of a conductive layer to which a die pad is attached, the first semiconductor chip being attached to the die pad; a surface of a conductive layer to which the first semiconductor chip is attached; a surface area of a heat sink attached to a conductive layer, the first semiconductor chip being attached to the conductive layer; a surface area of an array of heat sinks attached to a conductive layer, the first semiconductor chip being attached to the conductive layer; a surface area of a plurality of fins attached to a conductive layer, the first semiconductor chip being attached to the conductive layer; and a surface area of a heat sink attached to a conductive layer to which a die pad is attached, the first semiconductor chip being attached to the die pad.

Other aspects and advantages of the invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

Brief Description of the Drawings

The following detailed description of preferred embodiments of the invention will be better understood when read in conjunction with the appended drawings. The present invention is illustrated by way of example
5 and is not limited by the accompanying figures, in which like references indicate similar elements. It is to be understood that the drawings are not to scale and have been simplified for ease of understanding the invention.

FIGS. 1 through 4 illustrate a semiconductor packaging method in accordance with an embodiment of the present invention;

10 FIGS. 5 through 7 are enlarged cross-sectional views of semiconductor packages in accordance with embodiments of the present invention;

FIGS. 8 through 12 illustrate additional processing steps in the semiconductor packaging method in accordance with various embodiments of the present invention;

15 FIGS. 13 through 15 illustrate a semiconductor packaging method in accordance with another embodiment of the present invention;

FIGS. 16 through 18 are enlarged cross-sectional views of multi-chip semiconductor packages in accordance with embodiments of the present invention;

20 FIGS. 19 and 20 are enlarged cross-sectional views of stacked semiconductor packages in accordance with embodiments of the present invention;

FIGS. 21 through 24 illustrate a semiconductor packaging method in accordance with yet another embodiment of the present invention;

25 FIGS. 25 through 27 illustrate a semiconductor packaging method in accordance with still another embodiment of the present invention;

FIGS. 28 and 29 illustrate a semiconductor packaging method in accordance with yet another embodiment of the present invention;

FIG. 30 illustrates a semiconductor packaging method in accordance with a further embodiment of the present invention;

5 FIGS. 31 and 32 are enlarged cross-sectional views of stacked semiconductor packages in accordance with a further embodiment of the present invention;

FIGS. 33 through 35 illustrate a semiconductor packaging method in accordance with another embodiment of the present invention;

10 FIGS. 36 and 37 illustrate a semiconductor packaging method in accordance with yet another embodiment of the present invention;

FIGS. 38 and 39 illustrate a semiconductor packaging method in accordance with still another embodiment of the present invention;

15 FIG. 40 illustrates a semiconductor packaging method in accordance with another embodiment of the present invention;

FIGS. 41 and 42 illustrate a semiconductor packaging method in accordance with yet another embodiment of the present invention;

FIG. 43 illustrates a semiconductor packaging method in accordance with still another embodiment of the present invention; and

20 FIGS. 44 and 45 are enlarged cross-sectional views of stacked semiconductor packages in accordance with other embodiments of the present invention.

Detailed Description Of The Invention

25 The detailed description set forth below in connection with the appended drawings is intended as a description of the presently preferred

embodiments of the invention, and is not intended to represent the only form in which the present invention may be practiced. It is to be understood that the same or equivalent functions may be accomplished by different embodiments that are intended to be encompassed within the scope of the invention. In the drawings, like numerals are used to indicate like elements throughout.

A semiconductor packaging method will now be described below with reference to FIGS. 1 through 4.

Referring now to FIG. 1, a carrier 10 having a plurality of semiconductor chip receiving areas 12 is provided. A plurality of first semiconductor chips 14 are attached to the semiconductor chip receiving areas 12.

The carrier 10 serves as a support and may be made of any suitable material that is relatively rigid for ease of handling during processing. The carrier 10 may have a thickness of between about 50 millimetres (mm) and about 500 mm. In one embodiment, the carrier 10 may be in the form of a panel made of steel or copper. In an alternative embodiment, the carrier 10 may include a first or base layer and a second or top layer formed of a first conductive material provided on the first layer. The first or base layer may be made of, for example, steel or aluminum and the second or top layer may be made of, for example, copper.

The first semiconductor chips 14 may be any type of circuit such as, for example, a digital signal processor (DSP) or a special function circuit, and are not limited to a particular technology such as complementary metal-oxide-semiconductor (CMOS), or derived from any particular wafer technology. Each of the first semiconductor chips 14 has an active surface and a back surface opposite to the active surface. The first semiconductor chips 14 may have a thickness of between about 30 microns (μm) and about 50 μm .

In the embodiment shown, the semiconductor chip receiving areas 12 include a plurality of die pads 16 provided on the carrier 10. In one embodiment, the die pads 16 may be formed on the carrier 10 by photolithography or electroplating. In an alternative embodiment where the carrier 10 includes a first or support layer and a second or working layer, the die pads 16 may be formed by patterning the second or top layer by etching away portions of the second or top layer.

An adhesive 18 may be used to attach the first semiconductor chips 14 to the die pads 16 with an active surface of the first semiconductor chips 14 facing away from the die pads 16. The adhesive 18 may be pre-deposited on the die pads 16 or a back surface of the first semiconductor chips 14 before attachment. Accordingly, the back surface of the first semiconductor chips 14 may be attached to the die pads 16 by means of the adhesive 18 pre-disposed on the die pads 16 or pre-formed on the back surface of the first semiconductor chips 14. The adhesive 18 may be a material with high thermal conductivity of about 2 watts per metre per Kelvin (W/mK) to about 20 W/mK, such as thermal adhesives from Arctic Silver™.

Referring now to FIG. 2, a top plan view of the carrier 10 in the form of a panel is shown. In the embodiment shown, a pattern of die pads 16 is provided on the carrier 10 and a plurality of first semiconductor chips 14 is disposed correspondingly thereon. As can be seen from FIG. 2, although two (2) semiconductor chip receiving areas 12 and two (2) first semiconductor chips 14 are illustrated in FIG. 1, it should be understood that the carrier 10 is not limited by the number of semiconductor chip receiving areas 12 and first semiconductor chips 14 shown and may in fact be used to package a greater number of first semiconductor chips 14 simultaneously. Advantageously, processing a gang of package units simultaneously on a panel scale helps reduce assembly cost.

Referring now to FIG. 3, the first semiconductor chips 14 are encapsulated with a first encapsulant 20. A first dielectric layer 22 is thus

disposed on the carrier 10 to encapsulate the first semiconductor chips 14 and the die pads 16 and this may be by process of molding, lamination or printing. In one embodiment, the first dielectric layer 22 may be formed using a thermosetting polymer material, such as an epoxy-based or phenol-based compound, in the form of a film sheet or paste. In another embodiment, the material may come in the form of a pellet or powder. Typically, the material may further comprises fillers such as silica. Preferably the first dielectric layer 22 is formed of a Ajinomoto Build-up Film (ABF) or epoxy molding compound (EMC). The first dielectric layer 22 may have a thickness of between about 100 μm and about 800 μm . The thickness of the first dielectric layer 22 may be thinned by grinding or polishing without exposing the first semiconductor chips 14.

After encapsulation, a plurality of electrical connections 24 is formed to the first semiconductor chips 14. In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 includes forming a plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chips 14, and forming a plurality of first traces 28 on a surface of the first encapsulant 20, the first traces 28 being electrically connected by the first vias 26 to the first semiconductor chips 14.

The first via 26 may be formed by forming a plurality of first openings 30 in the first dielectric layer 22 to expose an active surface of the first semiconductor chips 14, the locations of the first openings 30 correspond to input/output (I/O) pad locations on the active surface of the first semiconductor chips 14. The first openings 30 may be formed by laser drilling or photolithography.

The first vias 26 and the first traces 28 may be formed by a semi-additive electroplating process. More particularly, a metal seed layer may be deposited on the surface of the first dielectric layer 22 and the sidewalls of the first openings 30 by electroless plating. Thereafter, the first vias 26 are formed in the first openings 30 and the first traces 28 are formed on the seed

layer with a conductive material such as, for example, copper. Exposed portions of the seed layer are then removed. The first vias 26 electrically connect I/O pads on the active surface of the first semiconductor chips 14 to the first traces 28.

5 In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 further includes encapsulating the first traces 28 with a second encapsulant 32, and forming a plurality of second openings 34 through the second encapsulant 32 to expose a surface of the first traces 28. A second dielectric layer 36 is thus formed on the first dielectric layer 22, the
10 second dielectric layer 36 encapsulating the first traces 28. The second dielectric layer 36 may be formed by screening printing using, for example, a soldermask and the second openings 34 may be formed in the second dielectric layer 36 by photolithography. The exposed surface of the first traces 28 may be coated with a finishing layer, such as, for example, tin (Sn),
15 a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP). The second openings 34 may subsequently be filled with a conductive material such as, for example, solder paste.

Referring now to FIG. 4, at least a portion of the carrier 10 is removed to provide a heat release area 38. In the present embodiment, the heat
20 release area 38 is an exposed surface area of the die pads 16 after removal of the carrier 10. The carrier 10 may be removed by chemical etching or physical separation to expose the die pads 16. The exposed surface area of the die pads 16 may be coated with an anti-corrosion or anti-oxidation layer such as, for example, nickel (Ni) or an organic solderability preservative
25 (OSP).

After removal of the carrier 10 to expose the die pads 16, a plurality of semiconductor packages 40 thus formed may be separated along the vertical line A-A into individual package units by laser or mechanical dicing.

As can be seen from FIG. 4, each of the semiconductor packages 40
30 includes a first semiconductor chip 14, a first encapsulant 20 encapsulating

the first semiconductor chip 14, a plurality of electrical connections 24 to the first semiconductor chip 14, and a heat release area 38 arranged to release heat generated by the first semiconductor chip 14. In the present embodiment, the heat release area 38 includes a surface of a die pad 16 to which the first semiconductor chip 14 is attached.

In the embodiment shown, the electrical connections 24 to the first semiconductor chip 14 includes a plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chip 14, and a plurality of first traces 28 on a surface of the first encapsulant 20. The first traces 28 are electrically connected by the first vias 26 to the first semiconductor chip 14. A second encapsulant 32 encapsulates the first traces 28, and a plurality of openings 34 extends through the second encapsulant 32 to expose a surface of the first traces 28. Alternatively, the second encapsulant may be omitted and the first traces 28 is completely exposed on the first dielectric layer 22 for connection to external devices or circuits.

Advantageously, thin profile semiconductor packages 40 with a thickness of between about 150 μm and about 200 μm may be formed with the described semiconductor packaging method.

Alternative package forms with different types of electrical connections 24 to the first semiconductor chip 14 will now be described below with reference to FIGS. 5 through 7.

Referring now to FIG. 5, a semiconductor package 42 is shown. The semiconductor packaging method by which the semiconductor package 42 is formed differs from the earlier embodiment in that the step of forming the electrical connections 24 to the first semiconductor chips 14 includes forming a plurality of first conductive studs 44 on the first traces 28. The first conductive studs 44 may be formed on the first traces 28 by photolithography and electroplating.

Thereafter, the first traces 28 and the first conductive studs 44 are encapsulated with a second encapsulant 32. A second dielectric layer 36 is thus formed on the first dielectric layer 22, the second dielectric layer 36 encapsulating the first traces 28 and the first conductive studs 44. The second dielectric layer 36 may be formed on the first dielectric layer 22 by process of molding, lamination or printing. In one embodiment, the second dielectric layer 36 is formed using a thermosetting polymer material, such as an epoxy-based or phenol-based compound, in the form of a film sheet or paste. In another embodiment, the material may come in the form of a pellet or powder. Typically, the material may further comprise fillers such as silica. Preferably the second dielectric layer 36 is formed of a Ajinomoto Build-up Film (ABF) or epoxy molding compound (EMC).

A portion of the second encapsulant 32 is then removed to expose a surface of the first conductive studs 44. In one embodiment, the second dielectric layer 36 may be thinned down to expose the surface of the first conductive studs 44 by grinding or polishing. The exposed surface of the first conductive studs 44 may be coated with a finishing layer such as, for example, tin (Sn), a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP).

The semiconductor package 42 shown in FIG. 5 differs from the semiconductor package 40 shown in FIG. 4 in that the semiconductor package 42 includes a plurality of first conductive studs 44 on the first traces 28, and a second encapsulant 32 encapsulates the first traces 28 and the first conductive studs 44. A portion of the second encapsulant 32 is removed, exposing a surface of the first conductive studs 44.

Referring now to FIG. 6, a semiconductor package 46 is shown. The semiconductor packaging method by which the semiconductor package 46 is formed differs from the previous embodiments in that the step of forming the electrical connections 24 to the first semiconductor chips 14 further includes forming a plurality of second traces 48 on a surface of the second

encapsulant 32. In the present embodiment, a plurality of second vias 50 is formed in the second openings 34. Accordingly, the locations of the second openings 34 correspond to predetermined via locations on the surface of the first traces 28. The second traces 48 and the second vias 50 may be formed by a semi-additive electroplating process. More particularly, a metal seed layer may be deposited on the surface of the second dielectric layer 36 and the sidewalls of the second openings 34 by electroless plating. Thereafter, the second vias 50 are formed in the second openings 34 and the second traces 48 are formed on the seed layer with a conductive material such as, for example, copper. Exposed portions of the seed layer are then removed. The second vias 50 electrically connect the first traces 28 to the second traces 48.

The semiconductor package 46 may be completed by encapsulating the second traces 48 with a third encapsulant 52, and forming a plurality of third openings 54 through the third encapsulant 52 to expose a surface of the second traces 48. A third dielectric layer 56 is thus formed on the second dielectric layer 36, the third dielectric layer 56 encapsulating the second traces 48. The third dielectric layer 56 may be formed by screening printing using, for example, a soldermask and the third openings 54 may be formed in the third dielectric layer 56 by photolithography. The exposed surface of the second traces 48 may be coated with a finishing layer, such as, for example, tin (Sn), a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP). The third openings 54 may subsequently be filled with a conductive material such as, for example, solder paste.

Referring now to FIG. 7, a semiconductor package 58 is shown. The semiconductor packaging method by which the semiconductor package 58 is formed differs from the previous embodiment in that the semiconductor package 58 is completed by forming a plurality of second conductive studs 60 on the second traces 48. The second conductive studs 60 may be formed on the second traces 48 by photolithography and electroplating.

Thereafter, the second traces 48 and the second conductive studs 60 are encapsulated with a third encapsulant 52. A third dielectric layer 56 is thus formed on the second dielectric layer 36, the third dielectric layer 56 encapsulating the second traces 48 and the second conductive studs 60. The third dielectric layer 56 may be formed on the second dielectric layer 36 by process of molding, lamination or printing. In one embodiment, the third dielectric layer 56 is formed using a thermosetting polymer material, such as an epoxy-based or phenol-based compound, in the form of a film sheet or paste. In another embodiment, the material may come in the form of a pellet or powder. Typically, the material may further comprises fillers such as silica. Preferably the third dielectric layer 56 is formed of a Ajinomoto Build-up Film (ABF) or epoxy molding compound (EMC).

A portion of the third encapsulant 52 is then removed to expose a surface of the second conductive studs 60. In one embodiment, the third dielectric layer 56 may be thinned down to expose the surface of the second conductive studs 60 by grinding or polishing. The exposed surface of the second conductive studs 60 may be coated with a finishing layer such as, for example, tin (Sn), a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP).

The semiconductor package 46 shown in FIG. 6 and the semiconductor package 58 shown in FIG. 7 differ from the earlier embodiments in that the semiconductor packages 46 and 58 further include a plurality of second traces 48 on a surface of the second encapsulant 32 and are formed with multiple electrical connection layers. Similar steps may be repeated to obtain semiconductor packages having more multiple layers electrical connection layer for greater routing density and higher functionality applications.

In the embodiments described above, the semiconductor packages 40, 42, 46 and 58 are formed with a planar package back surface and a sunk-in thermal pad or die pad 16.

Various methods of prepping the first semiconductor chip 14 for formation of the first vias 12 and/or forming the first vias 12 will now be described below with reference to FIGS. 8 through 12.

Referring now to FIG. 8, an enlarged sectional view of a portion of an active surface of the first semiconductor chip 14 is shown. The first semiconductor chip 14 includes a circuit layer 62 provided on a bulk silicon layer 64, a plurality of circuit pads 66 electrically connected to the circuit layer 62 and a passivation layer 68 provided over the circuit layer 62 exposing an area of the circuit pads 66 on the active surface of the first semiconductor chip 14. In an alternative embodiment, a repassivation layer (not shown) may be provided over the passivation layer 68, the repassivation layer exposing a smaller area of the circuit pads 66.

The circuit pads 66 may be formed of aluminum (Al), the passivation layer 68 may be formed of silicon nitride (SiN) or silicon dioxide (SiO) and the repassivation layer may be formed of polyimide.

In the present embodiment, the semiconductor packaging method further includes forming an electrically conductive layer 70 over at least one of the circuit pads 66 of the first semiconductor chip 14 prior to forming the electrical connections 24 to the first semiconductor chip 14. Accordingly, a semiconductor package thus formed further includes an electrically conductive layer 70 over at least one of a plurality of circuit pads 66 of the first semiconductor chip 14.

The electrically conductive layer 70 may be formed by electroless plating of nickel, copper, gold finishing or a nickel/copper (Ni/Cu) layering or a nickel/gold (Ni/Au) layering on the circuit pads 66.

In a subsequent step of forming the first openings 30 in the first dielectric layer 22, the first openings 30 expose only the electrically conductive layer 70 on the active surface of the first semiconductor chip 14. The area of the first openings 30 in the first dielectric layer 22 is thus smaller

than the surface area of the electrically conductive layer 70 formed over each of the circuit pads 66. Accordingly, in a subsequent step of forming the first vias 26, the first vias 26 are only formed on a portion of the electrically conductive layer 70 exposed by the first openings 30.

5 Referring now to FIG. 9, an alternative form of the electrically conductive layer 70 is shown. In the embodiment shown, a surface area of the electrically conductive layer 70 is greater than a surface area of the circuit pad 66 over which the electrically conductive layer 70 is formed.

The electrically conductive layer 70 of the present embodiment may be
10 formed by sputtering the passivation layer 68 with a seed layer of a titanium-tungsten/copper (TiW/Cu) layering or a titanium/copper (Ti/Cu) layering, disposing a photoresist layer on the seed layer, processing the photoresist layer to form a pattern of openings exposing portions of the seed layer, electroplating copper (Cu) on the exposed portions of the seed layer
15 corresponding to the locations of the circuit pads 66, removing the photoresist layer, and etching away the exposed seed layer to expose the passivation layer 68.

In the present embodiment where the width and surface area of the electrically conductive layer 70 is greater than a width and surface area of the
20 circuit pad 66 over which the electrically conductive layer 70 is formed, portions of the electrically conductive layer 70 extend onto the passivation layer 68 around the circuit pads 66. Advantageously, the larger width and surface area of the electrically conductive layer 70 compared to the width and surface area of the circuit pad 66 provides greater flexibility and tolerance in
25 terms of the size and/or positioning of the subsequently formed first openings 30 and first vias 26 as in such an embodiment, the first openings 30 and the subsequent first vias 26 may be formed outside the area of the circuit pads 66. This makes formation of a larger first via 26 possible, the larger first via 26 with greater area and volume providing greater mechanical strength and
30 better thermal and electrical performance. A larger first via 26 is also better

able to accommodate an offset when the first openings 30 are formed by laser firing. This increases the reliability of the semiconductor packages formed.

Further advantageously, in both the embodiments shown in FIGS. 8 and 9, because the first openings 30 and the first vias 26 are formed on the electrically conductive layer 70, the interface between the first encapsulant 20 and the passivation layer 68 is prevented from coming into direct contact with chemicals used in the subsequent processing steps and this helps to prevent damage of the passivation layer 68, for example, from delamination, in the subsequent processing steps.

Referring now to FIG. 10, a schematic plan view of the circuit pad 66 over which the electrically conductive layer 70 of FIG. 9 and the first via 26 are formed is shown. In the embodiment shown, the first via 26 is formed in an oval shape. Advantageously, this allows for a narrower pitch between the subsequently formed first traces 28.

In alternative embodiments, the first openings 30 and the first vias 26 may be formed of other shapes such as, for example, a circular shape or a rectangular shape. The first openings 30 may also be formed of a series of overlapping laser firings to provide an opening with an elongate shape.

Referring now to FIG. 11, another form of the electrically conductive layer 70 is shown. In the embodiment shown, the electrically conductive layer 70 includes a pad portion 72 positioned above the circuit pad 66 over which the electrically conductive layer 70 is formed and a line portion 74 extending away from the circuit pad 66. In the present embodiment, the electrical connections 24 to the first semiconductor chip 14 are formed from the line portion 74 of the electrically conductive layer 70.

In the embodiment shown, the pad portion 72 of the electrically conductive layer 70 covers the circuit pad 66 and the line portion of the electrically conductive layer 70 extends away on the passivation layer 68 from the location of the circuit pad 66 to the location of the first opening 30. The

first opening 30 and the first via 26 are thus formed away from the circuit pad 66. In this manner, and advantageously, the electrically conductive layer 70 provides another layer for routing of electrical signals prior to connecting to the first vias 26 and the first traces 28.

5 Referring now to FIG. 12, a schematic plan view of the circuit pad 66 over which the electrically conductive layer 70 of FIG. 11 and the first via 26 are formed is shown. As can be seen from FIG. 12, an area of the pad portion 72 of the electrically conductive layer 70 is greater than a corresponding area of the circuit pad 66 such that the pad portion 72 covers
10 the whole of the circuit pad 66. In the embodiment shown, a width of the line portion 74 of the electrically conductive layer 70 is greater than a width of the first opening 30 and the first via 26. The first opening 30 exposes only a portion of the line portion 74 of the electrically conductive layer 70 and the first via 26 is formed only on the exposed area of the line portion 74.

15 In the present embodiment, the first via 26 is formed in a circular shape. In alternative embodiments, the first openings 30 and the first vias 26 may be formed of other shapes such as, for example, an oval shape or a rectangular shape with a major axis parallel to a length of the line portion 74. The first openings 30 may also be formed of a series of overlapping laser
20 firings to provide an opening with an elongate shape. An elongate shape such as an oval or a rectangular shape increases a contact area between the first via 26 and the first traces 28, increasing mechanical strength and providing better thermal and electrical performance.

Another semiconductor packaging method will now be described below
25 with reference to FIGS. 13 through 15.

Referring now to FIG. 13, the semiconductor packaging method of the present embodiment differs from the earlier embodiments in that the semiconductor packaging method includes forming a plurality of connectors or columns 76 on the carrier 10 prior to the encapsulation step.

Referring now to FIG. 14, the connectors 76 may be disposed away from the die pads, preferably around the die pads 16 as shown.

Referring again to FIG. 13, the connectors 76 may be formed to a level lower than a surface of the first semiconductor chips 14 in the present embodiment. In such an embodiment, a surface of the connectors 76 is lower than an active surface of the first semiconductor chips 14 and the active surface of the first semiconductor chips 14 is further away from the carrier 10 than the surface of the connectors 76.

The first semiconductor chips 14 and the connectors 76 are then encapsulated with a first encapsulant 20. A first dielectric layer 22 is thus disposed on the carrier 10 to encapsulate the first semiconductor chips 14, the die pads 16 and the connectors 76, and this may be by process of molding, lamination or printing. In one embodiment, the first dielectric layer 22 may be formed using using a thermosetting polymer material, such as an epoxy-based or phenol-based compound, in the form of a film sheet or paste. In another embodiment, the material may come in the form of a pellet or powder. Typically, the material may further comprises fillers such as silica. Preferably the first dielectric layer 22 is formed of a Ajinomoto Build-up Film (ABF) or epoxy molding compound (EMC). The first dielectric layer 22 may have a thickness of between about 100 μm and about 800 μm . The thickness of the first dielectric layer 22 may be thinned by grinding or polishing without exposing the first semiconductor chips 14 and the connectors 76.

After encapsulation, a plurality of electrical connections 24 is formed to the first semiconductor chips 14 and the connectors 76. In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 includes forming a plurality of first openings 30 through the first dielectric layer 22 to expose an active surface of the first semiconductor chips 14 and a surface of the connectors 76. This may be by laser drilling. The locations of the first openings 30 correspond to the I/O pad locations on the

active surface of the first semiconductor chips 14 and the locations of the connectors 76 on the carrier 10.

A plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chips 14 and the connectors 76 and a plurality of first traces 28 on a surface of the first encapsulant 20 are then formed. The first traces 28 are electrically connected by the first vias 26 to the first semiconductor chips 14.

The first vias 26 and the first traces 28 may be formed by a semi-additive electroplating process. More particularly, a metal seed layer may be deposited on the surface of the first dielectric layer 22 and the sidewalls of the first openings 30 by electroless plating. Thereafter, the first vias 26 are formed in the first openings 30 and the first traces 28 are formed on the seed layer with a conductive material such as, for example, copper. Exposed portions of the seed layer are then removed. The first vias 26 electrically connect I/O pads on the active surface of the first semiconductor chips 14 and the connectors 76 to the first traces 28.

In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 further includes encapsulating the first traces 28 with a second encapsulant 32, and forming a plurality of second openings 34 through the second encapsulant 32 to expose a surface of the first traces 28. A second dielectric layer 36 is thus formed on the first dielectric layer 22, the second dielectric layer 36 encapsulating the first traces 28. The second dielectric layer 36 may be formed by screening printing using, for example, a soldermask and the second openings 34 may be formed in the second dielectric layer 36 by photolithography. The exposed surface of the first traces 28 may be coated with a finishing layer, such as, for example, tin (Sn), a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP). The second openings 34 may subsequently be filled with a conductive material such as, for example, solder paste.

At least a portion of the carrier 10 is then removed to provide a heat release area 38. In the present embodiment, the heat release area 38 is an exposed surface area of the die pads 16 after removal of the carrier 10. In the embodiment shown, a surface of the connectors 76 is also exposed after removing the at least a portion of the carrier 10.

The carrier 10 may be removed by chemical etching or physical separation to expose the die pads 16 and the surface of the connectors 76. The exposed surface area of the die pads 16 and the surface of the connectors 76 may be coated with an anti-corrosion or anti-oxidation layer such as, for example, nickel (Ni) or an organic solderability preservative (OSP).

After removal of the carrier 10 to expose the die pads 16 and the surface of the connectors 76, a plurality of semiconductor packages 78 thus formed may be separated along the vertical line A-A into individual package units by laser or mechanical dicing.

As can be seen from FIG. 13, each of the semiconductor packages 78 thus formed differs from the semiconductor package 40 of FIG. 4 in that the semiconductor package 78 includes a plurality of connectors 76 encapsulated by the first encapsulant 20. Preferably, the first vias 26 connected to the connectors 76 have a smaller area than that of the connectors 76 and thus reduces the necessary contact area to the first traces 28. This improves the routability of the electrical connection layer of the first traces.

Referring now to FIG. 15, another semiconductor packaging method will now be described. The semiconductor packaging method of the present embodiment differs from the previous embodiment in that the semiconductor packaging method includes forming a plurality of pads 80 on the carrier 10 prior to the encapsulation step.

In one embodiment, the pads 80 may be formed on the carrier 10 by photolithography or electroplating. In an alternative embodiment where the

carrier 10 includes a first or support layer and a second or working layer, the pads 80 may be formed by patterning the second or working layer by etching away portions of the second or working layer.

5 In the present embodiment, a plurality of connectors or columns 76 is formed on the pads 80. Each of the pads 80 of the present embodiment has a larger surface area than the corresponding connector 76. The pads 80 and the connectors 76 may be disposed around the die pads 16.

10 A further difference between the semiconductor packaging method of the present embodiment and the previous embodiment is that in the present embodiment, the connectors 76 are formed to a level higher than a surface of the first semiconductor chips 14. In such an embodiment, a surface of the connectors 76 is higher than an active surface of the first semiconductor chips 14 and the active surface of the first semiconductor chips 14 is nearer to the carrier 10 than the surface of the connectors 76.

15 The first semiconductor chips 14 and the connectors 76 are then encapsulated with a first encapsulant 20. A first dielectric layer 22 is thus disposed on the carrier 10 to encapsulate the first semiconductor chips 14, the die pads 16, the connectors 76 and the pads 80, and this may be by process of molding, lamination or printing. In one embodiment, the first
20 dielectric layer 22 may be formed using a thermosetting polymer material, such as an epoxy-based or phenol-based compound in the form of a film sheet or paste. In another embodiment, the material may come in the form of a pellet or powder. Typically, the material may further comprises fillers such as silica. Preferably the first dielectric layer 22 is formed of a Ajinomoto Build-
25 up Film (ABF) or epoxy molding compound (EMC). The first dielectric layer 22 may have a thickness of between about 100 μm and about 800 μm . The thickness of the first dielectric layer 22 may be thinned by grinding or polishing to expose a surface of the connectors 76.

30 After encapsulation, a plurality of electrical connections 24 is formed to the first semiconductor chips 14. In the present embodiment, forming the

electrical connections 24 to the first semiconductor chips 14 includes forming a plurality of first openings 30 through the first dielectric layer 22 to expose an active surface of the first semiconductor chips 14. This may be by laser drilling. The locations of the first openings 30 correspond to the I/O pad locations on the active surface of the first semiconductor chips 14.

A plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chips 14 and a plurality of first traces 28 on a surface of the first encapsulant 20 are then formed. The first traces 28 are electrically connected by the first vias 26 to the first semiconductor chips 14. The first traces 28 are also electrically connected to the connectors 76.

The first vias 26 and the first traces 28 may be formed by a semi-additive electroplating process. More particularly, a metal seed layer may be deposited on the surface of the first dielectric layer 22 and the sidewalls of the first openings 30 by electroless plating. Thereafter, the first vias 26 are formed in the first openings 30 and the first traces 28 are formed on the seed layer with a conductive material such as, for example, copper. Exposed portions of the seed layer are then removed. The first vias 26 electrically connect I/O pads on the active surface of the first semiconductor chips 14 to the first traces 28. Consequent to the formation of the first traces 28, some of the connectors 76 may become further extended upwards from the surface of the first dielectric layer 22.

In the present embodiment, the step of forming the electrical connections 24 to the first semiconductor chips 14 includes forming a plurality of first conductive studs 44 on the first traces 28. The first conductive studs 44 may be formed on the first traces 28 by photolithography and electroplating.

Thereafter, the first traces 28 and the first conductive studs 44 are encapsulated with a second encapsulant 32. A second dielectric layer 36 is thus formed on the first dielectric layer 22, the second dielectric layer 36 encapsulating the first traces 28 and the first conductive studs 44. The

second dielectric layer 36 may be formed on the first dielectric layer 22 by process of molding, lamination or printing. In one embodiment, the second dielectric layer 36 is formed using a thermosetting polymer material, such as an epoxy-based or phenol-based compound, in the form of a film sheet or paste. In another embodiment, the material may come in the form of a pellet or powder. Typically, the material may further comprises fillers such as silica. Preferably the first dielectric layer 22 is formed of a Ajinomoto Build-up Film (ABF) or epoxy molding compound (EMC).

A portion of the second encapsulant 32 is then removed to expose a surface of the first conductive studs 44. In one embodiment, the second dielectric layer 36 may be thinned down to expose the surface of the first conductive studs 44 by grinding or polishing. The exposed surface of the first conductive studs 44 may be coated with a finishing layer such as, for example, tin (Sn), a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP).

At least a portion of the carrier 10 is then removed to provide a heat release area 38. In the present embodiment, the heat release area 38 is an exposed surface area of the die pads 16 after removal of the carrier 10. In the embodiment shown, a surface of the pads 80 is also exposed after removing the at least a portion of the carrier 10.

The carrier 10 may be removed by chemical etching or physical separation to expose the die pads 16 and the surface of the pads 80. The exposed surface area of the die pads 16 and the surface of the pads 80 may be coated with an anti-corrosion or anti-oxidation layer such as, for example, nickel (Ni) or an organic solderability preservative (OSP).

After removal of the carrier 10 to expose the die pads 16 and the surface of the pads 80, a plurality of semiconductor packages 82 thus formed may be separated along the vertical line A-A into individual package units by laser or mechanical dicing.

As can be seen from FIG. 15, each of the semiconductor packages 82 thus formed differs from the semiconductor package 78 of FIG. 13 in that the semiconductor package 78 includes a plurality of connectors 76 and a plurality of pads 80 encapsulated by the first encapsulant 20.

5 Advantageously, provision of the connectors 76 in the embodiments described above with reference to FIGS. 13 through 15 facilitates formation of multi-chip semiconductor packages and stacked semiconductor packages.

Various multi-chip package structures that may be formed with the semiconductor packaging method described above will now be described
10 below with reference to FIGS. 16 through 18.

Referring now to FIG. 16, a multi-chip semiconductor package 84 is shown. The multi-chip semiconductor package 84 includes a first semiconductor chip 14, a first encapsulant 20 encapsulating the first semiconductor chip 14, a plurality of electrical connections 24 to the first
15 semiconductor chip 14, and a heat release area 38 arranged to release heat generated by the first semiconductor chip 14. In the present embodiment, the heat release area 38 includes a surface of a die pad 16 to which the first semiconductor chip 14 is attached. In the embodiment shown, a plurality of connectors 76 and a plurality of pads 80 to which the connectors are attached
20 are also encapsulated by the first encapsulant 20.

In the present embodiment, a second semiconductor chip is attached to the die pad 16. A plurality of wire bonds 88 electrically connects the second semiconductor chip 86 to respective ones of the pads 80. A third encapsulant 52 encapsulates the second semiconductor chip 86 and the wire
25 bonds 88.

Referring now to FIG. 17, another multi-chip semiconductor package 90 is shown. The multi-chip semiconductor package 84 differs from the previous embodiment in that the multi-chip semiconductor package 84 includes a second semiconductor chip 86 attached to the die pad 16, and a

plurality of solder bumps 92 electrically connect the second semiconductor chip 86 to respective ones of the pads 80.

Referring now to FIG. 18, yet another multi-chip semiconductor package 94 is shown. The multi-chip semiconductor package 94 differs from the previous embodiment in that the multi-chip semiconductor package 94 includes a second semiconductor chip 86 having a plurality of solder bumps 92 attached, the solder bumps 92 electrically connecting the second semiconductor chip 86 to the exposed surface of the first traces 28.

Various stacked semiconductor packages that may be formed with the semiconductor packaging method described above will now be described below with reference to FIGS. 19 and 20.

Referring now to FIG. 19, a stacked semiconductor package 96 is shown. The stacked semiconductor package 96 includes a first semiconductor package 40 having a plurality of solder bumps 92 attached to the exposed surface of the first traces 28. The first semiconductor package 40 is stacked on a second semiconductor package 98 formed with a plurality of connectors 76 on a plurality of pads 80. The solder bumps 92 are electrically coupled to the pads 80 of the second semiconductor package 98.

The solder bumps 92 may be formed of any conductive bonding material such as, for example, a tin-based solder.

Referring now to FIG. 20, another stacked semiconductor package 100 is shown. The stacked semiconductor package 100 includes a first semiconductor package 102 formed with a plurality of connectors 76 on a plurality of first pads 104. The first semiconductor package 102 is stacked on a second semiconductor package 106 formed with a plurality of connectors 76 on a plurality of second pads 108. A solder material 110 electrically couples a first die pad 112 of the first semiconductor package 102 to a second die pad 114 of the second semiconductor package 106 and the first pads 104 of the

first semiconductor package 102 to the second pads 108 of the second semiconductor package 106.

In the embodiment shown, a dummy pad 116 is provided on each of the first semiconductor package 102 and the second semiconductor package 106 for attachment.

Another semiconductor packaging method will now be described below with reference to FIGS. 21 through 24.

Referring now to FIG. 21, the semiconductor packaging method of the present embodiment differs from the earlier embodiments in that the carrier 10 includes a first or support layer 118 and a second or working layer 120 provided on the first layer 118, the second layer 120 being formed of a first conductive material.

The first or support layer 118 may be made of steel and the second or working layer 120 may be made of copper. In one embodiment, the first or support layer 118 is a polymer resin sheet.

A plurality of die pads 16 are provided on the carrier 10. This may be by etching away portions of the second or working layer 120 outside a predetermined region without exposing the first or support layer 118. In an alternative embodiment, the die pads 16 may be formed by electroplating on the second or working layer 120. The locations of the die pads 16 may be pre-determined and patterned using photolithography. As can be seen from FIG. 21, a surface of the die pads 16 is elevated from a surface of the second or working layer 120.

A plurality of first semiconductor chips 14 are then attached to the die pads 16 with an active surface of the first semiconductor chips 14 facing away from the die pads 16. An adhesive 18 may be used to attach the first semiconductor chips 14 to the die pads 16. When in the form of a die-attach paste, the adhesive 18 may be pre-deposited on the die pads 16 before

attachment of the first semiconductor chips 14. When in the form of a die-attach film, the adhesive 18 may be provided on a back surface of the first semiconductor chips 14.

5 The first semiconductor chips 14 are then encapsulated with a first encapsulant 20. A first dielectric layer 22 is thus disposed on the carrier 10 to encapsulate the first semiconductor chips 14 and the die pads 16.

10 After encapsulation, a plurality of electrical connections 24 is formed to the first semiconductor chips 14. In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 includes forming a plurality of first openings 30 through the first dielectric layer 22 to expose an active surface of the first semiconductor chips 14. The locations of the first openings 30 correspond to the I/O pad locations on the active surface of the first semiconductor chips 14.

15 A plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chips 14 and a plurality of first traces 28 on a surface of the first encapsulant 20 are then formed. The first traces 28 are electrically connected by the first vias 26 to the first semiconductor chips 14. More particularly, the first vias 26 electrically connect I/O pads on the active surface of the first semiconductor chips 14 to the first traces 28.

20 In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 further includes encapsulating the first traces 28 with a second encapsulant 32, and forming a plurality of second openings 34 through the second encapsulant 32 to expose a surface of the first traces 28. A second dielectric layer 36 is thus formed on the first dielectric layer 22, the second dielectric layer 36 encapsulating the first traces 28. The exposed surface of the first traces 28 may be coated with a finishing layer, such as, for example, tin (Sn), a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP). The second openings 34 may subsequently be filled with a conductive material such as, for example, solder paste.

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Referring now to FIG. 22, at least a portion of the carrier 10 is removed to provide a heat release area 38. In the present embodiment, the step of removing the at least a portion of the carrier 10 to provide the heat release area 38 includes removing at least a portion of the first layer 118 of the carrier 10. More particularly, the first or support layer 118 of the carrier 10 is removed to expose the second or working layer 120. Accordingly, the heat release area 38 in the embodiment shown is a surface of a conductive layer 120 to which the die pads 16 are attached. The exposed surface of the second or working layer 120 may be coated with an anti-corrosion or anti-oxidation layer such as, for example, nickel (Ni) or an organic solderability preservative (OSP).

After removal of the first layer 118 of the carrier 10 to expose the second or working layer 120, a plurality of semiconductor packages 122 thus formed may be separated along the vertical line A-A into individual package units by laser or mechanical dicing. The exposed second or working layer 120 forms a thermal plane for the finished package structure 122.

As can be seen from FIG. 22, each of the semiconductor packages 122 thus formed includes a first semiconductor chip 14, a first encapsulant 20 encapsulating the first semiconductor chip 14, a plurality of electrical connections 24 to the first semiconductor chip 14, and a heat release area 38 arranged to release heat generated by the first semiconductor chip 14. In the present embodiment, the heat release area 38 includes a surface of a conductive layer 120 to which the die pad 16 is attached, the first semiconductor chip 14 being attached to the die pad 16.

In an alternative embodiment, the semiconductor packages 122 may be completed with a plurality of first conductive studs 44 on the first traces 28 as described above in an earlier embodiment. In another embodiment, die pads 16 in FIG. 21 and 22, and the semiconductor packages 122 may be omitted and the first semiconductor chip 14 is attached to the conductive layer 120.

Referring now to FIG. 23, the thermal plane may be omitted in an alternative embodiment by removing the second or working layer 120 of the carrier 10 after removing the first or support layer 118 of the carrier 10 before unit separation. This exposes the surface of the die pads 16 and the first
5 dielectric layer 22 and may be by chemical etching or physical separation.

Still further, the die pads 16 and the adhesive 18 may also be removed after removing the second or working layer 120 of the carrier 10 before unit separation. The die pads 16 may be removed by chemical etching and the adhesive may be removed by chemical dissolving or washing. This creates a
10 cavity 124 in the package structure that exposes a back surface of the first semiconductor chips 14. In such an embodiment, the heat release area 38 comprises an exposed surface of the first semiconductor chips 14 after removal of the carrier 10 and the die pads 16.

As can be seen from FIG. 23, the back surface of the first
15 semiconductor chips is lower than a surface of the first dielectric layer 22. The back surface of the first semiconductor chips 14 may only be partially exposed if the size (area) of the die pads 16 is smaller than the size (area) of the first semiconductor chips 14. The exposed back surface of the first semiconductor chips may be coated or sputtered with a protective layer such
20 as, for example, titanium (Ti) or chromium (Cr).

Each of the semiconductor packages 126 thus formed includes a first semiconductor chip 14, a first encapsulant 20 encapsulating the first semiconductor chip 14, a plurality of electrical connections 24 to the first semiconductor chip 14, and a heat release area 38 arranged to release heat
25 generated by the first semiconductor chip 14. In the present embodiment, the heat release area 38 includes a non-active surface of the first semiconductor chip 14.

Referring now to FIG. 24, another semiconductor packaging method will now be described. The semiconductor packaging method of the present
30 embodiment differs from the previous embodiment in that the semiconductor

packaging method includes attaching a plurality of passive components 128 to the carrier 10 prior to the encapsulation step.

The passive components 128 may be disposed on a surface of the second or working layer 120 around a periphery of each of the die pads or platforms 16. The passive components 128 may be capacitors, resistors, diodes, integrated passive devices (IPD) or combinations thereof. A component adhesive 130 may be used to attach the passive components 128 to the surface of the second or working layer 120. The locations where the passive components 128 are to be mounted may be pre-marked using laser or other engraving means on the surface of the second or working layer 120. The component adhesive 130 may be pre-deposited on the second or working layer 120 (die-attach paste) or on the back surface of the passive components 128 (die-attach film) before attachment.

The first semiconductor chips 14 are attached to the die pads or platforms 16 with an active surface of the first semiconductor chips 14 facing away from the die pads or platforms 16. An adhesive 18 may be used to attach the first semiconductor chips 14 to the die pads 16. The die pads or platforms 16 may be used to compensate for the difference in thickness between the first semiconductor chips 14 and the passive components 128, especially in the case of thin chips. The thickness of the die pads or platforms 16 may be pre-determined and formed such that the active surface of the first semiconductor chips 14 is substantially level or higher than a surface of the passive components 128.

The first semiconductor chips 14 and the passive components 128 are then encapsulated with a first encapsulant 20. A first dielectric layer 22 is thus disposed on the carrier 10 to encapsulate the first semiconductor chips 14, the die pads 16 and the passive components 128.

After encapsulation, a plurality of electrical connections 24 is formed to the first semiconductor chips 14. In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 includes forming

a plurality of first openings 30 through the first dielectric layer 22 to expose electrodes on an active surface of the first semiconductor chips 14 and the passive components 128. This may be by laser drilling or photolithography. The locations of the first openings 30 correspond to the electrode locations on the active surface of the first semiconductor chips 14 and the passive components 128. The depth of the first openings 30 to both the active surface of the first semiconductor chips 14 and the passive components 128 may be substantially equal as a result of using the die pads or platforms 16 to compensate for the difference in thickness between the first semiconductor chips 14 and the passive components 128.

A plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chips 14 and a plurality of first traces 28 on a surface of the first encapsulant 20 are then formed. The first traces 28 are electrically connected by the first vias 26 to the first semiconductor chips 14. The first traces 28 are also electrically connected to the passive components 128. The first vias 26 electrically connect the electrodes on the active surface of the first semiconductor chips 14 and the passive components 128 to the first traces 28.

At least a portion of the carrier 10 is then removed to provide a heat release area 38. In the present embodiment, the step of removing the at least a portion of the carrier 10 to provide the heat release area 38 includes removing at least a portion of the first layer 118 of the carrier 10. More particularly, the first or support layer 118 of the carrier 10 is removed to expose the second or working layer 120.

In the embodiment shown, a portion of the second layer 120 of the carrier 10 is also removed to form a plurality of component pads 132 after removing the first layer 118 of the carrier 10. More particularly, the second or working layer 120 may be patterned by removing portions of the second or working layer 120 of the carrier 10 after removing the first or support layer 118 of the carrier 10 before unit separation. This may be by photolithography and

chemical etching and exposes a surface of the die pads or platforms 16 and the first dielectric layer 22. The remaining portions of the second or working layer 120 forms the component pads 130 corresponding to the locations of the passive components 128 such that the component adhesive 130 component pads 132 is covered and not exposed. The exposed surface of the die pads 16 and the remaining portions of the second or working layer 120 may be coated with an anti-corrosion or anti-oxidation layer such as, for example, nickel (Ni) or an organic solderability preservative (OSP). Each of the die pads 16 forms a thermal pad for the finished package structure.

10 After removal of the carrier 10 to expose the die pads 16 and to form the component pads 132, a plurality of semiconductor packages 134 thus formed may be separated along the vertical line A-A into individual package units by laser or mechanical dicing.

15 As can be seen from FIG. 24, each of the semiconductor packages 134 thus formed differs from the semiconductor packages of the previous embodiments in that each of the semiconductor packages 134 includes a plurality of passive components 128 encapsulated by the first encapsulant 20.

20 In an alternative embodiment, the semiconductor packages 134 may be completed with a plurality of first conductive studs 44 on the first traces 28 as described above in an earlier embodiment.

In yet another embodiment, the semiconductor packages 134 may be provided with a plurality of connectors 76 or a plurality of connectors 76 formed on a plurality of pads 80 as described above in earlier embodiments, instead of the passive components 128.

25 Another semiconductor packaging method will now be described below with reference to FIGS. 25 through 27.

Referring now to FIG. 25, the semiconductor packaging method of the present embodiment differs from the earlier embodiments in that the first

semiconductor chips 14 are attached to the semiconductor chip receiving areas 12 defined on the second or working layer 120 of the carrier 10 with an active surface of the first semiconductor chips 14 facing away from the semiconductor chip receiving areas 12. An adhesive 18 may be used to
5 attach the first semiconductor chips 14 to the semiconductor chip receiving areas 12. In the embodiment shown, a plurality of connectors or columns 76 is also provided on the second or working layer 120 of the carrier 10.

The first semiconductor chips 14 and the connectors 76 are encapsulated with a first encapsulant 20. A first dielectric layer 22 is thus
10 disposed on the carrier 10 to encapsulate the first semiconductor chips 14 and the connectors 76. The first dielectric layer 22 may be formed using a thermosetting polymer material, such as epoxy-based or phenol-based, in the form of a film sheet or paste. In another embodiment, the material may come in the form of a pellet or powder. Typically, the material may further comprises
15 fillers such as silica. Preferably the first dielectric layer 22 is formed of an Ajinomoto buildup film (ABF) or an epoxy compound.

After encapsulation, a plurality of electrical connections 24 is formed to the first semiconductor chips 14. In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 includes forming
20 a plurality of first openings 30 through the first dielectric layer 22 to expose an active surface of the first semiconductor chips 14 and a surface of the connectors 76. The locations of the first openings 30 correspond to the I/O pad locations on the active surface of the first semiconductor chips 14 and the locations of the connectors 76 on the carrier 10.

25 A plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chips 14 and the connectors 76 and a plurality of first traces 28 on a surface of the first encapsulant 20 are then formed. The first traces 28 are electrically connected by the first vias 26 to the first semiconductor chips 14.

In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 further includes encapsulating the first traces 28 with a second encapsulant 32, and forming a plurality of second openings 34 through the second encapsulant 32 to expose a surface of the first traces 28.

5 A second dielectric layer 36 is thus formed on the first dielectric layer 22, the second dielectric layer 36 encapsulating the first traces 28. The exposed surface of the first traces 28 may be coated with a finishing layer, such as, for example, tin (Sn), a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP). The second openings 34 may subsequently be filled with
10 a conductive material such as, for example, solder paste.

At least a portion of the carrier 10 is removed to provide a heat release area 38. In the present embodiment, the step of removing the at least a portion of the carrier 10 to provide the heat release area 38 includes removing at least a portion of the first layer 118 of the carrier 10. More particularly,
15 portions of the first or support layer 118 of the carrier 10 are selectively removed and the remaining portions of the first or support layer 118 provide a plurality of heat sinks or thermal blocks 136 on the second or working layer 120 of the carrier 10. In this manner, a plurality of heat sinks 136 is formed from removal of a portion of the first layer 118 of the carrier 10.
20 Advantageously, the heat sinks 136 increase the surface area to the surrounding for better heat dissipation. The selective removal of the first or support layer 118 may be by photolithography and chemical etching. The exposed surface of the second or working layer 120 of the carrier 10 may be coated with an anti-corrosion or anti-oxidation layer such as, for example,
25 nickel (Ni) or an organic solderability preservative (OSP). In this embodiment, the second or working layer 120 forms a thermal plane for the finished package structure.

In the present embodiment, the connectors 76 embedded within the first dielectric layer 22 connect the top of the package unit to the base of the
30 package unit, connecting the second or working layer 120 with the heat sinks or thermal blocks 136 to external pads of the package for external

connections. The heat sinks 136 may also act as a ground shield and the first semiconductor chips 14 may be electrically connected to the heat sinks 136 via a path of the first traces 28, the first vias 26 and the connectors 76 for grounding purpose. In one embodiment, a plurality of vertical connectors 76
5 may be disposed in a peripheral arrangement and be connected to the heat sinks 136, serving as an electromagnetic shield for shielding the first semiconductor chips 14 from external electrical disturbances.

In the embodiment shown, a coating layer 138 is formed over an exposed portion of the second layer 120 of the carrier 10 and the heat sinks
10 136 after removing the at least a portion of the first layer 118 of the carrier 10. The coating layer 138 may be formed on the exposed surface of the second or working layer 120 and the heat sinks or thermal blocks 136 by electrolytic plating using the second or working layer 120 as a conductive plane for the whole panel. The coating layer 138 may be of a different material than the
15 heat sinks or thermal blocks 136 to create a differential thermal conductivity for enhanced thermal dissipation. The heat sinks or thermal blocks 136 may be made of steel and the coating layer 138 may be made of copper or nickel. The coating layer 138 may also be an anti-corrosion or anti-oxidation layer such as, for example, nickel (Ni) or an organic solderability preservative
20 (OSP).

A plurality of semiconductor packages 140 thus formed may be separated along the vertical line A-A into individual package units by laser or mechanical dicing. Because singulation takes place along the regions of the exposed second or working layer 120 where a thickness of the carrier 10 has
25 been significantly reduced after selectively removing portions of the first or support layer 118, the singulation process is facilitated. This translates, for example, into faster sawing times and reduced sawblade wear.

As can be seen from FIG. 25, an area of each of the heat sinks or thermal blocks 136 is smaller than an area of the corresponding
30 semiconductor package 140. As such, a step is present around a periphery of

each of the semiconductor packages 140 such that a thickness of the semiconductor package 140 around the periphery is less than the thickness of the semiconductor package 140 at a central region. The area of each of the heat sinks or thermal blocks 136 may be larger than an area of the
5 corresponding first semiconductor chip 14.

Each of the semiconductor packages 140 thus formed includes a first semiconductor chip 14, a first encapsulant 20 encapsulating the first semiconductor chip 14, a plurality of electrical connections 24 to the first semiconductor chip 14, and a heat release area 38 arranged to release heat
10 generated by the first semiconductor chip 14. In the present embodiment, the heat release area 38 includes a surface area of a heat sink 136 attached to a first surface of a conductive layer 120, the first semiconductor chip 14 being attached to a second surface of the conductive layer 120. In the embodiment shown, the semiconductor package 140 includes a coating layer 138 over the
15 heat release area 38.

In an alternative embodiment, the semiconductor packages 140 may be completed with a plurality of first conductive studs 44 on the first traces 28 as described above in an earlier embodiment.

In other embodiments, the semiconductor packages 140 may be
20 formed without the connectors 76, with the connectors 76 formed on a plurality of pads 80, with a plurality of passive components 128 and/or with a plurality of die pads 16 as described above in earlier embodiments.

In an embodiment where a die pad 16 is provided on a first surface of the second or working layer 120 and the first semiconductor chip 14 is
25 attached to the die pad 16, the heat release area 38 may include a surface area of a heat sink 136 attached to a second surface of the conductive layer 120, the die pad 16 being attached to the first surface of the conductive layer 120.

The thermal blocks 136 may be provided in different configurations. Examples of these will now be described below with reference to FIGS. 26 and 27.

Referring now to FIG. 26, a bottom plan view of an array of heat sinks 136 formed from removal of a portion of the first layer 118 of the carrier 10 is shown. In the embodiment shown, the first or support layer 118 is formed into an array of thermal blocks on the second or working layer 120 of the carrier 10. Advantageously, the array of heat sinks 136 increases the surface area to the surrounding for increased heat dissipation.

In the embodiment shown, the heat release area 38 includes a surface area of an array of heat sinks 136 attached to a first surface of a conductive layer 120, the first semiconductor chip 14 being attached to a second surface of the conductive layer 120.

Referring now to FIG. 27, a bottom plan view of a plurality of fins 142 formed from removal of a portion of the first layer 118 of the carrier 10 is shown. In the embodiment shown, the first or support layer 118 is formed into an array of thermal fins or walls on the second or working layer 120 of the carrier 10. Advantageously, the array of fins 142 increases the surface area to the surrounding for increased heat dissipation.

In the present embodiment, the heat release area 38 includes a surface area of a plurality of fins 142 attached to a first surface of a conductive layer 120, the first semiconductor chip 14 being attached to a second surface of the conductive layer 120.

Yet another semiconductor packaging method will now be described below with reference to FIGS. 28 and 29.

Referring now to FIG. 28, the semiconductor packaging method of the present embodiment includes providing a carrier 10 having a plurality of semiconductor chip receiving areas 12. The carrier 10 of the present

embodiment includes a first or support layer 118 and a second or working layer 120 provided on the first layer 118, the second layer 120 being formed of a first conductive material. The first or support layer 118 may be made of steel or aluminum and the second or working layer 120 may be made of copper.

A plurality of first semiconductor chips 14 is attached to the semiconductor chip receiving areas 12 defined on the second or working layer 120 of the carrier 10 with an active surface of the first semiconductor chips 14 facing away from the semiconductor chip receiving areas 12. A back surface of the first semiconductor chips 14 opposite to the active surface of the first semiconductor chips 14 may be provided with a barrier layer. The barrier layer may be formed by sputtering using a titanium/chromium (Ti/Cr) layering or a chromium/copper (Cr/Cu) layering.

An adhesive 18 may be used to attach the first semiconductor chips 14 to the semiconductor chip receiving areas 12.

The first semiconductor chips 14 are encapsulated with a first encapsulant 20. A first dielectric layer 22 is thus disposed on the carrier 10 to encapsulate the first semiconductor chips 14.

After encapsulation, a plurality of electrical connections 24 is formed to the first semiconductor chips 14. In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 includes forming a plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chips 14, and forming a plurality of first traces 28 on a surface of the first encapsulant 20, the first traces 28 being electrically connected by the first vias 26 to the first semiconductor chips 14.

In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 further includes encapsulating the first traces 28 with a second encapsulant 32, and forming a plurality of second openings 34 through the second encapsulant 32 to expose a surface of the first traces 28.

A second dielectric layer 36 is thus formed on the first dielectric layer 22, the second dielectric layer 36 encapsulating the first traces 28. The exposed surface of the first traces 28 may be coated with a finishing layer, such as, for example, tin (Sn), a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP). The second openings 34 may subsequently be filled with a conductive material such as, for example, solder paste.

At least a portion of the carrier 10 is removed to provide a heat release area 38. In the present embodiment, the first or support layer 118 of the carrier 10 is removed and at least one fourth opening 144 is formed through the second layer 120 of the carrier 10 to expose a surface of at least one of the first semiconductor chips 14 after removing the first layer 118 of the carrier 10. The first or support layer 118 of the carrier 10 may be removed by chemical etching and the fourth openings 144 may be formed by laser drilling. The locations of the openings correspond to a back surface of the first semiconductor chips 14. In the process of forming the fourth openings 144, a portion of the second or working layer 120 and a portion of the adhesive 18 are removed to expose a back surface of the first semiconductor chips 14.

In the embodiment shown, three (3) fourth openings 144 are formed through the second layer 120 of the carrier 10. Nevertheless, it should be appreciated by those of ordinary skill in the art that the present invention is not limited by the number of fourth openings 144 formed. In alternative embodiments, greater or fewer numbers of fourth openings 144 may be formed depending on the package requirements.

In the present embodiment, the at least one fourth opening 144 is filled with a solder material 146. In this manner, a plurality of third vias 148 is formed through the adhesive 18 and the second or working layer 120 of the carrier 10. The third vias 148 may be formed by depositing a metal seed layer on a surface of the second or working layer 120 and the sidewalls of the fourth openings 144 by electroless plating. The fourth openings 144 are then filled by solder electroplating, reflowing the solder paste and letting the solder

material flow within the fourth openings 144. Any exposed portions of the seed layer are removed. After reflowing, the reflowed surface of the solder material 146 may be higher than a surface of the second or working layer 120 of the carrier 10.

5 A plurality of semiconductor packages 150 thus formed may be separated along the vertical line A-A into individual package units by laser or mechanical dicing.

10 As can be seen from FIG. 28, each of the semiconductor packages 150 includes a first semiconductor chip 14, a first encapsulant 20 encapsulating the first semiconductor chip 14, a plurality of electrical connections 24 to the first semiconductor chip 14, and a heat release area 38 arranged to release heat generated by the first semiconductor chip 14. In the present embodiment, the heat release area 38 includes a surface of a conductive layer 120 to which the first semiconductor chip 14 is attached.

15 In the embodiment shown, the semiconductor package 150 further includes at least one fourth opening 144 extending through the conductive layer 120 to the non-active surface of the first semiconductor chip 14. In the present embodiment, the at least one fourth opening 144 is filled with a solder material 146.

20 The third vias 148 may be formed within the die region of the semiconductor package 150 and function as channels for dissipating heat generated during chip operation. The third vias 148 may be formed at hot spots of the first semiconductor chip 14 where most heat is generated during semiconductor chip functioning.

25 Referring now to FIG. 29, another semiconductor packaging method will now be described. The semiconductor packaging method of the present embodiment differs from the previous embodiment in that the at least one fourth opening 144 is filled with a second conductive material 152 to form the third vias 148 through the adhesive 18 and the second or working layer 120 of

the carrier 10. The third vias 148 may be formed by a semi-additive electroplating process involving depositing a metal seed layer on the surface of the second or working layer 120 of the carrier 10 and the sidewalls of the fourth openings 144 by electroless plating, filling the fourth openings 144 with a conductive material such as, for example, copper, and removing any exposed portions of the seed layer. The electroplated surface of the third vias 148 may be lower than a surface of the second or working layer 120 of the carrier 10.

The semiconductor package 152 of FIG. 29 differs from that shown in FIG. 28 in that the at least one fourth opening 144 is filled with a conductive material 152. Additionally, in the embodiment shown, the semiconductor package 152 further includes a layer of the conductive material 152 on the conductive layer 120.

Referring now to FIG. 30, another embodiment of the semiconductor packaging method will now be described. The semiconductor packaging method of the present embodiment includes providing a carrier 10 having a plurality of semiconductor chip receiving areas 12. The carrier 10 of the present embodiment includes a first or support layer 118 and a second or working layer 120 provided on the first layer 118, the second layer 120 being formed of a first conductive material. The first or support layer 118 may be made of steel or aluminum and the second or working layer 120 may be made of copper.

In the present embodiment, a plurality of connectors 76 is formed on the second or working layer 120. The connectors 76 may be formed by electroplating on the second or working layer 120. The locations of the connectors 76 may be pre-determined and patterned using photolithography. A surface of the connectors 76 is elevated from a surface of the second or working layer 120.

A plurality of first semiconductor chips 14 is attached to the semiconductor chip receiving areas 12 defined on the second or working layer

120 of the carrier 10 with an active surface of the first semiconductor chips 14 facing away from the semiconductor chip receiving areas 12.

An adhesive 18 may be used to attach the first semiconductor chips 14 to the semiconductor chip receiving areas 12.

5 The first semiconductor chips 14 and the connectors 76 are encapsulated with a first encapsulant 20. A first dielectric layer 22 is thus disposed on the carrier 10 to encapsulate the first semiconductor chips 14 and the connectors 76. The thickness of the first dielectric layer 22 may be thinned by grinding or polishing to expose a surface of the connectors 76.

10 After encapsulation, a plurality of electrical connections 24 is formed to the first semiconductor chips 14. In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 includes forming a plurality of first openings 30 through the first dielectric layer 22 to expose an active surface of the first semiconductor chips 14. The locations of the first
15 openings 30 correspond to electrode locations on the active surface of the first semiconductor chips 14.

A plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chips 14 and a plurality of first traces 28 on a surface of the first encapsulant 20 are then formed. The first traces 28 are electrically
20 connected by the first vias 26 to the first semiconductor chips 14.

In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 further includes encapsulating the first traces 28 with a second encapsulant 32, and forming a plurality of second openings 34 through the second encapsulant 32 to expose a surface of the first traces 28.
25 A second dielectric layer 36 is thus formed on the first dielectric layer 22, the second dielectric layer 36 encapsulating the first traces 28. The second dielectric layer 36 may be formed by screening printing using, for example, a soldermask and the second openings 34 may be formed in the second dielectric layer 36 by photolithography. The exposed surface of the first

traces 28 may be coated with a finishing layer, such as, for example, tin (Sn), a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP). The second openings 34 may subsequently be filled with a conductive material such as, for example, solder paste.

5 At least a portion of the carrier 10 is removed to provide a heat release area 38. In the present embodiment, the first or support layer 118 of the carrier 10 is removed and the second or working layer 120 forms a thermal plane for the finished package structure. In the embodiment shown, a plurality of fifth openings 156 is formed in the second layer or thermal plane
10 120 to expose a surface of the connectors 76. This may be by photolithography or laser drilling.

A plurality of semiconductor packages 158 thus formed may be separated along the vertical line A-A into individual package units by laser or mechanical dicing.

15 Each of the semiconductor packages 158 includes a first semiconductor chip 14, a first encapsulant 20 encapsulating the first semiconductor chip 14 and a plurality of connectors 76, a plurality of electrical connections 24 to the first semiconductor chip 14, and a heat release area 38 arranged to release heat generated by the first semiconductor chip 14. In the
20 present embodiment, the heat release area 38 includes a surface of a conductive layer 120 to which the first semiconductor chip 14 is attached.

In the embodiment shown, the semiconductor package 158 further includes a plurality of fifth openings 156 formed in the conductive layer 120, the fifth openings 156 exposing a surface of the connectors 76.

25 As can be seen from FIG. 30, the connectors 76 are formed in the first dielectric layer 22 and are outside the die region of the semiconductor package 158. The connectors 76 may be used to connect a variety of second semiconductor packages. In an alternative embodiment, the connectors 76

may additionally be formed in the first dielectric layer 22 at one or more corner portions of the semiconductor packages 158.

In yet another alternative embodiment, the connectors 76 may be formed to a height that is lower than the active surface of the first semiconductor chip 14. In such an embodiment, a plurality of third vias 148
5 may be formed to electrically connect the connectors 76 to the first traces 28.

Various stacked semiconductor packages that may be formed with the semiconductor package 158 described above will now be described below with reference to FIGS. 31 and 32.

10 Referring now to FIG. 31, a stacked semiconductor package 160 is shown. The stacked semiconductor package 160 includes a first semiconductor package 40 having a plurality of solder bumps 92 attached to the exposed surface of the first traces 28. The first semiconductor package 40 is stacked on a second semiconductor package 158 formed with a plurality
15 of connectors 76. The solder bumps 92 are electrically coupled to the exposed surface of the connectors 76 of the second semiconductor package 158.

The solder bumps 92 may be formed of any conductive bonding material such as, for example, a tin-based solder.

20 Referring now to FIG. 32, another stacked semiconductor package 162 is shown. The stacked semiconductor package 162 includes a first semiconductor package 158 formed with a plurality of connectors 76. A second semiconductor package 164 is stacked on the first semiconductor package 158. In the present embodiment, the second semiconductor
25 package 164 is a wafer-level package having a plurality of solder bumps 92. The solder bumps 92 are electrically coupled to the exposed surface of the connectors 76 of the first semiconductor package 158.

In embodiment shown, the second semiconductor package 164 is a flip-chip chip scale package (CSP).

Another semiconductor packaging method will now be described below with reference to FIGS. 33 through 35.

5 Referring now to FIG. 33, the semiconductor packaging method of the present embodiment differs from the earlier embodiments in that at least one strengthening element 166 is formed on the carrier 10 prior to the encapsulation step.

10 Referring now to FIG. 34, a top plan view of the carrier 10 having a plurality of strengthening elements 166 formed thereon is shown. In the embodiment shown, the strengthening elements 166 are disposed around the die pad 16. In the present embodiment, the strengthening elements 166 are provided in a grid like arrangement. The strengthening elements 166 may be formed by photolithography and electroplating. Advantageously, the provision
15 of the strengthening elements 166 helps to strengthen the semiconductor package and reduce fragility of the semiconductor package.

In one embodiment, the strengthening elements 166 may be provided as strengthening fins around the first semiconductor chip 14. In such an embodiment, the electroplated strengthening fins may extend to a peripheral
20 surface of the semiconductor package.

Referring now to FIG. 35, a top plan view of the carrier 10 having a different arrangement of the at least one strengthening element 166 is shown. In the present embodiment, the at least one strengthening element 166 is a pre-formed metal grid or a strengthening grid structure provided around the
25 first semiconductor chip 14.

Referring again to FIG. 33, the first semiconductor chips 14 and the at least one strengthening element 166 are encapsulated with a first encapsulant 20. A first dielectric layer 22 is thus disposed on the carrier 10 to encapsulate

the first semiconductor chips 14, the die pads 16 and the at least one strengthening element 166. The thickness of the first dielectric layer 22 may be thinned by grinding or polishing without exposing the first semiconductor chips 14 and the at least one strengthening element 166.

5 After encapsulation, a plurality of electrical connections 24 is formed to the first semiconductor chips 14. In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 includes forming a plurality of first openings 30 through the first dielectric layer 22 to expose an active surface of the first semiconductor chips 14. The locations of the first
10 openings 30 correspond to the I/O pad locations on the active surface of the first semiconductor chips 14.

A plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chips 14 and a plurality of first traces 28 on a surface of the first encapsulant 20 are then formed. The first traces 28 are electrically
15 connected by the first vias 26 to the first semiconductor chips 14. More particularly, the first vias 26 electrically connect I/O pads on the active surface of the first semiconductor chips 14 to the first traces 28.

In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 further includes encapsulating the first traces 28
20 with a second encapsulant 32, and forming a plurality of second openings 34 through the second encapsulant 32 to expose a surface of the first traces 28. A second dielectric layer 36 is thus formed on the first dielectric layer 22, the second dielectric layer 36 encapsulating the first traces 28. The exposed surface of the first traces 28 may be coated with a finishing layer, such as, for
25 example, tin (Sn), a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP). The second openings 34 may subsequently be filled with a conductive material such as, for example, solder paste.

At least a portion of the carrier 10 is then removed to provide a heat release area 38. In the present embodiment, the heat release area 38 is an
30 exposed surface area of the die pads 16 after removal of the carrier 10. In the

embodiment shown, a surface of the at least one strengthening element 166 is also exposed after removing the at least a portion of the carrier 10.

After removal of the carrier 10 to expose the die pads 16 and the surface of the at least one strengthening element 166, a plurality of semiconductor packages 168 thus formed may be separated along the vertical line A-A into individual package units by laser or mechanical dicing.

As can be seen from FIG. 33, each of the semiconductor packages 168 thus formed differs from the semiconductor packages of the previous embodiments in that each of the semiconductor packages 168 includes at least one strengthening element 166 encapsulated by the first encapsulant 20.

In an alternative embodiment, the semiconductor packages 168 may be formed with a carrier 10 having a first or support layer and a second or working layer provided on the first layer, the second layer being formed of a conductive material. In such an embodiment, the first semiconductor chips 14 and the at least one strengthening element 166 may be attached to the second or working layer.

Another semiconductor packaging method will now be described below with reference to FIGS. 36 and 37.

Referring now to FIG. 36, the semiconductor packaging method of the present embodiment differs from the earlier embodiments in that an electromagnetic shielding structure 170 is formed on the carrier 10 prior to the encapsulation step.

Referring now to FIG. 37, a top plan view of the carrier 10 having the electromagnetic shielding structure 170 formed thereon is shown. In the embodiment shown, the electromagnetic shielding structure 170 is disposed around the die pad 16. In the present embodiment, the electromagnetic shielding structure 170 is of a wall-like structure and may be formed by

photolithography and electroplating. Advantageously, the provision of the electromagnetic shielding structure 170 helps contain electromagnetic radiation and reduce the amount of electromagnetic radiation that is emitted.

5 In alternative embodiments, the electromagnetic shielding structure 170 may be a circular wall structure extending around the first semiconductor chip 14 or a rectangular wall structure with curved corners extending around the first semiconductor chip 14.

Referring again to FIG. 36, the first semiconductor chips 14 and the electromagnetic shielding structure 170 are encapsulated with a first
10 encapsulant 20. A first dielectric layer 22 is thus disposed on the carrier 10 to encapsulate the first semiconductor chips 14, the die pads 16 and the electromagnetic shielding structure 170. The thickness of the first dielectric layer 22 may be thinned by grinding or polishing without exposing the first semiconductor chips 14.

15 After encapsulation, a plurality of electrical connections 24 is formed to the first semiconductor chips 14. In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 includes forming a plurality of first openings 30 through the first dielectric layer 22 to expose an active surface of the first semiconductor chips 14. The locations of the first
20 openings 30 correspond to the I/O pad locations on the active surface of the first semiconductor chips 14.

A plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chips 14 and a plurality of first traces 28 on a surface of the first encapsulant 20 are then formed. The first traces 28 are electrically
25 connected by the first vias 26 to the first semiconductor chips 14. More particularly, the first vias 26 electrically connect I/O pads on the active surface of the first semiconductor chips 14 to the first traces 28.

In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 further includes encapsulating the first traces 28

with a second encapsulant 32, and forming a plurality of second openings 34 through the second encapsulant 32 to expose a surface of the first traces 28. A second dielectric layer 36 is thus formed on the first dielectric layer 22, the second dielectric layer 36 encapsulating the first traces 28. The exposed surface of the first traces 28 may be coated with a finishing layer, such as, for example, tin (Sn), a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP). The second openings 34 may subsequently be filled with a conductive material such as, for example, solder paste.

At least a portion of the carrier 10 is then removed to provide a heat release area 38. In the present embodiment, the heat release area 38 is an exposed surface area of the die pads 16 after removal of the carrier 10. In the embodiment shown, a surface of the electromagnetic shielding structure 170 is also exposed after removing the at least a portion of the carrier 10.

After removal of the carrier 10 to expose the die pads 16 and the surface of the electromagnetic shielding structure 170, a plurality of semiconductor packages 172 thus formed may be separated along the vertical line A-A into individual package units by laser or mechanical dicing.

As can be seen from FIG. 36, each of the semiconductor packages 172 thus formed differs from the semiconductor packages of the previous embodiments in that each of the semiconductor packages 172 includes an electromagnetic shielding structure 170 encapsulated by the first encapsulant 20.

In an alternative embodiment, the semiconductor packages 172 may be formed with a carrier 10 having a first or support layer and a second or working layer provided on the first layer, the second layer being formed of a conductive material. In such an embodiment, the first semiconductor chips 14 and the electromagnetic shielding structure 170 may be attached to the second or working layer.

Another semiconductor packaging method will now be described below with reference to FIGS. 38 and 39.

Referring now to FIG. 38, the semiconductor packaging method of the present embodiment differs from the earlier embodiments in that a pattern of
5 embedded traces 174 is formed on the carrier 10 prior to the encapsulation step. The embedded traces 174 may be formed on the carrier 10 by photolithography or electroplating. In an alternative embodiment where the carrier 10 includes a first or support layer and a second or working layer, the embedded traces 174 may be formed by patterning the second or working
10 layer by etching away portions of the second or working layer. The pattern of embedded traces 174 is exposed on the same surface with the heat release area 38 of the semiconductor package 176. The pattern of embedded traces 174 may be an inductor coil.

In the present embodiment, a plurality of connectors or columns 76 is
15 formed on the embedded traces 174.

Referring now to FIG. 39, a top plan view of the carrier 10 having the embedded traces 174 formed thereon is shown. In the embodiment shown, the embedded traces 174 are disposed around the die pad 16.

In alternative embodiments, the embedded traces 174 may be
20 disposed away from the die pad 16 or the first semiconductor chip 14 in the absence of a die pad. In one embodiment, the embedded traces 174 may be formed at a side of the die pad 16 or the first semiconductor chip 14.

Referring again to FIG. 38, the first semiconductor chips 14, the embedded traces 174 and the connectors 76 are encapsulated with a first
25 encapsulant 20. A first dielectric layer 22 is thus disposed on the carrier 10 to encapsulate the first semiconductor chips 14, the die pads 16, the connectors 76 and the embedded traces 174. The thickness of the first dielectric layer 22 may be thinned by grinding or polishing without exposing the first semiconductor chips 14 and the connectors 76. In an alternative

embodiment, the thickness of the first dielectric layer 22 may be thinned to expose a surface of the connectors 76.

After encapsulation, a plurality of electrical connections 24 is formed to the first semiconductor chips 14. In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 includes forming a plurality of first openings 30 through the first dielectric layer 22 to expose an active surface of the first semiconductor chips 14 and a surface of the connectors 76. The locations of the first openings 30 correspond to the I/O pad locations on the active surface of the first semiconductor chips 14 and the locations of the connectors 76.

A plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chips 14 and the surface of the connectors 76 and a plurality of first traces 28 on a surface of the first encapsulant 20 are then formed. The first traces 28 are electrically connected by the first vias 26 to the first semiconductor chips 14. More particularly, the first vias 26 electrically connect I/O pads on the active surface of the first semiconductor chips 14 and the connectors 76 to the first traces 28.

In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 further includes encapsulating the first traces 28 with a second encapsulant 32, and forming a plurality of second openings 34 through the second encapsulant 32 to expose a surface of the first traces 28. A second dielectric layer 36 is thus formed on the first dielectric layer 22, the second dielectric layer 36 encapsulating the first traces 28. The exposed surface of the first traces 28 may be coated with a finishing layer, such as, for example, tin (Sn), a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP). The second openings 34 may subsequently be filled with a conductive material such as, for example, solder paste.

At least a portion of the carrier 10 is then removed to provide a heat release area 38. In the present embodiment, the heat release area 38 is an exposed surface area of the die pads 16 after removal of the carrier 10. In the

embodiment shown, a surface of the embedded traces 174 is also exposed after removing the at least a portion of the carrier 10.

After removal of the carrier 10 to expose the die pads 16 and the surface of the embedded traces 174, a plurality of semiconductor packages 176 thus formed may be separated along the vertical line A-A into individual package units by laser or mechanical dicing.

As can be seen from FIG. 38, each of the semiconductor packages 176 thus formed differs from the semiconductor packages of the previous embodiments in that each of the semiconductor packages 176 includes an embedded traces 174 encapsulated by the first encapsulant 20.

Referring now to FIG. 40, another semiconductor packaging method will now be described. The semiconductor packaging method of the present embodiment differs from the embodiment shown in FIG. 24 in that the semiconductor packaging method includes forming a plurality of pads 80 on the carrier 10 and attaching a plurality of passive components 128 to the pads 80 prior to the encapsulation step.

Each of the pads 80 of the present embodiment has a larger surface area than the corresponding passive component 128. The pads 80 and the passive components 128 may be disposed around the die pads 16. In one embodiment, the pads 80 may be formed on the carrier 10 by photolithography or electroplating. In an alternative embodiment where the carrier 10 includes a first or support layer and a second or working layer, the pads 80 may be formed by patterning the second or working layer by etching away portions of the second or working layer.

The passive components 128 may be capacitors, resistors, diodes, integrated passive devices (IPD) or combinations thereof. A component adhesive 130 may be used to attach the passive components 128 to the pads 80. The component adhesive 130 may be pre-deposited on the pads 80 (die-

attach paste) or on the back surface of the passive components 128 (die-attach film) before attachment.

The first semiconductor chips 14 are attached to the die pads or platforms 16 with an active surface of the first semiconductor chips 14 facing away from the die pads or platforms 16. An adhesive 18 may be used to attach the first semiconductor chips 14 to the die pads 16. The die pads or platforms 16 may be used to compensate for the difference in thickness between the first semiconductor chips 14 and the passive components 128, especially in the case of thin chips. The thickness of the die pads or platforms 16 may be pre-determined and formed such that the active surface of the first semiconductor chips 14 is substantially level or higher than a surface of the passive components 128.

The first semiconductor chips 14 and the passive components 128 are then encapsulated with a first encapsulant 20. A first dielectric layer 22 is thus disposed on the carrier 10 to encapsulate the first semiconductor chips 14, the die pads 16 and the passive components 128.

After encapsulation, a plurality of electrical connections 24 is formed to the first semiconductor chips 14. In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 includes forming a plurality of first openings 30 through the first dielectric layer 22 to expose electrodes on an active surface of the first semiconductor chips 14 and the passive components 128. This may be by laser drilling or photolithography. The locations of the first openings 30 correspond to the electrode locations on the active surface of the first semiconductor chips 14 and the passive components 128. The depth of the first openings 30 to both the active surface of the first semiconductor chips 14 and the passive components 128 may be substantially equal as a result of using the die pads or platforms 16 to compensate for the difference in thickness between the first semiconductor chips 14 and the passive components 128.

A plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chips 14 and a plurality of first traces 28 on a surface of the first encapsulant 20 are then formed. The first traces 28 are electrically connected by the first vias 26 to the first semiconductor chips 14. The first traces 28 are also electrically connected to the passive components 128. The first vias 26 electrically connect the electrodes on the active surface of the first semiconductor chips 14 and the passive components 128 to the first traces 28.

At least a portion of the carrier 10 is then removed to provide a heat release area 38. In the present embodiment, the heat release area 38 is an exposed surface area of the die pads 16 after removal of the carrier 10. In the embodiment shown, a surface of the pads 80 is also exposed after removing the at least a portion of the carrier 10.

The carrier 10 may be removed by chemical etching or physical separation to expose the die pads 16 and the surface of the pads 80. The exposed surface area of the die pads 16 and the surface of the pads 80 may be coated with an anti-corrosion or anti-oxidation layer such as, for example, nickel (Ni) or an organic solderability preservative (OSP).

After removal of the carrier 10 to expose the die pads 16 and the surface of the pads 80, a plurality of semiconductor packages 178 thus formed may be separated along the vertical line A-A into individual package units by laser or mechanical dicing.

As can be seen from FIG. 40, each of the semiconductor packages 178 thus formed differs from the semiconductor packages of the previous embodiments in that each of the semiconductor packages 134 includes a plurality of passive components 128 provided on a plurality of pads 80 and encapsulated by the first encapsulant 20.

In an alternative embodiment, the semiconductor packages 134 may be completed with a plurality of first conductive studs 44 on the first traces 28 as described above in an earlier embodiment.

Another semiconductor packaging method will now be described below
5 with reference to FIGS. 41 and 42.

Referring now to FIG. 41, the semiconductor packaging method of the present embodiment differs from the earlier embodiments in that an electromagnetic shielding structure 170 is formed on the carrier 10 prior to the encapsulation step. In this embodiment, the electromagnetic shielding
10 structure 170 includes a platform portion 180 to which the first semiconductor chip 14 is attached and a wall portion 182 extending around a periphery of the first semiconductor chip 14. The electromagnetic shielding structure 170 may be formed by photolithography and electroplating. Advantageously, the provision of the electromagnetic shielding structure 170 helps contain
15 electromagnetic radiation and reduce the amount of electromagnetic radiation that is emitted.

Referring now to FIG. 42, a top plan view of the carrier 10 having the electromagnetic shielding structure 170 formed thereon is shown. In the embodiment shown, the wall portion 182 of the electromagnetic shielding
20 structure 170 is a rectangular or squarish wall structure with curved corners extending around the first semiconductor chip 14. In alternative embodiments, the wall portion 182 of the electromagnetic shielding structure 170 may be a circular wall structure extending around the first semiconductor chip 14.

Referring again to FIG. 41, the first semiconductor chips 14 and the
25 electromagnetic shielding structure 170 are encapsulated with a first encapsulant 20. A first dielectric layer 22 is thus disposed on the carrier 10 to encapsulate the first semiconductor chips 14 and the electromagnetic shielding structure 170. The thickness of the first dielectric layer 22 may be

thinned by grinding or polishing without exposing the first semiconductor chips 14.

After encapsulation, a plurality of electrical connections 24 is formed to the first semiconductor chips 14. In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 includes forming a plurality of first openings 30 through the first dielectric layer 22 to expose an active surface of the first semiconductor chips 14. The locations of the first openings 30 correspond to the I/O pad locations on the active surface of the first semiconductor chips 14. In the embodiment shown, the first openings 30 are also formed to the wall portion 182 of the electromagnetic shielding structure 170.

A plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chips 14 and the wall portion 182 of the electromagnetic shielding structure 170 and a plurality of first traces 28 on a surface of the first encapsulant 20 are then formed. The first traces 28 are electrically connected by the first vias 26 to the first semiconductor chips 14. More particularly, the first vias 26 electrically connect I/O pads on the active surface of the first semiconductor chips 14 to the first traces 28.

In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 further includes encapsulating the first traces 28 with a second encapsulant 32, and forming a plurality of second openings 34 through the second encapsulant 32 to expose a surface of the first traces 28. A second dielectric layer 36 is thus formed on the first dielectric layer 22, the second dielectric layer 36 encapsulating the first traces 28. The exposed surface of the first traces 28 may be coated with a finishing layer, such as, for example, tin (Sn), a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP). The second openings 34 may subsequently be filled with a conductive material such as, for example, solder paste.

At least a portion of the carrier 10 is then removed to provide a heat release area 38. In the present embodiment, the heat release area 38 is an

exposed surface area of the platform portion 180 of the electromagnetic shielding structure 170 after removal of the carrier 10.

After removal of the carrier 10 to expose the platform portion 180 of the electromagnetic shielding structure 170, a plurality of semiconductor packages 184 thus formed may be separated along the vertical line A-A into individual package units by laser or mechanical dicing.

As can be seen from FIG. 41, each of the semiconductor packages 184 thus formed differs from the semiconductor packages of the previous embodiments in that each of the semiconductor packages 184 includes an electromagnetic shielding structure 170 encapsulated by the first encapsulant 20.

Referring now to FIG. 43, another embodiment of the semiconductor packaging method will now be described. The semiconductor packaging method of the present embodiment includes providing a carrier 10 having a plurality of semiconductor chip receiving areas 12. The carrier 10 of the present embodiment includes a first or support layer 118 and a second or working layer 120 provided on the first layer 118, the second layer 120 being formed of a first conductive material. The first or support layer 118 may be made of steel or aluminum and the second or working layer 120 may be made of copper.

In the present embodiment, a plurality of connectors 76 is formed on the second or working layer 120. The connectors 76 may be formed by electroplating on the second or working layer 120. The locations of the connectors 76 may be pre-determined and patterned using photolithography. A surface of the connectors 76 is elevated from a surface of the second or working layer 120.

A plurality of first semiconductor chips 14 is attached to the semiconductor chip receiving areas 12 defined on the second or working layer

120 of the carrier 10 with an active surface of the first semiconductor chips 14 facing away from the semiconductor chip receiving areas 12.

An adhesive 18 may be used to attach the first semiconductor chips 14 to the semiconductor chip receiving areas 12.

5 The first semiconductor chips 14 and the connectors 76 are encapsulated with a first encapsulant 20. A first dielectric layer 22 is thus disposed on the carrier 10 to encapsulate the first semiconductor chips 14 and the connectors 76.

10 After encapsulation, a plurality of electrical connections 24 is formed to the first semiconductor chips 14. In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 includes forming a plurality of first openings 30 through the first dielectric layer 22 to expose an active surface of the first semiconductor chips 14. The locations of the first openings 30 correspond to electrode locations on the active surface of the
15 first semiconductor chips 14. In the embodiment shown, the first openings 30 are also formed to the connectors 76.

 A plurality of first vias 26 extending through the first encapsulant 20 to the first semiconductor chips 14 and the connectors 76 and a plurality of first traces 28 on a surface of the first encapsulant 20 are then formed. The first
20 traces 28 are electrically connected by the first vias 26 to the first semiconductor chips 14.

 In the present embodiment, forming the electrical connections 24 to the first semiconductor chips 14 further includes encapsulating the first traces 28 with a second encapsulant 32, and forming a plurality of second openings 34
25 through the second encapsulant 32 to expose a surface of the first traces 28. A second dielectric layer 36 is thus formed on the first dielectric layer 22, the second dielectric layer 36 encapsulating the first traces 28. The second dielectric layer 36 may be formed by screening printing using, for example, a soldermask and the second openings 34 may be formed in the second

dielectric layer 36 by photolithography. The exposed surface of the first traces 28 may be coated with a finishing layer, such as, for example, tin (Sn), a nickel/gold (Ni/Au) layering or an organic solderability preservative (OSP). The second openings 34 may subsequently be filled with a conductive material such as, for example, solder paste.

At least a portion of the carrier 10 is removed to provide a heat release area 38. In the present embodiment, the first or support layer 118 of the carrier 10 is removed and the second or working layer 120 forms a thermal plane for the finished package structure. In the embodiment shown, a plurality of fifth openings 156 is formed in the second layer or thermal plane 120 to expose a surface of the connectors 76. This may be by photolithography or laser drilling.

A plurality of semiconductor packages 186 thus formed may be separated along the vertical line A-A into individual package units by laser or mechanical dicing.

Each of the semiconductor packages 186 includes a first semiconductor chip 14, a first encapsulant 20 encapsulating the first semiconductor chip 14 and a plurality of connectors 76, a plurality of electrical connections 24 to the first semiconductor chip 14, and a heat release area 38 arranged to release heat generated by the first semiconductor chip 14. In the present embodiment, the heat release area 38 includes a surface of a conductive layer 120 to which the first semiconductor chip 14 is attached.

In the embodiment shown, the semiconductor package 186 further includes a plurality of fifth openings 156 formed in the conductive layer 120, the fifth openings 156 exposing a surface of the connectors 76.

As can be seen from FIG. 43, the connectors 76 are formed in the first dielectric layer 22 and are outside the die region of the semiconductor package 186. The connectors 76 may be used to connect a variety of second semiconductor packages. In an alternative embodiment, the connectors 76

may additionally be formed in the first dielectric layer 22 at one or more corner portions of the semiconductor packages 186.

Various stacked semiconductor packages that may be formed with the semiconductor package 186 described above will now be described below
5 with reference to FIGS. 44 and 45.

Referring now to FIG. 44, a stacked semiconductor package 188 is shown. The stacked semiconductor package 188 includes a first semiconductor package 40 having a plurality of solder bumps 92 attached to the exposed surface of the first traces 28. The first semiconductor package
10 40 is stacked on a second semiconductor package 186 formed with a plurality of connectors 76. The solder bumps 92 are electrically coupled to the exposed surface of the connectors 76 of the second semiconductor package 186.

The solder bumps 92 may be formed of any conductive bonding
15 material such as, for example, a tin-based solder.

Referring now to FIG. 45, another stacked semiconductor package 190 is shown. The stacked semiconductor package 190 includes a first semiconductor package 186 formed with a plurality of connectors 76. A second semiconductor package 164 is stacked on the first semiconductor
20 package 186. In the present embodiment, the second semiconductor package 164 is a wafer-level package having a plurality of solder bumps 92. The solder bumps 92 are electrically coupled to the exposed surface of the connectors 76 of the first semiconductor package 186.

In embodiment shown, the second semiconductor package 164 is a
25 flip-chip chip scale package (CSP). As is evident from the foregoing discussion, the present invention provides an efficient semiconductor packaging method for forming semiconductor packages with improved thermal characteristics.

The description of the preferred embodiments of the present invention have been presented for purposes of illustration and description, but are not intended to be exhaustive or to limit the invention to the forms disclosed. It will be appreciated by those skilled in the art that changes could be made to the embodiments described above without departing from the broad inventive concept thereof. It is understood, therefore, that this invention is not limited to the particular embodiments disclosed, but covers modifications within the scope of the present invention as defined by the appended claims.

Further, unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise", "comprising" and the like are to be construed in an inclusive as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to".

CLAIMS

1. A semiconductor packaging method, comprising:
providing a carrier having a plurality of semiconductor chip receiving
5 areas;
attaching a plurality of first semiconductor chips to the semiconductor
chip receiving areas;
encapsulating the first semiconductor chips with a first encapsulant;
forming a plurality of electrical connections to the first semiconductor
10 chips; and
removing at least a portion of the carrier to provide a heat release area.
2. The semiconductor packaging method of claim 1, wherein the
semiconductor chip receiving areas comprise a plurality of die pads provided
15 on the carrier.
3. The semiconductor packaging method of claim 2, wherein the heat
release area comprises an exposed surface area of the die pads after
removal of the carrier.
20
4. The semiconductor packaging method of claim 2, wherein the heat
release area comprises an exposed surface of the first semiconductor chips
after removal of the carrier and the die pads.
- 25 5. The semiconductor packaging method of claim 1, wherein the step of
forming the electrical connections to the first semiconductor chips comprises:
forming a plurality of vias extending through the first encapsulant to the
first semiconductor chips; and
forming a plurality of first traces on a surface of the first encapsulant,
30 wherein the first traces are electrically connected by the vias to the first
semiconductor chips.

6. The semiconductor packaging method of claim 5, wherein the step of forming the electrical connections to the first semiconductor chips further comprises:

- encapsulating the first traces with a second encapsulant; and
- 5 forming a plurality of openings through the second encapsulant to expose a surface of the first traces.

7. The semiconductor packaging method of claim 5, wherein the step of forming the electrical connections to the first semiconductor chips further
10 comprises:

- forming a plurality of conductive studs on the first traces;
- encapsulating the first traces and the conductive studs with a second encapsulant; and
- removing a portion of the second encapsulant to expose a surface of
15 the conductive studs.

8. The semiconductor packaging method of claim 7, wherein the step of forming the electrical connections to the first semiconductor chips further comprises:

- 20 forming a plurality of second traces on a surface of the second encapsulant.

9. The semiconductor packaging method of claim 1, further comprising:

- forming an electrically conductive layer over at least one of a plurality
25 of circuit pads of the first semiconductor chips prior to forming the electrical connections to the first semiconductor chips.

- 10. The semiconductor packaging method of claim 9, wherein a surface area of the electrically conductive layer is greater than a surface area of the
30 circuit pad over which the electrically conductive layer is formed.

11. The semiconductor packaging method of claim 9, wherein the electrically conductive layer comprises a pad portion positioned above the circuit pad over which the electrically conductive layer is formed and a line portion extending away from the circuit pad.

5

12. The semiconductor packaging method of claim 11, wherein the electrical connections to the first semiconductor chips are formed from the line portion of the electrically conductive layer.

10 13. The semiconductor packaging method of claim 1, further comprising:
forming at least one of a plurality of pads, a plurality of connectors, at least one strengthening element, an electromagnetic shielding structure and an inductor coil on the carrier prior to the encapsulation step.

15 14. The semiconductor packaging method of claim 13, wherein the connectors are formed to a level higher than a surface of the first semiconductor chips.

20 15. The semiconductor packaging method of claim 13, wherein the connectors are formed to a level lower than a surface of the first semiconductor chips.

25 16. The semiconductor packaging method of claim 13, wherein a surface of the connectors is exposed after removing the at least a portion of the carrier.

17. The semiconductor packaging method of claim 1, further comprising:
attaching a plurality of passive components to the carrier prior to the encapsulation step.

30

18. The semiconductor packaging method of claim 1, wherein the carrier comprises:

a first layer; and

a second layer provided on the first layer, wherein the second layer is formed of a first conductive material.

5 19. The semiconductor packaging method of claim 18, wherein the step of removing the at least a portion of the carrier to provide the heat release area comprises removing at least a portion of the first layer of the carrier.

10 20. The semiconductor packaging method of claim 19, further comprising removing a portion of the second layer of the carrier to form a plurality of component pads after removing the first layer of the carrier.

15 21. The semiconductor packaging method of claim 19, wherein at least one of a plurality of heat sinks, an array of heat sinks and a plurality of fins is formed from removal of a portion of the first layer of the carrier.

20 22. The semiconductor packaging method of claim 21, further comprising forming a coating layer over an exposed portion of the second layer of the carrier and the at least one of the heat sinks, the array of heat sinks and the fins after removing the at least a portion of the first layer of the carrier.

25 23. The semiconductor packaging method of claim 19, further comprising forming at least one opening through the second layer of the carrier to expose a surface of at least one of the first semiconductor chips after removing the first layer of the carrier.

30 24. The semiconductor packaging method of claim 23, further comprising filling the at least one opening with at least one of a second conductive material and a solder material.

25. A semiconductor package, comprising:
a first semiconductor chip;

a first encapsulant encapsulating the first semiconductor chip;
a plurality of electrical connections to the first semiconductor chip; and
a heat release area arranged to release heat generated by the first semiconductor chip, wherein the heat release area comprises one of:

5 a surface of a die pad to which the first semiconductor chip is attached;

 a non-active surface of the first semiconductor chip;

 a surface of a conductive layer to which a die pad is attached, wherein the first semiconductor chip is attached to the die pad;

10 a surface of a conductive layer to which the first semiconductor chip is attached;

 a surface area of a heat sink attached to a conductive layer, wherein the first semiconductor chip is attached to the conductive layer;

15 a surface area of an array of heat sinks attached to a conductive layer, wherein the first semiconductor chip is attached to the conductive layer;

 a surface area of a plurality of fins attached to a conductive layer, wherein the first semiconductor chip is attached to the conductive layer; and

20 a surface area of a heat sink attached to a conductive layer to which a die pad is attached, wherein the first semiconductor chip is attached to the die pad.

25 26. The semiconductor package of claim 25, wherein the electrical connections to the first semiconductor chip comprises:

 a plurality of vias extending through the first encapsulant to the first semiconductor chip; and

30 a plurality of first traces on a surface of the first encapsulant, wherein the first traces are electrically connected by the vias to the first semiconductor chip.

27. The semiconductor package of claim 26, further comprising:
a second encapsulant encapsulating the first traces; and
a plurality of openings extending through the second encapsulant to
expose a surface of the first traces.

5

28. The semiconductor package of claim 27, further comprising:
a second semiconductor chip;
a plurality of solder bumps attached to the second semiconductor chip
and electrically connecting the second semiconductor chip to the exposed
surface of the first traces.

10

29. The semiconductor package of claim 26, further comprising:
a plurality of conductive studs on the first traces; and
a second encapsulant encapsulating the first traces and the conductive
studs, wherein a portion of the second encapsulant is removed, exposing a
surface of the conductive studs.

15

30. The semiconductor package of claim 29, further comprising a plurality
of second traces on a surface of the second encapsulant.

20

31. The semiconductor package of claim 25, further comprising an
electrically conductive layer provided over at least one of a plurality of circuit
pads of the first semiconductor chip.

25 32. The semiconductor package of claim 31, wherein a surface area of the
electrically conductive layer is greater than a surface area of the circuit pad
over which the electrically conductive layer is formed.

33. The semiconductor package of claim 31, wherein the electrically
conductive layer comprises a pad portion positioned above the circuit pad
over which the electrically conductive layer is formed and a line portion
extending away from the circuit pad.

30

34. The semiconductor package of claim 33, wherein the electrical connections to the first semiconductor chip are formed from the line portion of the electrically conductive layer.

5

35. The semiconductor package of claim 25, further comprising at least one of a plurality of pads, a plurality of connectors, a plurality of passive components, at least one strengthening element, an electromagnetic shielding structure and an inductor coil encapsulated by the first encapsulant.

10

36. The semiconductor package of claim 35, further comprising a plurality of openings formed in the conductive layer, the openings exposing a surface of the connectors.

15

37. The semiconductor package of claim 35, further comprising:
a second semiconductor chip attached to the die pad;
a plurality of wire bonds electrically connecting the second semiconductor chip to respective ones of the pads; and
a third encapsulant encapsulating the second semiconductor chip and
the wire bonds.

20

38. The semiconductor package of claim 35, further comprising:
a second semiconductor chip attached to the die pad; and
a plurality of solder bumps electrically connecting the second
semiconductor chip to respective ones of the pads.

25

39. The semiconductor package of claim 25, further comprising a coating layer over the heat release area.

30

40. The semiconductor package of claim 25, further comprising at least one opening extending through the conductive layer to the non-active surface of the first semiconductor chip.

41. The semiconductor package of claim 40, further comprising at least one of a conductive material and a solder material filling the at least one opening.

5

42. The semiconductor package of claim 40, further comprising a layer of the conductive material on the conductive layer.

43. A stacked semiconductor package, comprising:

10 a first semiconductor package in accordance with claim 27;
a plurality of solder bumps attached to the exposed surface of the first traces;

a second semiconductor package in accordance with claim 35, wherein the solder bumps are electrically coupled to the pads of the second semiconductor package.

15

44. A stacked semiconductor package, comprising:

a first semiconductor package in accordance with claim 35;
a second semiconductor package in accordance with claim 35; and
20 a solder material electrically coupling a first die pad of the first semiconductor package to a second die pad of the second semiconductor package and a plurality of first pads of the first semiconductor package to a plurality of second pads of the second semiconductor package.

20

25 45. A stacked semiconductor package, comprising:

a first semiconductor package in accordance with claim 27;
a plurality of solder bumps attached to the exposed surface of the first traces;

a second semiconductor package in accordance with claim 36, wherein the solder bumps are electrically coupled to the exposed surface of the connectors of the second semiconductor package.

30

46. A stacked semiconductor package, comprising:
- a first semiconductor package in accordance with claim 36;
 - a second semiconductor package, wherein the second semiconductor package is a wafer-level package having a plurality of solder bumps and
- 5 wherein the solder bumps are electrically coupled to the exposed surface of the connectors of the first semiconductor package.

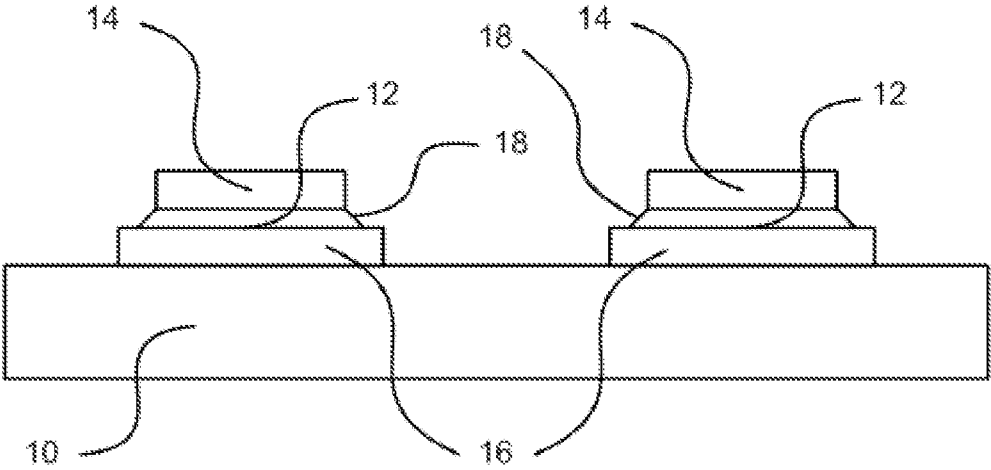


FIG. 1

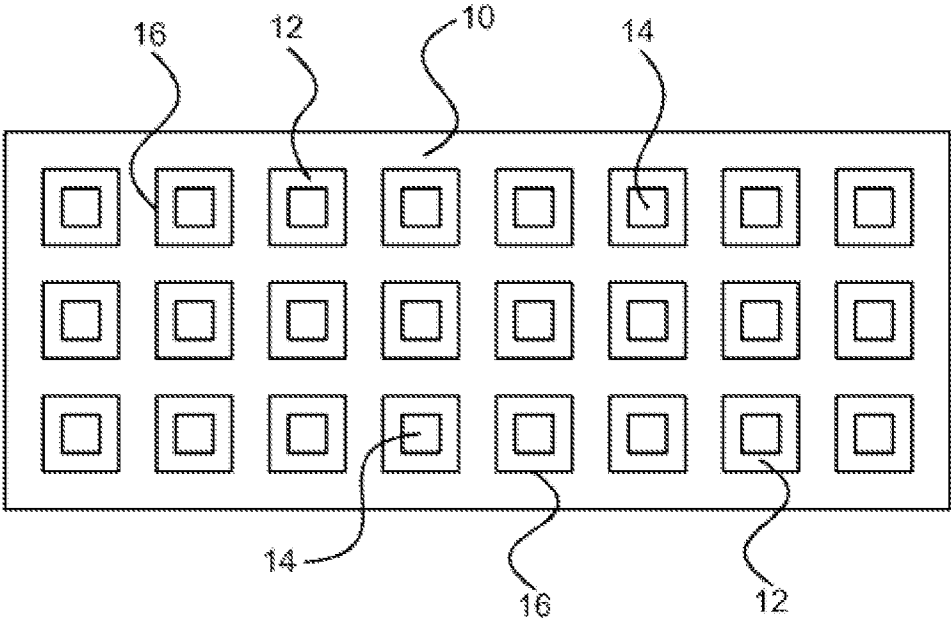


FIG. 2

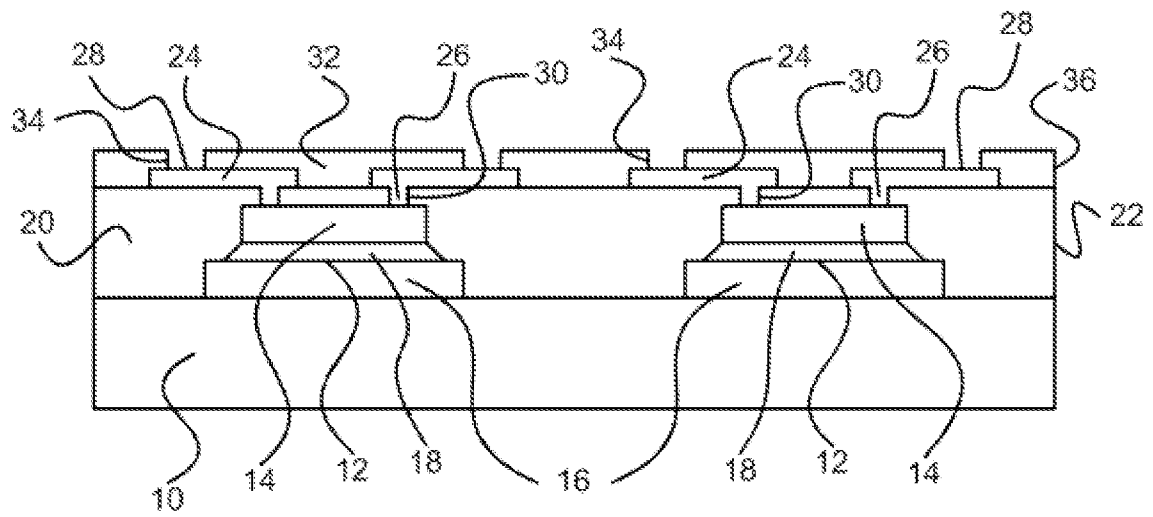


FIG. 3

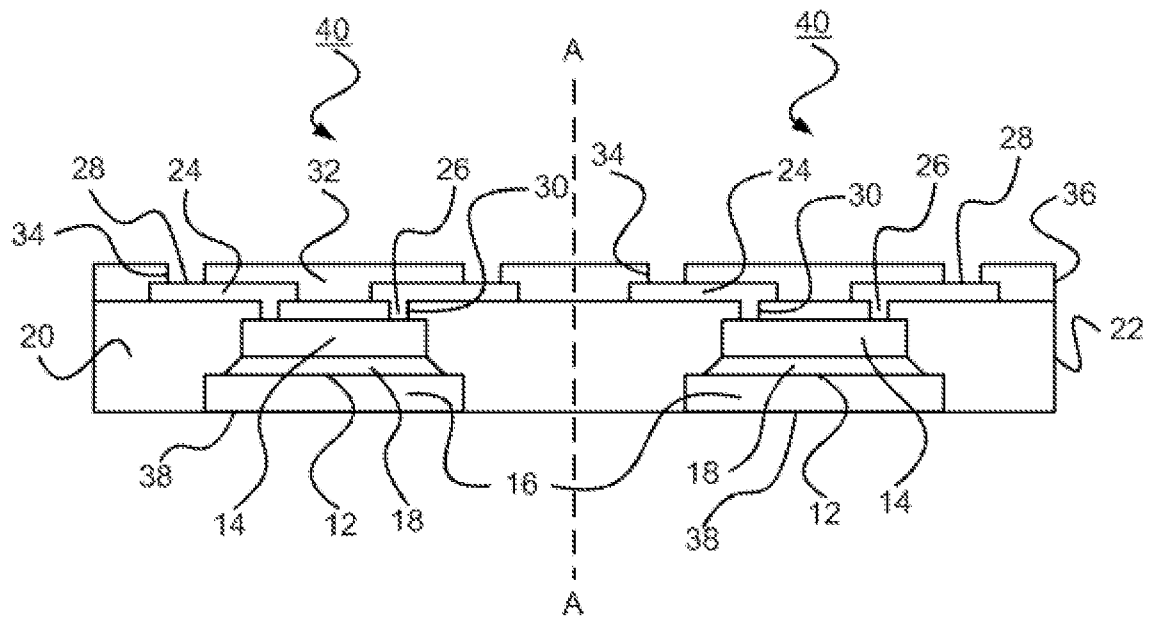


FIG. 4

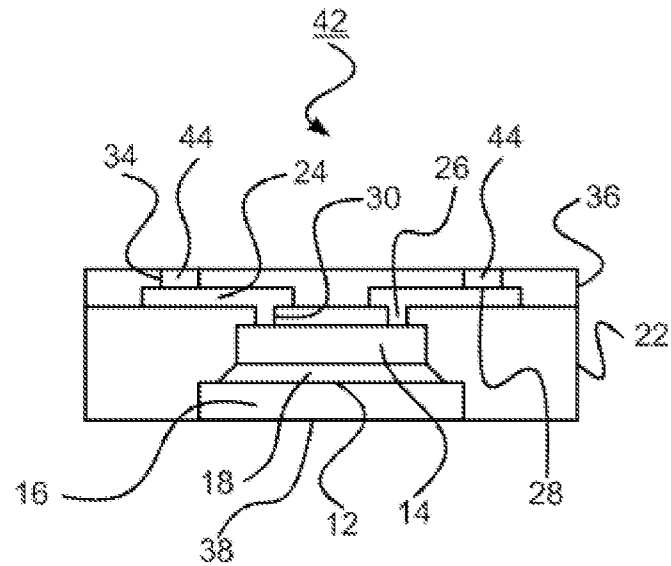


FIG. 5

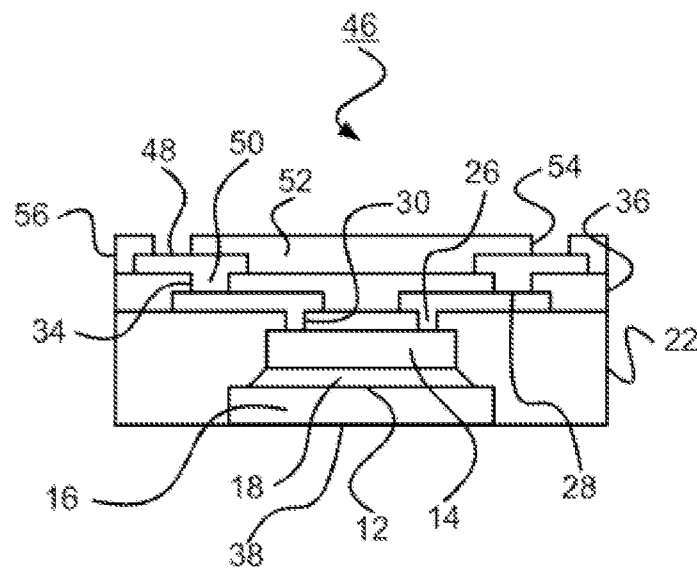


FIG. 6

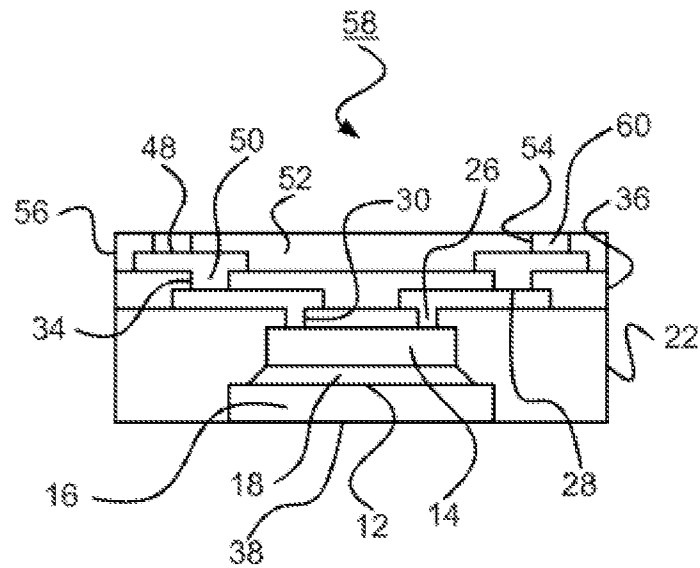


FIG. 7

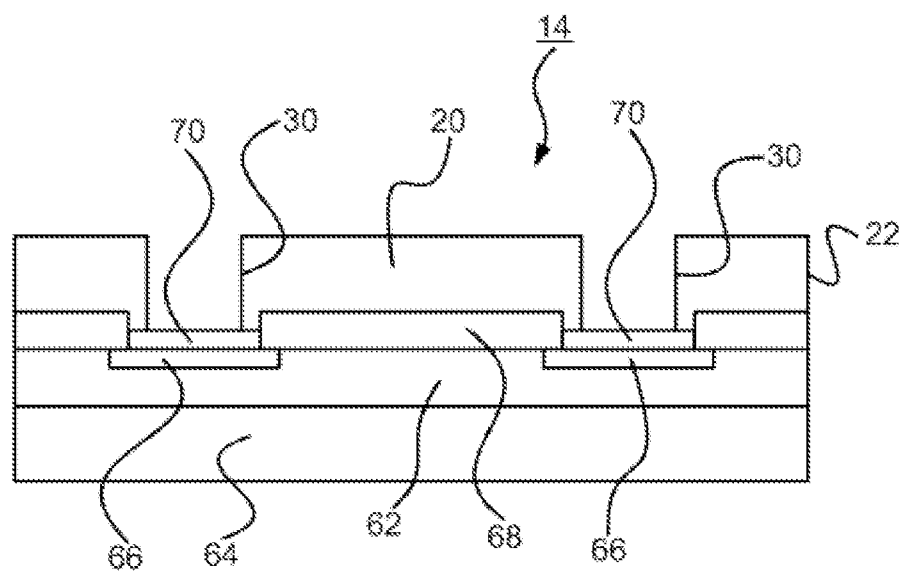


FIG. 8

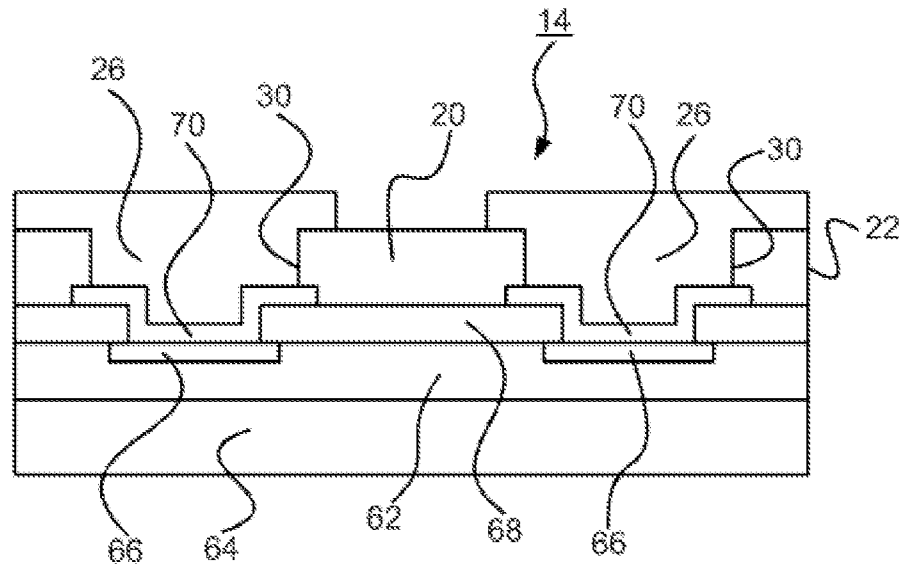


FIG. 9

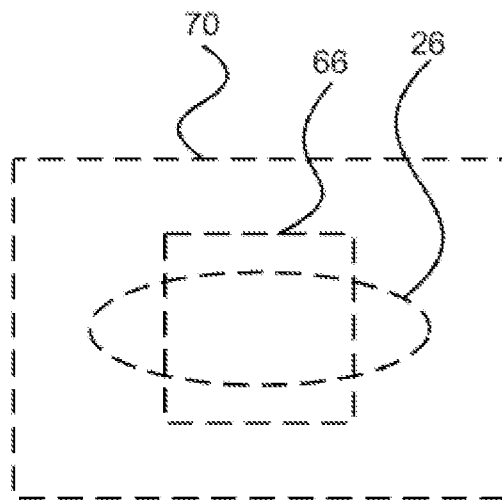


FIG. 10

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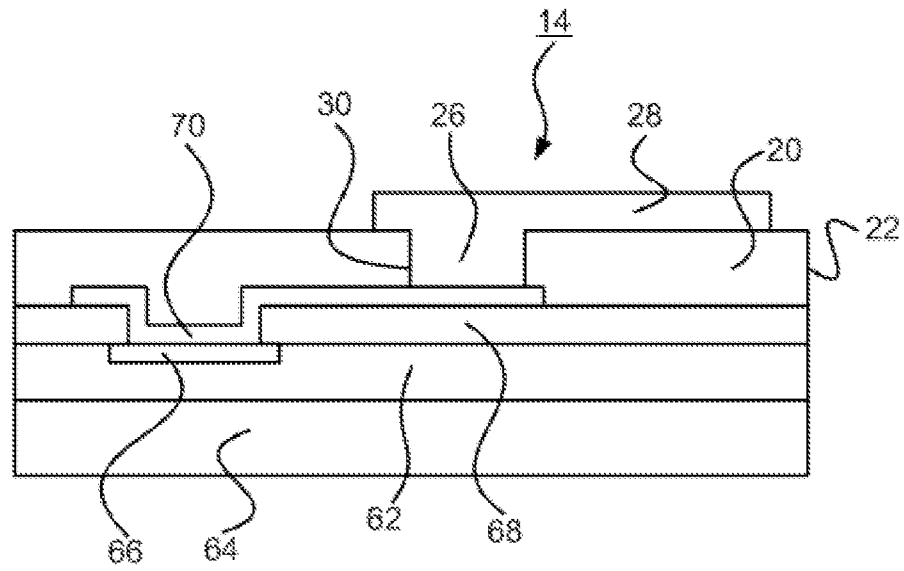


FIG. 11

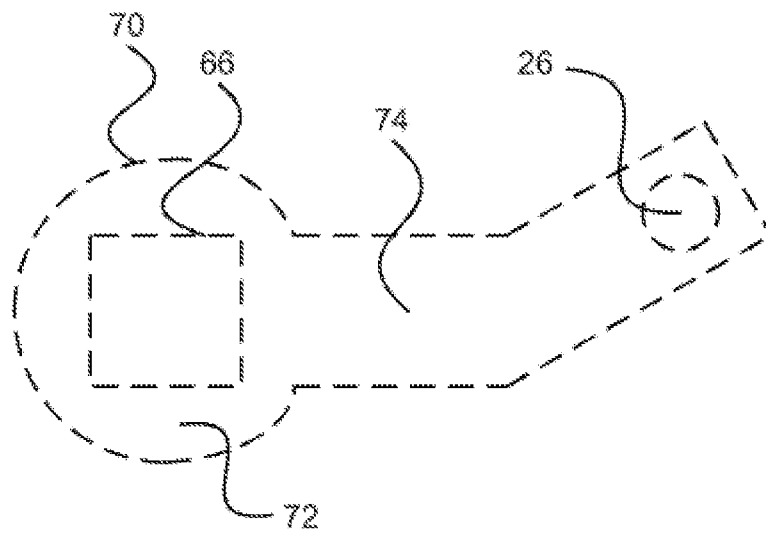


FIG. 12

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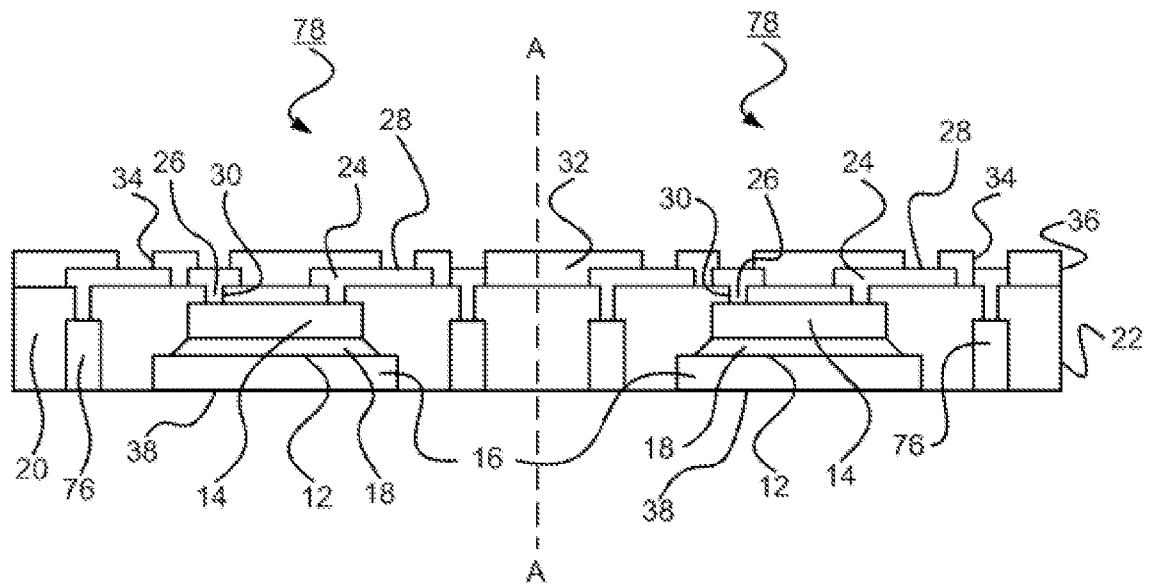


FIG. 13

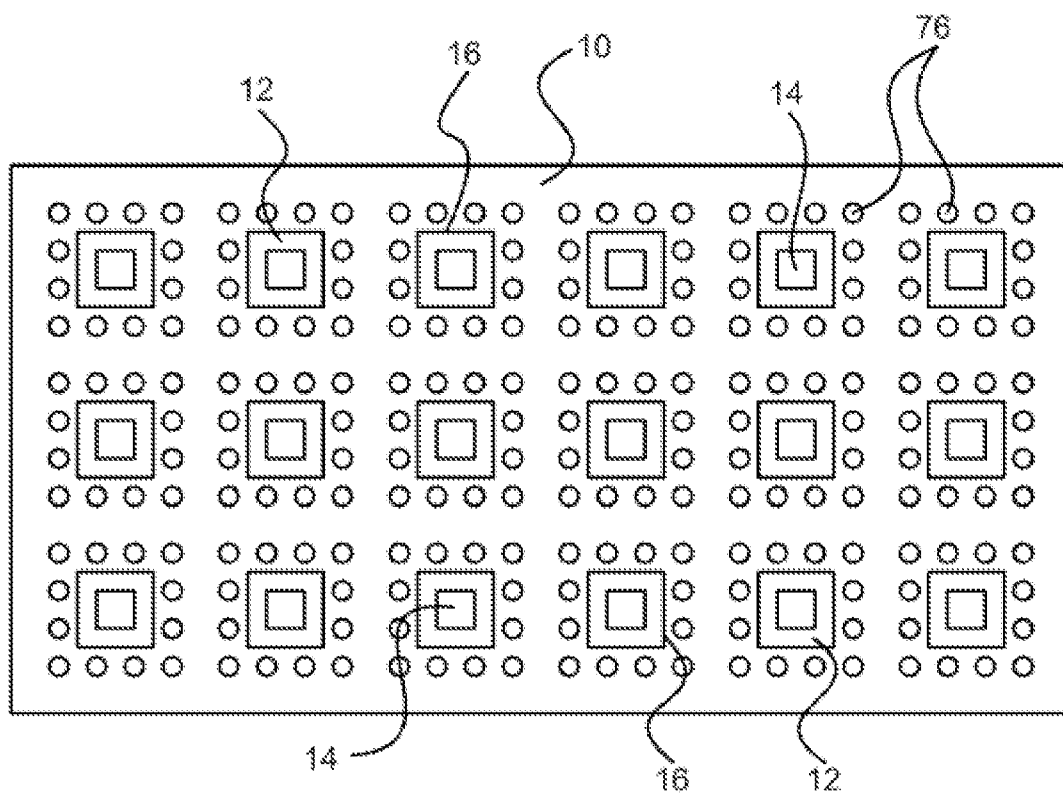


FIG. 14

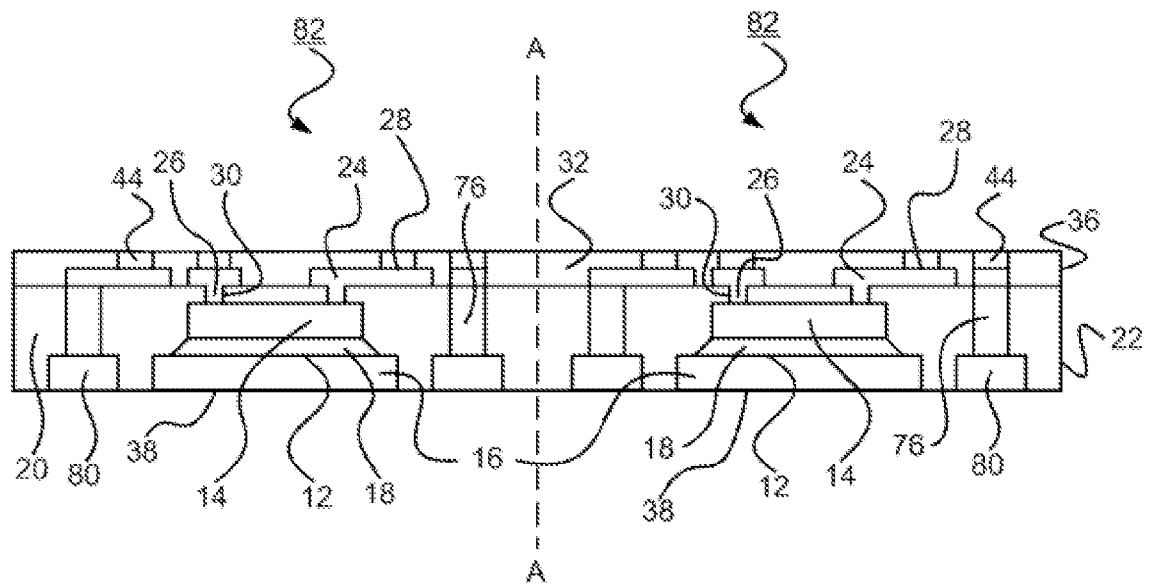


FIG. 15

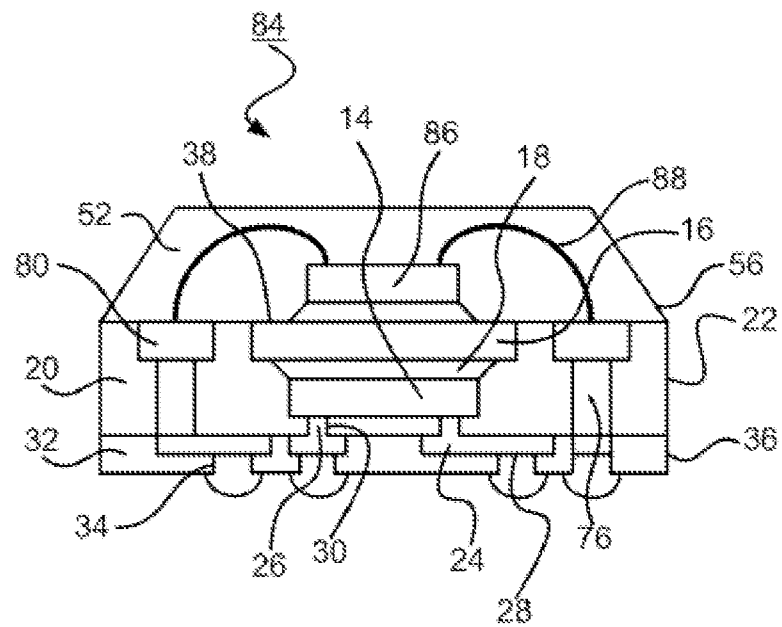


FIG. 16

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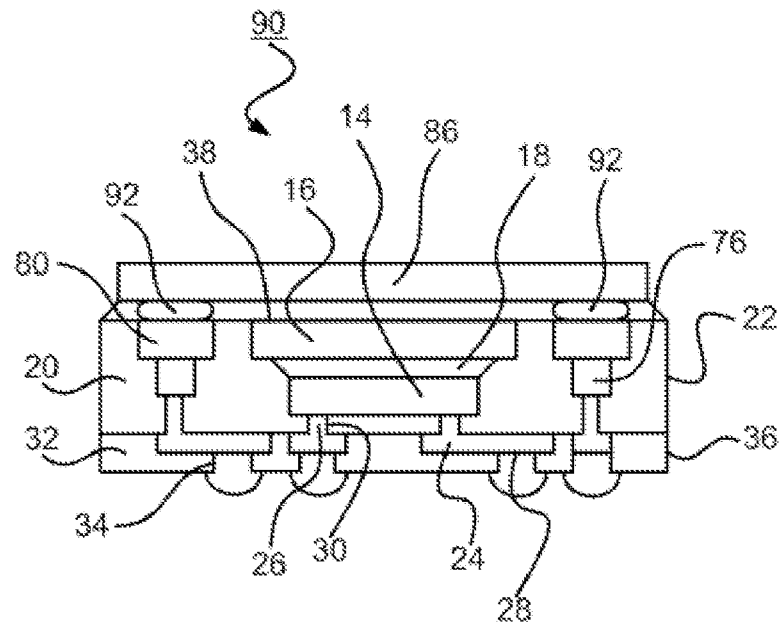


FIG. 17

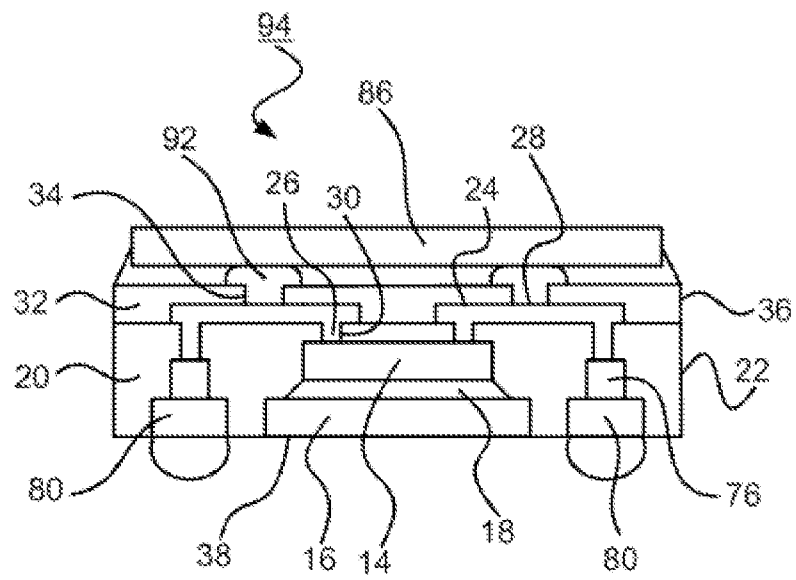


FIG. 18

10/23

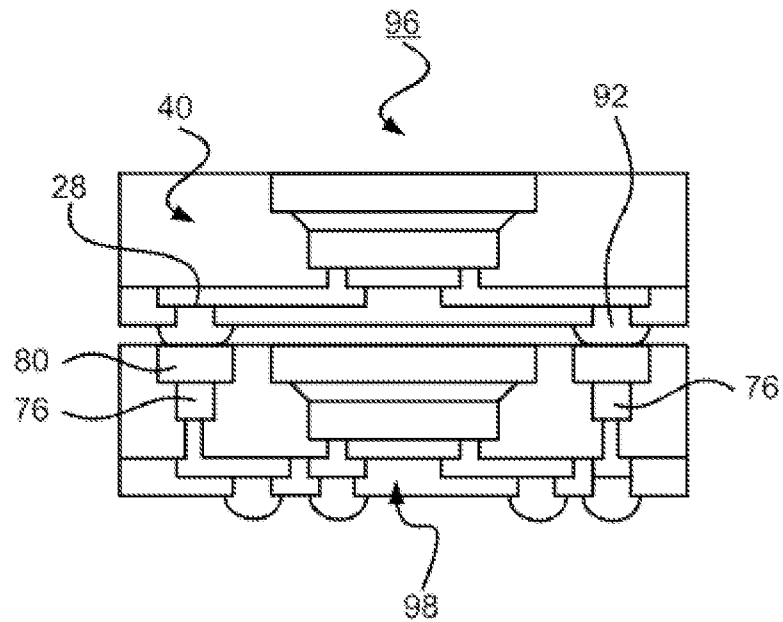


FIG. 19

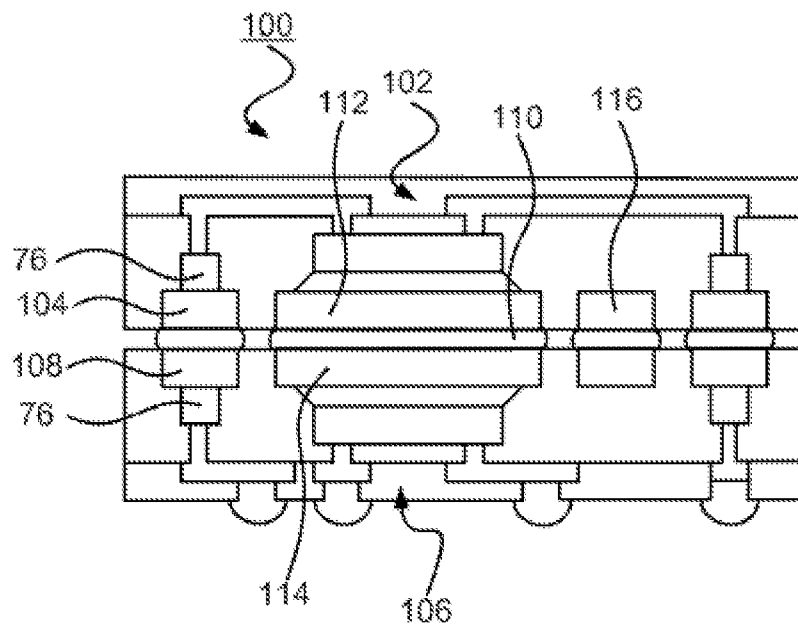


FIG. 20

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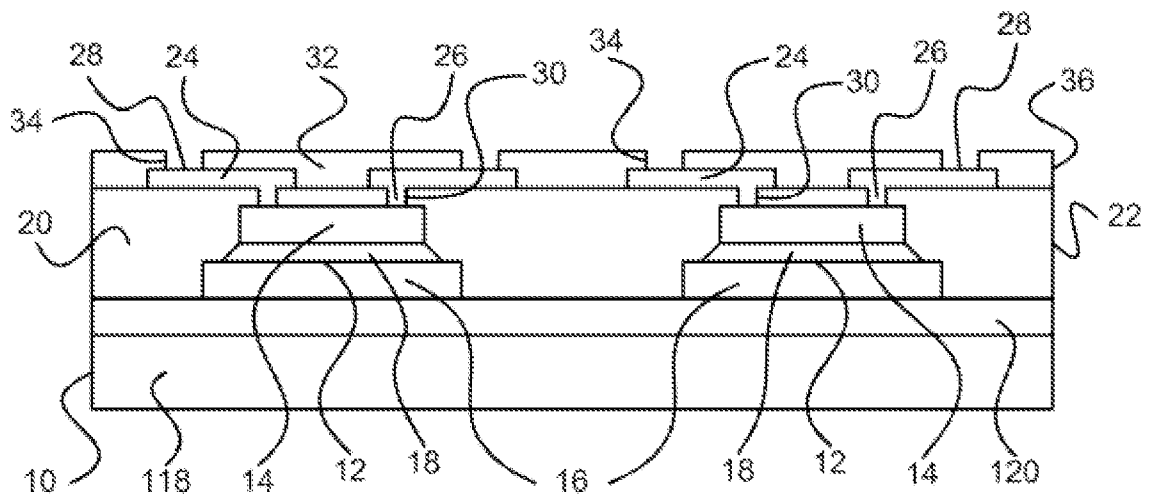


FIG. 21

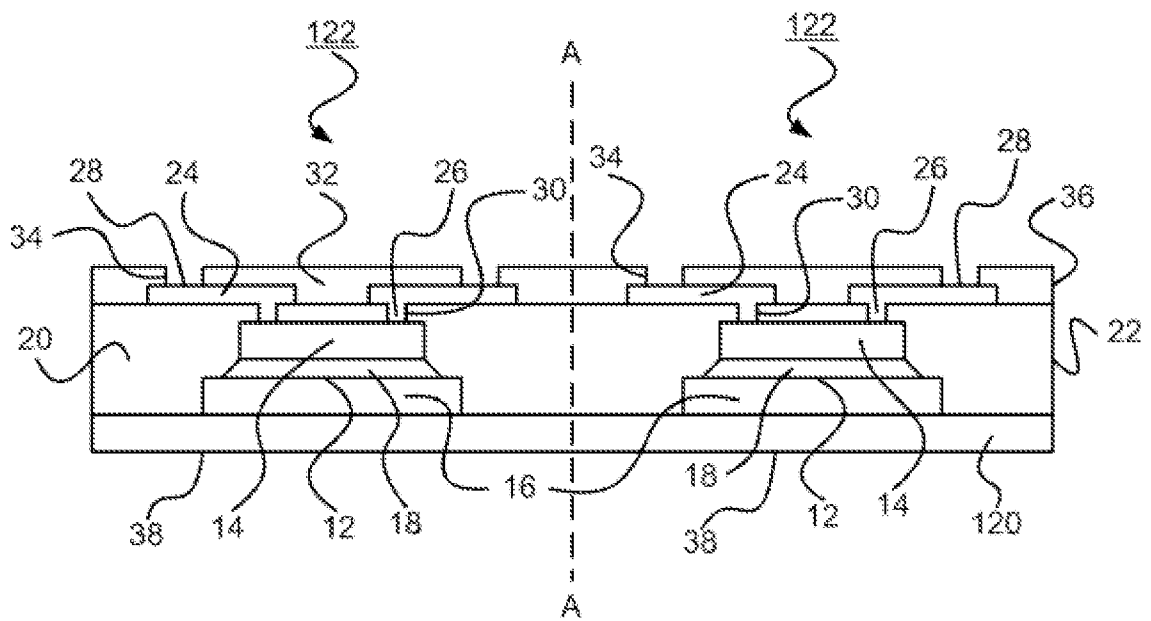


FIG. 22

12/23

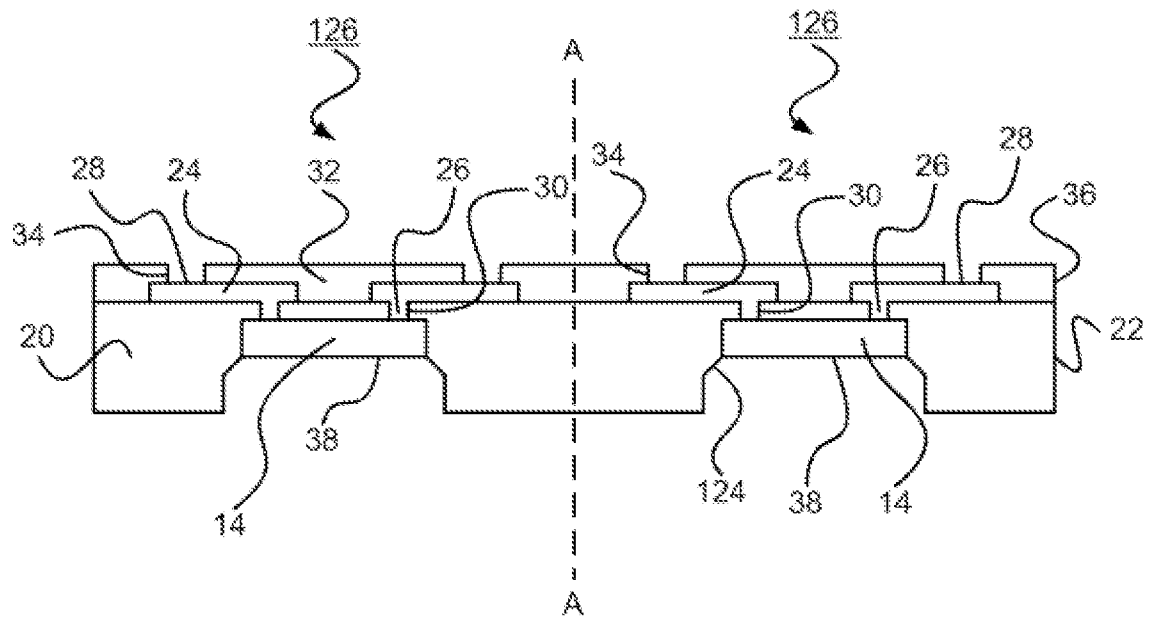


FIG. 23

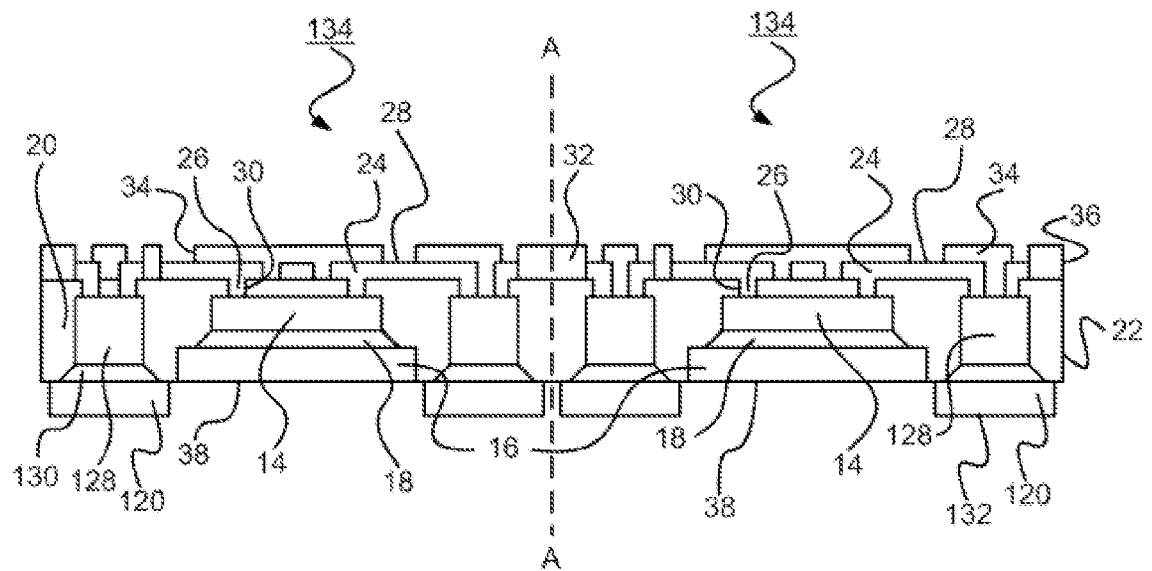


FIG. 24

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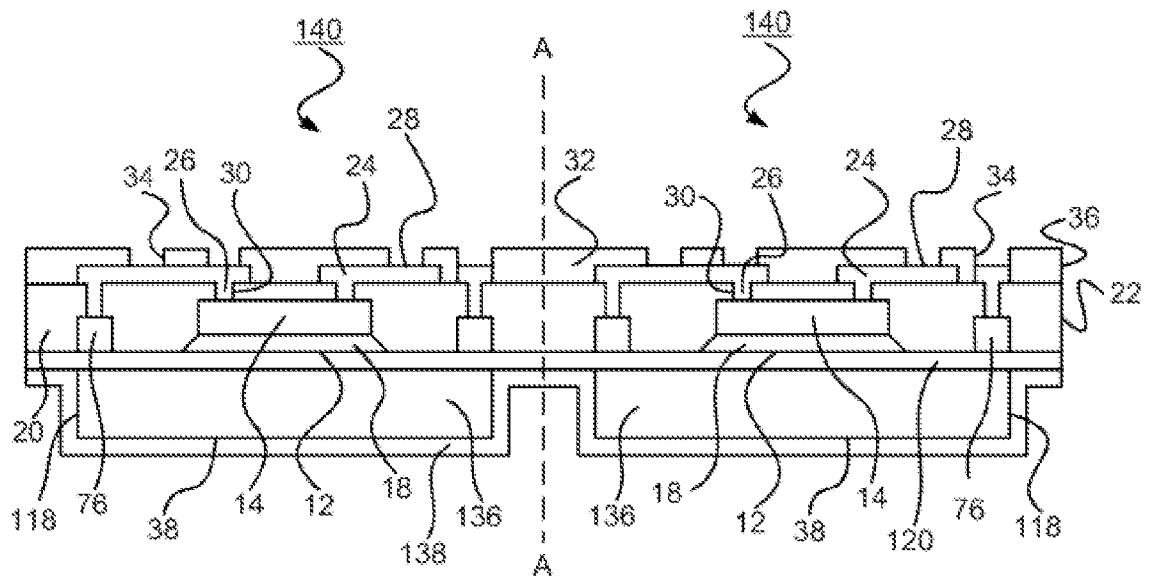


FIG. 25

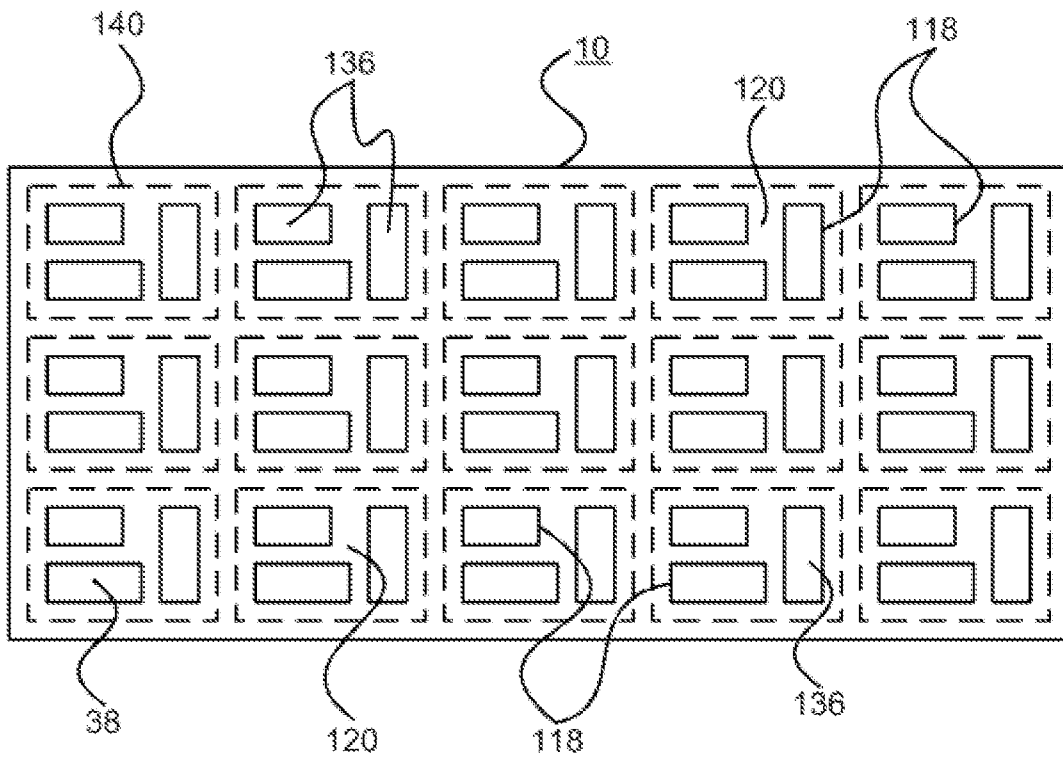


FIG. 26

14/23

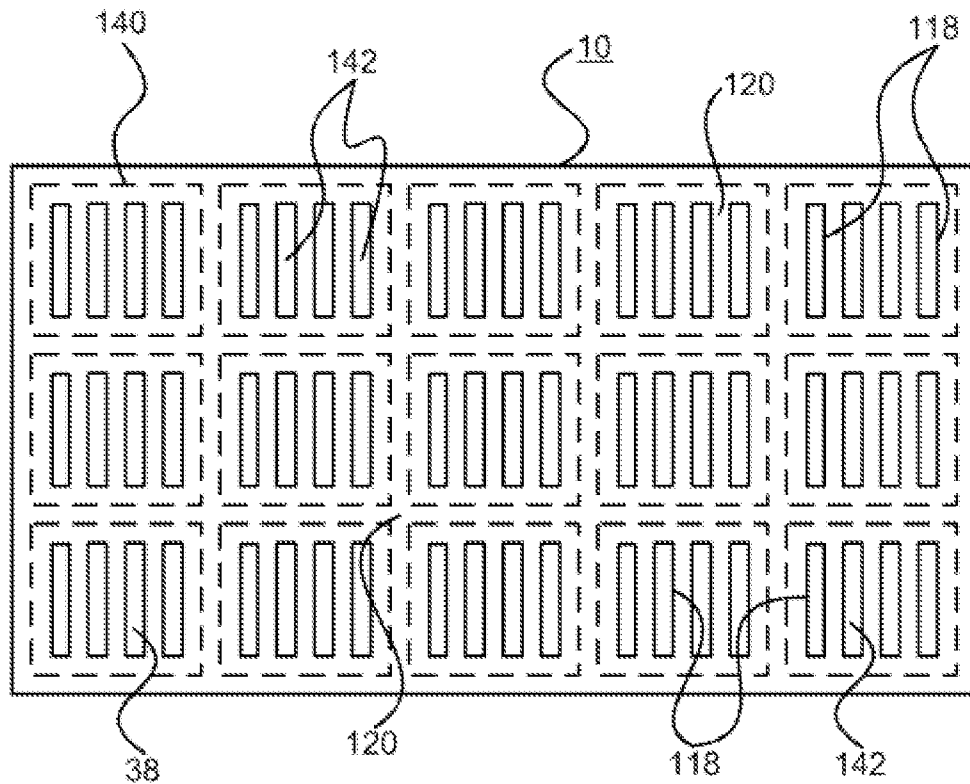


FIG. 27

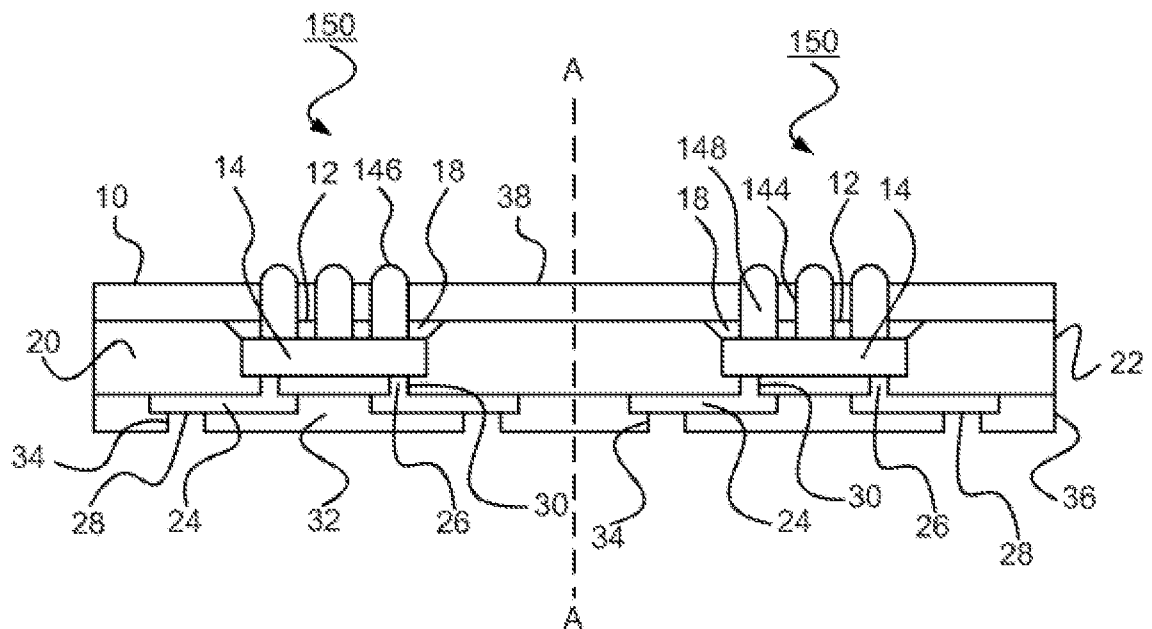


FIG. 28

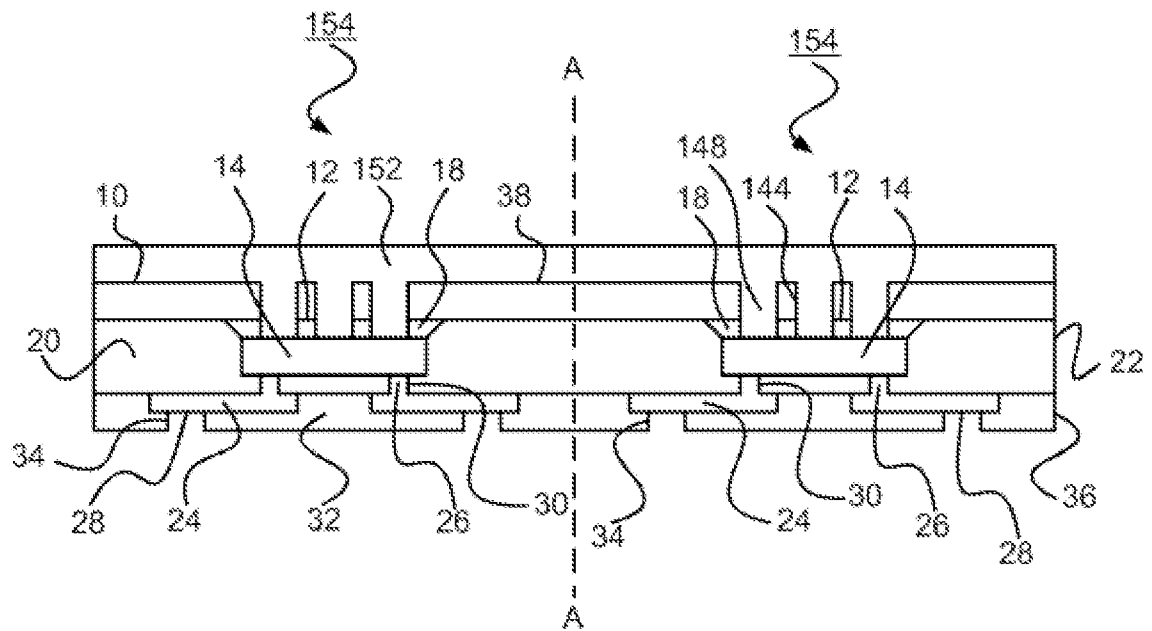


FIG. 29

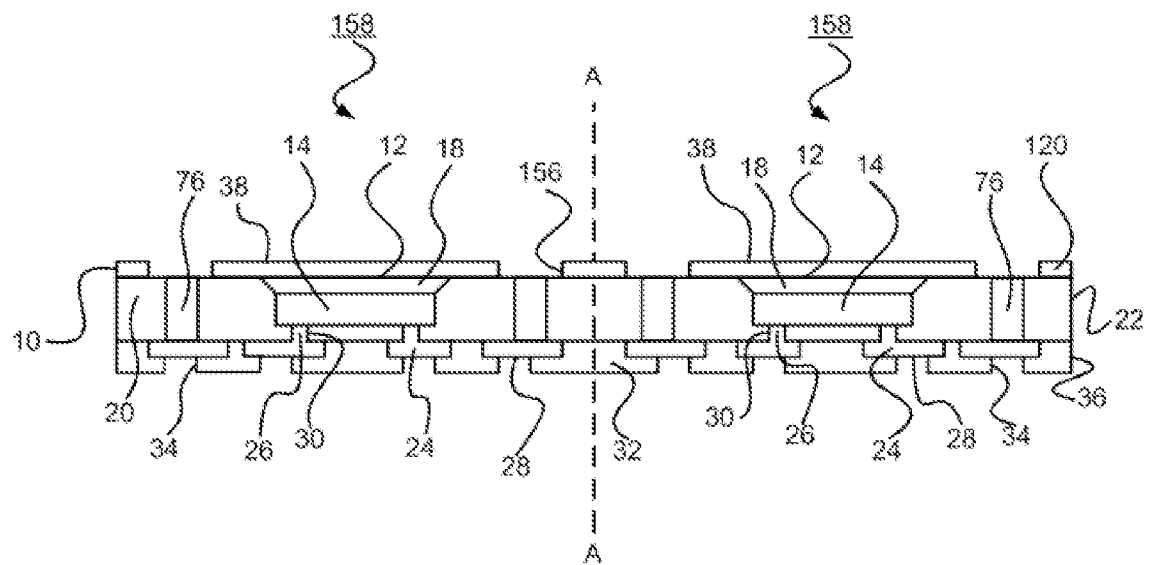
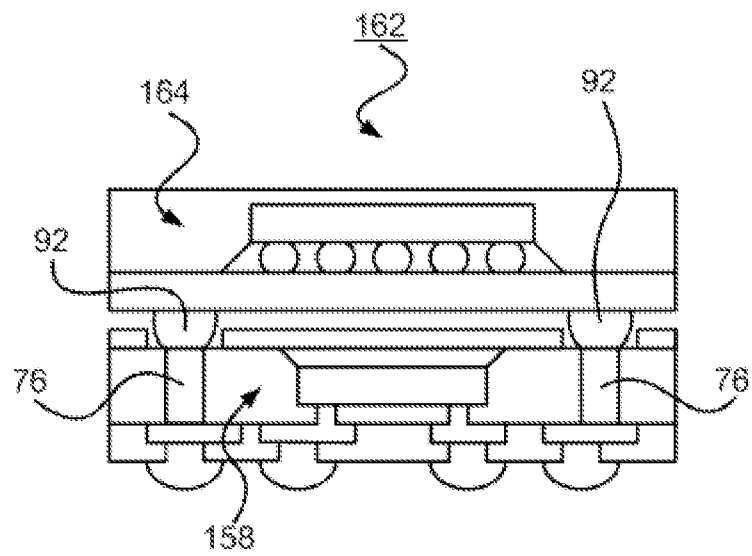
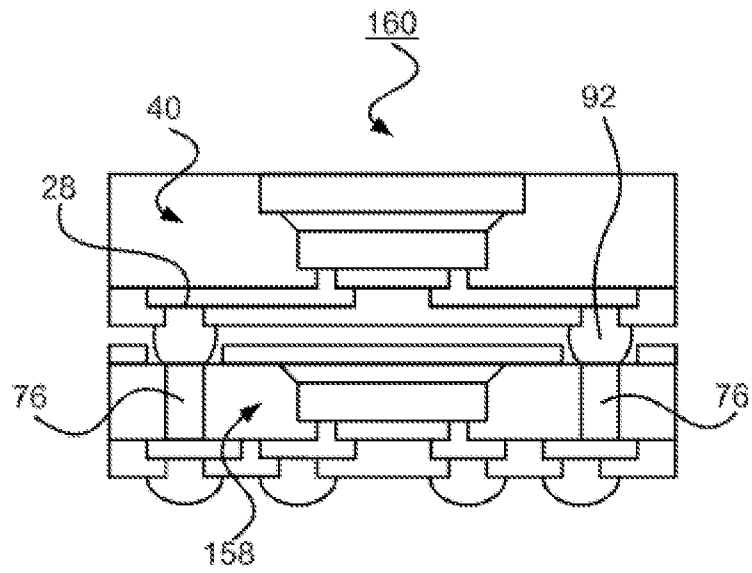


FIG. 30



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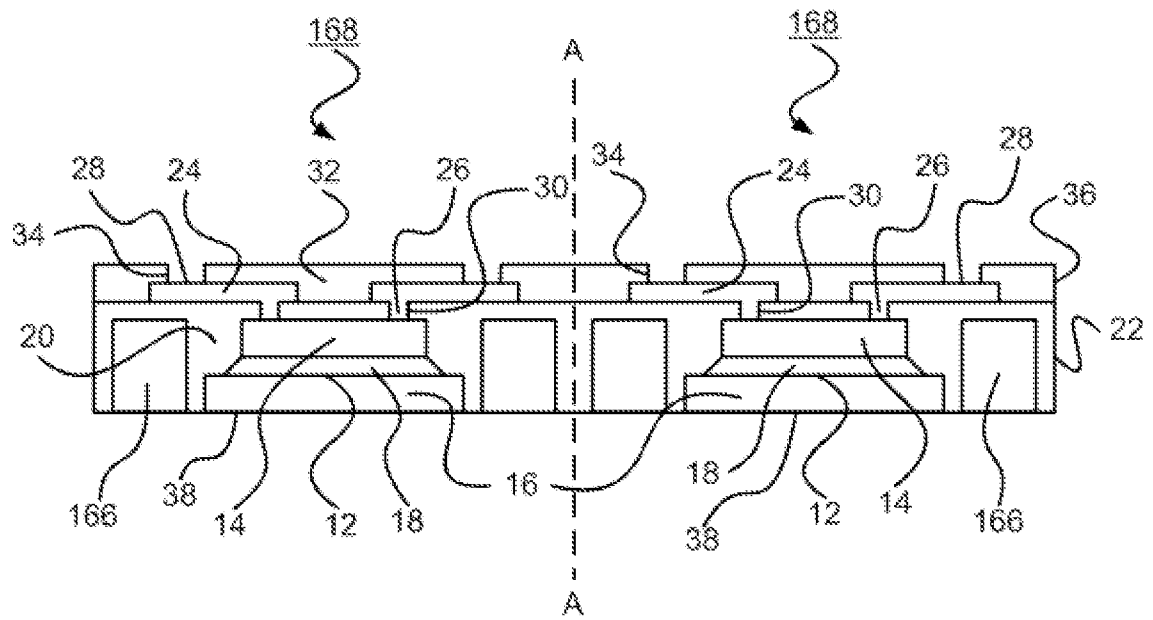


FIG. 33

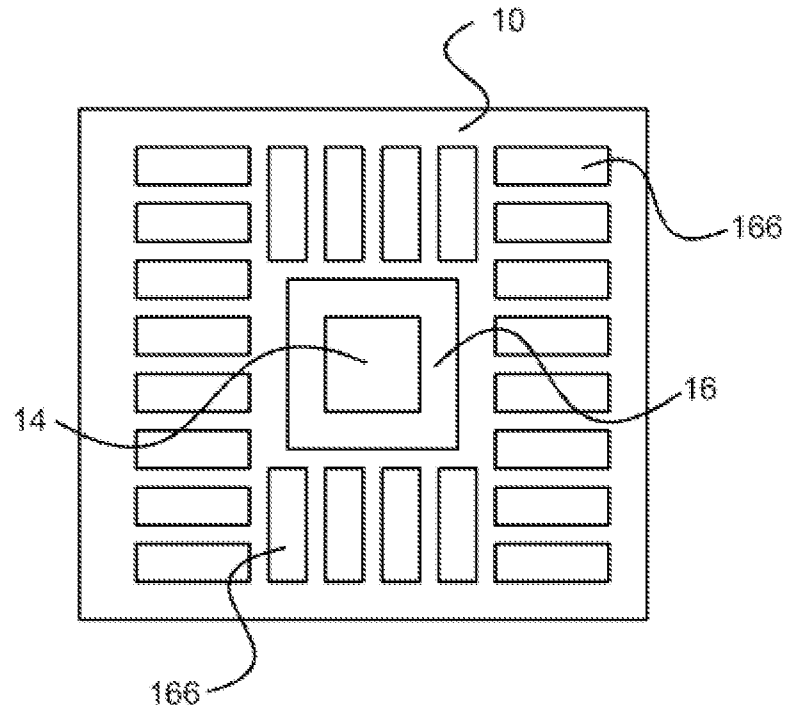


FIG. 34

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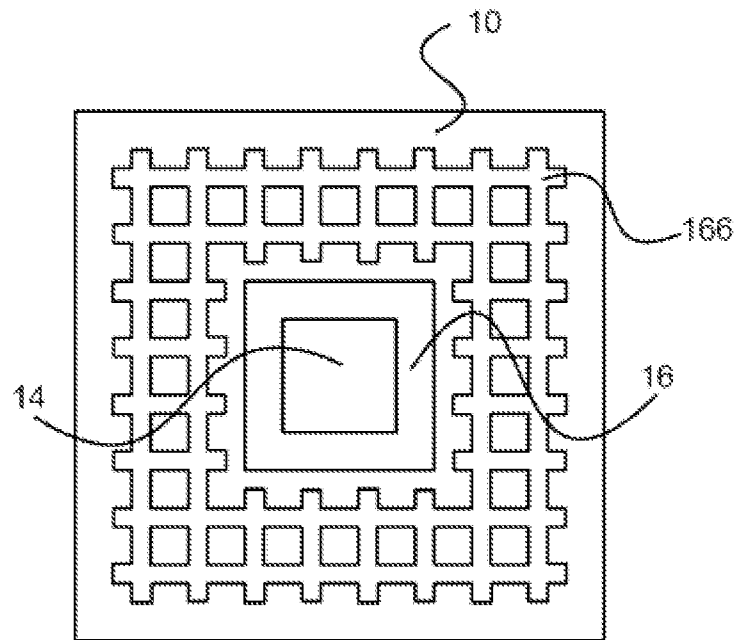


FIG. 35

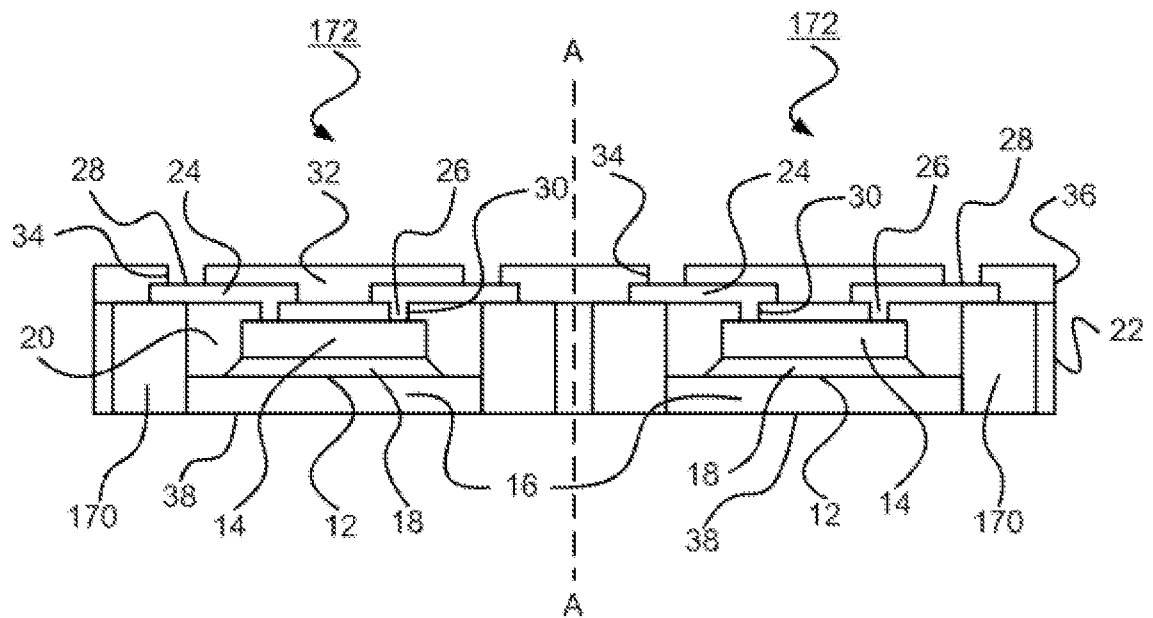


FIG. 36

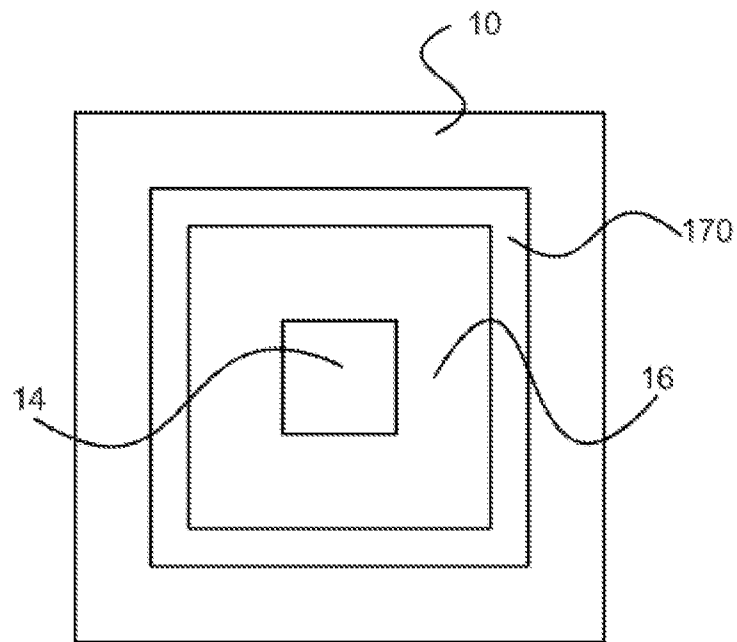


FIG. 37

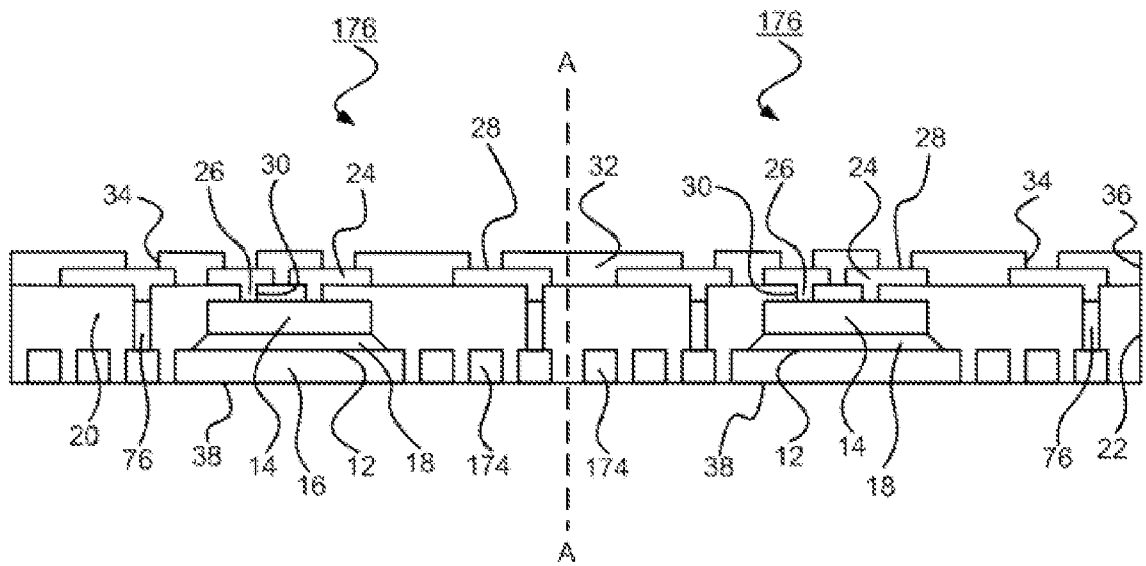


FIG. 38

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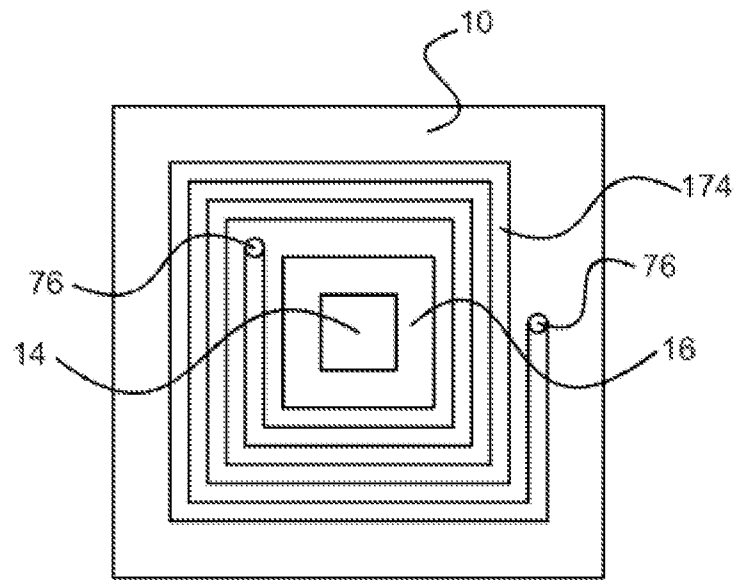


FIG. 39

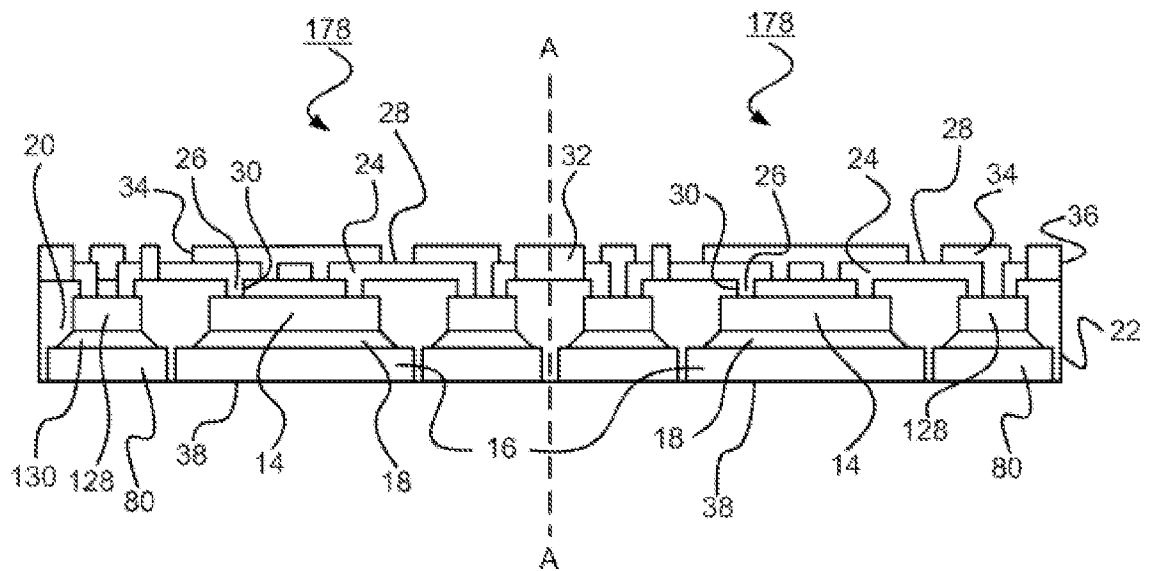


FIG. 40

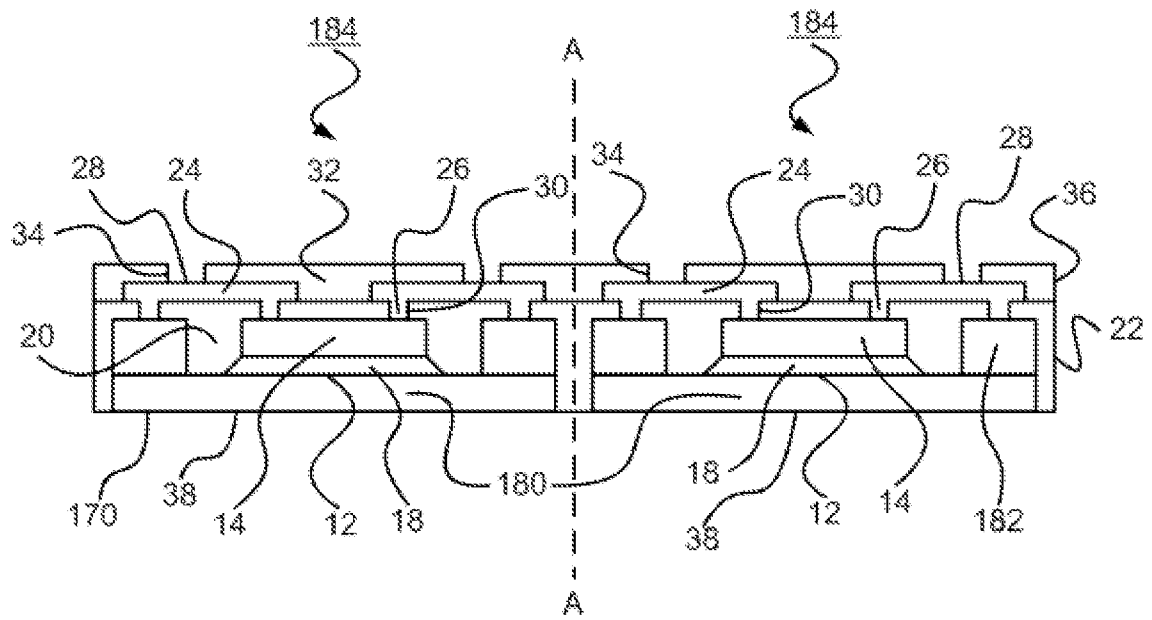


FIG. 41

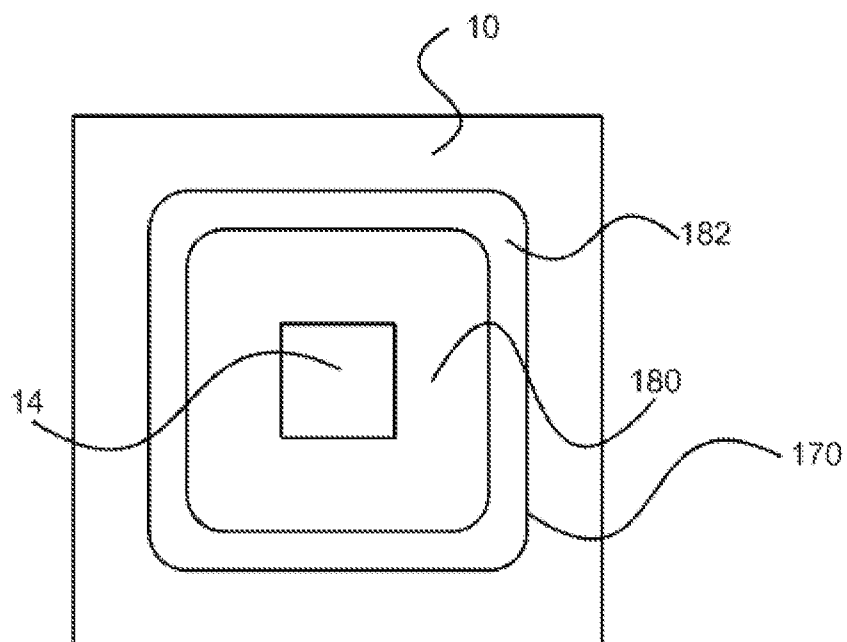


FIG. 42

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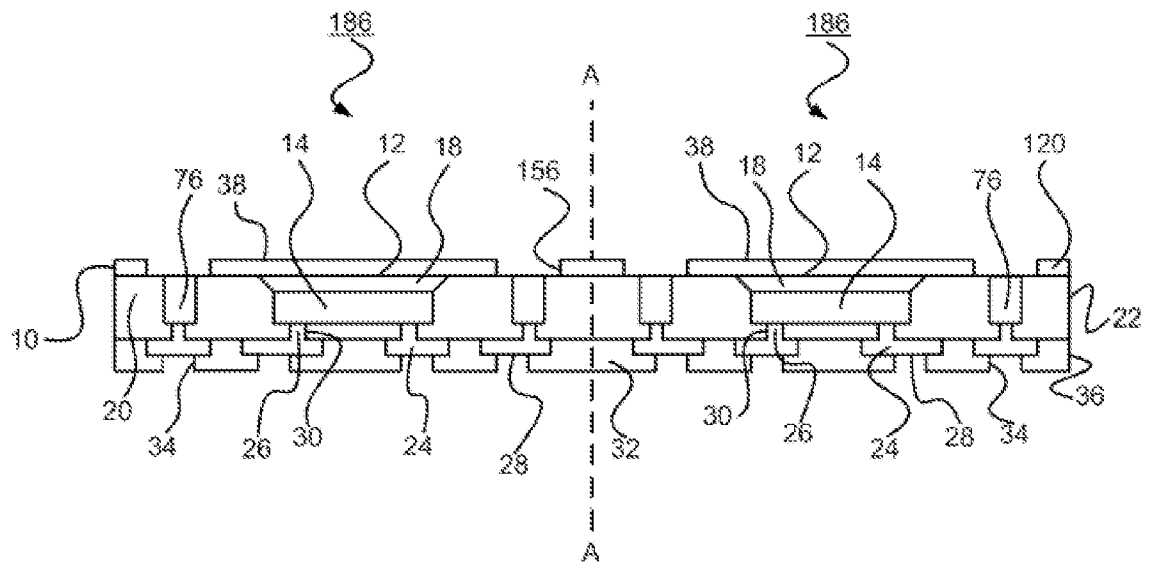


FIG. 43

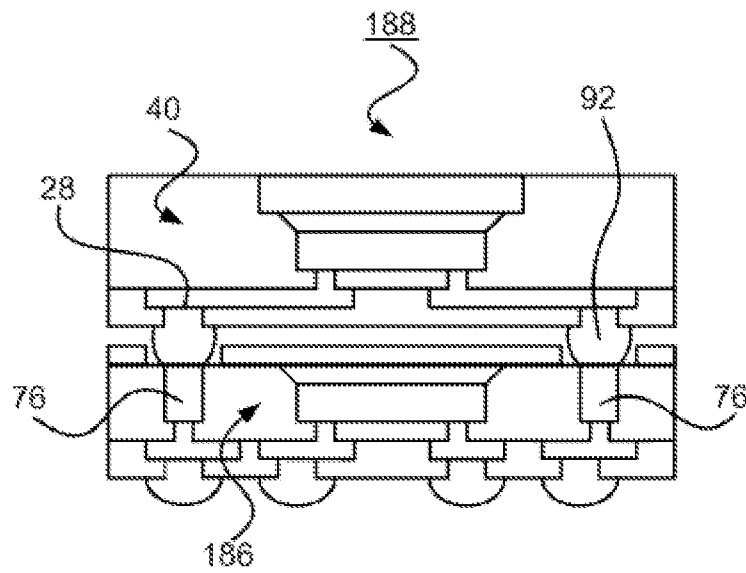


FIG. 44

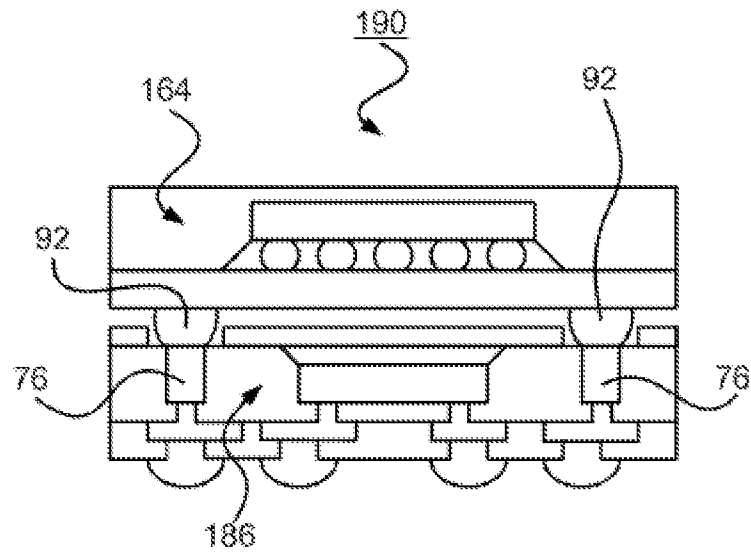


FIG. 45

INTERNATIONAL SEARCH REPORT

 International application No.
PCT/SG2016/050290

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/64 (2010.01) H01L 23/34 (2006.01) H01L 33/52 (2010.01) H01L 21/98 (2006.01) H01L 21/56 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases: WPI, EPODOC, INSPEC and keywords: chip, dice, die, wafer, IC, integrated circuit, CMOS, heat sink, heat radiator, heat fin, heat spreader, heat remover, heat collector, heat transmitter, heat dissipater, heat transfer, heat exchange, cooler, pad, contact, terminal, bonding, connector, conductor, electrode, encapsulate, laminate, shield, cover, enclosing, removing, detaching, peeling, lift off, etching, carrier, substrate, wafer, support, and similar terms.

Applicant(s)/Inventor(s) name searched in internal databases provided by IP Australia.

Applicant(s)/Inventor(s) name search in Espacenet, AusPat, Google Patents/Google scholar: Applicant name: PEP INNOVATION PTE LTD; Inventor name: CHEW, Yi Xin; keywords: semiconductor packaging, chips, die, heat release, removing carrier and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	



Further documents are listed in the continuation of Box C



See patent family annex

* "A"	Special categories of cited documents: document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family
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Date of the actual completion of the international search 2 November 2016	Date of mailing of the international search report 02 November 2016
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA Email address: pct@ipaustalia.gov.au	Authorised officer Jayati Ray AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No. 0262223654

INTERNATIONAL SEARCH REPORT		International application No.
C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		PCT/SG2016/050290
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/0198752 A1 (NONDHASITTHICHA ET AL.) 18 August 2011 Figs. 1, 1A, 2 and paragraphs 0072-0079	1-4, 9-19, 21-22, 25, 31-35, 37-39, 44
X	US 2015/0333232 A1 (OSRAM OPTO) 19 November 2015 & WO2014/095923 A1 Fig. 1A-1E, paragraphs 0047-0056,	1, 9-17, 25, 31-35, 44
X	US 2014/0091445 A1 (TEH ET AL.) 03 April 2014 Figs. 1-2H, paragraphs 0021-0035,	1, 5-13, 17-36, 39-46
X	US 2011/0037165 A1 (OH ET AL.) 17 February 2011 Figs. 3a-4, paragraphs 0033-0042	1, 5-13, 17-19, 25-35, 43-44,
X	US 2014/0264817 A1 (STATS CHIP-PAC, LTD.) 18 September 2014 Figs. 4a-5, paragraphs 0050-0063	1, 5-13, 17, 25-35, 43-44,
A	US 2008/0258293 A1 (YANG ET AL.) 23 October 2008 Figs. 3, 5 and the associated text	23, 43-45

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INTERNATIONAL SEARCH REPORT		International application No.	
Information on patent family members		PCT/SG2016/050290	
This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.			
Patent Document/s Cited in Search Report		Patent Family Member/s	
Publication Number	Publication Date	Publication Number	Publication Date
US 2011/0198752 A1	18 August 2011	US 2011198752 A1	18 Aug 2011
		US 8492906 B2	23 Jul 2013
		US 8310060 B1	13 Nov 2012
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		US 2015104907 A1	16 Apr 2015
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		US 2016027757 A1	28 Jan 2016
		WO 2014051714 A1	03 Apr 2014
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		US 8003496 B2	23 Aug 2011
Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.			

INTERNATIONAL SEARCH REPORT Information on patent family members		International application No. PCT/SG2016/050290	
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Patent Document/s Cited in Search Report		Patent Family Member/s	
Publication Number	Publication Date	Publication Number	Publication Date
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		TW 200843055 A	01 Nov 2008
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