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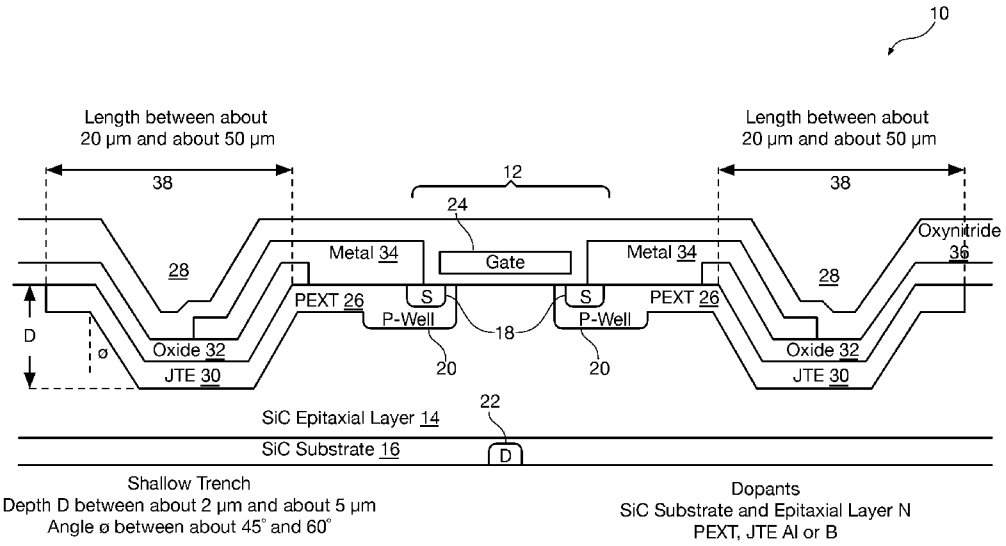

FIG. 1

(57) Abstract: A high-voltage termination for a semiconductor device includes a substrate, an implanted device region, a shallow trench adjacent to the implanted device region, and a doped extension region between the implanted device region and a first edge of the shallow trench adjacent to the implanted device region. A junction termination extension region is formed in the shallow trench contacting the extension region and extending past a second edge of the shallow trench opposite the implanted device region. An insulating layer is formed over at least a portion of the extension region and over the junction termination extension region. A metal layer is formed over the insulating layer.

[Continued on next page]

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SPACE EFFICIENT HIGH-VOLTAGE TERMINATION AND PROCESS FOR FABRICATING THE SAME

TECHNICAL FIELD

[0001] The present invention relates to semiconductor device structures and manufacturing processes. More particularly, the present invention relates to a high-voltage termination structure for a semiconductor device and to a process for fabricating that structure.

BACKGROUND

[0002] For voltage nodes carrying 600 V and higher, the high-voltage termination structure accounts for a significant portion of the die total footprint, in some cases amounting to more than half of the footprint. Hence, reducing the length of the termination structure would reduce the size and cost of the dies.

[0003] Most of the prior-art high-voltage termination designs rely on floating field ring (FFR), junction termination extension (JTE), and/or deep trench designs. The FFR design provides a very robust termination however it has a large footprint (typically 10 times the thickness of the epitaxy). The JTE design is more compact (about 3 times the thickness of the epitaxy) but has the drawback of being highly sensitive to normal process variations. The deep trench design is very compact but expensive to fabricate in that it is difficult to control the dry etch process used.

BRIEF DESCRIPTION

[0004] The present invention relies on the combination of a shallow trench, a JTE region,

and a field plate to provide a high breakdown voltage close to the full capability of the substrate, which may be a semiconductor substrate, a well formed in a semiconductor substrate or an epitaxial layer formed on a substrate.

[0005] The underlying principle is to suppress any high electric fields near convex junctions so that the avalanche breakdown of the termination is governed by the electric field of a planar junction.

[0006] The shallow trench allows the convex junction of the doped extension to be etched away. The JTE and field plate are designed to relax the electric field at the interface between the extension and the trench.

[0007] According to an aspect of the invention, a high-voltage termination for a semiconductor device includes a substrate of a first conductivity type, an implanted device region of a second conductivity type of the semiconductor device, a shallow trench disposed in the substrate adjacent to the implanted device region, a doped extension region of the second conductivity type extending between the implanted device region and a first edge of the shallow trench adjacent to the implanted device region, a junction termination extension region of the second conductivity type formed in the shallow trench contacting the extension region and extending past a second edge of the shallow trench opposite the implanted device region, an insulating layer formed over at least a portion of the extension region and over the junction termination extension region, and a metal layer formed over the insulating layer extending into at least a portion of the shallow trench and electrically connected to the extension region.

[0008] According to an aspect of the invention, a length of the shallow trench and the doped extension region together form a termination length of the high-voltage termination.

[0009] According to an aspect of the invention, a second insulating layer is formed over

the metal layer and the insulating layer.

[0010] According to an aspect of the invention, sidewalls of the shallow trench are at angles between about 45° and about 60°.

[0011] According to an aspect of the invention, the substrate of the first conductivity type is an epitaxial layer disposed over an underlying substrate.

[0012] According to an aspect of the invention, the epitaxial layer is an epitaxial SiC layer, and the underlying substrate is a SiC substrate.

[0013] According to an aspect of the invention, the epitaxial SiC layer is doped with nitrogen, and the underlying SiC substrate is doped with nitrogen.

[0014] According to an aspect of the invention, the epitaxial SiC layer is doped with nitrogen to a concentration of from about 1e14/cm^3 to about 2e16/cm^3, and the underlying SiC substrate is doped with nitrogen to a resistivity of about 0.02 ohm-cm.

[0015] According to an aspect of the invention, the extension region is implanted with one of aluminum and boron, and the junction termination extension region is implanted with one of aluminum and boron.

[0016] According to an aspect of the invention, the extension region is implanted with one of aluminum and boron with a dose of between about 1e13/cm^2 to about 1e15/cm^2, and the junction termination extension region is implanted with one of aluminum and boron with a dose of between about 1e11/cm^2 to about 1e13/cm^2,

[0017] According to an aspect of the invention, the doping of the junction termination extension region is less than the doping of the extension region.

[0018] According to an aspect of the invention, the shallow trench has a depth of between about 2 μm to about 5 μm, and a termination length defined by a width of the shallow

trench and an extension of the junction termination extension region beyond the trench is selected to withstand a preselected blocking voltage.

[0019] According to an aspect of the invention, the termination length is between about 21 μm to about 55 μm.

[0020] According to an aspect of the invention, a method for forming a high voltage termination in a semiconductor device includes providing a substrate of a first conductivity type, performing an ion implantation to form an extension region of a second conductivity type opposite the first conductivity type in the substrate, forming a shallow trench in the substrate adjacent to an active area of the substrate, the shallow trench extending past an edge of the extension region, performing an ion implantation to form a junction termination extension region of the second conductivity type in the shallow trench and intersects the extension region, forming an insulating layer over the extension region and the junction termination extension region, and forming a metal layer formed over the insulating layer, the metal layer extending into the shallow trench, the metal layer electrically connected through a via in the insulating layer to the extension region.

[0021] According to an aspect of the invention, performing an ion implantation to form an extension region of a second conductivity type opposite the first conductivity type in the substrate comprises performing the ion implantation to form the extension region that extends from an edge of the shallow trench opposite the active area to define a termination length for the high-voltage termination.

[0022] According to an aspect of the invention, forming a shallow trench in the substrate comprises forming a shallow trench in the substrate having sidewalls disposed at angles between about 45° and about 60°.

[0023] According to an aspect of the invention, providing a substrate of a first

conductivity type comprises providing a SiC epitaxial layer over a SiC substrate. According to an aspect of the invention, providing a substrate of a first conductivity type comprises providing a SiC epitaxial layer doped with nitrogen over a SiC substrate doped with nitrogen. According to an aspect of the invention, forming an extension region of a second conductivity type comprises performing an implantation with one of aluminum and boron, and with a dose of between about 1e13/cm^2 to about 1e15/cm^2, and forming the junction termination extension region of a second conductivity type comprises performing an implantation with one of aluminum and boron, and with a dose of between about 1e11/cm^2 to about 1e13/cm^2, and the doping of the junction termination extension region is less than the doping of the extension region.

According to an aspect of the invention, a transistor with high-voltage termination, includes a substrate of a first conductivity type, an active area in the substrate including source and drain regions of the transistor, a gate disposed over the source and drain regions, a shallow trench disposed in the substrate adjacent to the active area of the substrate, a doped extension region of a second conductivity type, opposite the first conductivity type, formed in the substrate and extending from a first edge of the shallow trench and contacting the source of the transistor, a junction termination extension region of the second conductivity type formed in the shallow trench and contacting the extension region, the junction termination region extending past a second edge of the shallow trench opposite the first edge, an insulating layer formed over at least a portion of the extension region and over the junction termination extension region, and a metal layer formed over the insulating layer, the metal layer extending into at least a portion of the shallow trench, the metal layer electrically connected through a via in the insulating layer to the extension region.

[0024] According to an aspect of the invention, the source region is disposed in a p-well formed in the substrate, and the doped extension region contacts the p-well.

[0025] According to an aspect of the invention, a length of the shallow trench and the doped extension region together form a termination length of the high-voltage termination for the transistor.

BRIEF DESCRIPTION OF THE DRAWING FIGURES

[0026] The invention will be explained in more detail in the following with reference to embodiments and to the drawing in which are shown:

[0027] FIG. 1 is a cross-sectional diagram of a portion of a semiconductor device including a high-voltage termination in accordance with an aspect of the present invention;

[0028] FIGS. 2A through 2H are cross-sectional diagrams of the high-voltage termination of FIG. 1 showing progressive steps in an illustrative fabrication process in accordance with an aspect of the present invention; and

[0029] FIG. 3A and 3B are cross-sectional diagrams of a portion of a semiconductor device including a high-voltage termination in accordance with an aspect of the present invention formed in different examples of substrates.

DETAILED DESCRIPTION

[0030] Persons of ordinary skill in the art will realize that the following description is illustrative only and not in any way limiting. Other embodiments will readily suggest themselves to such skilled persons.

[0031] The present invention is particularly advantageous when employed with silicon carbide (SiC) Schottky diodes and SiC MOSFETS but persons of ordinary skill in the art will appreciate that the present invention can be used with other devices.

[0032] The word “substrate” is used herein and may have several meanings that will be

apparent from the context in which it is used. A substrate may be the layer in which the implanted regions are directly formed. In some instances it may be a substrate with no overlying layers. In other instances it may be in the form of an epitaxial layer formed over an underlying substrate. In other instances it may be in the form of a well structure formed in an underlying substrate. In any event persons of ordinary skill in the art will be readily able to determine the meaning of "substrate" by examining the context in which it is used.

[0033] Referring first of all to FIG. 1, an illustrative embodiment of high-voltage termination 10 for a semiconductor device in accordance with an aspect of the present invention is shown in cross-sectional view along with a SiC MOSFET transistor 12 to be protected. The particular embodiment shown in FIG. 1 is formed on an SiC epitaxial layer 14 grown on a SiC substrate 16 in a conventional manner. In one embodiment of the invention, the thickness of the SiC substrate 16 is about 350 μm +/- 25μm. The substrate 16 is doped with an n-type dopant, such as nitrogen, to achieve a typical resistivity of 0.02 ohm-cm and the epitaxial layer 14 is doped with nitrogen to a typical concentration of about 1e14/cm^3 to 2e16/cm^3.

[0034] The thickness of the epitaxial layer 14 is chosen depending on the desired voltage rating, and the thickness of the epitaxial layer 14 varies approximately linearly with the desired voltage rating. In addition, a good approximation for a JTE termination is that it has a length equal to about 3 times the thickness of the epitaxial layer 14. For example, the thickness of the epitaxial layer 14 for a 1700 V rating should be about 13.5 μm-thick which results in a 40.5 μm-long JTE termination. The epitaxial layer 14 thicknesses for 700 V, 1,200 V, 3,300 V, and 6,500 V ratings are 5 μm, 10 μm, 30 μm, and 60 μm respectively.

[0035] The MOSFET transistor 12 has a source region 18 formed in a p-well 20 disposed

in the epitaxial layer 14. In exemplary embodiments of the invention aluminum or boron is used for doping of the p-well 20. In one illustrative embodiment of the invention, the p-well 20 is doped with aluminum or boron with a dose of between about 5e12cm^{-2} and about 1e15cm^{-2}.

[0036] In the particular embodiment depicted in FIG. 1, the transistor 12 has a drain 22 formed on the back side of the substrate 16 and a gate 24 insulated from the surface of the epitaxial layer 14 as is known in the art. As will be appreciated by persons of ordinary skill in the art, the transistor 12 may take the form of an annular transistor or have other geometries such as, for example, long stripes. The present invention is applicable to all such transistor geometries.

[0037] A p-type doped extension (PEXT) region 26 is formed on the surface of the SiC epitaxial layer 14 and extends to and is connected to the p-well 20. The PEXT region 26 is doped with a species such as aluminum or boron. In one illustrative embodiment of the invention, the PEXT region 26 is doped with an implantation dose of about 1e13cm^{-2} to 1e15cm^{-2}, although the present invention is not limited to this doping range. The PEXT region 26 is more heavily doped than the p-well 20. Junction depths of PEXT region 26 depend on the implantation energy which is usually between about 200 keV to 500 keV.

[0038] A shallow trench 28 having a length L and a depth D as shown in FIG. 1. The shallow trench 28 is formed in the upper surface of the SiC epitaxial layer 14 and intersects the PEXT region 26. In one embodiment the shallow trench 28 has a length L of about 20 μm to 50 μm. The shallow trench 28 is formed to a depth D of about 2 μm to 5 μm.

[0039] It has been found that the slope of the wall of the shallow trench 28 should be preferably optimized for any particular design and should preferably be between about 45° and about 60°.

[0040] A p-type doped junction termination extension (JTE) region 30 is formed in the shallow trench 28 and intersects the PEXT region 26. The JTE region 30 additionally extends beyond the edge of the trench 28 in the direction opposite the transistor 12. The p-type doped JTE region 30 is implanted with a species such as aluminum (or boron), and a dose of about 1e11/cm^2 to 1e13 /cm^2 (typically about 1e12/cm^2). Preferably the doping of JTE region 30 is less than that of PEXT region 26, and further preferably 2 orders of magnitude less. The junction depth of JTE region 30 is about 1 μm. It is necessary that for any given design the JTE implantation dose be selected to assure that the JTE region is fully "depleted" under the reverse bias applied to the device. A dielectric layer 32 formed from for example deposited silicon dioxide (oxide) to a thickness of between about 1 μm to 3 μm is disposed over a portion of the PEXT region 26 and over the JTE region 30.

[0041] A metal layer 34 is disposed over a portion of the dielectric layer 32 and extends into the trench 28. The metal layer 34 extends beyond the edge of the trench 28 towards the transistor 12 and is in electrical contact with the source 18 of the transistor 12, with the p-well 20 and with PEXT region 26 through a via. The metal layer 34 is formed from a metal such as but not limited to a stack of titanium and aluminum to a thickness of between about 1 μm to 5 μm, depending on the application. The targeted thickness is measured with respect to a flat surface, and then conforms to the topology. For high power devices the thickness of the metal layer 34 can be about 5 μm. If the present invention is incorporated into a low voltage integrated circuit, then a 1 μm thick layer of the metal used for that technology will be satisfactory. A dielectric layer 36 formed from a material such as oxynitride to a thickness of between about 1 μm and about 4 μm is disposed over the portion of the dielectric layer 32 not covered by metal layer 34 and over the metal layer 34.

[0042] The length of the trench 28 plus the extension of the JTE region 30 beyond the edge of the trench 28 in the direction opposite the transistor 12 is referred to herein as the termination length. The JTE region 30 extends beyond the edge of the trench 28 in the direction opposite the transistor 12 by at least 1 μm and typically extends beyond the edge of the trench 28 by between about 1 μm and about 5 μm. The termination length is tailored to meet the blocking voltage requirement and is shown at arrows 38. In an embodiment where the blocking voltage is about 1,700V, the termination length 38 is about 40.5 μm. The termination length 38 scales linearly with blocking voltage.

[0043] The high-voltage termination of the present invention presents a narrower design than other solutions such as floating field ring designs. The metal layer 34 acts as a field plate to extend the applied voltage to a defined area and spreads the charge to reduce the electric field and avoid avalanche breakdown at relatively low voltages. The high-voltage termination of the present invention presents a blocking voltage close to the full capability of the epitaxial layer 14 and exhibits a lower leakage current, hence improved reliability. The breakdown voltage is significantly higher for the high voltage termination structure that spans the termination length 38 than for the active area of the transistor 12, resulting in a higher reliability under harsh electrical and environmental conditions.

[0044] Referring now to FIGS. 2A through 2H, a series of cross-sectional diagrams show the structure resulting after selected steps in an illustrative fabrication process have been performed. In the illustrative embodiment depicted in FIGS. 2A through 2H, the p-well 20 for the transistor 12 is shown as being formed prior to the PEXT region 26 and the JTE region 30. Persons of ordinary skill in the art will appreciate that embodiments of the invention are contemplated where the PEXT region 26 and the JTE region 30 are formed prior to forming the p-well 20.

[0045] Referring first to FIG. 2A, a cross-sectional view shows the structure resulting

after an epitaxial SiC layer 14 doped with an n-type dopant such as, for example, nitrogen to a concentration from between 1e14/cm^3 to 2e16/cm^3 has been formed on a SiC substrate 16 having a resistivity typically close to 0.02 ohm-cm using an epitaxy growth process as is known in the art. A p-well 20 has been formed in the epitaxial layer 14. In one illustrative embodiment of the invention, the p-well 20 is doped with aluminum or boron with a dose of between about 5e12cm^{-2} and about 1e15cm^{-2}.

[0046] Referring now to FIG. 2B, a cross-sectional view shows the structure resulting after a p-type doped extension (PEXT) region 26 has been formed using a masked implant process as is known in the art and the mask has been removed. The PEXT region 26 has been implanted using a dopant species such as aluminum (or boron) with a dose of between about 1e13/cm^2 to 1e15/cm^2, with an implant energy of from about 200 keV to 500 keV although the invention is not limited to this range. The PEXT region 26 partially overlaps the p-well 20 in an area opposite where the channel of the transistor 12 of FIG. 1 will be formed and will result in the dopant concentration of that portion of the p-well 20 being higher than the portion of the p-well 20 that is proximate to the channel of the transistor 12 of FIG. 1. This will not affect the performance of the transistor 12. The PEXT region 26 is generally more heavily doped than the p-well 20.

[0047] Referring now to FIG. 2C, a cross-sectional view shows the structure resulting after a shallow trench 28 has been formed in the epitaxial SiC layer 12 using conventional semiconductor processing techniques. In one embodiment of the invention the shallow trench 28 has a length of about 20 μm to 50 μm, depending on the blocking voltage requirement, and is formed to a depth of about 2 μm to 5 μm. The shallow trench 28 consumes a portion of the PEXT implant 26 as shown in FIG. 2C.

[0048] Referring now to FIG. 2D, a cross-sectional view shows the structure resulting after a p-type doped junction termination extension (JTE) region 30 has been formed in

the trench 28 using a masked implant process as is known in the art and the mask has been removed. The p-type doped JTE region 30 intersects the p-type extension region 26 and further extends beyond the edge of the trench 28 in the direction opposite the transistor 12 by at least 1 μm and typically extends beyond the edge of the trench 28 by between about 1 μm and about 5 μm. FIG. 2D shows the JTE region 30 separately from the PEXT implant 26 to illustrate the edges of the mask used to perform the masked implant process.

[0049] The p-type doped JTE region 30 is doped with a species such as aluminum or boron, using an implant dose of from about 1e11/cm^2 to 1e13 /cm^2 (typically about 1e12/cm^2). Preferably the doping of JTE region 30 is less than that of PEXT region 26, and further preferably 2 orders of magnitude less. The junction depth may be about 1 μm.

[0050] Referring now to FIG. 2E, a cross-sectional view shows the structure resulting after an activation step has been performed to activate the implanted dopant atoms in PEXT region 26 and p-type doped JTE region 30.

[0051] Referring now to FIG. 2F, a cross-sectional view shows the structure resulting after a dielectric layer 32 has been formed from, for example, deposited silicon dioxide to a thickness of between about 1 μm to 3 μm over the surface of the structure including the PEXT and p-type doped JTE regions 26 and 30. The dielectric layer 32 extends past the edges of the p-type doped JTE region 30. A via 40 has been formed in the dielectric layer 32 using conventional semiconductor processing techniques to expose the upper surface of the PEXT region 26 outside of the edge of the shallow trench 28 as well as the source 18 of the transistor 12 and the p-well 20 (as shown in FIG. 1).

[0052] Referring now to FIG. 2G, a cross-sectional view shows the structure resulting after a metal layer 34 has been deposited and patterned using a metal such as, but not

limited to, a stack of titanium and aluminum employing conventional semiconductor processing techniques over the surface of the structure and into the via 40 to make an electrical connection to the PEXT region 26 and to the source 18 of the transistor 12 and p-well 20 (as shown in FIG. 1). The thickness of the metal layer 34 is typically between about 1 μm to 5 μm, depending on the application. Power devices will employ thicker metal layers. If the present invention is practiced in an integrated circuit then a 1 μm thick layer of the metal used for that technology will be satisfactory.

[0053] Referring now to FIG. 2H, a cross-sectional view shows the structure resulting after a dielectric layer 36 formed from a material such as silicon oxynitride has been deposited over the exposed portion of the dielectric layer 32 and the metal layer 34.

[0054] Persons of ordinary skill in the art will appreciate that while the present invention has been disclosed using illustrative embodiments where p-type implants are used in n-type substrates and wells, it should be apparent that embodiments that employ n-type implants in p-type substrates and wells are contemplated to be within the scope of the present invention.

[0055] Persons of ordinary skill in the art will appreciate that the SiC epitaxial layer 14 over SiC substrate 16 embodiment described with reference to FIGS. 1 and 2A through 2H is illustrative only and is non-limiting. Such skilled persons will appreciate that the high-voltage termination structure of the present invention may be formed using other technologies. FIGS. 3A and 3B illustrate how the present invention may be practiced using two other exemplary technologies.

[0056] FIG. 3A shows an embodiment of the high-voltage termination structure of the present invention formed on a substrate 50. Substrate 50 may be an n-type substrate and the PEXT region 26 and JTE region 30 may be p-type implants. Substrate 50 may also be a p-type substrate and the PEXT region 26 and p-type doped JTE region 30 may be

replaced with n-type regions.

[0057] FIG. 3B shows an embodiment of the high-voltage termination structure of the present invention formed in a well 52 formed in a substrate 50. The well 52 may be an n-well formed in a p-type substrate 50 and the PEXT region 26 and JTE region 30 may be p-type regions. The well 52 may also be a p-well formed in an n-type substrate and the PEXT region 26 and p-type doped JTE region 30 may be replaced with n-type regions.

[0058] The present invention may be employed in high-voltage designs where the output voltage nodes can support voltages up to about 10,000 V.

[0059] While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

What is claimed is:

1. A high-voltage termination for a semiconductor device comprising:

a substrate of a first conductivity type;

an implanted device region of a second conductivity type, opposite the first conductivity type, forming a part of the semiconductor device;

a shallow trench disposed in the substrate adjacent to the implanted device region;

a doped extension region of the second conductivity type formed in the substrate, the doped extension region extending between the implanted device region and a first edge of the shallow trench adjacent to the implanted device region;

a junction termination extension region of the second conductivity type formed in the shallow trench and contacting the extension region, the junction termination region extending past a second edge of the shallow trench opposite the implanted device region;

an insulating layer formed over at least a portion of the extension region and over the junction termination extension region; and

a metal layer formed over the insulating layer, the metal layer extending into at least a portion of the shallow trench, the metal layer electrically connected through a via in the insulating layer to the extension region.

2. The high-voltage termination of claim 1 wherein a length of the shallow trench and the doped extension region together form a termination length of the high-voltage termination.

3. The high-voltage termination of claim 1 further comprising a second insulating layer formed over the metal layer and the insulating layer.

4. The high-voltage termination of claim 1 wherein sidewalls of the shallow trench are at angles between about 45° and about 60°.

5. The high-voltage termination of claim 1 wherein the substrate of the first conductivity type is an epitaxial layer disposed over an underlying substrate.

6. The high-voltage termination of claim 5 wherein:
the epitaxial layer is an epitaxial SiC layer; and
the underlying substrate is a SiC substrate.

7. The high-voltage termination of claim 6 wherein:
the epitaxial SiC layer is doped with nitrogen; and
the underlying SiC substrate is doped with nitrogen.

8. The high-voltage termination of claim 7 wherein:
the epitaxial SiC layer is doped with nitrogen to a concentration of from about 1e14/cm^3 to about 2e16/cm^3; and
the underlying SiC substrate is doped with nitrogen to a resistivity of about 0.02 ohm-cm.

9. The high-voltage termination of claim 1 wherein:
the extension region is implanted with one of aluminum and boron; and
the junction termination extension region is implanted with one of aluminum and boron.

10. The high-voltage termination of claim 9 wherein:

the extension region is implanted with one of aluminum and boron with a dose of between about 1e13/cm^2 to about 1e15/cm^2; and

the junction termination extension region is implanted with one of aluminum and boron with a dose of between about 1e11/cm^2 to about 1e13/cm^2,

wherein the doping of the junction termination extension region is less than the doping of the extension region.

11. The high-voltage termination of claim 1 wherein:

the shallow trench has a depth of between about 2 μm to about 5 μm; and

a termination length defined by a width of the shallow trench and an extension of the junction termination extension region beyond the trench is selected to withstand a preselected blocking voltage.

12. The high-voltage termination of claim 1 wherein the termination length is between about 21 μm to about 55 μm.

13. A method for forming a high voltage termination for a semiconductor device comprising:

providing a substrate of a first conductivity type, the substrate having a semiconductor device including at least one implanted device region;

performing an ion implantation to form an extension region of a second conductivity type opposite the first conductivity type in the substrate, the extension region contacting the at least one implanted device region;

forming a shallow trench in the substrate, the shallow trench having a first edge defining an end of the extension region;

performing an ion implantation to form a junction termination extension region of the second conductivity type in the shallow trench, the junction termination extension region connected to the extension region;

forming an insulating layer over the extension region and the junction termination extension region; and

forming a metal layer formed over the insulating layer, the metal layer extending into the shallow trench, the metal layer electrically connected through a via in the insulating layer to the extension region.

14. The method of claim 13 wherein performing the ion implantation to form the junction termination extension region of the second conductivity type opposite the first conductivity type in the substrate comprises performing the ion implantation to form the junction termination extension region that extends from a second edge of the shallow trench opposite the first edge to define a termination length for the high-voltage termination.

15. The method of claim 13 wherein:

forming the shallow trench in the substrate comprises forming the shallow trench in the substrate having sidewalls disposed at angles between about 45° and about 60°.

16. The method of claim 13 wherein:

providing a substrate of a first conductivity type comprises providing a SiC epitaxial layer over a SiC substrate.

17. The method of claim 16 wherein providing the substrate of the first conductivity type comprises providing a SiC epitaxial layer doped with nitrogen over a SiC substrate doped with nitrogen.

18. The method of claim 16 wherein:

forming the extension region of the second conductivity type comprises performing an implantation with one of aluminum and boron, and with a dose of between about 1e13/cm^2 to about 1e15/cm^2; and

forming the junction termination extension region of the second conductivity type comprises performing an implantation with one of aluminum and boron, and with a dose of between about 1e11/cm^2 to about 1e13/cm^2:

wherein the doping of the junction termination extension region is less than the doping of the extension region

19. A transistor with high-voltage termination, comprising:

a substrate of a first conductivity type;

an active area in the substrate including source and drain regions of the transistor;

a gate disposed over the source and drain regions;

a shallow trench disposed in the substrate adjacent to the active area of the substrate;

a doped extension region of a second conductivity type, opposite the first conductivity type, formed in the substrate and extending from a first edge of the shallow trench and contacting the source of the transistor;

a junction termination extension region of the second conductivity type formed in the shallow trench and contacting the doped extension region, the junction

termination region extending past a second edge of the shallow trench opposite the first edge in a direction away from the active area;

an insulating layer formed over at least a portion of the extension region and over the junction termination extension region; and

a metal layer formed over the insulating layer, the metal layer extending into at least a portion of the shallow trench, the metal layer electrically connected through a via in the insulating layer to the extension region.

20. The transistor of claim 19 wherein:

the source region is disposed in a p-well formed in the substrate; and

the doped extension region contacts the p-well,

wherein the extension region is doped to a greater concentration than both the p-well and the junction termination extension region.

21. The high-voltage termination of claim 19 wherein a length of the shallow trench and the extension of the junction termination region past the second edge of the shallow trench together form a termination length of the high-voltage termination for the transistor.

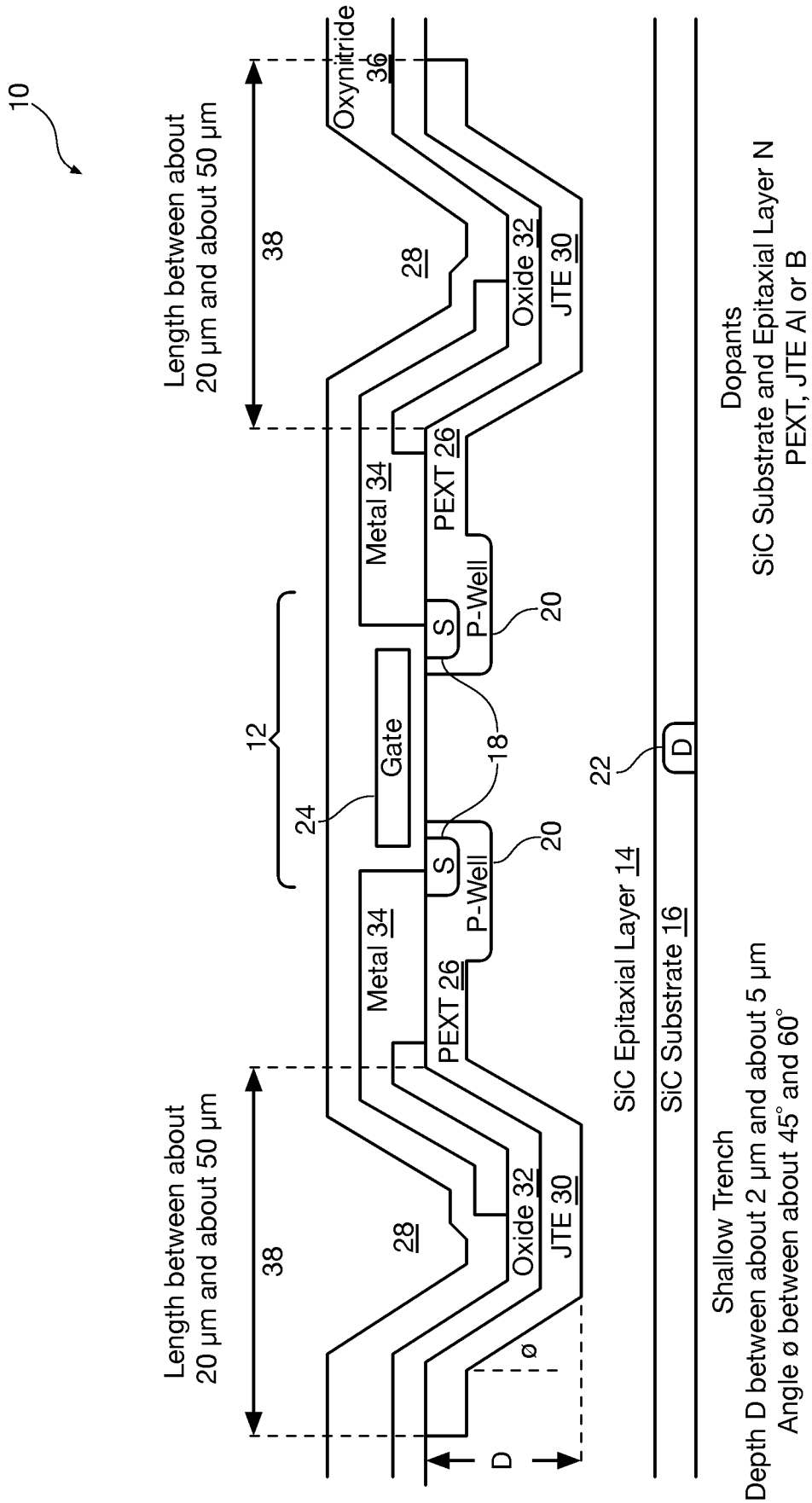
10
Length between about
20 µm and about 50 µm
38
Oxynitride
36
28
Oxide 32
JTE 30
Metal 34
PEXT 26
S
P-Well
20
12
24
Gate
18
22
D
SiC Epitaxial Layer 14
SiC Substrate 16
Dopants
SiC Substrate and Epitaxial Layer N
PEXT, JTE Al or B
Shallow Trench
Depth D between about 2 µm and about 5 µm
Angle ø between about 45° and 60°
ø

FIG. 1

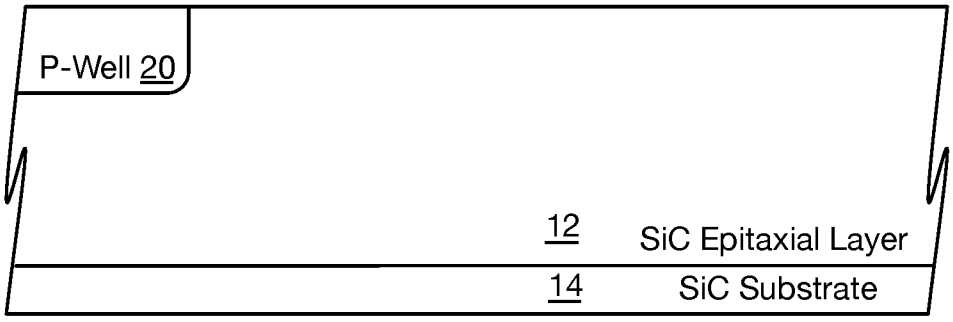

FIG. 2A

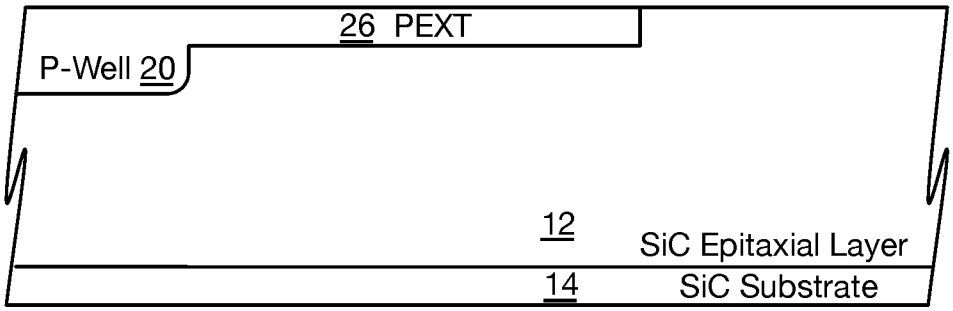

FIG. 2B

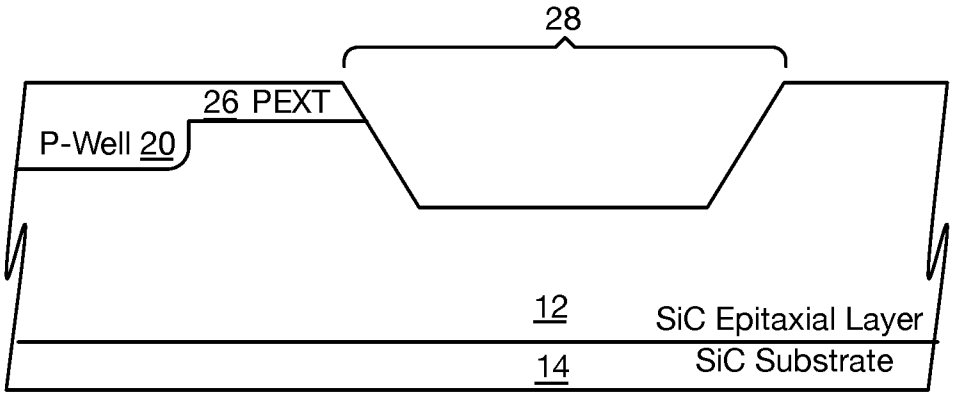

FIG. 2C

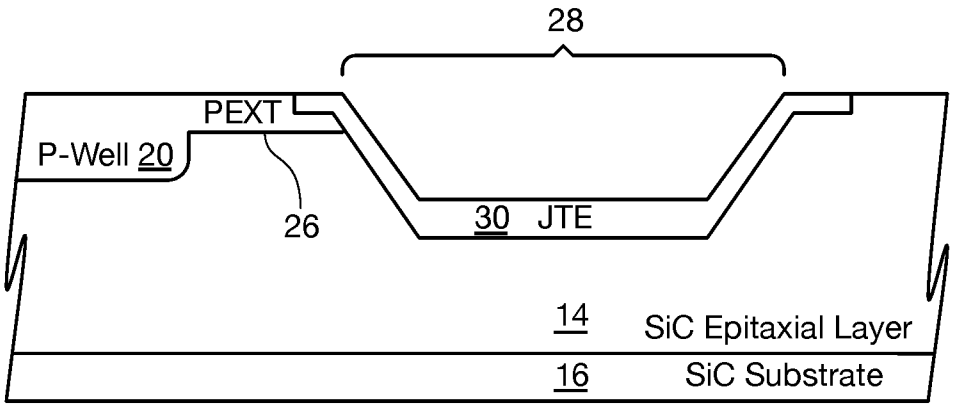

FIG. 2D

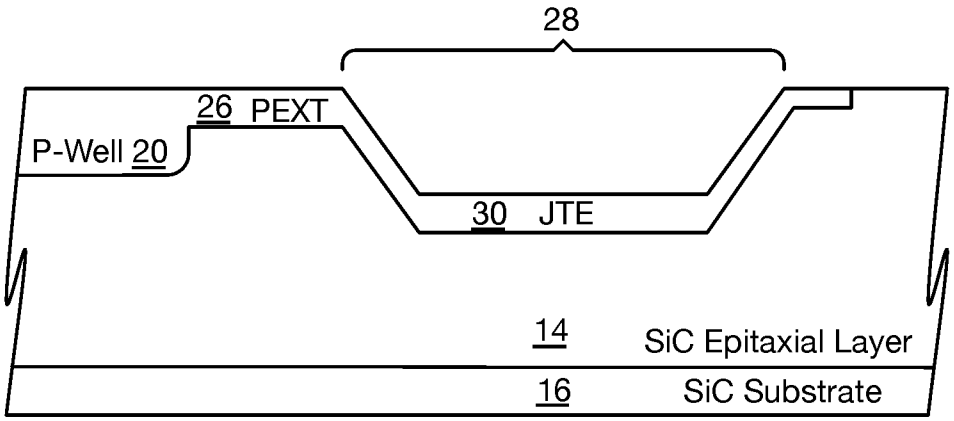

FIG. 2E

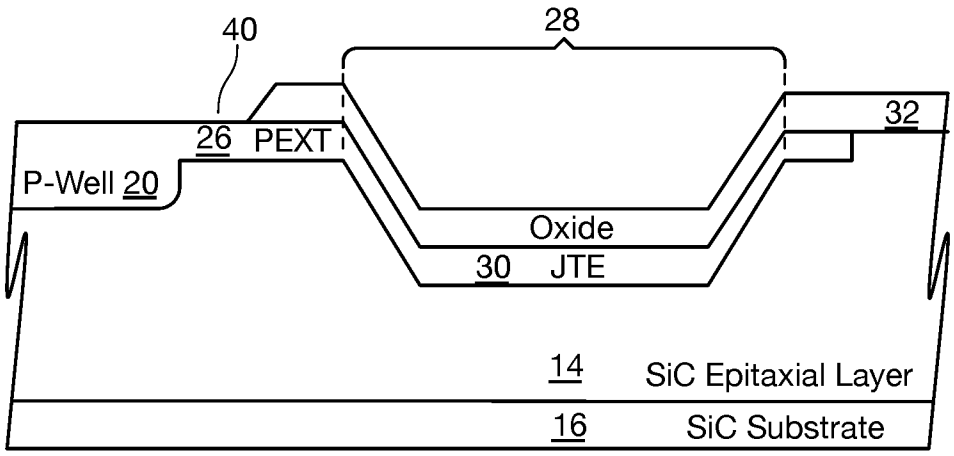

FIG. 2F

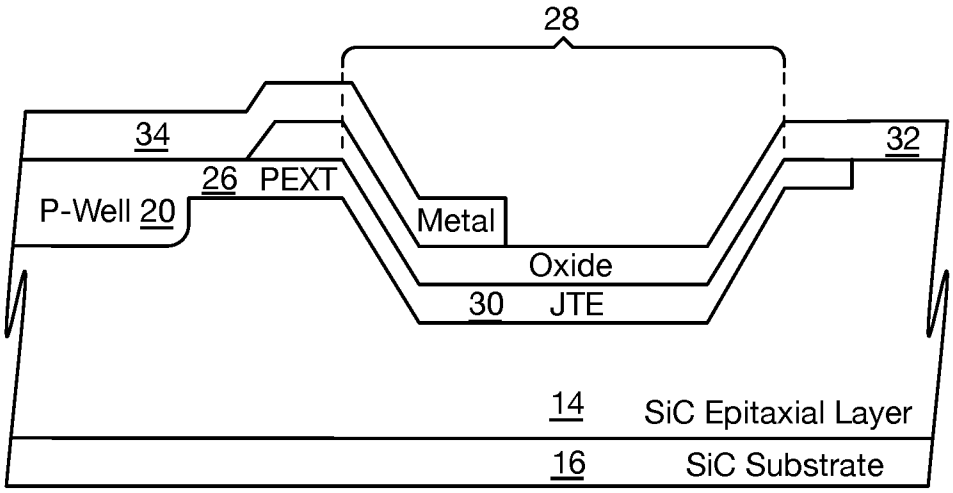
28
34
32
26 PEXT
P-Well 20
Metal
Oxide
30 JTE
14 SiC Epitaxial Layer
16 SiC Substrate

FIG. 2G

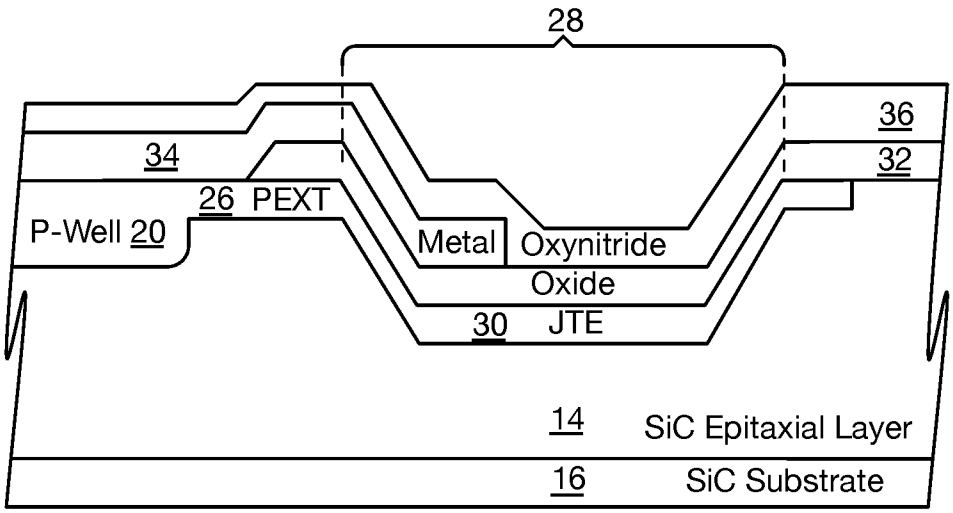
28
36
34
32
26 PEXT
P-Well 20
Metal
Oxynitride
Oxide
30 JTE
14 SiC Epitaxial Layer
16 SiC Substrate

FIG. 2H

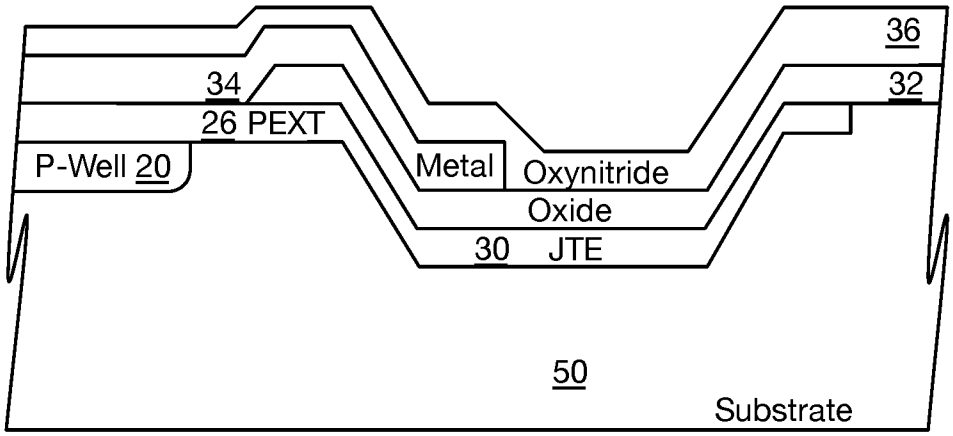
36
34
32
26 PEXT
P-Well 20
Metal
Oxynitride
Oxide
30 JTE
50
Substrate

FIG. 3A

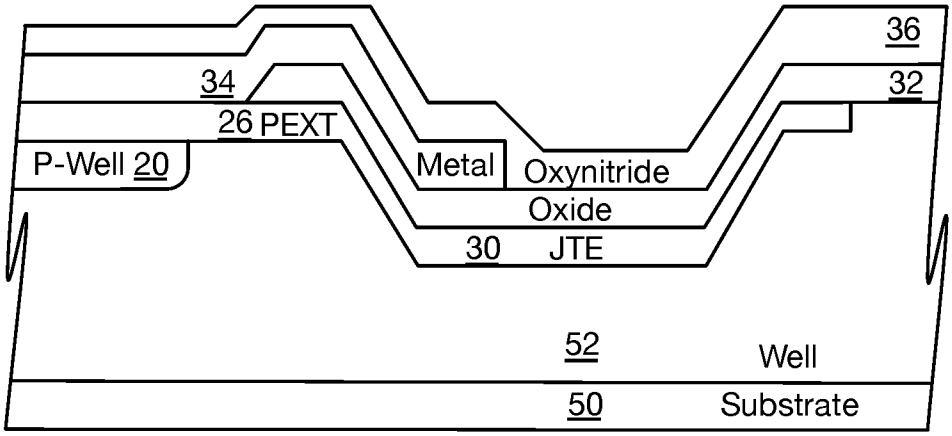
36
34
32
26 PEXT
P-Well 20
Metal
Oxynitride
Oxide
30 JTE
52
Well
50
Substrate

FIG. 3B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2019/061857

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/78 H01L29/06 H01L29/12 H01L21/336
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011/272735 A1 (SCHMIDT GERHARD [AT]) 10 November 2011 (2011-11-10) paragraph [0024] - paragraph [0036]; figures 1,2 paragraph [0045] paragraph [0048] paragraph [0052] - paragraph [0055]; figure 8 paragraph [0064] - paragraph [0069] ----- -/--	1-21

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 February 2020	24/02/2020

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Lantier, Roberta

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2019/061857

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2015/108501 A1 (IWAMURO NORIYUKI [JP] ET AL) 23 April 2015 (2015-04-23) paragraph [0019] - paragraph [0020] paragraph [0054]; figures 1A-1B paragraph [0064] - paragraph [0066]; figures 3,4 paragraph [0067] - paragraph [0074]; figures 5-12	1-9, 11-17, 19,21

Y	US 2002/063300 A1 (MIYAJIMA TAKESHI [JP]) 30 May 2002 (2002-05-30) paragraph [0007] paragraph [0023] - paragraph [0027]; figure 2 paragraph [0037] - paragraph [0043]; figures 4-6	10,18,20

A	JP H06 151867 A (SHARP KK) 31 May 1994 (1994-05-31) the whole document	1-21

2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2019/061857

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		DE 102011075601 A1	10-11-2011
		US 2011272735 A1	10-11-2011
US 2015108501 A1	23-04-2015	CN 104303307 A	21-01-2015
		DE 112013002213 T5	16-04-2015
		JP 5818099 B2	18-11-2015
		JP 2013232562 A	14-11-2013
		US 2015108501 A1	23-04-2015
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		JP H06151867 A	31-05-1994