

(19)



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) Publication number:

0 316 147 B1

(12)

EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification: **04.08.93** (51) Int. Cl.⁵: **G05F 3/22**, G05F 3/28

(21) Application number: **88310525.6**

(22) Date of filing: **09.11.88**

(54) **High gain driver circuit and method.**

(30) Priority: **09.11.87 US 118710**

(43) Date of publication of application:
17.05.89 Bulletin 89/20

(45) Publication of the grant of the patent:
04.08.93 Bulletin 93/31

(84) Designated Contracting States:
DE FR GB IT

(56) References cited:
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US-A- 3 629 691
US-A- 4 085 359
US-A- 4 338 646

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Description

BACKGROUND OF THE INVENTION

The present invention relates to electronic circuits and more specifically, to methods and circuitry for optimizing the operating characteristics of driver designs which function efficiently and independently of loading conditions.

Driver circuits or digital peripheral drivers may be described as interface devices which are frequently employed to switch high current, high voltage loads in response to standard digital logic input signals. Examples of such loads may include relays, solenoids, lamps, or other peripheral circuit elements.

In any driver circuit design, one of the most important design considerations is the conservation of drive current to an output transistor. This requires a careful analysis of numerous worst case conditions including process variations which affect a change in transistor beta or resistor values, as well as the effects of temperature and voltage variations on transistor betas, resistor values, and base to emitter voltages (V_{be}). Once these conditions are well understood, a circuit designer may elect to implement a circuit which demonstrates a drive current having a value of the worst case drive current plus a 50% overdrive.

While the above approach to designing driver circuits guarantees operation within the range of anticipated variations, the resulting circuits generate excessive drive currents under optimum operating conditions as well as undesirable power dissipation. Moreover, many power drivers in the past have been designed to have current ratings which are two to four times the actual load which results in even further excessive waste of current. Finally, driver circuits are typically designed to operate with a particular load. Any change of loading condition to such designs may result in undesirable operating characteristics. Namely, replacing the "designed load" with one that requires less drive current is at best inefficient, while substituting a load that requires greater drive current may render the driver insufficient. In the later situation, the driver may in fact come out of the saturated state and dissipate excessive power. This in turn may cause a thermally generated loss of functionality if the device is thermally protected and a catastrophic device failure if it is not.

Accordingly, a need has arisen for a high efficiency, high gain driver circuit that is suitable for power applications. In particular, a need has arisen for a driver circuit that optimizes the utilization of drive current for a variety of loading conditions. Such a driver circuit should ideally be suitable for implementation in integrated circuit form and ca-

pable of fulfilling the need for such a design in a broad variety of applications including high power automotive and portable equipment operating environments.

In EP-A-0 121 287, there is described a current stabilizing circuit for establishing a controlled current between two conductors. The circuit comprises two current mirrors, one of which includes an emitter resistor providing an offset, with the current input conductor of each mirror connected to the current output conductor of the other mirror. The two current mirrors provide different factors relating their input and output currents, so that with the offset provided by the resistor the input and output currents are stabilized at the values determined by the intersection of the current relationships. A starter circuit is provided for feeding initial currents to both conductors interconnecting the current mirrors.

It is a primary object of this invention to provide an improved current driver circuit which provides unlimited drive current that is self adjusted to the load requirements and which employs over current limiting. Another object is to provide a current driver circuit which may be used for both high and low side driver applications. yet another object is to provide a current driver circuit which dissipates minimal power and reduced standby current. Finally, it is a further object to provide a current drive circuit that requires no input current to turn off.

According to a first aspect of the present invention there is provided a circuit for controlling the current fed to a load device through the circuit, comprising

first and second terminals from one to the other of which the controlled current flows,

a regulating circuit comprising first and second current mirror circuits connected respectively to said first and second terminals and having the current input conductor of each current mirror circuit connected to the current output conductor of the other current mirror circuit, with a resistor connected in the emitter circuit of a transistor providing the current output of the second current mirror circuit, and

a start-up circuit connected to supply an initiating current to the regulating circuit,

characterised in that the circuit includes

a driving transistor having a controlled current path and a control electrode, and

a pre-drive transistor having an electrode coupled by an output circuit to the control electrode of the driving transistor, a base and another electrode connected to the second terminal, the base of the pre-drive transistor being connected to a base connection of the transistors forming the second current mirror and to receive the initiating current from

the start-up circuit,

the controlled current path of the driving transistor being connected from the first terminal to the resistor so that the controlled current through the transistor flows through the resistor to the second terminal, the first current mirror circuit having a second current output conductor connected to the base of a control transistor that controls the base current fed to the pre-drive transistor and thereby the conductivity of the driving transistor in response to the voltage established across the resistor.

According to a second aspect of the present invention there is provided a method for controlling the current fed through a circuit to a load device including providing in said circuit two current mirrors, the output current of each of which is fed to the other as an input current, with an emitter resistor in one of the current mirrors, and feeding an initiating current to the current mirrors,

characterised in that the method includes

providing a driving transistor for producing a controlled current which is passed through the resistor in the current mirrors, and

regulating the current through the driving transistor in response to the sum of the initiating current and a current from one of the current mirrors.

In one embodiment, there is provided a four terminal, high efficiency, high gain driver circuit suitable for power application and which exhibits optimum operating characteristics independently of circuit loading conditions. This advantage and others are accomplished by providing a driver design having overcurrent limiting, a self-adjust predriver and minimal standby current. A startup transistor initiates a positive feedback loop that effects the turn-on of drive regulation transistors, predrive transistors, and finally a drive or output transistor. As the drive regulation transistors are driven beyond the level required for a given load, the collector to emitter voltage of the driving transistor decreases causing the drive regulation transistors to saturate. As a result, the input drive to the positive feedback loop is reduced and the drive current provided by the drive regulation transistors is automatically tailored to the load. Under current limiting conditions, the drive regulation transistors in conjunction with a current splitter and current sensing resistor operate to reduce the positive feedback loop drive and limit the load current.

In addition to initiation of circuit operation by the startup transistor, the control transistors together with the start-up transistor and control resistor provide a means to disable the positive feedback loop in the absence of a source off current to the control pin. Furthermore, current supplied from the current splitter is available to assist in driving the control transistors in the event that it is desir-

able to turn the driving circuit off from a conducting condition. Finally, by providing current to the control input, positive feedback loop operation is initiated by the start-up transistor as described above.

The driver circuit of the present invention is suitable for both low and high side driver applications. In high side applications, the circuit will provide a source of current to any load while in low side system designs the same circuit may be driven by any load. It is therefore possible to implement the driver circuit in a very broad range of applications.

BRIEF DESCRIPTION OF THE DRAWINGS

Further features and advantages of the invention will become apparent from the description of the following embodiment, taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a block diagram of the four terminal driver circuit of the present invention showing external bias and output connections for a high side application;

FIGURE 2 is a block diagram of the four terminal driver circuit of the present invention showing external bias and output connections for a low side application;

FIGURE 3 is a schematic diagram representing a preferred embodiment of the high gain driver circuit of the present invention; and

FIGURE 4 is a schematic diagram of an alternative embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring first to Figure 1, there is shown a block diagram of the four terminal driver circuit including the external bias arrangement for a high side driver application. As will be described in detail below, current sources 30 and 31 provide the current necessary to enable the driver circuit by activating an appropriate startup transistor. Terminal 40 labeled VBAT is coupled to a suitable source of supply voltage. For example, in an automotive application this terminal may be connected to the battery voltage supply. Terminal 41 is connected to the load 50 which may be, for example, a lamp or any electrical device requiring current drive. As is apparent from the arrangement wherein the load 50 is coupled between terminal 41 and ground, driver circuit 10 provides the necessary current source to meet the operational requirements of the load device.

Referring next to Figure 2, there is shown a block diagram of the four terminal driver circuit including the external bias arrangement for a low side driver application. All elements and operation

remain as described above for Figure 1 with the exception that circuit 10 is driven by the load 50 which is coupled between terminal 40 and a source of supply, and terminal 41 is coupled to circuit ground. In this low side application, driver circuit 10 provides the same features and advantages that are present in the high side arrangement of Figure 1. It should be obvious that an immediate advantage to the design of driver circuit 10 is the ability to connect the same circuit into either high or low side applications.

Referring now to Figure 3, there is shown a schematic diagram of the preferred embodiment of the present invention. Terminal 40 is connected to the emitter of startup PNP transistor 14 which has its base connected to the base of bias PNP transistor 15 as well as terminal 43. The emitter of bias transistor 15 is also connected to terminal 40. As described above, in operation terminal 43 is connected to an external bias source 30. Terminal 43 is also connected to the collector of bias transistor 15. Startup transistor 14 is a dual collector transistor having a collector 35 connected to the collector 32 of multiple collector current splitter transistor 11. Collector 35 of startup transistor 14 is connected to the collector of a first enabling control transistor 23 and also to the base of a second enabling control transistor 22. In addition, the base of transistor 23 is connected to control terminal 42 and one end of resistor 45 having a second end connected to terminal 41. The emitter of transistor 23 is also connected to terminal 41. In application, control terminal 42 is connected to a suitable source of control current 31 from external logic.

Referring again to startup transistor 14, the second collector 36 is connected to the base of a first predrive transistor 18 and the collector of transistor 22 which has an emitter connected to terminal 41. In addition, transistor 18 has an emitter connected to output terminal 41 as well as the emitter of a first drive regulation transistor 13. The collector of transistor 18 is connected to both the base and a first collector of a second predrive transistor 16 which has an emitter connected to both terminal 40 and the collector of the driving transistor 17. Transistor 16 has a second collector connected to the base of transistor 17. The base of transistor 16 is connected to one end of a resistor 48 having a second end connected to terminal 40. The emitter of driving transistor 17 is connected to one end of current sensing resistor 29 having a second end connected to terminal 41. The emitter of transistor 17 is also connected to the emitter of a second drive regulation transistor 12 which has a base connected to the bases of both transistor 13 and transistor 18. In addition, the base of transistor 12 is connected to the collector of transistor 13, a second collector 33 of current splitter transistor 11,

and one end of compensation capacitor 19 which has a second end connected to the collector of transistor 12. The collector of second drive regulation transistor 12 is also connected to the base of current splitter transistor 11 and a collector 34 of transistor 11. Finally, the emitter of PNP transistor 11 is connected to terminal 40.

Assuming normal load conditions for the high side driver application of Figure 1, the operation of the driver circuit 10 of Figure 3 will now be described in detail. Circuit 10 is enabled by providing a suitable source of voltage to terminal 40, a source of current 30 to bias terminal 43, and a source of current 31 to control terminal 42. The load to be driven by circuit 10 may be connected between terminal 41 and system ground for the high side design. Under the above conditions, startup transistor 14 will turn on and provide drive current to the base of first predrive transistor 18 as well as drive regulation transistors 12 and 13. By providing a source of current to terminal 42, the first control transistor 23 turns on which in turn keeps second control transistor 22 off allowing start-up transistor 14 to adequately drive transistors 18, 13 and 12.

In the conducting operating mode described above, drive regulation transistors 12 and 13 in conjunction with current splitter transistor 11 provide a positive feedback loop which supplies drive current to driving transistor 17 by driving the predrive transistors 16 and 18. Under typical loading conditions, start-up transistor 14 initiates the turn on of predrive transistor 18, and drive regulation transistors 12 and 13. Current splitter transistor 11 provides equal levels of current from collectors 33 and 34 to transistors 12 and 13; however, since transistor 12 is a larger area device, it will carry as much as four times the current of transistor 13. Transistor 18 may also be made larger in area than transistor 13 and functions to amplify the feedback loop current. As an example, transistor 18 may be designed to carry ten times the current carrying capacity of transistor 13. Capacitor 19 is coupled between the base-collector of transistor 12 and serves to reduce the high frequency loop gain to prevent unwanted oscillations. As the demand for load current increases, transistor 18 will continue to provide increased levels of drive to transistors 16 and 17. Once these devices are driven beyond the level required by a given load, their collector to emitter voltages are reduced, causing a reduction in the collector-emitter voltage of predrive transistor 18. As this voltage drops below the base-emitter voltage of transistor 18, the base current will begin to flow into the collector which in turn reduces the current drive to drive regulation transistors 12 and 13. It should be obvious that under these conditions the positive feedback loop action is dimin-

ished and the load current provided by driving transistor 17 is self-adjusted to the requirements of the load.

Referring now to the condition where the load approaches a short circuit or a direct connection of terminal 41 to system ground, current driving circuit 10 will operate in the following manner. As large amounts of current are demanded, transistor 12 is also turned on to provide additional current to the load through current sensing resistor 29. As mentioned previously, transistors 12 and 13 may be sized such that transistor 12 has a V_{be} that is smaller than the V_{be} of transistor 13 by, for example, a factor of four for equal collector currents. Current splitter transistor 11 provides equal amounts of current from collectors 33 and 34 to provide the current source for both transistors 12 and 13. Under these conditions, transistor 12 conducts a greater amount of current than transistor 13. As current begins to flow to the load from drive transistor 17 and conducting drive regulation transistor 12, a voltage drop is established across current sensing resistor 29. When this voltage drop exceeds the difference in V_{be} between transistors 12 and 13, transistor 13 will increasingly conduct and divert drive current from the base of transistor 18. This results in a reduction in the base drive to transistor 16 and driving transistor 17 which regulates the output current level. For the above described conditions, the output current will be limited to the V_{be} of transistor 13 minus the V_{be} of transistor 12 divided by the resistance of current sensing resistor 29.

Current driving circuit 10 may be conveniently disabled by the operation of control transistors 22 and 23, control resistor 45, startup transistor 14, and current splitter transistor 11. By removing the source of current 31 to control terminal 42, control transistor 23 will be turned off. Control resistor 45 references the base of transistor 23 to its emitter to ensure the off condition. With transistor 23 in a non-conducting state, a second control transistor 22 will turn on as base drive is provided by collector 35 of start-up transistor 14. This results in the removal of base drive from transistor 18 which inhibits feedback loop operation and disables driving circuit 10. Under operating conditions wherein circuit 10 was previously on, collector 32 of transistor 11 will provide additional current drive to the base of transistor 22 to ensure that the positive feedback loop is turned off. To again initiate the operation of circuit 10, current source 31 is applied to control terminal 42 which turns the first control transistor 23 on and turns the second control transistor off. Circuit operation is thereafter as described above.

It should be apparent from the foregoing discussion that a particular advantage to the present

design is that no control current is required to disable the current driver circuit 10. In addition, minimal standby current, for example less than 10 microamps, is required in the off condition. Moreover, during operation circuit 10 provides only that current necessary to drive a given load and therefore exhibits optimal power supply to ground current levels as well as reduced sensitivity to power supply voltage variations. Reduced power dissipation is made possible by the fact that current driving transistor 17 is maintained in a low "ON" state.

In certain applications, it may be desirable to employ the current driver circuit 10 in the low side driver configuration of Figure 2. In this case the circuit of Figure 3 may be externally connected as follows. As shown in Figure 2, the load 50 is connected from a source of supply voltage (V_{bat}) to terminal 40, terminal 41 is connected to circuit ground and control and bias sources 31 and 30 are respectively connected to terminals 42 and 43 as in the high side driver application described above. Control and operation of driver circuit 10 are as previously described for the high side application. In low side driver designs, the load will provide a source of current to driver circuit 10. Load current will be tailored to suit the given loading conditions as described above.

Referring next to Figure 4 there is shown an alternative embodiment of the present invention. The same reference numerals are given to those elements that function as in the previously described Figure 3 embodiment. In the design of Figure 4, terminal 40 is coupled to the emitter of startup transistor 14 through startup resistor 27 and also the emitter of bias transistor 15 through bias resistor 28. The collector-base of transistor 15 is connected to terminal 43 to which an external bias source 30 is connected during circuit operation. The base of transistor 15 is connected to the base of startup transistor 14 which is a dual collector PNP transistor having a first collector 36 connected to the collector of a first control transistor 23 and also a first collector 32 of dual collector transistor 11. Transistor 14 also has a second collector 35 connected to the collector of PNP transistor 47 and the collector of NPN transistor 21. Control transistor 23 has a base connected to terminal 42 and one end of a resistor 45 having a second end connected to terminal 41. During operation, terminal 42 is connected to an external current source 31. The collector of transistor 23 is connected to the base of a second control transistor 22 and the emitters of both control transistors 22 and 23 are connected to terminal 41. The collector of transistor 22 is connected to a first regulation transistor 21 having an emitter connected to terminal 41 as well as one end of current sensing resistor 29. The other end

of current sensing resistor 29 is connected to the emitter of a second regulation transistor 20 as well as the emitters of transistor 49, predrive transistor 18 and driving transistor 17. The base of transistor 20 is connected to its collector, to the collector of transistor 46, and also to the base of transistor 21.

Referring again to the regulation transistor 21, it is seen that the collector is also connected to the bases of both transistor 49 and predrive transistor 18. The collector of transistor 49 is connected to both the base and a second collector 34 of current source transistor 11. The first collector 32 is connected to both collector 36 of transistor 14 and the collector of control transistor 23. Transistors 11, 46 and 47 all have emitters coupled to terminal 40 through a current splitter resistor 24, a gain resistor 25, and a drive resistor 26 respectively.

Finally, predrive transistor 18 has a collector connected to the base of a second predrive transistor 16 and also to one end of a resistor 48 having a second end connected to terminal 40. The emitter of PNP transistor 16 is connected to terminal 40 as well as the collector of NPN driving transistor 17. The collector of predrive transistor 16 is connected to the base of driving transistor 17.

Operation of the circuit 10 of Figure 4 is similar to that of the circuit of Figure 3 and will be described for the high side driver application of Figure 1. The comments relating to the low side driver application for the preferred embodiment apply and will not be repeated here.

Referring again to Figure 4, the operation of driver circuit 10 begins by startup transistor conducting upon the application of a suitable source of supply voltage to terminal 40, and current sources to both terminals 43 and 42. The desired load is connected between terminal 41 and system ground. Under these conditions the first control transistor 23 is conducting which prevents the turn on of transistor 22 and allows the collector 35 of startup transistor 14 to drive the bases of both transistor 49 and 18 turning these devices on and establishing a positive feedback loop that turns on predrive transistor 16 and driving transistor 17. As the first predriver transistor 18 is driven beyond that level required by the selected load, the collector to emitter output voltage of transistor 17 decreases causing predrive transistor 18 to saturate and divert base drive from transistor 49. In this manner, the input to the positive feedback loop is reduced and output current from drive transistor 17 is automatically established at just that level required by the load. It should be noted that by ratioing the values of bias resistor 28 and startup resistor 27, the bias current required from bias source 30 may be reduced and power consumption optimized. Increasing the value of resistor 28 will accomplish a reduction in the bias current level.

Under current limiting or short circuit load conditions, regulation transistors 20 and 21 in conjunction with current sensing resistor 29 operate to regulate the output current. Transistor 20 may, for instance, be designed to have a larger area than transistor 21 and initially will conduct a larger amount of current. Transistors 46 and 47 provide a source of current to the collectors of transistors 20 and 21 which operate to increase feedback loop gain and circuit response time. As the voltage drop across current sensing resistor 29 increases, transistor 21 conducts greater amounts of current and diverts base drive from the positive feedback loop described above. As a result, current is limited to a desirable level.

The operation of control transistors 22 and 23 to enable circuit 10 is the same as described in the description of the preferred embodiment of Figure 3 and will not be repeated. It is noted that again it is not necessary to apply a source of current to control terminal 42 to disable the driver circuit and standby current is minimal. Furthermore, current supplied from the collector 34 of transistor 11 is available to assist in driving the base of transistor 22 in the event that it is desirable to turn the driving circuit off from a conducting condition.

Claims

1. A circuit for controlling the current fed to a load device through the circuit, comprising
 - first and second terminals (40,41) from one to the other of which the controlled current flows,
 - a regulating circuit comprising first (11) and second (12,13) current-mirror circuits connected respectively to said first and second terminals (40,41) and having the current-input conductor of each current mirror circuit connected to the current-output conductor of the other current-mirror circuit, with a resistor (29) connected in the emitter circuit of a transistor (12) providing the current-output of the second current-mirror circuit (12,13), and
 - a start-up circuit (14,15,30) connected to supply an initiating current to the regulating circuit,
 - characterised in that the circuit includes
 - a driving transistor (17) having a controlled current path and a control electrode, and
 - a pre-drive transistor (18) having one electrode coupled by an output circuit to the control electrode of the driving transistor (17), a base and another electrode connected to the second terminal, the base of the pre-drive transistor (18) being connected to a base connection of the transistors (12,13) forming the second current-mirror and to receive the initiating

current from the start-up circuit (14,15,30),

the controlled current path of the driving transistor (17) being connected from the first terminal (40) to the resistor (29) so that the controlled current through the transistor (17) flows through the resistor to the second terminal (41), the first current mirror circuit (11) having a second current-output conductor (32) connected to the base of a control transistor (22) that controls the base current fed to the pre-drive transistor (18) and thereby the conductivity of the driving transistor (17) in response to the voltage established across the resistor (29).

2. A circuit according to claim 1, wherein the control transistor (22) is part of a control circuit (22,23) having an input (42) for receiving a control signal, the control circuit being coupled to the initiating current output of said start-up circuit, and being effective to turn off said pre-drive (18) and driving (17) transistors when said control signal is at a selected level.

3. A circuit according to claim 1 or 2, wherein said start-up circuit comprises:

a start-up transistor (14) having a collector providing said initiating current to the base of said pre-drive transistor (18) and the common base connection of the transistors (12,13) of the second current mirror, a base coupled to a control terminal (43) for a source (30) of bias current, and an emitter connected to the first terminal (40); and

a bias transistor (15) having a base and a collector connected together and to said control terminal (43), and an emitter connected to the first terminal (40).

4. A circuit according to claim 3 wherein the emitters of the start-up (14) and bias (15) transistors are connected to the first terminal (40) through respective resistors (27,28), the values of which are ratioed to provide a selected initiating current.

5. A circuit according to any one of the preceding claims wherein said regulating circuit comprises:

as the first current mirror circuit a current splitter transistor (11) having an emitter connected to the first terminal (40), first and second collectors for providing equal collector current levels, and a base connected to the first collector; and as the second current mirror circuit a first drive regulation transistor (12) having a collector coupled to said first collector of the current splitter transistor (11), a base

coupled to said control electrode of said at least one pre-drive transistor (18) and an emitter connected to said second terminal (41) through the resistor (29); and

a second drive regulation transistor (13) having a collector and base coupled to said second collector of the current splitter transistor (11), the base also being coupled to said base of said first drive regulation transistor (12) and an emitter connected directly to said second terminal (41).

6. A circuit according to claim 1, wherein said control transistor (22) is also responsive to a control signal and has a collector connected to the initiating current output of the start-up circuit, the control transistor (22) being rendered conducting when said control signal is at a selected level, so as to divert substantially all of the initiating current from the regulating circuit and the pre-drive transistor (18), the second current output from the first current mirror circuit (11) serving to assist in rendering conductive the control transistor (22).

7. A circuit according to claim 1, wherein

the first current mirror comprises

first, second and third bipolar transistors (11,46,47) having their bases connected together and to a collector of the first transistor (11), and their emitters connected through respective resistors (24,25,26) to the first terminal,

and the second current mirror comprises

fourth, fifth and sixth bipolar transistors (49,20, 21), the emitters of the fourth and fifth transistors (49,20) being connected to the second terminal through the resistor (29), with the emitter of the sixth transistor (21) connected directly to the second terminal, the bases of the fifth and sixth transistors (20,21) being connected together and to the collector of the fifth transistor, and the base of the fourth transistor (49) being connected to the base of the pre-drive transistor (18) and the collector of the sixth transistor (21),

the collector of the first, second and third transistors being respectively connected to the collectors of the fourth, fifth and sixth transistors.

8. A method for controlling the current fed through a circuit to a load device including providing in said circuit two current mirrors, the output current of each of which is fed to the other as an input current, with an emitter resistor (29) in one of the current mirrors, and feeding an initiating current to the current mir-

rors,

characterised in that the method includes providing a driving transistor (17) for producing a controlled current which is passed through the resistor (29) in the current mirrors, and

regulating the current through the driving transistor (17) in response to the sum of the initiating current and a current from one of the current mirrors.

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Patentansprüche

1. Schaltung zur Steuerung des Stromes, der einer Lasteinrichtung durch die Schaltung zugeführt wird, mit

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ersten und zweiten Anschlußklemmen (40, 41), wobei der gesteuerte Strom von einer dieser Klemmen zur anderen fließt,

einer Regelschaltung mit ersten (11) und zweiten (12, 13) Stromspiegelschaltungen, die mit den ersten und zweiten Anschlußklemmen (40, 41) verbunden sind, wobei der Stromeingangsleiter einer jeden Stromspiegelschaltung mit dem Stromausgangsleiter der anderen Stromspiegelschaltung verbunden ist und ein Widerstand (29) in die Emitterschaltung eines Transistors (12) geschaltet ist, der den Ausgangsstrom der zweiten Stromspiegelschaltung (12, 13) liefert, und

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einer Startschaltung (14, 15, 30), die so verschaltet ist, daß sie der Regelschaltung einen Auslösestrom liefert,

dadurch gekennzeichnet, daß die Schaltung folgendes enthält:

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einen Treibertransistor (17) mit einem gesteuerten Stromweg und einer Steuerelektrode, und

einen Vortreibertransistor (18) mit einer Elektrode, die über eine Ausgangsschaltung mit der Steuerelektrode des Treibertransistors (17) gekoppelt ist, einer Basis und einer weiteren Elektrode, die mit der zweiten Anschlußklemme verbunden ist, wobei die Basis des Vortreibertransistors (18) mit einem Basisanschluß der Transistoren (12, 13) verbunden ist, die den zweiten Stromspiegel bilden, und dazu verbunden ist, den. Auslösestrom von der Startschaltung (14, 15, 30) zu empfangen,

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wobei der gesteuerte Stromweg des Treibertransistors (17) von der ersten Anschlußklemme (40) zu dem Widerstand (29) verschaltet ist, so daß der gesteuerte Strom durch den Transistor (17) durch den Widerstand zu der zweiten Anschlußklemme (41) fließt, und wobei die erste Stromspiegelschaltung (11) einen zweiten Stromausgangsleiter (32) aufweist, der mit der Basis des Steuertransistors (22) ver-

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bunden ist, der den Basisstrom steuert, der dem Vortreibertransistor (18) zugeführt wird, und damit die Leitfähigkeit des Treibertransistors (17) in Abhängigkeit von der über dem Widerstand (29) erzeugten Spannung.

2. Schaltung nach Anspruch 1, bei der der Steuertransistor (22) einen Teil einer Steuerschaltung (22, 23) mit einem Eingang (42) für den Empfang eines Steuersignals bildet, wobei die Steuerschaltung mit dem Auslösestromausgang der Startschaltung gekoppelt ist und das Ausschalten des Vortreibertransistors (18) und des Treibertransistors (17) bewirkt, wenn das Steuersignal einen ausgewählten Pegel aufweist.

3. Schaltung nach Anspruch 1 oder 2, bei der die Startschaltung folgendes enthält:

einen Starttransistor (14) mit einem Kollektor, der der Basis des Vortreibertransistors (18) und dem gemeinsamen Basisanschluß der Transistoren (12, 13) des zweiten Stromspiegels den Auslösestrom liefert, einer Basis, die mit einer Steueranschlußklemme (43) für eine Quelle (30) eines Vorstroms gekoppelt ist, und einem Emitter, der mit der ersten Anschlußklemme (40) verbunden ist, und

einen Vorbelastungstransistor (15) mit einer Basis und einem Kollektor, die untereinander sowie mit der Steueranschlußklemme (43) verbunden sind, und mit einem Emitter, der mit der ersten Anschlußklemme (40) verbunden ist.

4. Schaltung nach Anspruch 3, bei der die Emitter des Starttransistors (14) und des Vorbelastungstransistors (15) mit der ersten Anschlußklemme (40) über Widerstände (27, 28) verbunden sind, deren Werte im Verhältnis so gewählt sind, daß ein ausgewählter Auslösestrom geliefert wird.

5. Schaltung nach einem der vorhergehenden Ansprüche, bei der die Regelschaltung folgendes enthält:

als die erste Stromspiegelschaltung einen Stromteilertransistor (11) mit einem Emitter, der mit der ersten Anschlußklemme (40) verbunden ist, ersten und zweiten Kollektoren zum Liefern gleicher Kollektorstrompegel, und einer Basis, die mit dem ersten Kollektor verbunden ist, und als die zweite Stromspiegelschaltung einen ersten Treiberregeltransistor (12) mit einem Kollektor, der mit dem ersten Kollektor des Stromteilertransistors (11) verbunden ist, einer Basis, die mit der Steuerelektrode des wenigstens einen Vortreibertransi-

stors (18) gekoppelt ist, und einem Emitter, der über den Widerstand (29) mit der zweiten Anschlußklemme (41) verbunden ist, und

einen zweiten Treiberregeltransistor (13) mit einem Kollektor und einer Basis, die mit dem zweiten Kollektor des Stromteilertransistors (11) gekoppelt sind, wobei die Basis auch mit der Basis des ersten Treiberregeltransistors (12) gekoppelt ist, und einem Emitter, der unmittelbar mit der zweiten Anschlußklemme (41) verbunden ist.

6. Schaltung nach Anspruch 1, bei der der Steuertransistor (22) auch auf ein Steuersignal anspricht und einen Kollektor besitzt, der mit dem Auslösestromausgang der Startschaltung verbunden ist, wobei der Steuertransistor (22) zum Leiten gebracht wird, wenn das Steuersignal einen ausgewählten Pegel aufweist, so daß im wesentlichen der ganze Auslösestrom von der Regelschaltung und dem Vortreibertransistor (18) abgeleitet wird, wobei der zweite Stromausgang von der ersten Stromspiegelschaltung (11) dazu dient, das Leitendmachen des Steuertransistors (22) zu unterstützen.

7. Schaltung nach Anspruch 1, bei der der erste Stromspiegel folgendes enthält:
erste, zweite und dritte bipolare Transistoren (14, 46, 47), deren Basen untereinander und mit einem Kollektor des ersten Transistors (11) verbunden sind, und deren Emitter über Widerstände (24, 25, 26) mit der ersten Anschlußklemme verbunden sind,

und der zweite Stromspiegel folgendes enthält:

vierte, fünfte und sechste bipolare Transistoren (49, 20, 21), wobei die Emitter der vierten und fünften Transistoren (49, 20) über den Widerstand (29) mit der zweiten Anschlußklemme verbunden sind, der Emitter des sechsten Transistors (21) unmittelbar mit der zweiten Anschlußklemme verbunden ist, die Basen der fünften und sechsten Transistoren (20, 21) untereinander und mit dem Kollektor des fünften Transistors verbunden sind, und die Basis des vierten Transistors (49) mit der Basis des Vortreibertransistors (18) und dem Kollektor des sechsten Transistors (21) verbunden ist,

wobei die Kollektoren des ersten, zweiten und dritten Transistors mit dem Kollektor des vierten, fünften bzw. sechsten Transistors verbunden sind.

8. Verfahren zur Steuerung des Stromes, der über eine Schaltung einer Lasteinrichtung zugeführt wird, bei dem in der Schaltung zwei Stromspiegel vorgesehen werden, deren jewei-

liger Ausgangsstrom dem jeweils anderen Stromspiegel als Eingangsstrom zugeführt wird, wobei ein Emitterwiderstand (29) in einem der Stromspiegel vorgesehen ist, und bei dem den Stromspiegeln ein Auslösestrom zugeführt wird,

dadurch gekennzeichnet, daß das Verfahren folgendes enthält:

Vorsehen eines Treibertransistors (17) zur Erzeugung eines gesteuerten Stromes, der durch den Widerstand (29) in den Stromspiegeln fließt, und

Regeln des Stromes durch den Treibertransistor (17) in Abhängigkeit von der Summe des Auslösestromes und einem Strom von einem der Stromspiegel.

Revendications

1. Circuit pour commander le courant envoyé à un dispositif de charge par l'intermédiaire du circuit, comprenant

une première et une deuxième bornes (40, 41) à partir de l'une vers l'autre desquelles circule le courant commandé,

un circuit de régulation comprenant un premier (11) et un deuxième (12, 13) circuits miroirs de courant reliés respectivement auxdites première et deuxième bornes (40, 41) et ayant le conducteur d'entrée de courant de chaque circuit miroir de courant relié au conducteur de sortie de courant de l'autre circuit miroir de courant, une résistance (29) étant reliée au circuit d'émetteur d'un transistor (12) fournissant la sortie de courant du deuxième circuit miroir de courant (12, 13), et

un circuit d'initialisation (14, 15, 30) branché de manière à fournir un courant d'initialisation au circuit de régulation,

caractérisé en ce que le circuit comprend un transistor d'attaque (17) ayant un trajet de courant commandé et une électrode de commande, et

un transistor d'attaque préalable (18) ayant une électrode reliée par un circuit de sortie à l'électrode de commande du transistor d'attaque (17), une base et une autre électrode reliée à la deuxième borne, la base du transistor d'attaque préalable (18) étant reliée à une connexion de base des transistors (12, 13) formant le deuxième miroir de courant et étant agencée pour recevoir le courant d'initialisation du circuit d'initialisation (14, 15, 30),

le trajet de courant commandé du transistor d'attaque (17) étant relié de la première borne (40) vers la résistance (29), de sorte que le courant commandé dans le transistor (17) circule à travers la résistance vers la deuxième

- borne (41), le premier circuit miroir de courant (11) ayant un deuxième conducteur (32) de sortie de courant relié à la base d'un transistor de commande (22) qui commande le courant de base envoyé au transistor d'attaque préalable (18) et donc la conductivité du transistor d'attaque (17) en réponse à la tension établie aux bornes de la résistance (29). 5
2. Circuit selon la revendication 1, dans lequel le transistor de commande (22) fait partie d'un circuit de commande (22, 23) ayant une entrée (42) pour recevoir un signal de commande, le circuit de commande étant relié à la sortie de courant d'initialisation dudit circuit d'initialisation, et étant conçu pour bloquer lesdits transistors d'attaque préalable (18) et d'attaque (17) quand ledit signal de commande est à un niveau sélectionné. 10 15 20
3. Circuit selon la revendication 1 ou 2, dans lequel ledit circuit d'initialisation comprend :
un transistor d'initialisation (14) ayant un collecteur fournissant ledit courant d'initialisation à la base dudit transistor d'attaque préalable (18) et à la connexion commune des transistors (12, 13) du deuxième miroir de courant, une base reliée à une borne de commande (43) pour une source (30) de courant de polarisation, et un émetteur relié à une première borne (40) ; et 25
un transistor de polarisation (15) ayant une base et un collecteur reliés ensemble et à ladite borne de commande (43), et un émetteur relié à ladite première borne (40). 30 35
4. Circuit selon la revendication 3, dans lequel les émetteurs des transistors d'initialisation (14) et de polarisation (15) sont reliés à la première borne (40) par l'intermédiaire de résistances respectives (27, 28) dont les valeurs ont un rapport déterminé afin de fournir un courant d'initialisation sélectionné. 40
5. Circuit selon l'une quelconque des revendications précédentes, dans lequel ledit circuit de régulation comprend : 45
comme premier circuit miroir de courant, un transistor de séparation de courant (11) ayant un émetteur relié à la première borne (40), un premier et un deuxième collecteurs pour fournir des valeurs égales de courant de collecteur, et une base reliée au premier collecteur ; et comme deuxième circuit miroir de courant, un premier transistor de régulation d'attaque (12) ayant un collecteur relié audit premier collecteur du transistor de séparation de courant (11), une base reliée à ladite élec- 50 55
- trode de commande d'un au moins desdits transistors d'attaque préalable (18) et un émetteur relié à ladite deuxième borne (41) par l'intermédiaire de la résistance (29) ; et
un deuxième transistor de régulation d'attaque (13) ayant un collecteur et une base reliés audit deuxième collecteur du transistor de séparation de courant (11), la base étant aussi reliée à ladite base dudit premier transistor de régulation d'attaque (12), et un émetteur relié directement à ladite deuxième borne (41).
6. Circuit selon la revendication 1, dans lequel ledit transistor de commande (22) est aussi sensible à un signal de commande et possède un collecteur relié à la sortie de courant d'initialisation du circuit d'initialisation, le transistor de commande (22) étant rendu conducteur quand ledit signal de commande est à un niveau sélectionné afin de détourner du circuit de régulation et du transistor d'attaque préalable (18) sensiblement tout le courant d'initialisation, la deuxième sortie de courant du premier circuit miroir de courant (11) contribuant à rendre conducteur le transistor de commande (22).
7. Circuit selon la revendication 1, dans lequel le premier miroir de courant comprend
un premier, un deuxième et un troisième transistors bipolaires (11, 46, 47) ayant leurs bases reliées ensemble et à un collecteur du premier transistor (11), et leurs émetteurs reliés à la première borne par l'intermédiaire de résistances respectives (24, 25, 26),
et le deuxième miroir de courant comprend
un quatrième, un cinquième et un sixième transistors bipolaires (49, 20, 21), les émetteurs des quatrième et cinquième transistors (49, 20) étant reliés à la deuxième borne par l'intermédiaire de la résistance (29), l'émetteur du sixième transistor (21) étant relié directement à la deuxième borne, les bases des cinquième et sixième transistors (20, 21) étant reliées ensemble et au collecteur du cinquième transistor, et la base du quatrième transistor (49) étant reliée à la base du transistor d'attaque préalable (18) et au collecteur du sixième transistor (21),
les collecteurs du premier, deuxième et troisième transistors étant reliés respectivement aux collecteurs des quatrième, cinquième et sixième transistors.
8. Procédé pour commander le courant envoyé à travers un circuit vers un dispositif de charge, comprenant la formation dans ledit circuit de

deux miroirs de courant dont la sortie de courant de chacun d'eux est envoyée à l'autre comme courant d'entrée, avec une résistance d'émetteur (29) dans l'un des miroirs de courant,

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caractérisé en ce que le procédé comprend

la fourniture d'un transistor d'attaque (17) pour produire un courant commandé qui est envoyé par l'intermédiaire de la résistance (29) vers les miroirs de courant, et

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la régulation du courant circulant dans le transistor d'attaque (17) en réponse à la somme du courant d'initialisation et d'un courant provenant de l'un des miroirs de courant.

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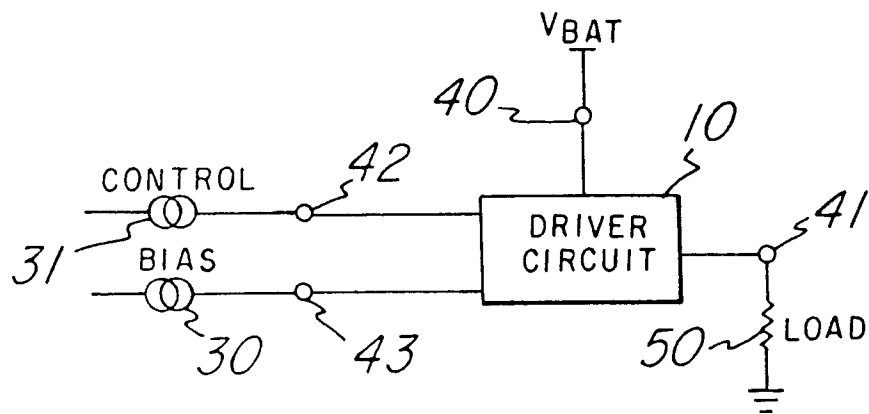


Fig. 1

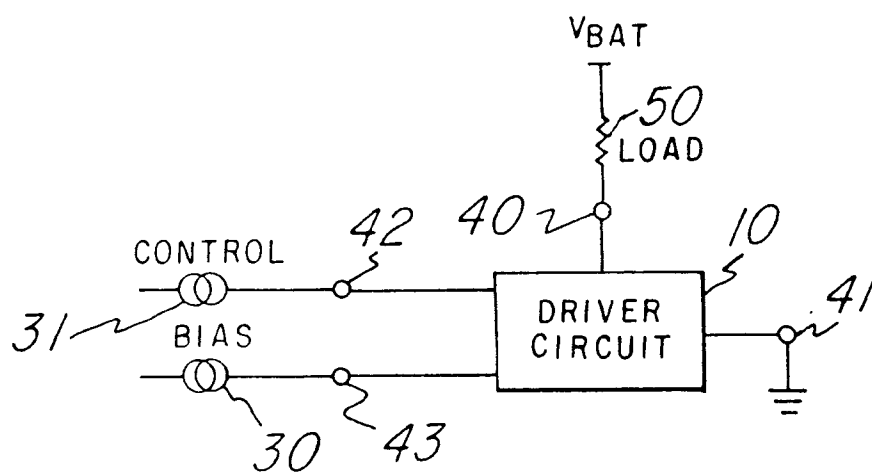


Fig. 2

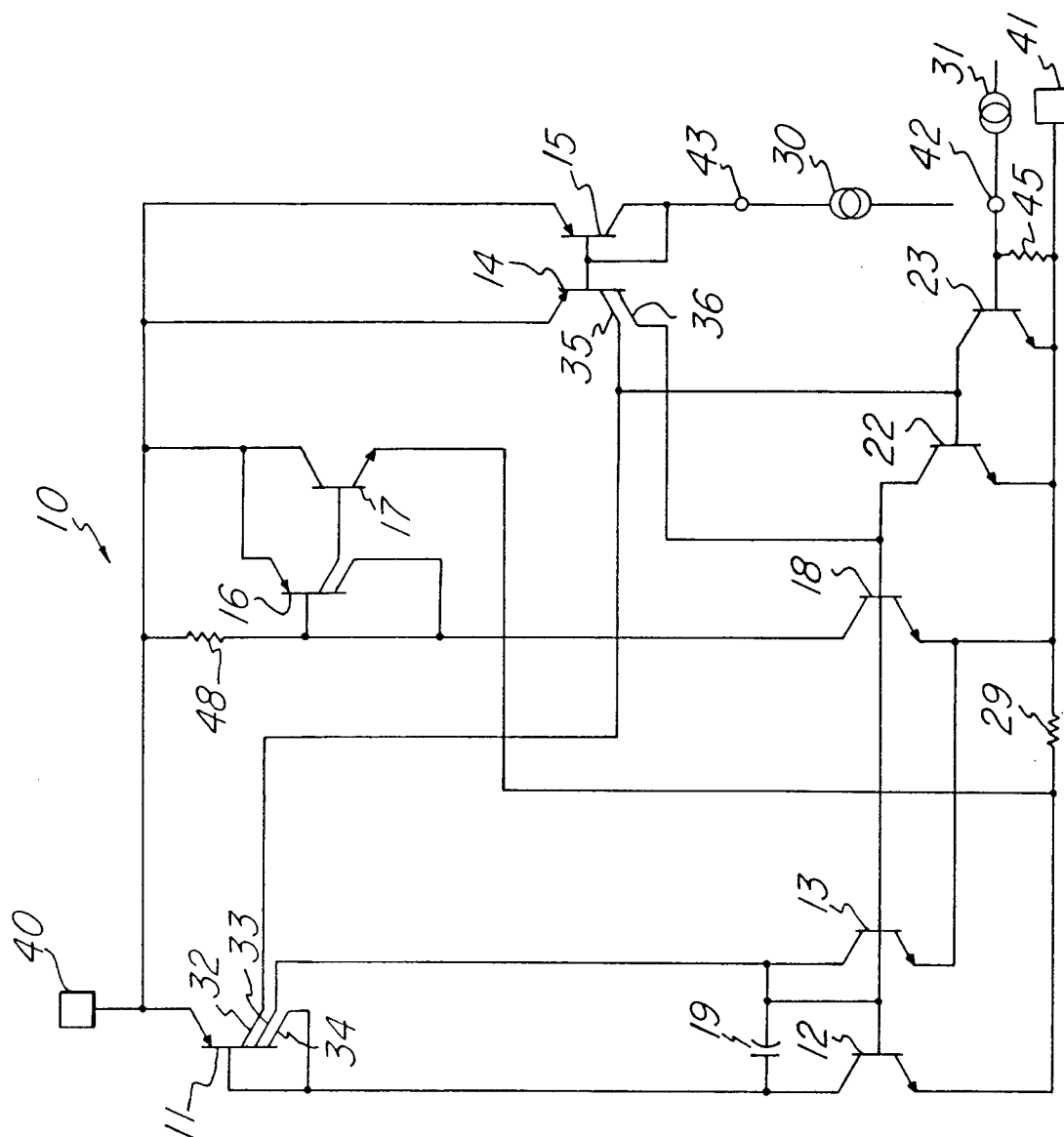


Fig.3

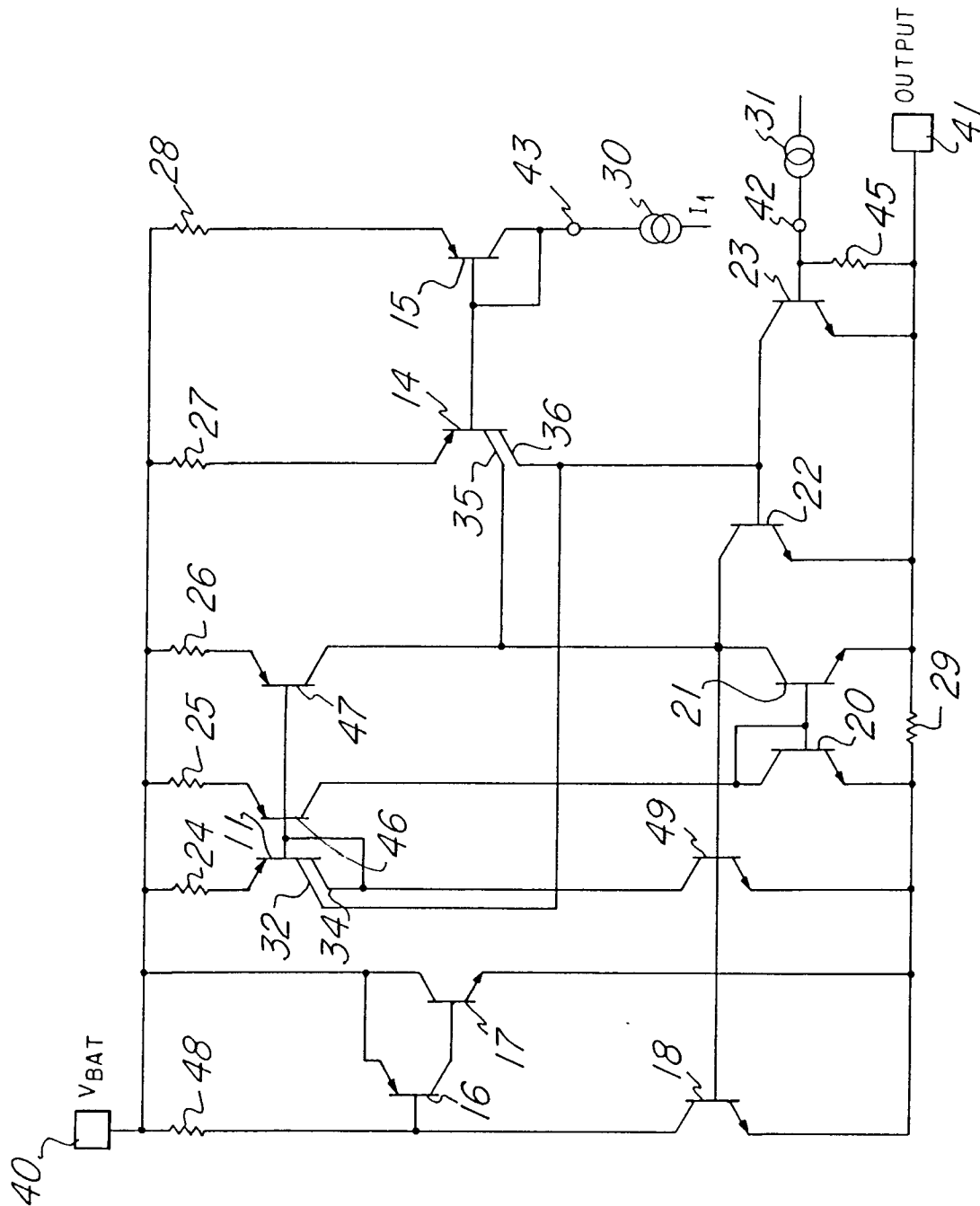


Fig. 4