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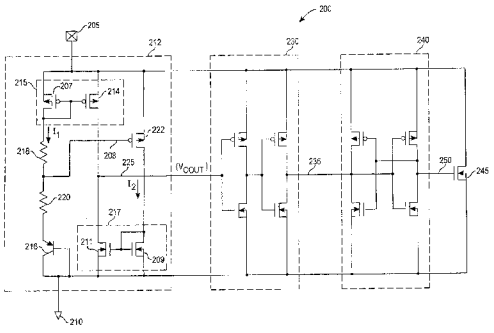

*Fig. 2*

(57) Abstract: Some disclosed embodiments of an electrostatic discharge protection circuit include a shunt device coupled between a power supply terminal and ground to shunt current from the power supply terminal to ground in response to a trigger signal received at an input of the shunt device and a latch coupled to the shunt device input to latch the trigger signal received at a latch input. Some embodiments also include a buffer coupled to the latch input to receive the trigger signal at a buffer input and a comparator coupled between the power supply terminal, ground, and the buffer input to respond to an electrostatic discharge event and produce the trigger signal at a comparator output. In some embodiments the comparator further includes a first current mirror comprising a first sense device coupled to the power supply terminal and a first mirror device coupled between a comparator output and the power supply terminal and a plurality of bias devices coupled to the first sense device, at least two of the plurality of bias devices coupled in series at a bias output line. In some embodiments the comparator further includes a transconductance device comprising an input coupled to the power supply terminal and a control input coupled to the bias output line and a second current mirror comprising a second sense device coupled between the transconductance device and ground and a second mirror device coupled between the comparator output and ground, the second mirror device coupled in series with the first mirror device. In some embodiments the comparator also includes a compensating device coupled between the plurality of bias devices and ground.

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# METHOD AND APPARATUS FOR ESD PROTECTION

## CLAIM OF PRIORITY

**[0001]** Benefit of Priority is hereby claimed to U.S. Patent Application No. 11/759,351, filed June 7, 2007 and entitled "THRESHOLD VOLTAGE METHOD AND APPARATUS FOR ESD PROTECTION", which is incorporated herein by reference in it entirety.

## TECHNICAL FIELD

**[0002]** Electrostatic discharge protection for integrated circuits.

## BACKGROUND ART

**[0003]** It is known in the integrated circuit industry that build up of static charge may lead to development of extremely high voltage near input of an integrated circuit. Electrostatic discharge (ESD) refers to the phenomenon of an electrical discharge of high current over a short duration where the current results from a buildup of static charge on or near the integrated circuit package. ESD is a serious problem for semiconductor devices since it has the potential to destroy the entire integrated circuit.

## BRIEF DESCRIPTION OF DRAWINGS

**[0004]** Fig. 1 is a schematic diagram of a first prior art shunting circuit for ESD protection.

**[0005]** Fig. 2 is a schematic diagram of an embodiment of an ESD event shunting circuit according to the present invention.

**[0006]** Fig. 3 is a current diagram of circuit elements according to Fig. 2.

**[0007]** Fig. 4 is an output voltage diagram of a current comparator according to Fig. 2.

**[0008]** Fig. 5 is a process flow diagram of a method for triggering protection from ESD events utilizing the circuit of Fig. 2.

## DETAILED DESCRIPTION

**[0009]** A method for protecting devices is a clamp circuit that connects to the power supply rails and distinguishes the ESD event from electronic signals propagating during normal applications.

**[0010]** Distinguishing the ESD event from nominal signals is done by a filter with an RC time constant. However, due to this approach to signal differentiation, rapid rise times occur during integrated circuit ESD events. Triggering of the protection clamping circuit may occur either due to rapid power-on conditions or during high current consumption, such as occurs with simultaneously switching outputs (SSO).

**[0011]** With reference to Fig. 1, a series configuration of a trigger capacitor 115 and a trigger resistor 120 connects between a power supply terminal 105 and ground 110 in a prior art ESD protection circuit 100. An ESD inverter 130 and a trigger latch 140 each connect between the power supply terminal 105 and ground 110. An ESD trigger line 125 connects between a series connection node (between the trigger capacitor 115 and the trigger resistor 120) and an input of the ESD inverter 130. A trigger line 135 connects between an output of the ESD inverter 130 and an input of the trigger latch 140. An ESD shunt device 145 connects between the power supply terminal 105 and ground 110. An ESD shunt trigger line 150 connects between an output of the trigger latch 140 and an input of the ESD shunt device 145.

**[0012]** The ESD protection circuit 100 uses an RC time constant to trigger the ESD shunt device 145, but uses the trigger latch 140 to maintain a triggered state of the ESD shunt device 145. Separating the ESD trigger elements (i.e., the trigger capacitor 115, the trigger resistor 120, and the ESD inverter 130) from an element sustaining the ESD trigger state (i.e., the trigger latch 140), means an RC time constant for triggering can be reduced by a factor of 100. Reduction of an RC time constant helps to eliminate risk of an accidental trigger during a rapid (on the order of hundreds of nanoseconds) power-on of a system. RC time constant reduction does not help in differentiating between ESD events with rise times similar to power-on events. An additional benefit of a reduction in an RC time constant is less risk of false triggering during a switching, which produces noise (on an order of

nanoseconds) on the power supply terminal 105 and is caused by simultaneously switching outputs (SSO) .

**[0013]** The ESD protection circuit 100 requires additional timeout circuitry (not shown) which produces a release of the trigger latch 140 typically after a few microseconds delay. A timeout circuit is required to release the trigger latch 140 in cases where false triggering has occurred due to RLC noise generation or IR drop during SSO.

**[0014]** In some embodiments, a triggering mechanism that properly triggers ESD shunting devices yet allows a rapid power-on of a device without a particular requirement for power-on slew rates below a certain minimum. Furthermore, false triggering of the ESD devices should be avoided in some embodiments during SSO events. It is also desirable to have an ESD shunt triggering mechanism, in some embodiments, that is not a function of RC parasitic components and thus avoids any processing variation in these component values as well as the corresponding expense in required chip area.

**[0015]** With reference to the embodiments shown in Fig. 2, a comparator 212 connects between a power supply terminal 205 and ground 210 in an exemplary ESD protection circuit 200. A buffer 230 and a latch 240 each connect between the power supply terminal 205 and ground 210. A comparator output line 225 connects between an output of the comparator 212 and an input of the buffer 230. A trigger line 235 connects between an output of the buffer 230 and an input of the latch 240. A shunt device 245 connects between the power supply terminal 205 and ground 210. A shunt trigger line 250 connects between an output of the latch 240 and an input of the shunt device 245.

**[0016]** The buffer 230 is, for example, a succession of two CMOS inverters in series between the comparator output line 225 and the trigger line 235. The latch 240 is, for example, a cross coupled set of CMOS inverters with a latch input at the trigger line 235 and a latch output coupled to the shut trigger line 250.

**[0017]** In the present exemplary embodiment the comparator 212 comprises a first current mirror 215 coupled between the power supply terminal 205, a first trigger resistor 218, and the comparator output line 225. A second trigger resistor 220 is coupled in series with the first trigger resistor 218 at a bias

output line 208. The second trigger resistor 220 is coupled to a compensating device 216.

**[0018]** The first current mirror 215 has a first sense device 207 coupled between the power supply terminal 205 and the first trigger resistor 218. The first current mirror 215 also has a first mirror device 214 coupled between the power supply terminal 205 and the comparator output line 225. The first sense device 207 and the first mirror device 214 may be, for example, PMOS transistors.

**[0019]** The comparator 212 further comprises a second current mirror 217 with a second sense device 209 coupled between a transconductance device 222 and ground 210. Within the second current mirror 217, a second mirror device 211 is coupled between the comparator output line 225 and ground 210. The second sense device 209 and the second mirror device 211 may be, for example, NMOS transistors.

**[0020]** The compensating device 216 serves as a voltage compensating device where variation in voltage across the compensating device 216 tracks, and thus compensates for, corresponding temperature variation in a threshold voltage of the first sense device 207. The compensating device 216 may be, for example, a bipolar transistor. Implemented as a bipolar transistor, the compensating device 216 couples to ground 210 in a diode configuration (i.e., with a transistor base terminal coupled to ground 210).

**[0021]** The first and second trigger resistors 218,220 are generally incorporated as bias devices. The first trigger resistor 218 may be, for example, 80 kilohms and the second trigger resistors 220 may be, for example, 1.2 megohms. These values are suited to, for example, a 0.18 micrometer (um) technology with a VDD supply voltage level of 3.3 volts (V). Generally, a given magnitude of VDD supply voltage level may affect selection of the values of the first or second trigger resistors 218, 220. One of the first or second trigger resistors 218, 220 being in the megohm range, for example, assures a limited current consumption by the ESD protection circuit during nominal operation (i.e., during non-ESD operation). A plurality of bias devices may be used in various configurations contrived by one skilled in the art to derive a voltage on the bias output line 208 capable of supplying a bias voltage suitable for operating the transconductance device 222.

**[0022]** A skilled artisan may conceive of other solid-state devices, such as field effect transistors, that would suitably equate to the PMOS or NMOS transistors utilized in the first current mirror 215 or the second current mirror 217 respectively. For example, an insulated gate device would be capable of being configured with a gate input connected to a drain node in a first device, for instance a sense device, with an identical device coupled at a gate input forming a mirror device. Other such equivalents may be contemplated by the skilled artisan that would suitably equate to a sense and mirror device.

**[0023]** A transconductance device input is coupled to the power supply terminal 205 and a control input of the transconductance device 222 is coupled to the bias output line 208. An output of the transconductance device 222 couples to the second sense device 209 of the second current mirror 217.

**[0024]** The ESD protection circuit 200 incorporates the comparator 212 to trigger the shunt device 245 and uses the latch 240 to maintain a triggered state of the shunt device 245. The ESD protection circuit 200 does not require additional timeout circuitry to release the latch 240 after a few microseconds delay, which is typically the case where passive components set the latch 240. A timeout circuit is required to release a latch in cases of prior art circuits where false triggering has occurred due to RLC noise generation or IR drop during SSO. In some embodiments, the triggering mechanism provided by the comparator 212 avoid such a requirement.

**[0025]** With reference to Fig. 3, a first sense current $I_1$, (Fig. 2) overlays a second sense current $I_2$ in an exemplary current vs. voltage diagram 300. The abscissa represents an input voltage $V_{IN}$ on the power supply terminal 205. For any extent of the input voltage $V_{IN}$ beyond a magnitude of expected power supply voltage $V_{DD}$, the input voltage $V_{IN}$ may be seen to represent an applied voltage corresponding to an ESD event on the power supply terminal 205. The first sense current $I_1$ increases, for example, essentially linearly from a point where the input voltage $V_{IN}$ is about 0.8 volts (V) through the full range of voltage depicted. The linear characteristic of the first sense current $I_1$ comes from the resistive electrical characteristics of an on-channel resistance within the first current mirror 215, the first trigger resistor 218, and the second trigger resistor 220.

**[0026]** The second sense current $I_2$ increases, for example, in a quadratic fashion from a point where the input voltage $V_{IN}$ is about 0.8 V through the full range of the input voltage $V_{IN}$ depicted. The quadratic characteristic is due to the inherent electrical characteristics of the transconductance device 222. The transconductance device may be, for example, a PMOS transistor operating in a saturation realm. The current characteristic of a PMOS transistor in this realm is a function of the $(V_{GS}-V_{TH})^2$ type of relationship for the device and so follows the quadratic nature of the current behavior versus the input voltage $V_{IN}$ behavior. In addition, the transconductance device may be, for example, a PMOS transistor operating in a linear conduction realm.

**[0027]** In continuing reference to Fig. 3, for the input voltage $V_{IN}$ ranging from 0.8 V to about 4.3 V, a first sense current $I_1$ exceeds a second sense current $I_2$ for the exemplary comparator 212 (Fig. 2). Since the first mirror device 214 of the first current mirror 215 is coupled in series with the second mirror device 211 of the second current mirror 217, the current through each mirror device is equal. The first mirror device 214 produces an incident current and the second mirror device 211 accepts an absorption current.

**[0028]** The incident current is a measure of the propensity of the first sense current $I_1$ to produce a mirror current in the first mirror device 214. Similarly, the absorption current is a measure of the propensity of the second sense current $I_2$ to induce acceptance of a series current through the second mirror device 211. For a given input voltage $V_{IN}$ applied at the power supply terminal 205, the first sense current $I_1$ is not equal to the second sense current $I_2$ (except at a cross over point, which is explained below).

**[0029]** Since the two mirror currents flowing through the series combination of the respective mirror devices 211,214 are equal (since they are the same current), the greater of the two sense currents $I_1$, $I_2$ prevails in producing the resultant series current through the mirror devices 211, 214. This comes about since the (relatively) greater of the two internal mirror voltages (not shown) within each current mirror 215, 217 is in effect producing the lower impedance through a corresponding one of the two mirror devices 211, 214.

**[0030]** Consequently, at a given operating condition of input voltage $V_{IN}$ on the power supply terminal 205, the one of the two current sense devices 207, 209 capable of inducing the greater mirror current has a relatively smaller voltage drop across the corresponding one of the two mirror devices 211, 214. The mirror device with the smaller voltage drop across it determines the series current through the two mirror devices 211, 214. The resulting current flowing through the remaining mirror device sustains a greater voltage drop across the device. This scenario provides the behavior of a voltage on the comparator output line $V_{COUT}$ (Fig. 2).

**[0031]** For a range of input voltage $V_{IN}$ from about 0.8 V to about 4.3 V there is less voltage across the first mirror device 214 than there is across the second mirror device 211. This produces a high output level for the voltage on the comparator output line $V_{COUT}$. With a high level comparator output voltage $V_{COUT}$, a corresponding high voltage level is produced on the trigger line 235 and a low voltage level is produced on the shunt trigger line 250. Therefore, for $V_{IN}$ ranging from 0.8-4.3 V the shunt device 245 is off leaving voltage on the power supply terminal 205 at a nominal supply voltage, for example, VDD. As the input voltage $V_{IN}$ ranges from about 0.8 V to about 4.3 V, for example, $V_{COUT}$ closely approximates $V_{IN}$ in magnitude.

**[0032]** In contrast, for $V_{IN}$ above a magnitude, for example, of 4.3 V, the above characteristics take on complementary relationships since the second mirror device 211 is capable of conducting more current than the first mirror device 214 in this realm. For an increasing magnitude of input voltage $V_{IN}$, a cross over point or a trigger supply voltage (considering that the input voltage $V_{IN}$ is applied to the power supply terminal 205) is defined where the second mirror device 211 begins to be capable of conducting more current than the first mirror device 214.

**[0033]** Therefore, above the trigger supply voltage, the voltage across the second mirror device 211 is less than the voltage across the first mirror devic 214. A condition follows that the comparator output voltage $V_{COUT}$ is at a low level and the shunt device 245 is turned on. With the shunt device 245 turned on, high levels of $V_{IN}$, for example above 4.3 V, the power supply terminal 205

is shunted to ground through the shunt device 245. High levels of $V_{IN}$ that produce the protective shunting effect, produced by the shunt device 245, correspond with elevated voltages like those produced by an ESD event on the power supply terminal 205. That is, the ESD protection circuit 200 produces protection against elevated voltages such as those of an ESD event. The protection is derived from a threshold voltage detection provided by a current comparator.

**[0034]** The characteristics of the first and second sense currents $I_1$, $I_2$ verses input voltage $V_{IN}$ may be complementary to the two instances given. The first sense current $I_1$ may increase, for example, in a quadratic fashion and the second sense current $I_2$ may increase, for example, in an essentially linear fashion. One skilled in the art may readily envision any of a number of types of functional variation of a sense current provided by current sensing devices where a cross over point is present in the combined sense current characteristics.

**[0035]** With reference to Fig. 4, a comparator output voltage $V_{COUT}$ attains a peak value prior to an input voltage $V_{IN}$ attaining a magnitude of 5 V in an exemplary comparator output voltage versus input voltage diagram 400. For $V_{IN}$ ranging from about, for example, 0.8-4.3 V, the shunt device 245 is off leaving voltage on the power supply terminal 205 at a nominal supply voltage, for example, VDD. Therefore, as the input voltage $V_{IN}$ ranges from about 0.8 V to about 4.3 V, for example, $V_{COUT}$ closely approximates $V_{IN}$ in magnitude.

**[0036]** Subsequent to the input voltage $V_{IN}$ attaining a magnitude of about, for example, 4.3 V, the comparator output voltage $V_{COUT}$ reduces to about 0.4 V for the input voltage $V_{IN}$ exceeding about 8 V. Above about the 4.3 V level for $V_{IN}$, the comparator output voltage $V_{COUT}$ is a trigger signal or ESD trigger voltage capable of causing the ESD protection circuit 200 (Fig. 2) to activate the shunt device 245. For $V_{IN}$ below about the 4.3 V level, and since $V_{COUT}$ closely approximates $V_{IN}$ for $V_{IN}$ ranging from about 0.8 V to about 4.3 V, $V_{COUT}$ does not vary from $V_{IN}$ enough to cause a trigger signal on the shunt trigger line 250.

**[0037]** With reference to Fig. 5, applying an electrostatic discharge to a power supply terminal 505 is a first step in some embodiments of a method of

protecting a device from electrostatic discharge 500. A next step is sensing a first sense current flowing through a first sense device 510 followed by a step of producing a mirror current through a first mirror device 515. A continuing step is producing a bias voltage from the first sense current 520 followed by a step of sensing a second sense current flowing through a second sense device 525. A subsequent step is accepting the first sense current through a second mirror device 530 and next producing a trigger signal at an output of the current comparator 535. A next step is taken of activating a shunt device coupled between the power supply terminal and ground 540 followed by shunting current from the electrostatic discharge to ground 545.

OVERVIEW

**[0038]** In Example 1, an electrostatic discharge protection circuit includes a shunt device coupled between a power supply terminal and ground to shunt current from the power supply terminal to ground in response to a trigger signal received at an input of the shunt device. The circuit also includes a latch coupled to the shunt device input to latch the trigger signal received at a latch input and a buffer coupled to the latch input to receive the trigger signal at a buffer input. The circuit also includes a comparator coupled between the power supply terminal, ground, and the buffer input to respond to an electrostatic discharge event and produce the trigger signal at a comparator output. The comparator additionally includes a first current mirror comprising a first sense device coupled to the power supply terminal and a first mirror device coupled between a comparator output and the power supply terminal and a plurality of bias devices coupled to the first sense device, at least two of the plurality of bias devices coupled in series at a bias output line. The comparator also includes a transconductance device comprising an input coupled to the power supply terminal and a control input coupled to the bias output line. The comparator further includes a second current mirror comprising a second sense device coupled between the transconductance device and ground and a second mirror device coupled between the comparator output and ground, the second mirror device coupled in series with the first mirror device. The comparator further includes a compensating device coupled between the plurality of bias devices and ground.

**[0039]** In Example 2, the electrostatic discharge protection circuit of Example 1 is optionally configured such that the plurality of bias devices is to produce a bias voltage on the bias output line proportionate to a first sense current flowing through the first sense device and the plurality of bias devices, the bias voltage to determine a second sense current flowing through the transconductance device.

**[0040]** In Example 3, the electrostatic discharge protection circuit of Examples 1 or 2 is optionally configured such that the comparator is to produce the trigger signal at the comparator output based on a current flowing through the first mirror device and the second mirror device.

**[0041]** In Example 4, the electrostatic discharge protection circuit of any of Examples 1 – 3 is optionally configured such that a resultant current through the series coupled mirror devices activates the trigger signal.

**[0042]** In Example 5, the electrostatic discharge protection circuit of any of Examples 1- 4 is optionally configured such that wherein the first mirror device is to produce an incident current and the second mirror device is to accept an absorption current.

**[0043]** In Example 6, the electrostatic discharge protection circuit of any of Examples 1- 5 is optionally configured such that the series coupling of mirror devices is to produce a resultant current equal to the greater of an incident current flowing through the first mirror device or an absorption current flowing through the second mirror device.

**[0044]** In Example 7, the electrostatic discharge protection circuit of any of Examples 1-6 is optionally configured such that the trigger signal is activated when the absorption current is greater than the incident current.

**[0045]** In Example 8, the electrostatic discharge protection circuit of any of Examples 1-7 is optionally configured such that a first sense current through the first sense device produces an incident current through the first mirror device and a second sense current through the second sense device produces an absorption current through the second mirror device.

**[0046]** In Example 9, the electrostatic discharge protection circuit of any of Examples 1-8 is optionally configured such that the first mirror device is to produce an incident current less than an absorption current through the second mirror device with a supply voltage on the power supply terminal equal to or

greater than a trigger supply voltage, the absorption current exceeding the incident current producing the trigger signal at the comparator output activating the shunt device.

**[0047]** In Example 10, the electrostatic discharge protection circuit of any of Examples 1-9 is optionally configured such that the compensating device is to compensate a temperature dependent variation of a threshold voltage of the first sense device, the compensating device is to provide a voltage drop across the compensating device corresponding to the voltage drop across the first sense device due to temperature variation.

**[0048]** In Example 11, an electrostatic discharge protection circuit includes a means for shunting coupled between a power supply terminal and ground. The circuit also includes a means for retaining a logic signal level, the retaining means coupled to the shunting means and a means for buffering coupled to the retaining means. The cicuit further includes a means for triggering coupled to the buffering means and a means for detecting coupled to the triggering means, the detecting means further comprising a first and second means for mirroring a current and a plurality of means for biasing.

**[0049]** In Example 12, the electrostatic discharge protection circuit of Example 11 is optionally configured such that the second means for mirroring is coupled between the means for triggering and ground.

**[0050]** In Example 13, the electrostatic discharge protection circuit of Example 11 or Example 12 is optionally configured such that the means for triggering includes a compensating device coupled between the plurality of means for biasing and ground.

**[0051]** In Example 14, the electrostatic discharge protection circuit of any of Examples 11-13 is optionally configured such that the first means for mirroring and the second means for mirroring are connected in series.

**[0052]** In Example 15, a method of protecting a device from electrostatic discharge includes applying an electrostatic discharge to a power supply terminal coupled to a current comparator. The method also includes sensing a first sense current flowing through a first sense device of a first current mirror and producing a mirror current through a first mirror device of the first current mirror. The method further includes producing a bias voltage from the first sense current flowing through a plurality of bias devices and sensing a second

sense current flowing through a second sense device of a second current mirror. The method also includes accepting the first sense current through a second mirror device of the second current mirror and producing a trigger signal at an output of the current comparator.

**[0053]** In Example 16, the method of Example 15 optionally further includes activating a shunt device coupled between the power supply terminal and ground. The method further includes shunting current from the electrostatic discharge to ground.

**[0054]** In Example 17. (New) The electrostatic discharge protection circuit of Example 15 or 16 is optionally further configured such that the means for triggering includes a transconductance device comprising an input coupled to the power supply terminal and a control input coupled to the bias output line.

**[0055]** In Example 18, the electrostatic discharge protection circuit any of Examples 15 - 17 is optionally further configured such that the second means for mirroring comprises a second sense device coupled between the transconductance device and ground.

**[0056]** In Example 19, an electrostatic discharge protection method includes applying an electrostatic discharge to a power supply terminal coupled to a current comparator. The method further includes filtering small current spikes during switching using an RC time constant at an input of the comparator and latching the output of the comparator. The method also includes activating a shunt device based on the latched value.

**[0057]** In Example 20, the method of Example 19 optionally further provides that latching includes buffering the value between the comparator and shunt device.

**[0058]** In Example 21, the method of Example 19 or 20 optionally further provides that latching includes incorporating a timeout circuit to release the latch during latch up caused by RLC noise generation.

**[0059]** In Example 22, the method of any of Examples 19 - 21 optionally further provides of sizing the resistors' RC time constant to compensate for various power supply voltages and process considerations.

**[0060]** In Example 23, the method of any of Examples 19 - 22 optionally further provides that filtering includes adding a compensating device at the input to lessen temperature variations.

**[0061]** In Example 24, the method of any of Examples 19 - 23 optionally further provides that applying includes comparing an incident current with a reference current to detect an electrostatic discharge.

**[0062]** It is to be understood that the above description is intended to be illustrative, and not restrictive. For example, the above-described embodiments (and/or aspects thereof) may be used in combination with each other. Many other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled. In the appended claims, the terms "including" and "in which" are used as the plain-English equivalents of the respective terms "comprising" and "wherein." Also, in the following claims, the terms "including" and "comprising" are open-ended, that is, a system, device, article, or process that includes elements in addition to those listed after such a term in a claim are still deemed to fall within the scope of that claim. Moreover, in the following claims, the terms "first," "second," and "third," etc. are used merely as labels, and are not intended to impose numerical requirements on their objects.

**[0063]** The Abstract is provided to comply with 37 C.F.R. §1.72(b), which requires that it allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. Also, in the above Detailed Description, various features may be grouped together to streamline the disclosure. This should not be interpreted as intending that an unclaimed disclosed feature is essential to any claim. Rather, inventive subject matter may lie in less than all features of a particular disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

Claims

1. An electrostatic discharge protection circuit, comprising:

a shunt device coupled between a power supply terminal and ground to shunt current from the power supply terminal to ground in response to a trigger signal received at an input of the shunt device;

a latch coupled to the shunt device input to latch the trigger signal received at a latch input;

a buffer coupled to the latch input to receive the trigger signal at a buffer input; and

a comparator coupled between the power supply terminal, ground, and the buffer input to respond to an electrostatic discharge event and produce the trigger signal at a comparator output, the comparator further comprising:

a first current mirror comprising a first sense device coupled to the power supply terminal and a first mirror device coupled between a comparator output and the power supply terminal;

a plurality of bias devices coupled to the first sense device, at least two of the plurality of bias devices coupled in series at a bias output line;

a transconductance device comprising an input coupled to the power supply terminal and a control input coupled to the bias output line;

a second current mirror comprising a second sense device coupled between the transconductance device and ground and a second mirror device coupled between the comparator output and ground, the second mirror device coupled in series with the first mirror device; and

a compensating device coupled between the plurality of bias devices and ground.

2. The electrostatic discharge protection circuit of claim 1, wherein the plurality of bias devices is to produce a bias voltage on the bias output line proportionate to a first sense current flowing through the first sense device and the plurality of bias devices, the bias voltage to determine a second sense current flowing through the transconductance device.

3. The electrostatic discharge protection circuit of claims 1 or 2, wherein the comparator is to produce the trigger signal at the comparator output based on a current flowing through the first mirror device and the second mirror device.

4. The electrostatic discharge protection circuit of any of claims 1 – 3, wherein a resultant current through the series coupled mirror devices activates the trigger signal.

5. The electrostatic discharge protection circuit of any of claims 1- 4, wherein the first mirror device is to produce an incident current and the second mirror device is to accept an absorption current.

6. The electrostatic discharge protection circuit of any of claims 1- 5, wherein the series coupling of mirror devices is to produce a resultant current equal to the greater of an incident current flowing through the first mirror device or an absorption current flowing through the second mirror device.

7. The electrostatic discharge protection circuit of any of claims 1-6, wherein the trigger signal is activated when the absorption current is greater than the incident current.

8. The electrostatic discharge protection circuit of any of claims 1-7, wherein a first sense current through the first sense device produces an incident current through the first mirror device and a second sense current through the second sense device produces an absorption current through the second mirror device.

9. The electrostatic discharge protection circuit of any of claims 1-8, wherein the first mirror device is to produce an incident current less than an absorption current through the second mirror device with a supply voltage on the power supply terminal equal to or greater than a trigger supply voltage, the absorption current exceeding the incident current producing the trigger signal at the comparator output activating the shunt device.

10. The electrostatic discharge protection circuit of any of claims 1-9, wherein the compensating device is to compensate a temperature dependent variation of a threshold voltage of the first sense device, the compensating device is to provide a voltage drop across the compensating device corresponding to the voltage drop across the first sense device due to temperature variation.

11. An electrostatic discharge protection circuit comprising:

a means for shunting coupled between a power supply terminal and ground;

a means for retaining a logic signal level, the retaining means coupled to the shunting means;

a means for buffering coupled to the retaining means;

a means for triggering coupled to the buffering means; and

a means for detecting coupled to the triggering means, the detecting means further comprising a first and second means for mirroring a current and a plurality of means for biasing.

12. The electrostatic discharge protection circuit of claim 11, wherein the second means for mirroring is coupled between the means for triggering and ground.

13. The electrostatic discharge protection circuit of claim 11 or claim 12, wherein the means for triggering includes a compensating device coupled between the plurality of means for biasing and ground.

14. The electrostatic discharge protection circuit of any of claims 11-13, wherein the first means for mirroring and the second means for mirroring are connected in series.

15. A method of protecting a device from electrostatic discharge, the method comprising:

applying an electrostatic discharge to a power supply terminal coupled to a current comparator;

sensing a first sense current flowing through a first sense device of a first current mirror;

producing a mirror current through a first mirror device of the first current mirror;

producing a bias voltage from the first sense current flowing through a plurality of bias devices;

sensing a second sense current flowing through a second sense device of a second current mirror;

accepting the first sense current through a second mirror device of the second current mirror; and

producing a trigger signal at an output of the current comparator.

16. The method of claim 15, further comprising:

activating a shunt device coupled between the power supply terminal and ground; and

shunting current from the electrostatic discharge to ground.

17. The electrostatic discharge protection circuit of claim 15 or 16, wherein the means for triggering includes a transconductance device comprising an input coupled to the power supply terminal and a control input coupled to the bias output line.

18. The electrostatic discharge protection circuit any of claims 15 - 17, wherein the second means for mirroring comprises a second sense device coupled between the transconductance device and ground.

19. An electrostatic discharge protection method, comprising:

applying an electrostatic discharge to a power supply terminal coupled to a current comparator;

filtering small current spikes during switching using an RC time constant at an input of the comparator;

latching the output of the comparator; and

activating a shunt device based on the latched value.

20. The method of claim 19, wherein in latching includes buffering the value between the comparator and shunt device.

21. The method of claim 19 or 20, wherein latching comprises incorporating a timeout circuit to release the latch during latch up caused by RLC noise generation.

22. The method of any of claims 19 - 21, further comprising sizing the resistors' RC time constant to compensate for various power supply voltages and process considerations.

23. The method of any of claims 19 - 22, wherein filtering comprises adding a compensating device at the input to lessen temperature variations.

24. The method of any of claims 19 - 23, wherein applying comprises comparing an incident current with a reference current to detect an electrostatic discharge.

25. The method of any of claims 19 - 24, wherein activating comprises activating a shunt device sized device to compensate for different power supply voltages.

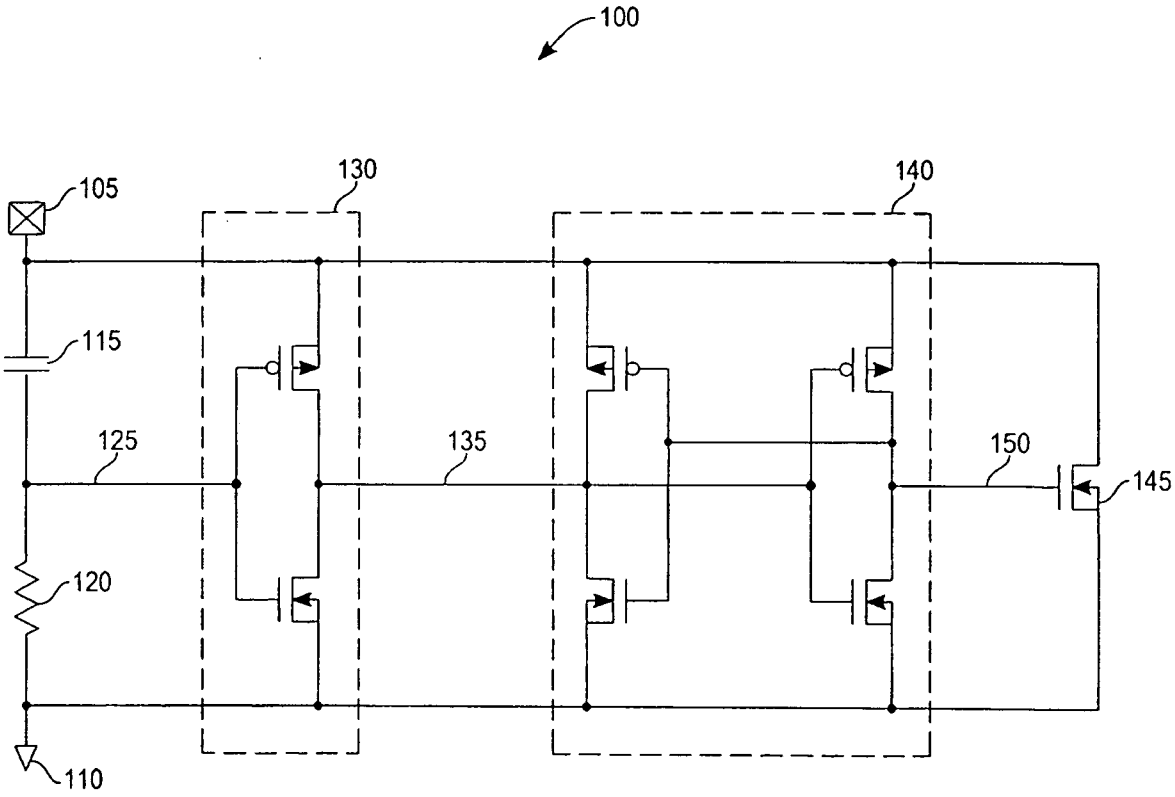
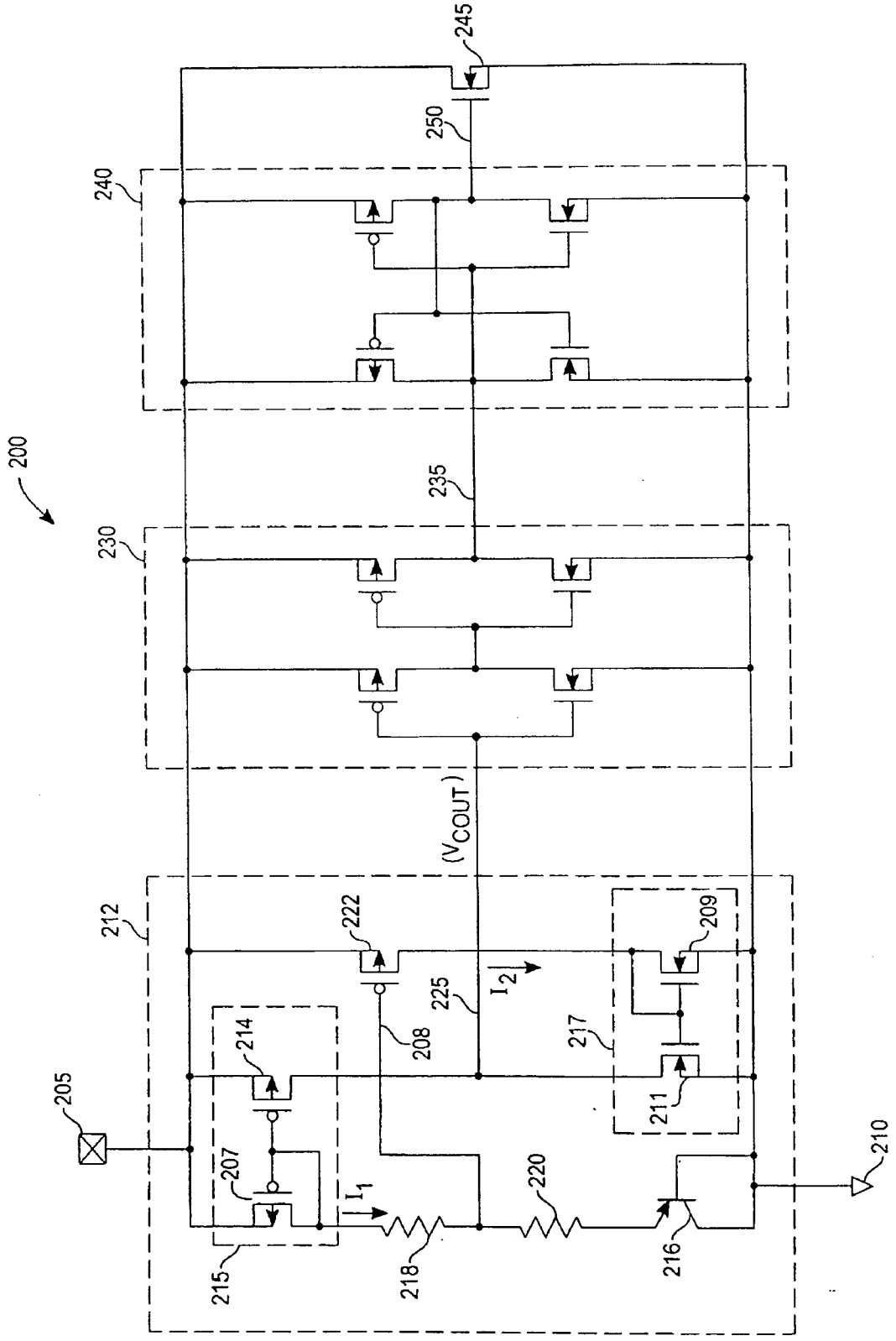



*Fig._ 1 (Prior Art)*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250
245
$I_1$
$I_2$
$(V_{COUT})$

Fig. 2

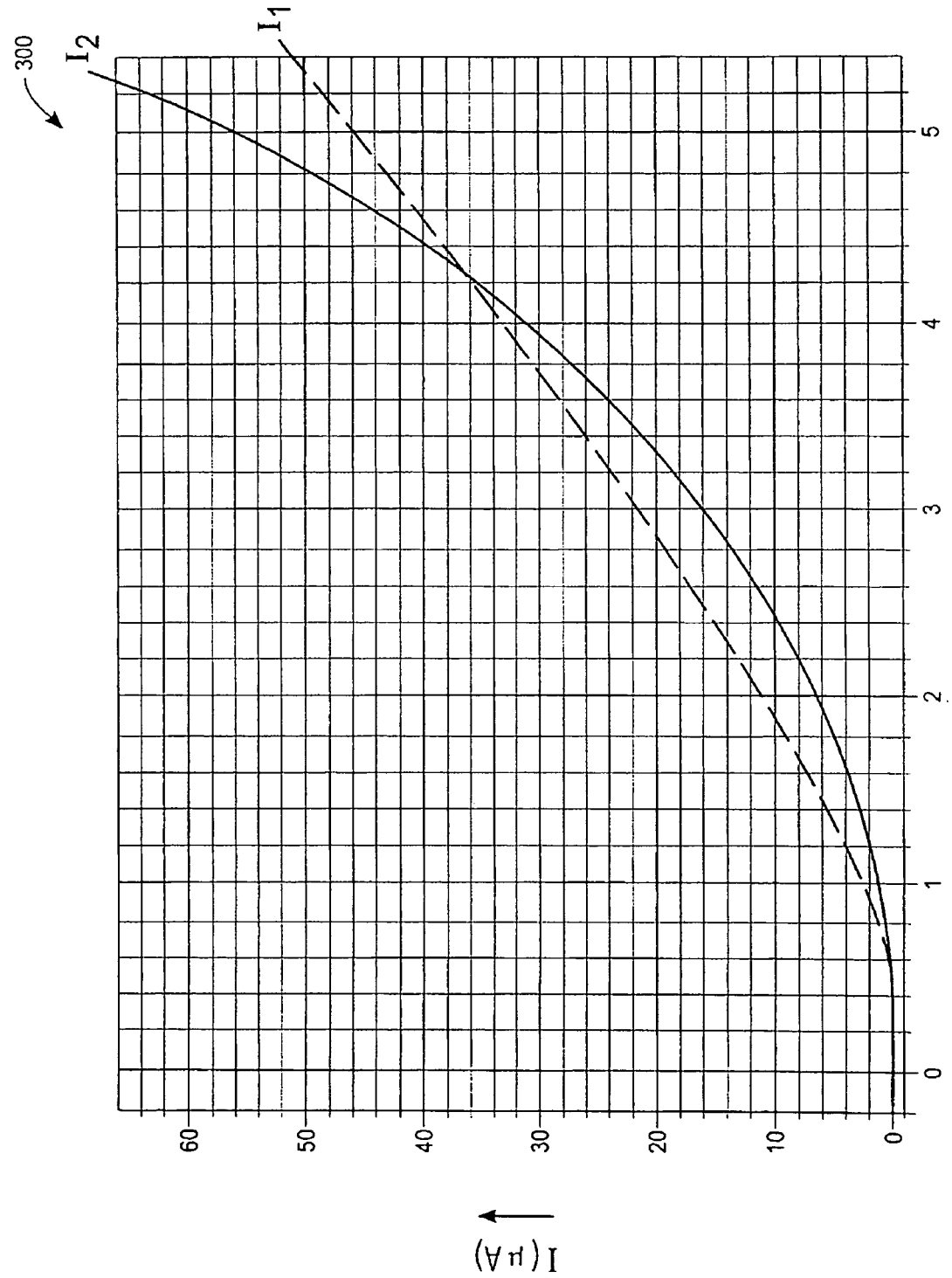


Fig. 3

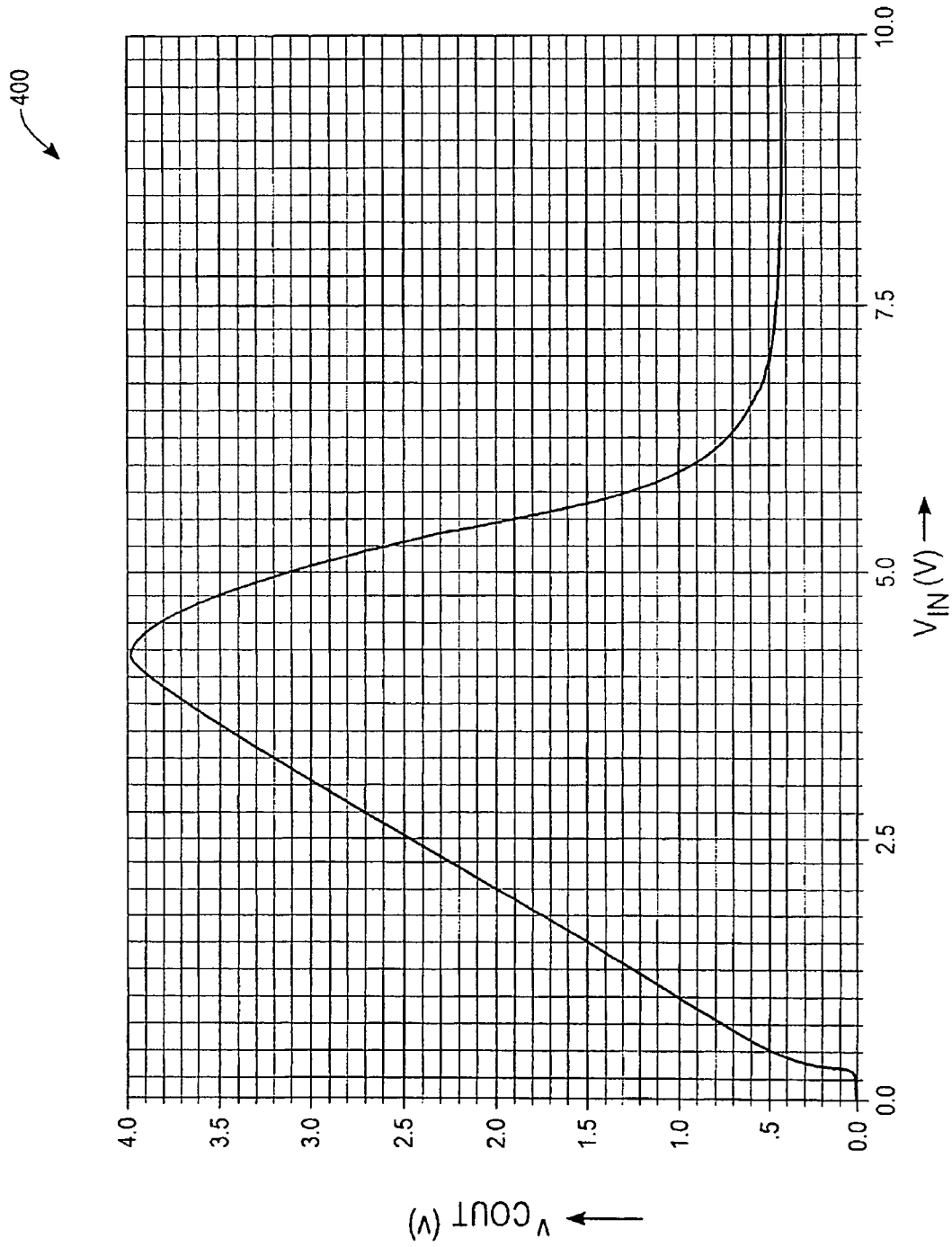


Fig. 4

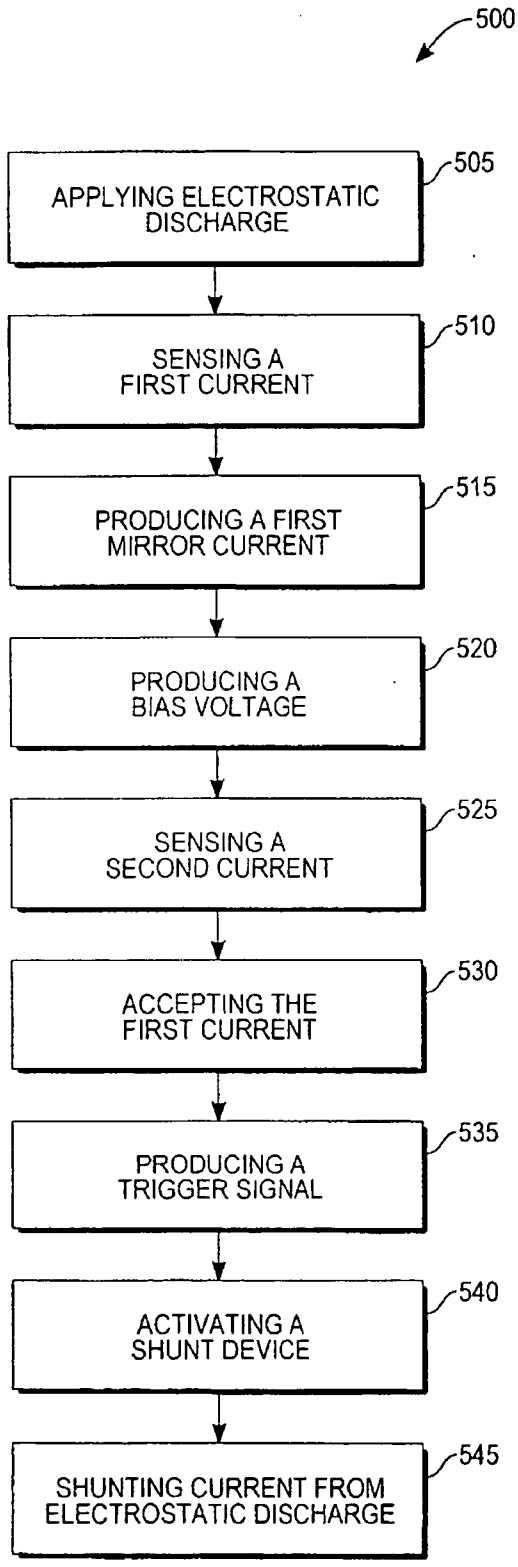
500
APPLYING ELECTROSTATIC DISCHARGE
505
SENSING A FIRST CURRENT
510
PRODUCING A FIRST MIRROR CURRENT
515
PRODUCING A BIAS VOLTAGE
520
SENSING A SECOND CURRENT
525
ACCEPTING THE FIRST CURRENT
530
PRODUCING A TRIGGER SIGNAL
535
ACTIVATING A SHUNT DEVICE
540
SHUNTING CURRENT FROM ELECTROSTATIC DISCHARGE
545

*Fig. 5*

# INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/007162

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K19/003

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br>A | US 5 483 406 A (BENNETT PAUL T [US] ET AL) 9 January 1996 (1996-01-09)<br>the whole document | 15<br>1,11,19 |
| A | US 4 659 944 A (MILLER SR JAMES A [US] ET AL) 21 April 1987 (1987-04-21)<br>the whole document | 1-25 |
| A | GB 2 427 768 A (AVAGO TECHNOLOGIES ECBU IP [SG]) 3 January 2007 (2007-01-03)<br>figures 2-5 | 1-25 |
| A | US 2002/131221 A1 (LIEN CHUEN-DER [US] ET AL) 19 September 2002 (2002-09-19)<br>figure 6 | 1-25 |
| A | US 5 319 259 A (MERRILL RICHARD B [US])<br>7 June 1994 (1994-06-07)<br>figure 11 | 1-25 |

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 20 October 2008 | 12/11/2008 |

| Name and mailing address of the ISA/ | Authorized officer |
|---|---|
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