

[54] **DISPLAY APPARATUS**

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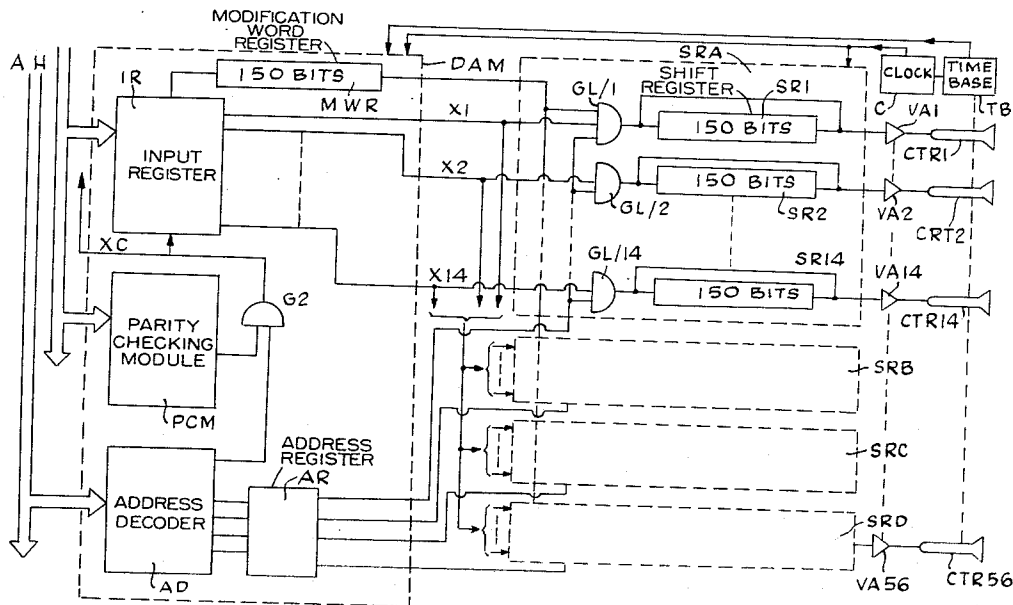
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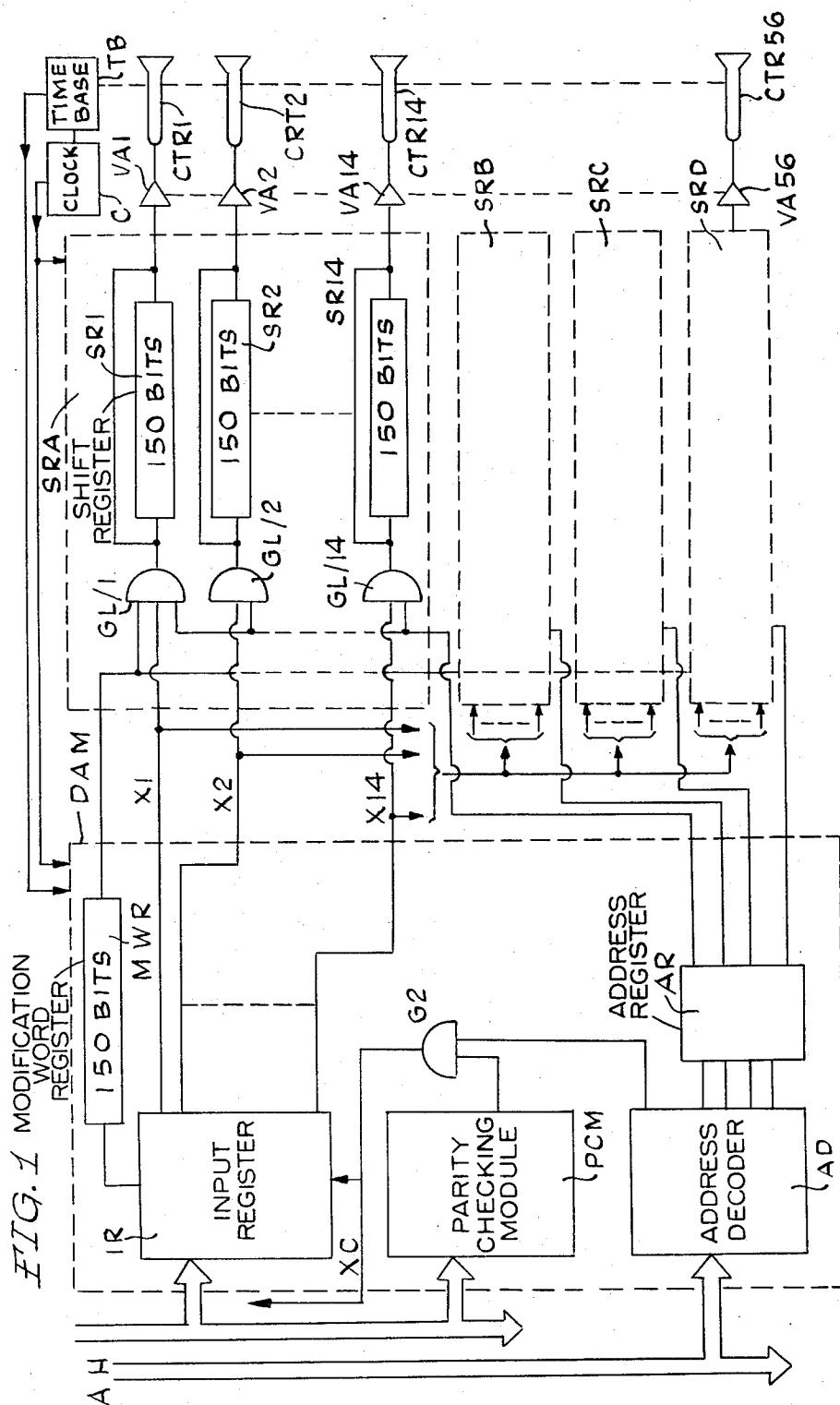
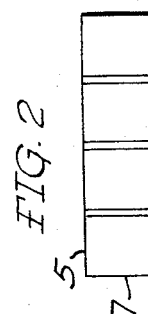
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[57] **ABSTRACT**

A train describer display apparatus displays train description information as a bright-up pattern of alphanumeric characters on the rasters of small cathode ray tubes by stepping a shift register operating with serial read-out in synchronism with the scanning circuits of the cathode ray tubes. The displayed data is changed by applying new information to a selected shift register from a store which is filled from a data highway the data highway also operating in conjunction with an address highway to determine which cathode ray tube out of a selected group of cathode ray tubes is to receive a modified display.

3 Claims, 2 Drawing Figures





DISPLAY APPARATUS

This invention relates to display apparatus and relates more especially to train describer display apparatus employing cathode ray tubes for displaying legible characters.

Train description apparatus is normally operable to present to an operator at a control panel representations of details of trains present in a railway track system represented by a track diagram of the area supervised by the operator. The track diagram is normally provided with such signal control switches and route setting and indication facilities as are required for the purposes of system control.

In response to received coded information concerning the states or conditions of operation of various portions of a railway track system, a computer may be provided to operate to apply to various ancillary functions via suitable data and address highways, coded output information concerning indications to be displayed or functions to be performed. These may include point sensing, signal operation, points setting, alarms and teleprinter operations. The indications may include the illumination of signal and points indication lights and track occupancy lights, together with displays of legible characters indicating to an operator details of trains and various positions in a railway territory covered by the system control.

According to the present invention there is provided display apparatus including a plurality of concomitantly scannable display units upon which characters are displayable the characters being formed by the presence or absence of excitation (such as bright-up signals) in allotted discrete positions, a plurality of groups of main storage means, one such means for each display device and each said main storage means having a plurality of data storage locations for storing "bits" representing the desired excitation of corresponding positions of the respective display unit and the main storage means being provided with means for operating them in synchronism with the respective display means to present the appropriate bits in sequence to the display means, the apparatus also including for generating the bits in the main storage means a shift register and an input register operable on recognition of a received address code to receive group by group from a data highway groups of bits and in turn to apply said received groups of bits to the shift register and means responsive to a further address code for selecting the group of main storage means which contains a specific main storage means to which bit-contents of the shift register are to be transferred.

Preferably, the means for selecting groups of storage means to which the contents of the shift register is to be applied is responsive to further addressing means and means responsive to further received data bits in the input register for selecting the storage means in a selected group.

In order that the invention may be more clearly understood and readily carried into effect, the same will be further described by way of example with reference to the accompanying drawing of which,

FIG. 1 illustrates in schematic form a cathode ray tube train describer apparatus employing the invention and

FIG. 2 illustrates the format of character display on each cathode ray tube.

Referring to FIG. 1 of the drawing, the apparatus operates to provide displays of four legible characters each of 56 cathode ray tubes CRT1, CRT2 . . . CRT56. These cathode ray tubes are divided into four groups of 14 tubes the first two and the fourteenth of the first group of these tubes and the last of the last group namely the fifty sixth tube are shown. Conventional scanning time base circuits are provided represented by block TB for scanning all the tubes CRT1 to CRT56 concomitantly and cyclicly to display characters in accordance with applied excitation or bright-up signals. The scanning takes place in response to a master clock generator C which also governs the progression of bright-up signals to the display tubes and provides clock pulses to the other parts of the apparatus D and SRA. The scanning of the tubes is such that four characters displayed on each tube are produced five by seven dot patterns arranged side-by-side as indicated by the four frames shown in FIG. 2. The scanning is arranged to operate line-by-line vertically proceeding across the respective displays of the four characters. Thus, the scanning proceeds down one seven-dot line up the next seven-dot line and so on, the time base waveform leaving a space between each display character as also indicated in FIG. 2.

For the purposes of supplying the excitation bright-up signals for the first group of cathode ray tubes CRT1 to CRT14, a first group of commercially available integrated circuit shift registers SR1 to SR14 is provided. Three further such groups SRB, SRC, SRD of shift registers are provided and shown dotted in the drawing, for the three other groups of 14 cathode ray tubes, all the shift registers being operated in step with the master clock. The signals derived from these registers are applied via suitably available video-amplifiers (the first two VA1, VA2 and two others VA14 and VA56 of which are shown) to the respective cathode ray tubes CRT1 to CRT56. The video-amplifiers VA1 to VA56 are typically conveniently provided in circuit modules each of which may comprise 28 amplifiers, the arrangement thus requiring two such modules for the 56 tubes provided.

As shown, the shift registers such as SR1 to SR14 are each provided with cycling paths such that the four display characters on each tube are presented repetitively to produce in known manner a visually continuous display.

For the purposes of establishing or changing the signals in the shift registers SR1 to SR56, there are provided a plurality of gates GL/1 to GL/56 in the input to these shift registers (only GL/1, GL/2 and GL/14 which are shown) via which modified display data for a given tube can be applied to the respective shift register from a modification word register MWR of a display access module DAM. The modification word register derives data bits from an input register IR in module DAM which is arranged when addressed to receive eleven 14-bit words successively in parallel fashion from a 16-bit data highway DH. The first 10 words comprise, as will be explained hereafter, one hundred and 40 modification bits for subsequent serial read-out to the modification word register MWR and the eleventh word of the input register IR has a single suitably positioned bit to indicate on one of output lines X1 to X14 the destination register in the display storage means of one selected group SRA, SRB, SRC or SRD of 14 registers the contents of which is to be modified.

In addition to the 14 bits presented at any given time to the input register IR from the data highway, the remaining two bits positions afford two further bits for the purposes of parity checking of the input 14-bit words to the input register IR. These parity bits are applied from the 16-bit data highway to the parity checking module PCM a check output from which is applied as one control input to a gate G2, the second control input to gate G2 is derived from an address decoder AD connected to the 8-bit address highway AH. The address decoder also has four further address decode outputs to an address register AR the addresses affected by this register AR being the gates G1 to G14, G15 to G28, G29 to G42 and G43 to G56 associated with the respective groups of display storage shift registers referred to above.

In operation of the apparatus shown in FIG. 1, it will be appreciated from the foregoing that four alphanumeric characters can be displayed on each of the 56 cathode ray tubes at one time. Bright-up data for the cathode ray tubes is stored in the 150 bit shift registers SR1 to SR56 and the bits in these registers are shifted one place to the right each time that the cathode ray tube beams are deflected to a new dot position on the screen. The stored pattern in the shift registers is thus shifted along 140 times during the time taken to scan the whole face of a cathode ray tube. The further 10 shifts provided by the one hundred and fifty bit registers do not produce output digits to the respective display tubes but serve to accommodate the time base fly-back time for the tubes. As each bit of the bright-up pattern attains the end of the register it is displaced on the cathode ray tube and returned to the "front" of the register. The re-circulating train description characters in each shift register are thus stored and displayed continuously until, when required, new data is substituted for it.

Whenever the input conditions to the train describer indicate that a movement of a train from one berth to another is required to be displayed the computer which is not shown in arranged to feed the new data to the 16-bit data highway DH and to the address highway AH a code pattern corresponding to the train description group SRA, SRB, SRC or SRD which contains the display data which is to be changed and inserts it into the store associated with the new berth position. The 16-bit words from the computer shared between the input register IR and the parity check module PCM contain, as mentioned above, 14 data bits and two parity checks. The 14 data bits therefore correspond to two vertical columns of a character to be displayed on a given cathode ray tube. The address decoder AD of the display access module DAM answers to a total of five address codes.

The first address indicates to DAM that the data associated with it is part of a train description bright-up pattern and is decoded as an input to G2 whilst the other transmitted one of four addresses is employed to indicate the one group of shift registers, as referred to above, containing the one shift register the contents of which is to be changed.

The individual shift system is indicated by a bit in the data word associated with these other four addresses. In order to up-date a given cathode ray tube display, 14 data words have to be transferred to the data access and modify module DAM accompanied by a first address code A1 to which the module responds to provide

an input to G2, followed by an eleventh word accompanied by one of the other addresses to together determine which display tube of a selected group of 14 cathode ray is to be modified. When the first of the group of words is output from the computer to the module DAM, the parity is checked by the parity check module PCM and if the parity is correct and the appropriate address is received by AD, the data thus checked is gated into the input register IR by an input signal from gate G2, and then shifted serially into the first 14 positions of the 150-bit shift register MWR. The signal from G2 also provides a "data-accepted" signal back to the computer on line KC. The subsequent transfers from the computer to the input register IR occur in a similar fashion and are progressively shifted serially into the modification word register MWR until all 140 bits of new data have been received and stored in MWR. The eleventh word of the group, if its parity is correct, is gated into the input register but not shifted into the shift register. At the same time, the address A2, A3, A4, A5 with which the eleventh word is associated is registered in the address register AR. As indicated above this address along with the single bit eleventh word in IR dictates via the gates GL/1 to GL/56, the shift register out of SR1 to SR56 of which the contents is required to be up-date. As shown in the drawing a connection is shown between the time base unit and DAM. At the commencement of the next complete time base scan of the registers SR1 to SR56, as given by a signal over the said connection the cycling path for the selected 150-bit register is interrupted by gate means (not shown) for the duration of the scan and the bright-up pattern stored in the shift register MWR is transferred serially during this cycle into the appropriate selected shift register. At the end of this particular time base cycle, the cycling path for the selected 150-bit register is reclosed and the display continues to proceed as before, the selected shift register now containing the newer modified display bright-up pattern.

Apparatus embodying the present invention can be constructed in modular form employing integrated circuit storage using techniques which are known of themselves and most failures which may occur may be arranged to result in the loss of the output to one cathode ray display tube only. Other facilities moreover may be visualised by those skilled in the art. For example, in the event that it is required to clear the display on all or a selected number of cathode ray display tubes, the stores SR1 to SR56 may be selected and in one cycle by suitable gating means the contents of the thus selected registers can be cleared. It is not therefore necessary to employ 56 cycles (for example) to clear the 56 stores.

Having thus described our invention what we claim is:

1. Display apparatus including a plurality of concomitantly scannable display units upon which characters are displayable, the characters being formed by the presence or absence of excitation in allotted discrete positions, a plurality of groups of main storage means, one such means being associated with each display device and each said main storage means having a plurality of data storage locations for storing bits representing the desired excitation of corresponding positions of the associated display unit and the main storage means including means for operating said main storage means in synchronism with the associated display means to

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present the appropriate bits in sequence to the display means, the apparatus also including means for generating the bits in the main storage means, a shift register and an input register for responsive to the recognition of a received address code, receiving, group by group from a data highway, groups of bits and for, in turn, applying said received groups of bits to the shift register and means responsive to a further address code for selecting the group of main storage means which contains a specific main storage means to which bit-contents of the shift register are to be transferred.

2. Display apparatus as claimed in claim 1 wherein the said input register includes storage locations for receiving an indentifying code indicative of the main storage means within a group to be selected in response to a said further address and gating means responsive to said indentifying code and the further address for selecting the indicated main storage means to receive data bits from the input register.

3. Display apparatus including a plurality of groups of concomitantly scanable display devices upon which characters are displayable, the characters being

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formed by the presence or absence of excitation signal operable corresponding to allotted positions, a main storage shifting register associated with each said device including a plurality of data bit storage locations for storing bits in the desired excitation pattern, means for stepping the registers in synchronism with scanning of the display units to present the excitation signals, the appropriate sequences to the display means, an input register for receiving up-dating data from a data highway for transfer to a said shift register and a selection code for determining which of the registers of a selected said group is to be selected, an address decoder responsive to an address presented on an address highway for determining which is the selected said group, a modification word register for receiving from the input register successive received words to make up a word to be transferred and gate means responsive to address decoded by the address decoder and a selection code from the input register for transferring a word in the modification word register to the selected main storage shift register.

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