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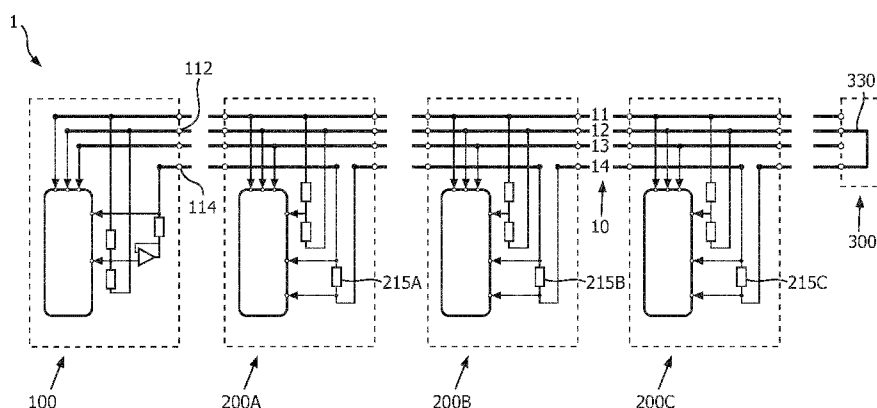
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(54) **Title:** MASTER/SLAVE CONTROL SYSTEM**FIG. 1**

(57) **Abstract:** A master/slave control system (1) comprises a bus (10), a master module (100) and a plurality of slave modules (200), wherein each slave module comprises a measuring resistor (215) and wherein all measuring resistors are connected in series, and wherein each slave module is adapted to measure the voltage drop over the measuring resistor and the voltage potential at one terminal of the measuring resistor and to calculate a unique communication address on the basis of both the voltage drop and the voltage potential measurements.

TITLE: Master/slave control system

FIELD OF THE INVENTION

The present invention relates in general to control systems where a master control device controls a plurality of controllable slave devices connected to a common bus. In a particular field of application, the system is a lighting system, comprising a plurality of near distance lighting units that are controlled by respective slave control units which in turn receive command signals from a central master. In the following, the invention will be specifically explained for such example, but this is not meant to restrict the scope of the invention.

BACKGROUND OF THE INVENTION

The system typically is of a modular nature, and a user can add or remove lighting modules as desired. This means that there is no way for the master to know in advance how many slaves need to be addressed, and there is no way for the master to automatically know the address of each slave in advance.

Further, the lighting modules do not have to be mutually identical. Different lighting modules can have lamps or LEDs of different nature, different intensity, different color, etc. The respective characteristics of the individual lighting modules are not known in advance to the master.

On the other hand, to obtain certain desirable illumination effects, it is desired that the master is capable of issuing individual command signals to the individual slaves. Thus, in an initialization phase, which typically is run each time on power-up of the system, the master must learn these characteristics of the individual lighting modules. This requires that the individual slave devices communicate to the master, telling the master the respective characteristics. With all slaves trying to communicate to the master, there is the problem for the master to distinguish the signals originating from the different slave devices during system power-up.

Further, once the master knows the respective characteristics of the individual lighting modules, so that the master would be capable of issuing the appropriate command signals, there is the problem that the correct slave must respond to the correct signal.

These problems are solved by giving each individual slave a unique communication address code. This address code is used in the command signals, so that each slave will recognize which signal is intended for that specific slave.

There are prior art systems where a user has to set the address manually in each slave. For that purpose, the slaves comprise an address setting member in hardware, typically in the form of a plurality of DIP switches or jumpers. Such is, however, quite inconvenient to the user, because he must set all address setting members in all slaves, making sure that any setting is used only once. Further, if the user wishes later to add one lighting module, he can not just add that module but he first must set the address, and for being able to select a unique communication address the user must first determine the addresses of all existing modules.

EP2007077(A1) discloses each slave having a resistor, multiple slaves forming a series resistor chain, one input voltage is applied from the start resistor to the ground, each slave measures a voltage from its resistor to the ground. Since these resistors are serial connected, this voltage is different for each slave, and these different voltages are used for addressing.

EP1284556A1 discloses a solution in which the potential at each slave unit is used for addressing. And EP2521041A2 discloses a solution in which the current through the slave module is used for addressing.

SUMMARY OF THE INVENTION

In the prior art, the master can not know how many slaves there are, and the master can not know the address of the slaves but must wait for the initiation from each slave to inform its addresses, because the master can not know what the different voltage is in each slave. Each slave must send its initiation to the master thus the initiations are most likely contention-based among these slaves and cost a lot of time. These unintelligent processes slow down the address allocation.

To overcome the above disadvantages and inconveniences, and to provide a lighting system with increased user-experience, an object of the present invention is to provide a master/slave control system with automatic and more sophisticated address allocation.

Instead of using an absolute voltage with respect to the ground or an absolute current, according to the invention, each slave is provided with means for determining its ranking number in the series of slaves via using both a potential on a measuring resistor and the voltage drop across the measuring resistor, such as from a ratio thereof, and this ranking number is taken as initial or temporary address code. This is a step each slave can do individually, and each slave would obtain a unique result. Using this initial address code, the slaves can communicate with the master, and in such communication the master can give the slaves a new, final address, if desired.

Particularly, the present invention provides a master module adapted for use in a master/slave control system, the master module being adapted for coupling to slave modules via a bus;

the master module comprising an auxiliary terminal for connection to an auxiliary bus line of the bus, a voltage source for generating an auxiliary voltage, and a master resistor connected between an output of said voltage source and said auxiliary terminal; and

the master module further comprising a communication terminal for connection to a communication line of the bus, and being adapted to generate at its communication terminal command signals for slave modules connected to such bus, wherein the master module is further adapted to transmit via the communication line instruction data and address data defining an address of an individual slave module, wherein the master module is capable of calculating the number of slaves if the master module comprises first voltage measuring means coupled to a first terminal of the master resistor and measuring a first voltage potential, and second voltage measuring means coupled to an opposite second terminal of the master resistor and measuring a second voltage potential;

wherein the master module is adapted to determine the higher or the lower of the first and second potentials, and to determine the potential difference across the master resistor.

In a further embodiment, the master module is adapted, using the said potential difference and either said higher potential or said lower potential, to calculate a total number of slave modules connected to the bus;

and wherein the master module is adapted, using said total number of slave modules, to calculate each slave's unique communication address.

In this case, For the master device, after it calculated the slave number N , it can proactively send inquiry command with slave address i ($1 \leq i \leq N$) on the bus to collect each slave parameter for control. In a prior art solution, master could not calculate the slave address without slave communication to master, which makes the initiation procedure complicated.

It is also desirable that the slaves know the number of slaves. This information can be communicated to the slaves in an embodiment wherein the master module is adapted to transmit over the communication line of said bus an information message containing digital data indicating the total number of slave modules. In an alternative embodiment, the master module further comprises a referencing terminal for connection to a referencing line of the bus, and wherein the master module is adapted to apply to said referencing line a referencing voltage equal to said auxiliary voltage. In another alternative embodiment, the master module further comprises a referencing terminal for connection to a referencing line of the bus, wherein said

voltage source comprises a voltage divider with a first division ratio, wherein an input of said voltage divider is connected to said referencing terminal for receiving an input voltage higher than said auxiliary voltage, and wherein the master module is adapted to apply an output of said voltage divider to said auxiliary terminal.

Further, the present invention provides a slave module adapted for use in a master/slave control system, the slave module being adapted for coupling to a master module via a bus;

wherein the slave module comprises a measuring resistor adapted for being connected in series in an auxiliary line of the bus to couple to an auxiliary terminal of the master module (100);

wherein the slave module comprises first voltage measuring means coupled to a first terminal of the measuring resistor and measuring a first voltage potential, and second voltage measuring means coupled to an opposite second terminal of the measuring resistor and measuring a second voltage potential;

wherein the slave module is adapted to determine the higher or the lower of the first and second potentials, and to determine the potential difference across the measuring resistor;

and wherein the slave module is adapted, using the said potential difference and either said higher potential or said lower potential, to calculate a unique

communication address for communication over the bus;

said slave module further comprises a communication terminal (213) adapted to couple to a communication terminal of the master module (100) via a communication line (13) and to receive instruction data and address data defining a unique communication address of the slave module.

In this embodiment, the slave could determine its rank position directly without master and other slave address involvement, which decoupled the master and slave device dependency for slave address assignment and configuration.

In a relatively simple embodiment, the slave module is adapted to calculate a ranking number according to either one of the formulas

$$j = V_H/\Delta V \quad \text{or} \quad j = 1 + V_L/\Delta V, \text{ respectively}$$

and to calculate the unique communication address from the calculated ranking number; wherein j indicates the ranking number, V_H indicates said higher potential, V_L indicates said lower potential.

If the slave module is adapted to calculate the unique communication address from the calculated ranking number by multiplying the calculated ranking number by a predetermined integer higher than or equal to 1, the influence of tolerances is reduced.

If the slave module is adapted to receive information representing the total number of slave modules, and wherein each slave module is adapted, before

calculating the unique communication address, to update the calculated ranking number according to the formula

$$1 + (N-j)$$

wherein N indicates the total number of slave modules, the slave nearest to the master will have ranking number 1.

In the prior art, the slave could not calculate its position in related to the master without the master or preceding/following slave involvement, and make the position associated configuration, control etc.. In this embodiment, the slave could determine its position in related to the master directly without master and other slave address involvement, which decoupled the master and slave device dependency for slave address assignment and configuration.

For calculating the total number of slave modules, it is advantageous if the slave module further comprises a referencing terminal for connection to a referencing line of the bus, wherein the slave module is adapted for measuring a referencing voltage at the referencing terminal, and wherein the slave module is adapted to calculate the total number of slave modules by dividing the referencing voltage by the potential difference across the measuring resistor.

Instead of providing the auxiliary voltage directly to the slaves, an embodiment is advantageous in which the slave module further comprises a referencing terminal for connection to a referencing line of the bus, wherein the slave module is adapted to receive at said referencing terminal an input voltage higher than said referencing voltage; wherein the slave module comprises a voltage divider having an input connected to the referencing terminal, the voltage divider having a ratio $\rho = V_a/V_{cc}$, in which V_{cc} indicates the input voltage at the referencing line and in which V_a indicates said referencing voltage; wherein the slave module comprises referencing voltage measuring means coupled to an output of the voltage divider for measuring an output voltage of the voltage divider as the referencing voltage; and wherein the slave module is adapted to calculate the total number of slave modules by dividing the referencing voltage by the potential difference across the measuring resistor.

Further, the present invention provides a master/slave control system comprising a master module and at least one slave module, wherein the master resistor of the master module has a resistance value equal to the resistance value of each of the measuring resistor of the at least one slave module, wherein the auxiliary bus line coupled to the ground after the last slave module and the master module and the slave modules are coupled to the same ground.

In a particularly preferred embodiment, communication is initiated in a relatively simple and reliable manner if each slave module is adapted to send an initiation message containing data representing the slave module's characteristics and the slave module's unique communication address, and wherein the master module is responsive to a received initiation message by sending a response message to the transmitting slave module while using the unique communication address contained in the initiation message.

It is also possible that communication is initiated by the master module, and in such case communication is initiated in a relatively simple and reliable manner if the master module is adapted to send an inquiry message with a unique communication address of one designated slave module, and wherein a slave module is responsive to a received inquiry message by sending a reply message containing data representing the slave module's characteristics and the slave module's unique communication address if that slave module's unique communication address is matching the communication address contained in the received inquiry message.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects, features and advantages of the present invention will be further explained by the following description of one or more preferred embodiments with reference to the drawings, in which same reference numerals indicate same or similar parts, and in which:

figure 1 schematically shows a block diagram of a control system;

figure 2 is a block diagram schematically illustrating a master control module;

figure 3 is a block diagram schematically illustrating a slave control module;

figure 4 is a block diagram schematically illustrating an end module.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 schematically shows a block diagram of a control system 1 according to the present invention. The control system 1 comprises one master control module 100, a plurality of slave control modules 200 which are illustrated as three in figure 1, and an end module 300. The slave control modules may be mutually identical. In the following, the slave control modules will be generally indicated by reference numeral 200, and components of the slave control modules will have reference numerals between 200 and 299. If it is intended to specifically distinguish individual slave

control modules from each other, letters A, B, C, etc. will be added to the reference numerals. It should be noted the number of the slave modules is not limited as three, but one, two or more than three are all applicable.

The control system 1 comprises a bus 10, which comprises a voltage line 11 carrying a first system voltage V_{cc} and a ground line 12 carrying a second system voltage GND. It will be assumed that the second system voltage is actually connected to ground, although that is not essential. In an alternative embodiment, the ground line 12 is removed and each slave module as well as the end module 300 connects to a common ground on their own. It will further be assumed that the first system voltage is higher than the second system voltage, although that also is not essential. For example, the first system voltage can also be a negative voltage.

The bus 10 further comprises a communication line 13 for conveying communication signals, and an auxiliary line 14 whose purpose is providing a daisy chain for addressing each slave and will be explained in detail later.

Figure 3 is a block diagram schematically illustrating a slave control module 200, hereinafter briefly indicated as "slave".

The slave 200 comprises two voltage terminals 211 and 221 connected together.

The slave 200 comprises two ground terminals 212 and 222 connected together.

The slave 200 comprises two communication terminals 213 and 223 connected together.

The slave 200 comprises two auxiliary terminals 214 and 224 connected together via an auxiliary resistor 215, also indicated as measuring resistor.

In use, these terminals are connected to the corresponding terminals of neighbouring slaves via the bus. Here, the word "neighbouring" does not indicate spatial proximity but instead indicates an order along the bus 10. Thus, by connecting an additional slave to a previous slave, the bus 10 is extended. The above applies to all slaves 200, except the "first" slave and the "last" slave. The first slave is the one closest to the master, and the last slave is the one at the end of the bus 10.

Figure 2 is a block diagram schematically illustrating a master control module 100, also briefly indicated as "master". The master 100 comprises a voltage terminal 111, a ground terminal 112, a communication terminal 113, and an auxiliary terminal 114. The master 100 comprises a voltage source or is connected to a voltage source for generating the first system voltage V_{cc} at the voltage terminal 111, which is connected to the voltage terminal 211 of the first slave 200A. Such voltage source is not shown for sake of simplicity. Likewise, the master 100 comprises a second voltage source or is connected to a second voltage source for generating the second system voltage GND at the ground terminal 112, which is connected to the ground

terminal 212 of the first slave 200A. This second voltage source, which also is not shown for sake of simplicity, may in practice typically be a ground connection.

The communication terminal 113 of the master 100 is connected to the communication terminal 213 of the first slave 200A. The auxiliary terminal 114 of the master 100 is connected to the auxiliary terminal 214 of the first slave 200A.

Figure 4 is a block diagram schematically illustrating an end module 300. The end module 300 may be implemented as a cap carrying 4 terminals, i.e. a voltage terminal 311, a ground terminal 312, a communication terminal 313, and an auxiliary terminal 314, for connecting this cap to the terminals 221, 222, 223, 224 of the last slave. The voltage terminal 311 and/or the communication terminal 313 may be omitted. In any case, the end module 300 comprises a connection line 330 connecting the ground terminal 312 and auxiliary terminal 314 together. The end module 300 may also be implemented as a jumper to be placed on the ground and connect to the auxiliary terminals 222, 224 of the last slave.

Referring again to figure 2, the master 100 comprises an auxiliary voltage source 140 for generating an auxiliary voltage V_a which is coupled to the auxiliary terminal 114 of the master 100. In the exemplary embodiment, the auxiliary voltage source 140 comprises a voltage divider 170 connected between the first system voltage V_{cc} and the second system voltage GND. The voltage divider 170 comprises a series arrangement of two resistors 171, 172 having resistance values R_{m0} , R_{m1} , respectively. The node between these two resistors 171, 172 carries a voltage V_0 that meets the formula

$$V_0 = R_{m1}/(R_{m0}+R_{m1}) * V_{cc} \quad (1)$$

Said node is connected to a voltage buffer 144, implemented by an opamp in the case shown, whose output carries the auxiliary voltage $V_a = V_0$.

A master resistor 145, having resistance value R_{m2} , connects the output of voltage buffer 144 to the auxiliary terminal 114.

The master control module 100 comprises a master control unit 150 which performs the control actions of the master control module 100. The master control unit 150 receives supply power from the system voltage V_{cc} . To this end, the master control unit 150 has referencing terminals 151, 152 connected to the voltage terminal 111 and ground terminal 112, respectively. Likewise, each slave control module 200 comprises a slave control unit 250 which performs the control actions of the slave control module 200. To this end, the slave control module 200 has referencing terminals 251, 252 connected to the voltage terminal 211 and ground terminal 212, respectively. Each such control unit 150, 250 may be implemented as a microprocessor, microcontroller or the like.

For being able to communicate with each other, the master control unit 150 has a signal terminal 153 connected to the communication terminal 113, and each slave control unit 250 has a signal terminal 253 connected to the corresponding communication terminals 213, 223.

Such communication involves command signals from the master control unit 150 to the slave control units 250, which signals are received by all slave control units 250 but usually intended for only one of them, for which purpose the signals issued by the master control unit 150 are provided with an address code recognized by the slave control units 250. Vice versa, the communication involves data signals from the slave control units 250 to the master control unit 150, which the master control unit 150 must recognize to determine which slave control unit is the sender, for which purpose the signals are provided with a sender address. But in an initial stage, the master does not "know" each slave yet, and each slave does not know itself yet. It is important that the slaves announce themselves to the master, perhaps already telling the master some device characteristics, but in any case assuming a unique communication address. It is to be noted that in this stage the communication may be initiated by the slaves, who announce themselves to the master, or that the communication may be initiated by the master, who invites an individual slave to specify its characteristics. An important issue in this stage is that each slave is addressed by a unique temporary address. It is further important to realize that this unique temporary address can not be allocated by the master, because the master does not have any means yet for addressing the individual slaves until after the slaves have assumed this unique temporary address. Thus, each slave must assume a temporary address, but these addresses must be mutually different, therefore a random address is not suitable.

According to the basic idea behind the present invention, each slave assumes a temporary address based on its ranking in the series of slaves along the bus 10. It should be clear that in a series of N slaves, the slaves may be numbered as 1, 2, 3, 4, N, and this number will per definition be unique, so this numbering may be used as temporary address. Therefore, each slave is provided with detecting means 260 for determining its ranking number in the series of slaves. These detection means 260 comprise the auxiliary resistor 215.

In figure 1, it will be recognized that all auxiliary resistors 215 of all slaves 200 together form a resistor chain, that has one end connected to the auxiliary terminal 114 of the master 100 and that has its opposite end connected to the ground terminal 112 of the master 100, via the connection line 330 in the end module 300. Thus, in each slave 200, the voltage at the auxiliary resistor would depend on the ranking of the slave.

The use of such resistor chain per se is already known in prior art. EP2007077 discloses a system in which a slave module measures the voltage at the auxiliary resistor with respect to ground. Indeed, each slave will measure a different voltage, but each slave does not have any means to compare this measure voltage with any reference. It remains difficult, and requires much communication with the master, to finally determine the slave's ranking. And the master does not know each slave in advance. According to the invention, each slave is capable to determine its ranking without needing communication input from the master.

According to the invention, the detection means 260 further comprises voltage detectors for sensing the respective voltage potentials at each end of the auxiliary resistor 215. Such voltage detectors may be integrated in the slave control unit 250: each slave control unit 250 in the embodiment shown has two sense input terminals 261, 262 connected to the terminals of the auxiliary resistor 215, or alternatively connected to the auxiliary bus terminals 214, 224. The slave control unit 250 is set to calculate the voltage difference between these two potentials.

It is noted that the slave control unit 250 may actually measure the potentials in Volts and calculate the voltage difference in Volts, but it is also possible that the slave control unit 250 uses a different scale: the actual scale used is of no relevance, as will be understood from the following.

The slave control unit 250 thus measures and calculates three values:
a first voltage potential $V1$ at its first sense input terminal 261;
a second voltage potential $V2$ at its second sense input terminal 262;
a voltage difference $\Delta V = |V1 - V2|$.

In the circuit of figure 1, and with reference to figure 3, it will be clear that the second sense input terminal 262 will sense the lower of the two potentials. This fact can be used if it is always clear which side of the slave (i.e. which side of the auxiliary resistor 215) is directed towards the master. However, in principle the slaves are symmetrical, so it is possible to mirror a slave and in such case the lower potential would be sensed at the first sense input terminal 261. To accommodate for this fact, the slave control unit 250 may be set to calculate the higher potential $VH = \max(V1, V2)$. Thus, in the circuit of figure 3, $VH = V1$.

It is important that the auxiliary resistors 215 in all slaves 200 have mutually identical resistance values, or at least within a certain tolerance. It is further important that the master resistor 145 in the master 100 has the same resistance value as the auxiliary resistors 215 in the slaves, or at least within a certain tolerance. This resistance value will be indicated as R .

With the number of slaves being indicated as N , it will then be seen that the load between the output of buffer 144 in the master 100 and the GND line consists of

a series of N+1 resistors of resistance R each. Consequently, in each slave 200(i) the voltage difference $\Delta V(i)$ will have the same value

$$\Delta V(i) = \Delta V = V_a / (N+1) \quad (2)$$

in which i indicates the ranking number of the slave concerned, counting from the master 100. In other words, in figure 1 the leftmost slave 200A will have ranking i=1.

For easy discussion, an inverse ranking j will be defined by starting the counting from the opposite direction of the series. In such case, in figure 1 the rightmost slave 200C will have ranking j=1, and the leftmost slave 200A will have ranking j=3. It will be seen that the following formula applies:

$$j + i = N + 1 \quad (3)$$

It will now also be seen that in each slave 200(j) the highest potential $V_H(j)$ measured obeys the following formula:

$$V_H(j) = j \times \Delta V \quad (4)$$

Therefore, each slave 200(j) is now easily capable to calculate a unique ranking number j according to the formula

$$j = V_H(j) / \Delta V \quad (5)$$

The calculation according to formula (5) should produce an integer value for j. Tolerances may however result in a calculation result that is not an exact integer. To cope with this, each slave may be adapted to round the calculation to the nearest integer. It is also possible that each slave is set to multiply the calculation result by a constant value, for instance multiply by 1000, and convert the result by rounding up or down to the nearest integer, which will also result in unique communication addresses. The range of j is N to 1. In this case, each slave module uses equation (4) or (5) to find j so as to calculate its unique communication address, and does not necessarily need to know N or i. In such a case, the referencing line 11 with terminal 211 and 221, the voltage divider 270 and the referencing voltage measuring means 254 can be removed from figure 3.

In the situation $V_H=V_L \neq 0$ is detected by master and/or slave, it indicates the line 14 is lost succeeding to this node: the connection to the downstreaming slave or the end cap is lost. In case $V_H=V_L=0$ is detected by a slave device, it indicates that the line 14 is lost preceding to this slave device.

It is noted that j is an inverse ranking number: the most remote slave as seen from the master will use inverse ranking number j=1. It may however be desirable to use the straight ranking number i. The straight ranking number i can be calculated if both V_a and ΔV are known, using the following formula:

$$N = V_a / \Delta V \quad (6)$$

In a first embodiment, the master 100 is provided with means for calculating ΔV . In the embodiment of figure 2, terminal 114 is coupled to an input 154 of the master control unit 150, allowing the master control unit 150 to sense the potential at terminal 114 and to calculate the voltage drop ΔV over the master resistor 145. The master 100 can now calculate N using formula (6) above. In this embodiment, after the slave 200 has communicated its inverse ranking number j , the straight ranking number i (or an address based on the straight ranking number) is calculated by the master 100 and communicated to the slave.

In a second embodiment, the master is designed as in the first embodiment, but after calculating N the master transmits over the communication line 13 of said bus an information message containing digital data indicating this value. The master transmits this information to all slaves. Now the slaves are able to calculate the straight ranking numbers i themselves.

In an alternative third embodiment, the slaves 200 are provided with means for calculating V_a . In the embodiment of figure 3, each slave 200 comprises a voltage divider 270, constituted by a series arrangement of two resistors 271, 272 having respective resistance values R_1 and R_2 , connected between the a referencing line 11 and the ground voltage bus 12. Although in the various slaves it is not essential that these resistors have exactly the same resistance values, it is important that the division ratio $DR_{200} = R_1/(R_1+R_2)$ in each slave 200 is substantially the same (some tolerance is allowed) as the division ratio $DR_{100} = R_{m0}/(R_{m0}+R_{m1})$ of the voltage divider 141 in the master 100. The node between the two resistors 271, 272 is coupled to a referencing voltage measuring means 254 of the slave control unit 250, allowing the slave control unit 250 to sense the potential at this node, which will be equal to V_a . The slave 200 can now calculate N using formula (5). In this embodiment, the slave 200 can use the straight ranking number i from the onset.

It is noted that it is possible that the division ratio DR_{200} in a slave 200 differs from the division ratio DR_{100} in the master 100, as long as the ratio $\rho = DR_{100}/DR_{200}$ is known to the corresponding slave control unit 250, so that this slave control unit 250 can multiply the calculated division ratio DR_{200} by ratio ρ to obtain the correct value.

It is further noted that, alternatively with respect to equation (5), j can be calculated on the basis of the lowest potential $VL(j) = \min(V_1, V_2)$ according to the formula $j = 1 + VL/\Delta V$.

From above description, microcontroller with ADC ports are used as the control unit 250 and the master control unit 150 for AD conversion, and certain some

basic algebra calculation is required to generate the slave address and communicate between the master and slave. Both the ADC and algebra calculation are required only at the power on stage, which consume very few processor resources. And the ADC resolution can be very low (e.g. 7bit) to generate decades of slave address.

- 5 Consequently, these hardware resource requirements are low and can be covered by the MCU in lighting system and by embedded microcontroller in the lighting units without any extra cost added.

As to the address that is finally used, the ranking number can be directly used
10 in the communication between the master and the slave. Alternatively the master can use the ranking number as a temporary address so as to signal another logic/permanent address. More specifically, the master calculates the slave number on the system, numerates and assigns a logic/ permanent address to each slave using the slave number, and told the new address to the slave directly by addressing
15 its ranking number/slave number. The master does not need to communicate with slaves to find each slave's ranking number, and after this all communication is based on the new logic address. This need to be done in each power on cycle when the luminaire is turn from off to on, which should cause the luminaire from power-on to lighting up delay; for instance in a 8 slave devices system, each consumes 50ms
20 (including the guard band time for master switch to next slave) for initiation and in total 400ms delay is a reasonable estimation.

Summarizing, the present invention provides a master/slave control system that comprises a bus, a master module and a plurality of slave modules, wherein
25 each slave module comprises a measuring resistor and wherein all measuring resistors are connected in series, and wherein each slave module is adapted to measure the voltage drop over the measuring resistor and the voltage potential at one terminal of the measuring resistor and to calculate the ranking of the slave and in turn a unique communication address on the basis of these measurements.
30 Preferably, the master also measures the voltage drop over the master resistor and the voltage potential at one terminal of the master resistor and to calculate the total number thus the unique communication address of the slave.

For implementation, the master and salve are logically separated. Physically,
35 the system can be in different form: 1) master and slaves resident inside one luminaire as the system; 2). or master and slave have its own physical enclosure, together form into a small controllable distributed lighting system.

While the invention has been illustrated and described in detail in the drawings and foregoing description, it should be clear to a person skilled in the art that such illustration and description are to be considered illustrative or exemplary and not restrictive. The invention is not limited to the disclosed embodiments; rather, several variations and modifications are possible within the protective scope of the invention as defined in the appending claims.

For instance, in the above, a slave's ranking number is used as temporary address. It is also possible to use this ranking number as starting point for calculating an address, using an invertible formula $y=f(x)$, i.e. a formula that has the property that for different x-values different y-values will result. The master and the slave should use the same mechanism to calculate the new address. Alternatively, the master and the slave may use different address as long as each of them can translate and match the address sent by each other.

Further, in the above, each slave via the bus receives information defining the auxiliary voltage V_a . This information can be transmitted over the communication line 13 in the form of data. This information can also be transmitted over a voltage line in the form of a voltage. In the example discussed, the voltage line is a referencing line transferring a supply voltage V_{cc} for the slave, and in turn it can be considered as a power supply line, and each slave module has information, either in the form of software information or in the form of a hardware voltage divider, defining the ratio between the auxiliary voltage and the supply voltage. Alternatively, the voltage line can be a separate referencing line and said voltage on the voltage line can be identical to the auxiliary voltage, in which case the slave control devices having an input terminal coupled directly to the referencing line.

Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure, and the appended claims. In the claims, the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. A single processor or other unit may fulfil the functions of several items recited in the claims. Even if certain features are recited in different dependent claims, the present invention also relates to an embodiment comprising these features in common. Any reference signs in the claims should not be construed as limiting the scope.

In the above, the present invention has been explained with reference to block diagrams, which illustrate functional blocks of the device according to the present invention. It is to be understood that one or more of these functional blocks may be implemented in hardware, where the function of such functional block is performed by individual hardware components, but it is also possible that one or more of these functional blocks are implemented in software, so that the function of such functional

block is performed by one or more program lines of a computer program or a programmable device such as a microprocessor, microcontroller, digital signal processor, etc.

CLAIMS

1. Master module (100) adapted for use in a master/slave control system (1), the master module (100) being adapted for coupling to slave modules (200) via a bus (10);
- 5 the master module (100) comprising an auxiliary terminal (114) for connection to an auxiliary bus line (14) of the bus (10), a voltage source (170, 144) for generating an auxiliary voltage (V_a), and a master resistor (145) connected between an output of said voltage source and said auxiliary terminal (114); and
- 10 the master module (100) further comprising a communication terminal (113) for connection to a communication line (13) of the bus (10), and being adapted to generate at its communication terminal command signals for slave modules connected to the bus (10), wherein the master module is further adapted to transmit via the communication line (13) instruction data and address data defining a unique communication address of an individual slave module,
- 15 wherein the master module (100) comprises first voltage measuring means (150, 154) coupled to a first terminal of the master resistor (145) and measuring a first voltage potential, and second voltage measuring means (150, 155) coupled to an opposite second terminal of the master resistor (145) and measuring a second voltage potential;
- 20 wherein the master module (100) is adapted to determine the higher (V_H) or the lower (V_L) of the first and second potentials, and to determine the potential difference (ΔV) across the master resistor (145);
- wherein the master module (100) is adapted, using the said potential difference (ΔV) and either said higher potential (V_H) or said lower potential (V_L), to calculate a
- 25 total number (N) of slave modules connected to the bus.
2. Master module according to claim 1, wherein the master module (100) is adapted, using said total number (N) of slave modules, to calculate each slave's unique communication address.
- 30
3. Master module according to claim 2, wherein the master module (100) is adapted to transmit over the communication line (13) of said bus an information message containing digital data indicating the total number (N) of slave modules.
- 35
4. Master module according to claim 1, wherein the master module (100) further comprises a referencing terminal for connection to a referencing line of the bus (10),

and wherein the master module (100) is adapted to apply to said referencing line a referencing voltage equal to said auxiliary voltage (Va).

5. Master module according to claim 1, wherein the master module (100) further
5 comprises a referencing terminal (111) for connection to a referencing line (11) of the bus, wherein said voltage source (170) comprises a voltage divider (171, 172) with a first division ratio, wherein an input of said voltage divider (171, 172) is connected to said referencing terminal (111) for receiving an input voltage (Vcc) higher than said auxiliary voltage (Va), and wherein the master module (100) is adapted to apply an
10 output of said voltage divider (171, 172) to said auxiliary terminal (114).

6. Slave module (200) adapted for use in a master/slave control system (1), the slave module (200) being adapted for coupling to a master module (100) via a bus (10);
15 wherein the slave module (200) comprises a measuring resistor (215) adapted for being connected in series in an auxiliary line (14) of the bus (10) to couple to an auxiliary terminal of the master module (100);
wherein the slave module (200) comprises first voltage measuring means (250, 261) coupled to a first terminal of the measuring resistor (215) and measuring a first
20 voltage potential, and second voltage measuring means (250, 262) coupled to an opposite second terminal of the measuring resistor (215) and measuring a second voltage potential;
wherein the slave module (200) is adapted to determine the higher (VH) or the lower (VL) of the first and second potentials, and to determine the potential
25 difference (ΔV) across the measuring resistor (215);
and wherein the slave module (200) is adapted, using the said potential difference (ΔV) and either said higher potential (VH) or said lower potential (VL), to calculate a unique communication address for communication over the bus;
said slave module further comprises a communication terminal (213) adapted to
30 couple to a communication terminal of the master module (100) via a communication line (13) and to receive instruction data and address data defining a unique communication address of the slave module.

7. Slave module according to claim 6, wherein the slave module (200) is adapted
35 to calculate a ranking number (j) according to either one of the formulas

$$j = V_H / \Delta V \quad \text{or} \quad j = 1 + V_L / \Delta V, \text{ respectively}$$

and to calculate the unique communication address from the calculated ranking number (j);

wherein j indicates the ranking number,

VH indicates said higher potential,
VL indicates said lower potential.

8. Slave module according to claim 7, wherein the slave module (200) is adapted to calculate the unique communication address from the calculated ranking number (j) by multiplying the calculated ranking number (j) by a predetermined integer higher than or equal to 1.

9. Slave module according to claim 8, wherein the slave module (200) is adapted to receive information representing the total number (N) of slave modules; and wherein each slave module (200) is adapted, before calculating the unique communication address, to update the calculated ranking number (j) according to the formula

$$1 + (N-j)$$

wherein N indicates the total number of slave modules.

10. Slave module according to claim 9, wherein the slave module (200) further comprises a referencing terminal for connection to a referencing line of the bus (10), wherein the slave module (200) is adapted for measuring a referencing voltage (Va) at the referencing terminal, and wherein the slave module (200) is adapted to calculate the total number (N) of slave modules by dividing the referencing voltage (Va) by the potential difference (ΔV) across the measuring resistor (215).

11. Slave module according to claim 9, wherein the slave module (200) further comprises a referencing terminal (211) for connection to a referencing line (11) of the bus (10),

wherein the slave module (200) is adapted to receive at said referencing terminal an input voltage (Vcc) higher than a referencing voltage (Va);

wherein the slave module (200) comprises a voltage divider (270) having an input connected to the referencing terminal, the voltage divider having a ratio $\rho = V_a/V_{cc}$,

in which Vcc indicates the input voltage at the referencing line (11) and in which Va indicates said referencing voltage;

wherein the slave module (200) comprises referencing voltage measuring means (250, 254) coupled to an output of the voltage divider (270) for measuring an output voltage (Vd) of the voltage divider as the referencing voltage (Va); and wherein the slave module (200) is adapted to calculate the total number (N) of slave modules by dividing the referencing voltage (Va) by the potential difference (ΔV) across the measuring resistor (215).

12. Master/slave control system (1) comprising a master module (100) according to any one of claims 1 to 5 and at least one slave module (200) according to any one of claims 6 to 11, wherein said master resistor (145) of the master module (100) has a resistance value equal to the resistance value of each the measuring resistor (215) of the at least one slave module (200), wherein the auxiliary bus line coupled to the ground after the last slave module and the master module and the slave modules are coupled to the same ground.
13. Master/slave control system (1) according to claim 12, wherein each slave module (200) is adapted to send an initiation message containing data representing the slave module's characteristics and the slave module's unique communication address, and wherein the master module (100) is responsive to a received initiation message by sending a response message to the transmitting slave module while using the unique communication address contained in the initiation message.
14. Master/slave control system (1) comprising a master module (100) according to claim 2 and at least one slave module (200) according to any one of claims 6 to 11, wherein the master module (100) is adapted to send an inquiry message with a unique communication address of one designated slave module, and wherein a slave module (200) is responsive to a received inquiry message by sending a reply message containing data representing the slave module's characteristics and the slave module's unique communication address if that slave module's unique communication address is matching the communication address contained in the received inquiry message.

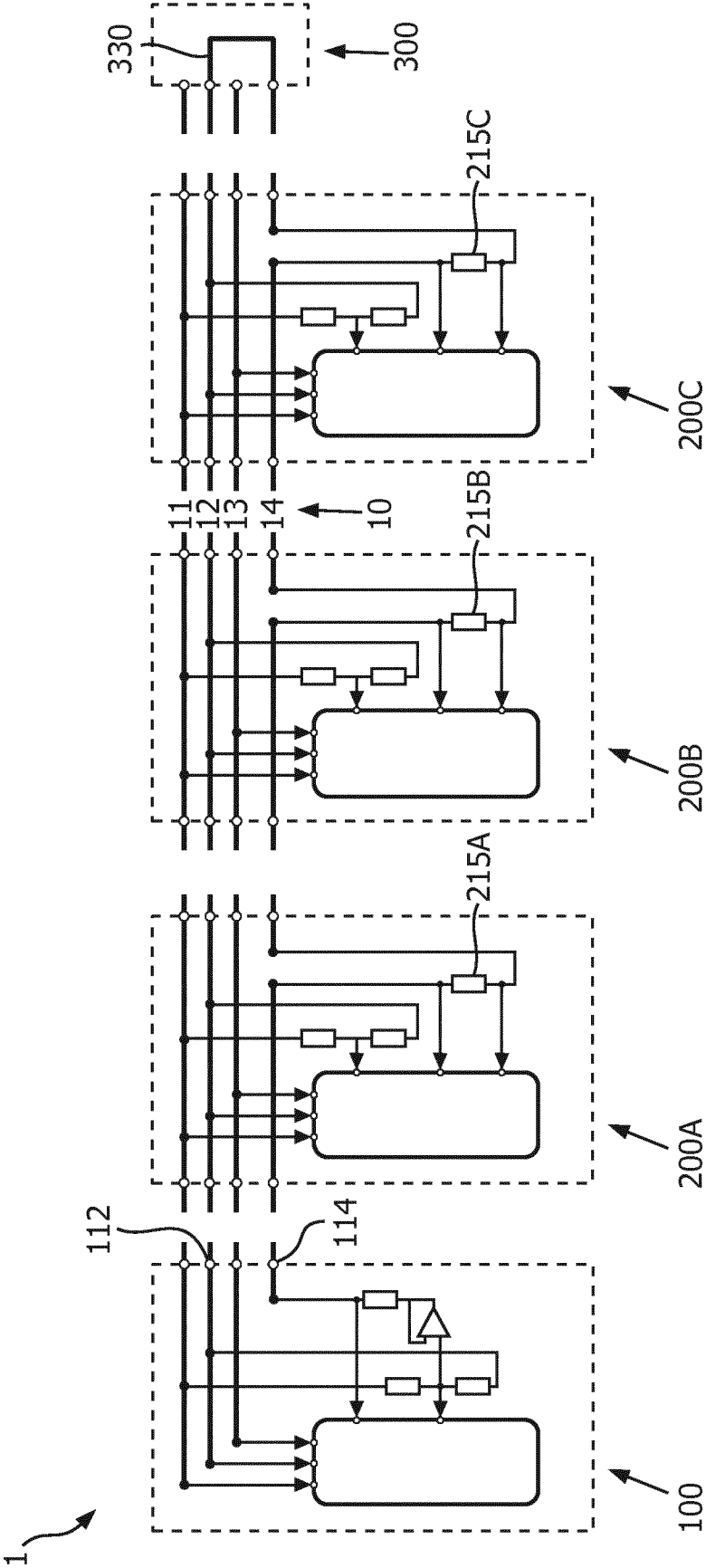


FIG. 1

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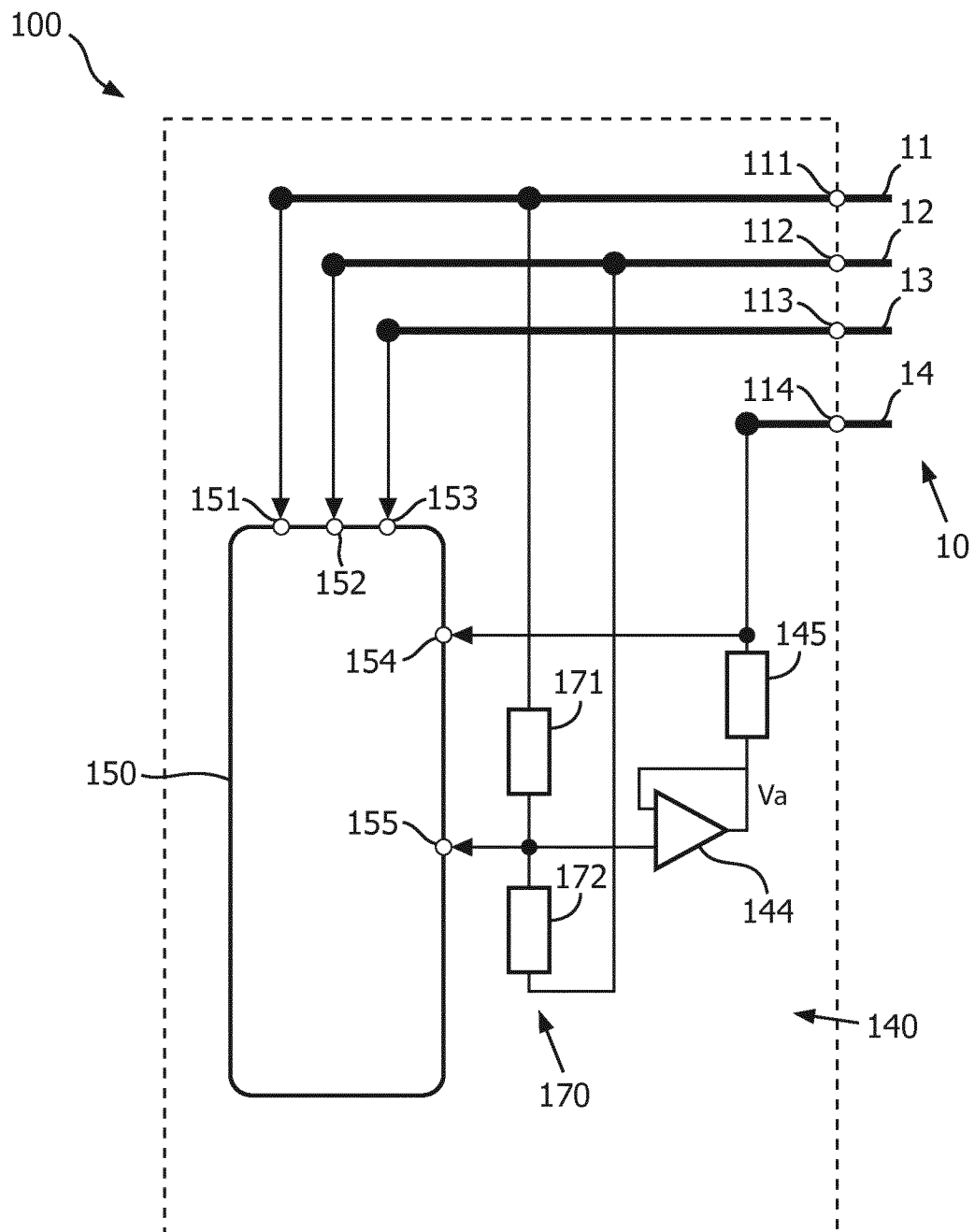


FIG. 2

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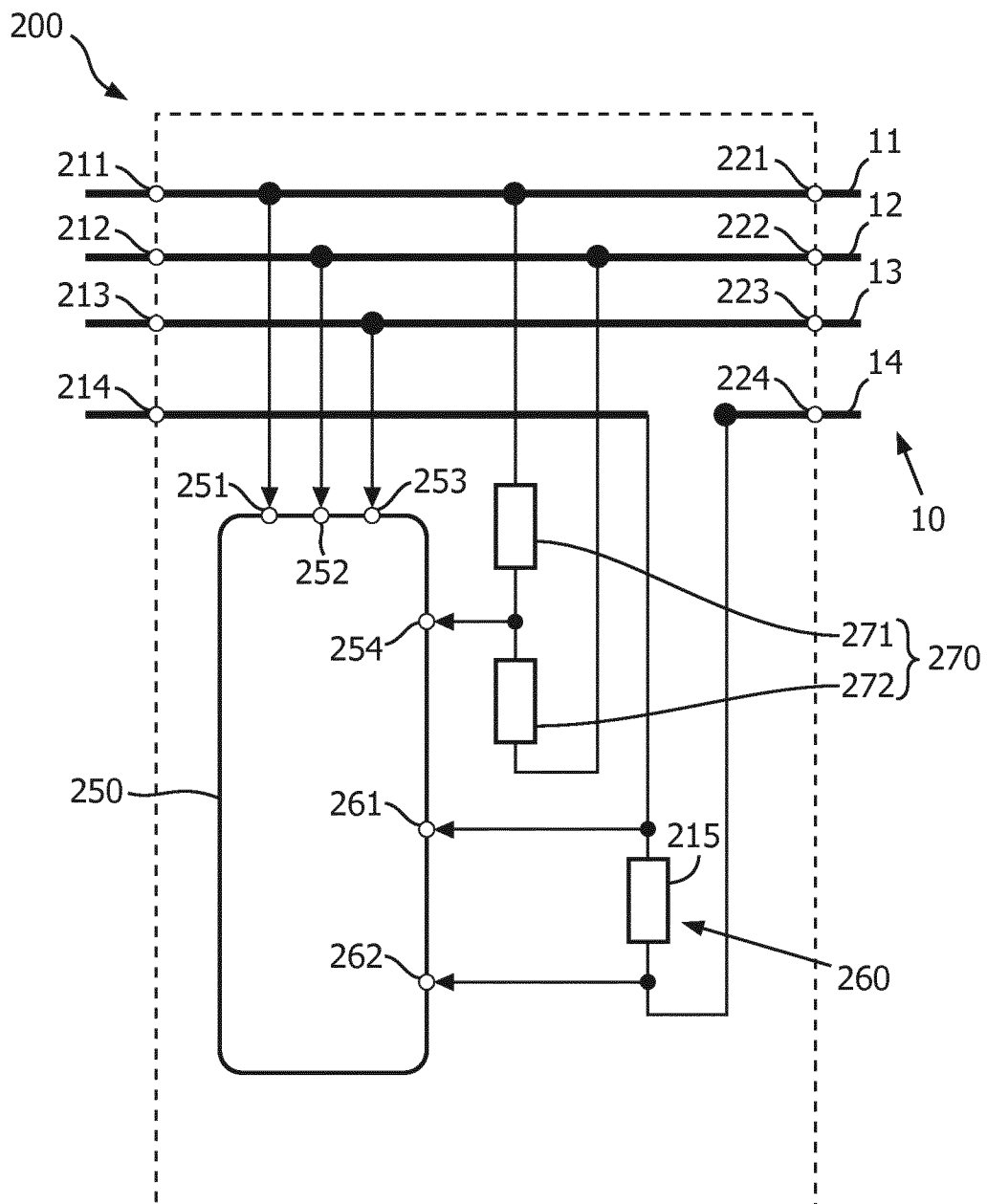


FIG. 3

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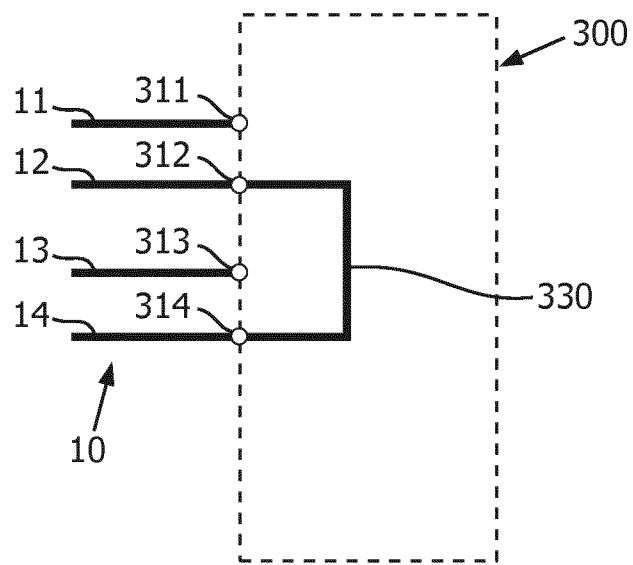


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2015/058443

A. CLASSIFICATION OF SUBJECT MATTER

INV. H04L12/40 H04L29/12 H05B37/02
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04L H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 2 154 831 A1 (SIEMENS AG [DE]) 17 February 2010 (2010-02-17) figures 1,3 paragraphs [0001] - [0003], [0005], [0011], [0012], [0025] - [0032] -----	1-14
Y	EP 1 284 556 A1 (SAIA BURGESS MURTEN AG [CH]) 19 February 2003 (2003-02-19) cited in the application figure 2 paragraphs [0011] - [0034] -----	1-14
Y	EP 2 521 041 A2 (DEERE & CO [US]) 7 November 2012 (2012-11-07) cited in the application figure 1 paragraphs [0004], [0008] - [0014], [0020] - [0024], [0038] - [0041], [0049] -----	1-10, 12-14
A	----- -/-	11



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

13 August 2015

Date of mailing of the international search report

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2015/058443

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 2 015 518 A1 (SIEMENS AG [DE]) 14 January 2009 (2009-01-14)	11
A	figures 1,2 paragraphs [0006] - [0012], [0016], [0021] -----	1,6, 12-14
A	US 2004/078097 A1 (BRUZY CHRISTOPHE [FR] ET AL) 22 April 2004 (2004-04-22) figures 4,5,7,17,19,20 paragraphs [0054], [0056], [0064] - [0091], [0128], [0129], [0137] - [0141] -----	1,2,6, 12-14
A	EP 2 007 077 A1 (SIEMENS AG [DE]) 24 December 2008 (2008-12-24) cited in the application figures 1, 2 paragraphs [0009] - [0019] -----	1,6, 12-14

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2015/058443

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 2154831	A1	17-02-2010	NONE
EP 1284556	A1	19-02-2003	NONE
EP 2521041	A2	07-11-2012	EP 2521041 A2 07-11-2012 US 2012284441 A1 08-11-2012
EP 2015518	A1	14-01-2009	AT 476808 T 15-08-2010 DE 102007028926 B3 16-10-2008 EP 2015518 A1 14-01-2009
US 2004078097	A1	22-04-2004	AT 497616 T 15-02-2011 EP 1364288 A1 26-11-2003 ES 2360210 T3 01-06-2011 FR 2821453 A1 30-08-2002 JP 4837238 B2 14-12-2011 JP 2004523045 A 29-07-2004 US 2004078097 A1 22-04-2004 US 2011060501 A1 10-03-2011 WO 02069149 A1 06-09-2002
EP 2007077	A1	24-12-2008	DE 102007028928 A1 02-01-2009 EP 2007077 A1 24-12-2008