US 20060043462A1

(19) **United States**
(12) **Patent Application Publication** (10) **Pub. No.: US 2006/0043462 A1**
Manning et al. (43) **Pub. Date: Mar. 2, 2006**

(54) **STEPPED GATE CONFIGURATION FOR NON-VOLATILE MEMORY**

(75) Inventors: **H. Montgomery Manning**, Eagle, ID (US); **Kunal Parekh**, Boise, ID (US)

Correspondence Address:
Attn: Christopher J. McLaughlin
LEFFERT JAY & POLGLAZE, P.A.
P.O. Box 581009
Minneapolis, MN 55402 (US)

(73) Assignee: **Micron Technology, Inc.**

(21) Appl. No.: **10/928,082**

(22) Filed: **Aug. 27, 2004**

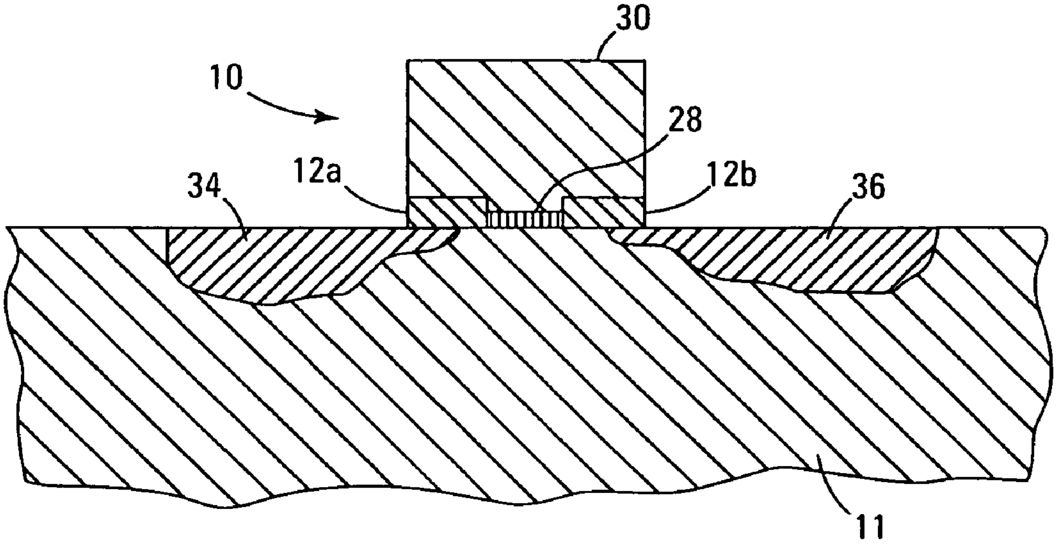
Publication Classification

(51) **Int. Cl.**
H01L 29/788 (2006.01)

(52) **U.S. Cl.** **257/316**

(57) **ABSTRACT**

A memory device having a field effect transistor with a stepped gate dielectric and a method of making the same are herein disclosed. The stepped gate dielectric is formed on a semiconductor substrate and consists of a pair of charge trapping dielectrics separated by a gate dielectric; a gate conductor is formed thereover. Source and drain areas are formed in the semiconductor substrate on opposing sides of the pair of charge trapping dielectrics. The memory device is made by forming a charge trapping dielectric layer on a semiconductor substrate. A trench is formed through the charge trapping dielectric layer to expose a portion of the semiconductor substrate. A gate dielectric layer is formed within the trench and a gate conductor layer is formed over the charge trapping and gate dielectric layers.



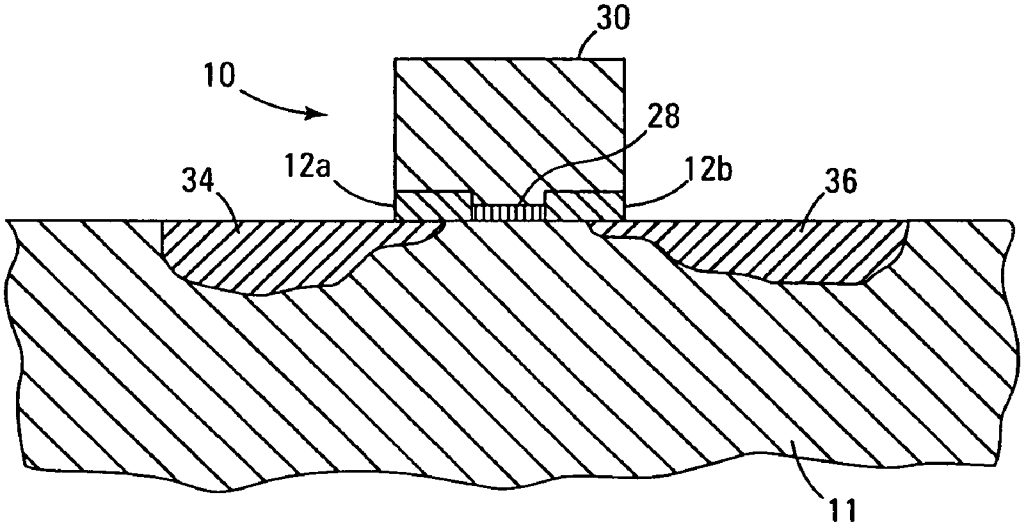


Fig. 1

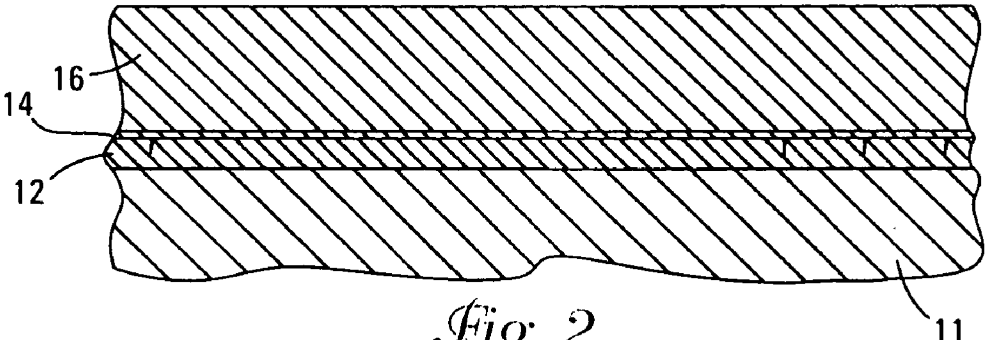


Fig. 2

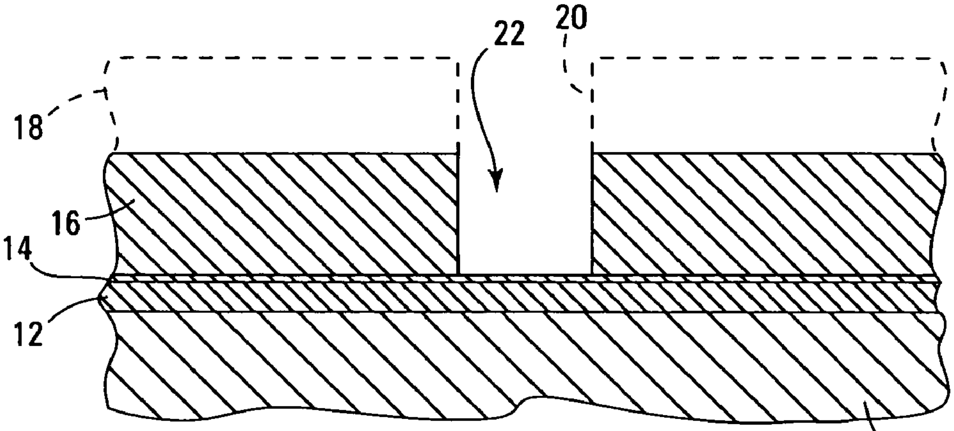


Fig. 3

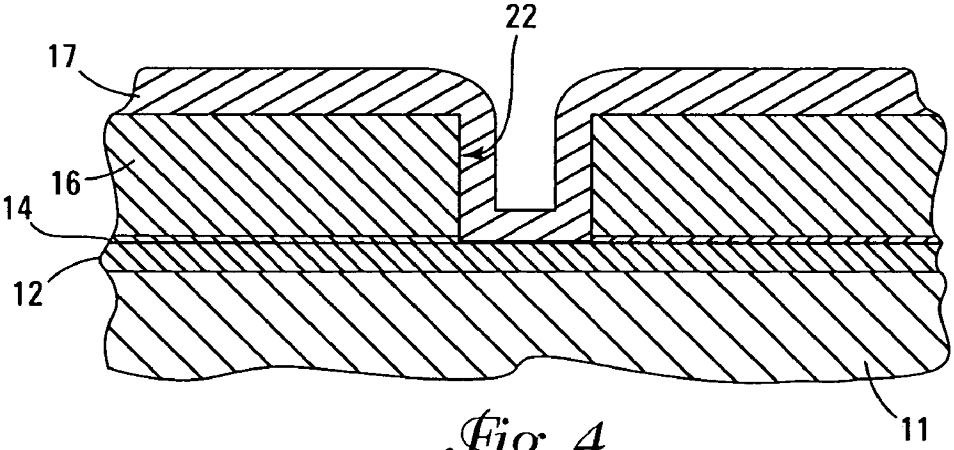


Fig. 4

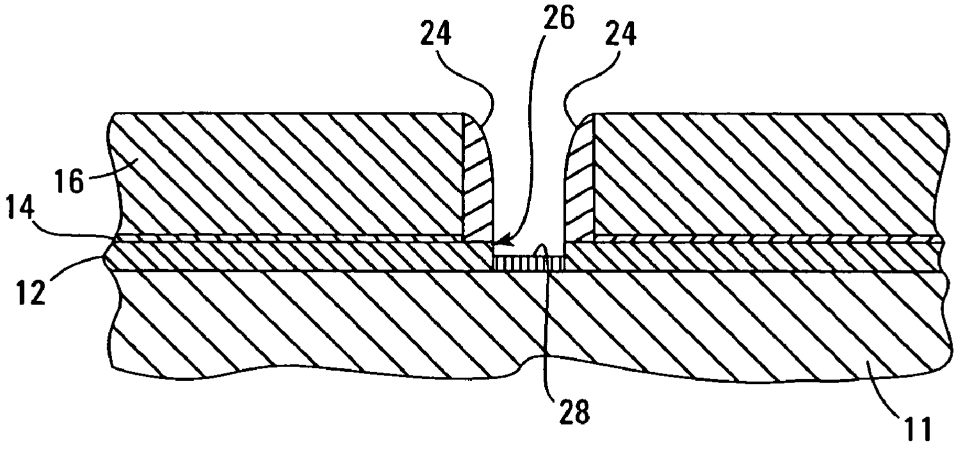


Fig. 5

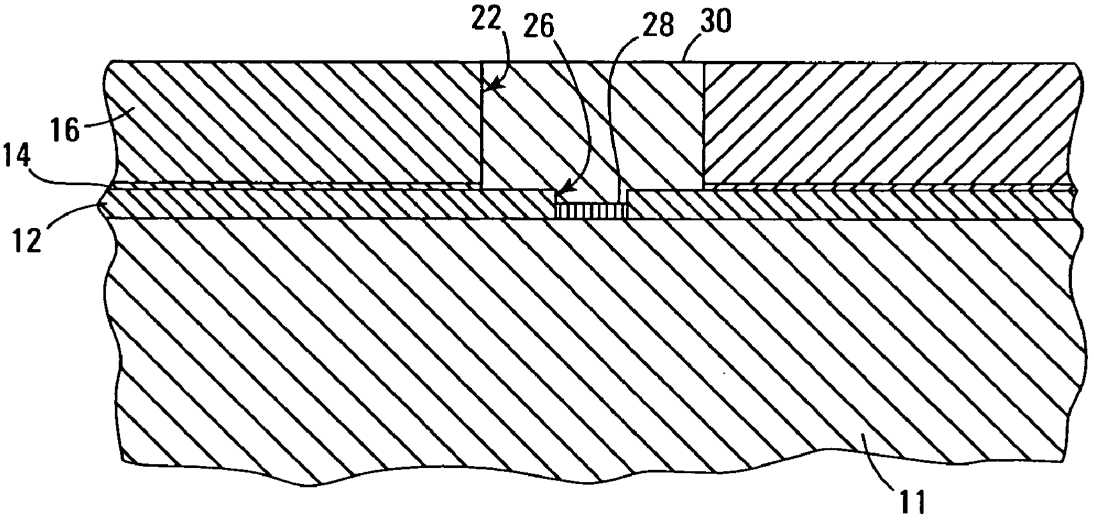


Fig. 6

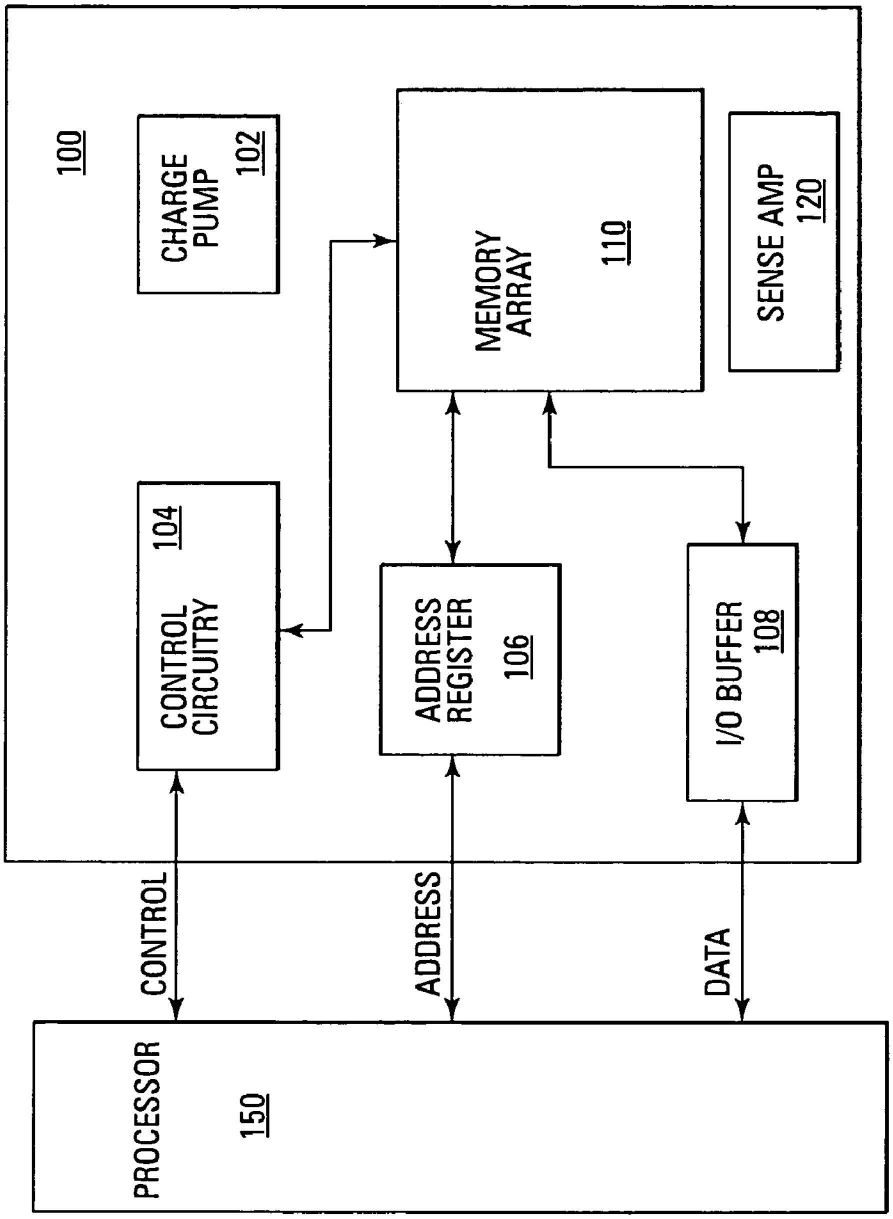

100
CHARGE PUMP 102
MEMORY ARRAY 110
SENSE AMP 120
CONTROL CIRCUITRY 104
ADDRESS REGISTER 106
I/O BUFFER 108
CONTROL
ADDRESS
DATA
PROCESSOR 150

Fig. 7

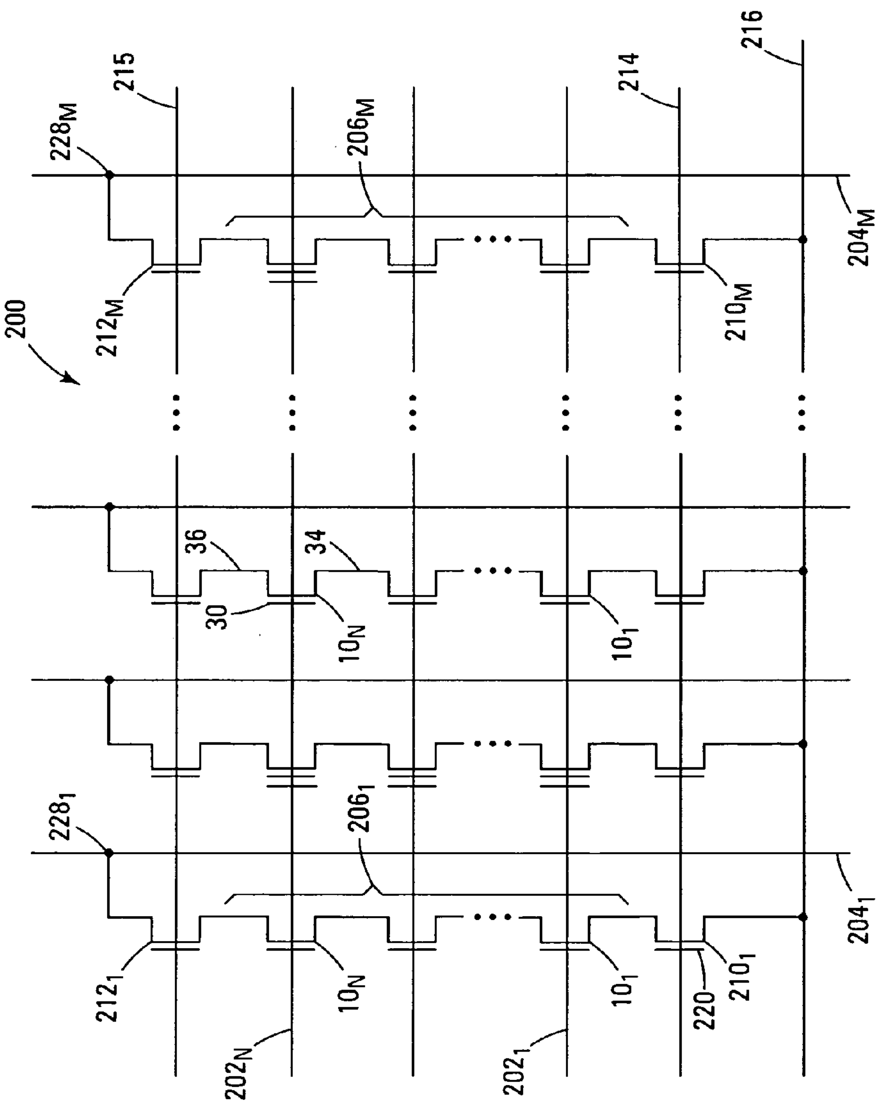

200
228M
215
206M
214
216
204M
212M
210M
36
34
30
10N
101
2281
2061
2041
2121
10N
101
220
2101
202N
2021

Fig. 8

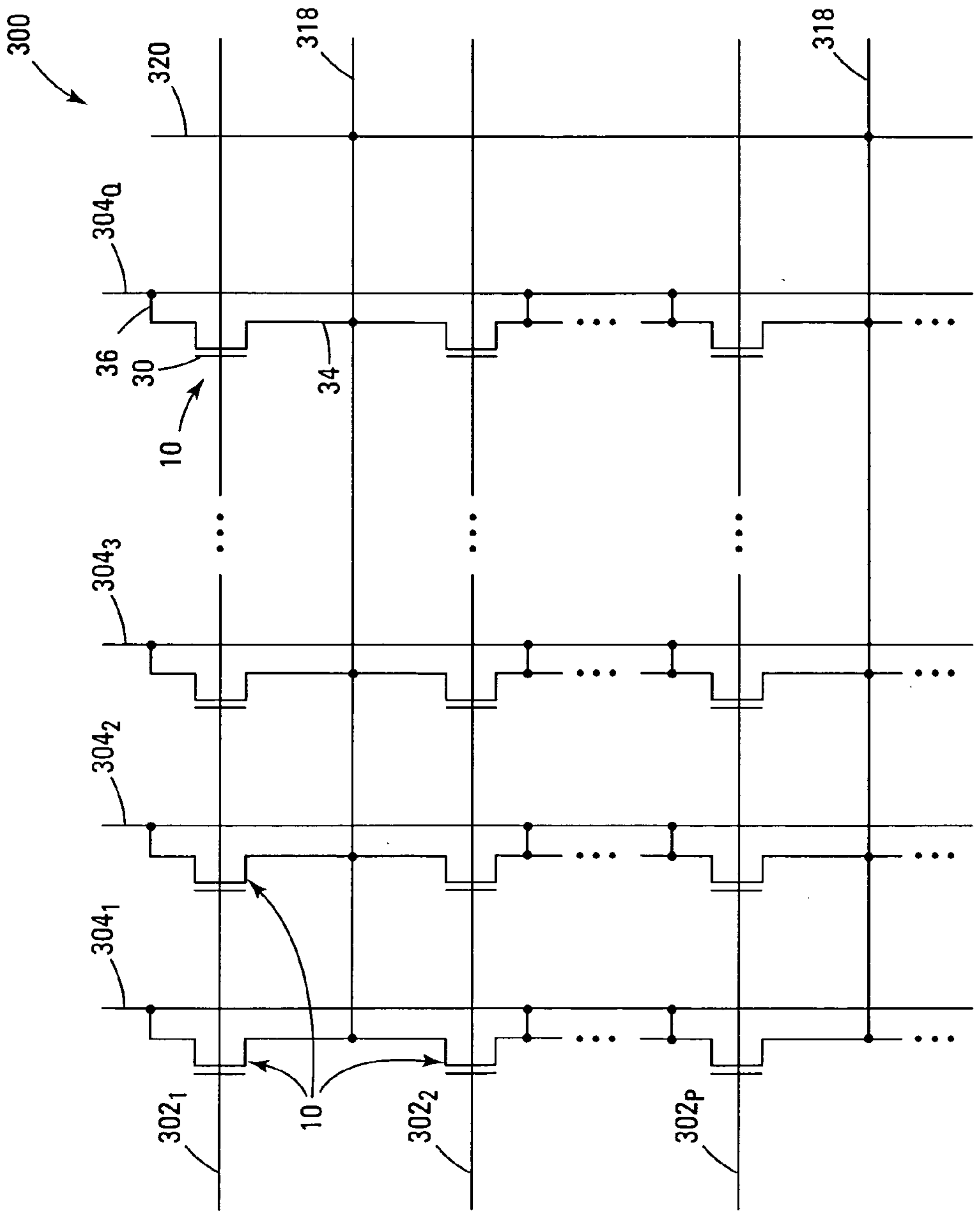

300
320
318
318
304a
36
30
34
10
304₃
304₂
304₁
302₁
10
302₂
302P

Fig. 9

STEPPED GATE CONFIGURATION FOR NON-VOLATILE MEMORY

TECHNICAL FIELD OF THE INVENTION

[**0001**] The present invention relates generally to memory devices and in particular, the present invention relates to field effect transistors having a stepped gate dielectric.

BACKGROUND OF THE INVENTION

[**0002**] Memory devices are typically provided as internal, semiconductor, integrated circuits in computers or other electronic devices. There are many different types of memory including random-access memory (RAM), read only memory (ROM), dynamic random access memory (DRAM), synchronous dynamic random access memory (SDRAM), and flash memory. One type of flash memory is a nitride read only memory (NROM). NROM has some of the characteristics of flash memory but does not require the special fabrication processes of flash memory. NROM integrated circuits can be implemented using a standard CMOS process.

[**0003**] Flash memory devices have developed into a popular source of non-volatile memory for a wide range of electronic applications. Flash memory devices typically use a one-transistor memory cell that allows for high memory densities, high reliability, and low power consumption. Common uses for flash memory include personal computers, personal digital assistants (PDAs), digital cameras, and cellular telephones. Program code and system data such as a basic input/output system (BIOS) are typically stored in flash memory devices for use in personal computer systems.

[**0004**] As the size of memory devices shrinks, so too does the charge trapping capacity of those devices. And, as the charge trapping capacity shrinks, so does the threshold voltage difference that differentiates the programmed states of the device. Because variations in the operational characteristics of these ever-shrinking memory devices can have serious effects on the ability of the memory devices to perform reliably, it is important to enhance the charge trapping ability of these memory devices. In this way, the effect of variations in the operational characteristics of a memory device can be more easily accommodated and it will be possible to more reliably discriminate between the programmed states of the device. Accordingly, there is a need for an improved memory device having an enhanced charge trapping ability.

BRIEF SUMMARY OF THE INVENTION

[**0005**] A memory device of the present invention may be realized in the provision of a field effect transistor that has a stepped gate dielectric. One embodiment of the present invention has a gate dielectric layer that is disposed between two charge trapping layers on a semiconductor substrate. The gate dielectric layer is generally thinner than the charge trapping layers that border it. A control gate overlies the gate dielectric and charge trapping layers.

[**0006**] One embodiment of the memory device of the present invention may be made by first forming a charge trapping dielectric layer on a semiconductor substrate. A trench is formed in the charge trapping dielectric layer and a gate dielectric is formed therein. A gate conductor is then formed to overlie the charge trapping dielectric layer and the gate dielectric. The charge trapping layer is then trimmed back to the edge of the gate conductor.

[**0007**] The invention further provides methods and apparatus of varying scope.

DESCRIPTION OF THE DRAWINGS

[**0008**] **FIG. 1** is a cross-sectional view of a portion of a memory device;

[**0009**] **FIGS. 2-6** are cross-sectional views of a portion of a memory device during various stages of fabrication in accordance with an embodiment of the invention;

[**0010**] **FIG. 7** is a simplified block diagram of an integrated memory device, according to an embodiment of the present invention;

[**0011**] **FIG. 8** is a simplified block diagram of a NAND memory array incorporating an embodiment of the present invention; and,

[**0012**] **FIG. 9** is a simplified block diagram of a NOR memory array incorporating an embodiment of the present invention.

DETAILED DESCRIPTION

[**0013**] In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The terms substrate or substrate used in the following description include any base semiconductor structure. Both are to be understood as including silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of a silicon supported by a base semiconductor structure, as well as other semiconductor structures well known to one skilled in the art. Furthermore, when reference is made to a substrate or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure, and terms substrate or substrate include the underlying layers containing such regions/junctions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

[**0014**] **FIG. 1** illustrates a memory cell or field effect transistor **10** having a stepped gate dielectric constructed and arranged according to the principles of the present invention. The field effect transistor **10** is formed on a substrate or semiconductor substrate **11** that is in one embodiment fashioned of a monocrystalline silicon material, though other materials may be used. The transistor **10** includes left and right charge trapping dielectrics **12*a***, **12*b***, a stepped gate dielectric **28**, and a gate conductor or control gate **30**. The left and right charge trapping dielectrics **12*a***, **12*b*** are typically associated with a source **34** and a drain **36**, respectively, though it is to be understood that the association of the source **34** and drain **36** with the charge trapping dielectrics **12***a*, **12***b* may be reversed where required.

[**0015**] **FIGS. 2-6** illustrate one embodiment of a method of fabricating a transistor **10**. In a first step illustrated in **FIG. 2**, a charge trapping dielectric layer **12** is deposited on the substrate **11**. The charge trapping dielectric layer **12** is preferably a composite structure that includes two or more dielectric materials laid down upon the substrate **11**. In one embodiment of the transistor **10**, the charge trapping dielectric layer **12** is formed of a first component layer of silicon dioxide and a second component layer of silicon nitride. The first component layer of silicon dioxide may be formed on the substrate **11** using, for example, a wet or dry oxidation process, an atomic layer deposition (ALD) process, or a chemical vapor deposition (CVD) process. The second component layer of silicon nitride may be deposited onto the previously grown silicon dioxide layer using, for example, a chemical vapor deposition technique to form the charge trapping dielectric layer **12**. Additional or alternative component layers may be added as required. Other materials that may be laid down as part of the charge trapping dielectric layer **12** either in lieu of, or in addition to, the materials described hereinabove may include, but are not limited to, Al_2O_3, HfO_2, HfON, HfOSiN, Ta_2O_5, or combinations thereof. In general, dielectric layer **12** includes one or more layers of material that individually or in combination have the ability to store and release an electric charge.

[**0016**] Once the charge trapping dielectric layer **12** has been formed, an etch stop layer **14** will preferably be deposited onto the charge trapping dielectric layer **12**. Note that the etch stop layer **14** is itself optional in that careful selection of subsequent etching processes may obviate the need for a distinct etch stop layer **14**. In some instances, however, if it is found that the etch stop layer **14** is beneficial to the operation of the transistor **10**, this layer, or some portion thereof, may remain part of the structure of the transistor **10**. Examples of some suitable materials that may form the etch stop layer **14** include, but are not limited to, titanium nitride and Al_2O_3. A sacrificial layer **16**, preferably of silicon nitride, is applied over the etch stop layer **14** to act as a hard mask. To the extent that the etch stop layer **14** is later removed, the total thickness of the sacrificial layer **16** and any remaining portion of the etch stop layer **14**, taken together, can define the height of the control gate **30**.

[**0017**] **FIG. 3** illustrates the formation of a groove or gap **22** in the sacrificial layer **16**. By way of example, the groove **22** may be formed by applying a photoresist layer **18** over the sacrificial layer **16** and then exposing the photoresist layer **18** to ultraviolet light in a preselected pattern. The photoresist layer **18** is subsequently developed to remove those portions of the photoresist layer **18** that remain undeveloped, thereby resulting in a gap **20** in the layer **18**. The width of the gap **20** generally defines the width of the control gate **30**. The groove **22** is then etched into and through the sacrificial layer **16**, and depending on the requirements of the application, into and/or through the etch stop layer **14** as well. In some instances, a portion of the etch stop layer **14** will remain after this etching step, and in other instances, the etching procedure will remove the entire etch stop layer **14**. It is preferred to utilize a plasma or ion-etching process for creating the groove **22**, though other directional etching methods or processes may be used as well. Once the groove **22** has been etched into the sacrificial layer **16** and etch stop layer **14**, the remaining photoresist layer **18** is removed such as by using a chemical wet stripping process, a plasma stripping process, or other suitable means.

[**0018**] After the remaining photoresist layer **18** has been removed, a layer of silicon dioxide or another suitable sacrificial material such as, for example TEOS oxide, is deposited over the sacrificial layer **16** to form spacers **24**. As one example, a spacer layer **17** could be blanket deposited over layers **12**, **14**, and **16** as shown in **FIG. 4**. This spacer layer **17** may then be anisotropically removed to leave spacers **24** as shown in **FIG. 5**.

[**0019**] Following the formation of the spacers **24**, an ion, plasma, or other directional removal process may then be employed to form a groove **26** through the charge trapping layer **12** as shown in **FIG. 5**. A gate dielectric **28** is then formed in the groove **26** on substrate **11**. Suitable gate dielectrics **28** may be composite structures having multiple layers of distinct materials, or may be fashioned of a single monolithic layer of a single material. Materials from which the gate dielectric **28** may be fashioned include, but are not limited to, high-K materials, metal oxides, or silicates. Some examples of these materials include silicon dioxide, SiO_xN_y, Ta_2O_5, TiO_2, Y_2O_3, CeO_2, $SrTiO_3$, Al_2O_3, La_2O_3, and silicates of hafnium and zirconium. The gate dielectric **28** may be deposited upon the substrate **11** in groove **26** using any one of a number of suitable processes including, but not limited to, physical vapor deposition (PVD), molecular beam epitaxy (MBE), sputtering, chemical solution deposition, chemical vapor deposition (CVD), thermal oxidation, and atomic layer deposition (ALD). Note that one or more adhesion or barrier layers may be formed over the gate dielectric layer and/or the charge trapping layers.

[**0020**] Once the gate dielectric **28** is formed and the spacers **24** removed, a gate conductor **30** is formed in the groove **22** as shown in **FIG. 6**. The gate conductor **30** may be formed of any suitable conductor that is compatible with the materials used in the construction of the field effect transistor **10** and the processes used in its manufacture. In one embodiment, polysilicon is used to form the gate conductor **30**. Note that polysilicon used to form the gate conductor **30** may be doped during or after the formation of the gate conductor **30**. Other materials that may be used, either by themselves, or as part of a multilayered or composite gate conductor structure include, but are not limited to suitable metals, metal silicides, conductive metal oxides, conductive metal nitrides, and the like. Some specific examples of suitable gate conductor materials include, Nb, Ir, Os, Ru and its oxide, Ta, TaN, TiN, Mo, W, Ni, and Pt. After deposition of the gate conductor **30**, by, for example, PVD or another suitable process, the top surface of the gate conductor **30** may be planarized back. The sacrificial layer **16** is then removed using a suitable stripping process such as a chemical wet stripping process, a plasma stripping process, or the like.

[**0021**] As described above, one or more intervening layers may be formed over the gate dielectric **28** and/or the charge trapping layers **12**. Such intervening layers may or may not, depending on the application, remain in place after the gate conductor **30** is formed overlying the gate dielectric **28** and/or charge trapping layers **12**. These intervening layers may include adhesion layers or barrier layers that provide or promote compatibility between device layers, protect against the migration of reactive materials, improve reliability of the device, etc.

[0022] Once the sacrificial layer **16** has been removed, a final removal step may be undertaken to trim the charge trapping layers **12***a* and **12***b* and any remaining portions of the etch stop layer **14**, if present, flush with the sides of the gate conductor **30**. This etching step is preferably carried out using a suitable directional dry etching process. Where appropriate, the gate conductor **30** may itself be used as the mask for this etching step, or a photoresist layer (not shown) may be applied and developed to provide a suitable mask for the etch. Once the structure of the field effect transistor **10** has been completed, source **34** and drain **36** may be formed by doping the substrate **11** with a suitable dopant such as boron, for a p-type transistor, or phosphorus or arsenic, for an n-type transistor.

[0023] **FIG. 7** is a simplified block diagram of a memory device **100** that incorporates a memory cell/field effect transistor **10** according to the present invention. Memory device **100** includes charge pump circuitry **102** to provide voltages of a predetermined level, such as a programming voltage (Vpp), to memory cells within a memory array **110** during memory operations. Control circuitry **104** is provided to control access to the memory array **110**. An address register **106** is used to receive address requests to memory array **110**. In addition, an input/output (I/O) buffer **108** is used to smooth out the flow of data to and from the memory array **110**. Sense amplifier and compare circuitry **120** is used to sense data stored in the memory cells and verify the accuracy of stored data.

[0024] **FIG. 7** also illustrates an exterior processor **150**, or memory controller, electrically coupled to memory device **100** for memory accessing as part of an electronic system. Processor **150** is coupled to the control circuitry **104** to supply control commands. Processor **150** is also coupled to the address register to supply address requests. Moreover, processor **150** is coupled to the **110** buffer **108** to send and receive data.

[0025] Non-volatile memory cells in accordance with the invention are suitable for use in a variety of memory array types. One example is a NAND memory array. **FIG. 8** is a schematic of a NAND memory array **200** as a portion of memory array **110** in accordance with another embodiment of the invention. As shown in **FIG. 8**, the memory array **200** includes word lines **202**$_1$ to 202$_N$ and intersecting local bit lines **204**$_1$ to 204$_M$. For ease of addressing in the digital environment, the number of word lines **202** and the number of bit lines **204** are each some power of two, e.g., 256 word lines **202** by 4,096 bit lines **204**. The local bit lines **204** are coupled to global bit lines (not shown) in a many-to-one relationship.

[0026] Memory array **200** includes NAND strings **206**$_1$ to **206**$_M$. Each NAND string includes field effect transistors **10**$_1$ to **10**$_N$, each located at an intersection of a word line **202** and a local bit line **204**. The field effect transistors **10** represent non-volatile memory cells for storage of data. The field effect transistors **10** of each NAND string **206** are connected in series source to drain between a source select gate **210** and a drain select gate **212**. The source and drain select gates **210**, **212** may be field effect transistors constructed according to an embodiment of the present invention or may be another suitable device. Each source select gate **210** is located at an intersection of a local bit line **204** and a source select line **214**, while each drain select gate **212** is located at an intersection of a local bit line **204** and a drain select line **215**.

[0027] A source of each source select gate **210** is connected to a common source line **216**. The drain of each source select gate **210** is connected to the source of the first field effect transistor **10** of the corresponding NAND string **206**. For example, the drain of source select gate **210**$_1$ is connected to the source of field effect transistor **10**$_1$ of the corresponding NAND string **206**$_1$. A control gate **220** of each source select gate **210** is connected to source select line **214**.

[0028] The drain of each drain select gate **212** is connected to a local bit line **204** for the corresponding NAND string at a drain contact **228**. For example, the drain of drain select gate **212**$_1$ is connected to the local bit line **204**$_1$ for the corresponding NAND string **206**$_1$ at drain contact **228**$_1$. The source of each drain select gate **212** is connected to the drain of the last field effect transistor **10** of the corresponding NAND string **206**. For example, the source of drain select gate **212**$_1$ is connected to the drain of field effect transistor **10**$_N$ of the corresponding NAND string **206**$_1$.

[0029] As described above in conjunction with **FIGS. 1-6**, the field effect transistors **10** include a source **34** and a drain **36**, and a control gate **30**, as shown in **FIG. 1**. Field effect transistors **10** have their control gates **30** coupled to a word line **202**. A column of the field effect transistors **10** are those NAND strings **206** coupled to a given local bit line **204**. A row of the field effect transistors **10** are those transistors commonly coupled to a given word line **202**.

[0030] Another example of an array type suitable for use with memory cells in accordance with the invention is a NOR memory array. **FIG. 9** is a schematic of a NOR memory array **300** as a portion of memory array **110** of **FIG. 7** in accordance with another embodiment of the invention. Memory array **300** includes word lines **302**$_1$ to **302**$_P$ and intersecting local bit lines **304**$_1$ to 304$_Q$. For ease of addressing in the digital environment, the number of word lines **302** and the number of bit lines **304** are each some power of two, e.g., 256 word lines **302** by 4,096 bit lines **304**. The local bit lines **304** are coupled to global bit lines (not shown) in a many-to-one relationship.

[0031] Field effect transistors **10** are in this embodiment located at each intersection of a word line **302** and a local bit line **304**. The field effect transistors **10** represent non-volatile memory cells for storage of data. As described above, typical construction of such field effect transistors **10** includes a source **34** and a drain **36**, and a control gate **30**.

[0032] Field effect transistors **10** having their control gates **30** coupled to a word line **302** typically share a common source depicted as array source **318**. As shown in **FIG. 9**, field effect transistors **10** coupled to two adjacent word lines **302** may share the same array source **318**. Field effect transistors **10** have their drains **36** coupled to a local bit line **304**. A column of the field effect transistors **10** includes those transistors commonly coupled to a given local bit line **304**. A row of the field effect transistors **10** includes those transistors commonly coupled to a given word line **302**.

[**0033**] To reduce problems associated with high resistance levels in the array source **318**, the array source **318** is regularly coupled to a metal or other highly conductive line to provide a low-resistance path to ground. The array ground **320** serves as this low-resistance path.

[**0034**] It is to be noted that the memory cells of memory arrays **200**, **300** may be programmed to correspond to single bit or multi-bit operation. Programming and sensing of charge-trapping memory cells is well understood in the art and will not be detailed herein.

CONCLUSION

[**0035**] The formation of memory cells having a stepped gate have been described herein to facilitate increases in charge trapping capacity generally independent of gating characteristics. Although specific embodiments have been illustrated and described herein it is manifestly intended that this invention be limited only by the following claims and equivalents thereof.

What is claimed is:

1. A non-volatile memory cell, comprising:

a stepped gate dielectric disposed on a semiconductor substrate, the stepped gate dielectric comprising:

two charge trapping dielectrics disposed on the semiconductor substrate, the charge trapping dielectrics being spaced apart from one another; and,

a distinct gate dielectric disposed on the semiconductor substrate between the charge trapping dielectrics so as to entirely separate the charge trapping dielectrics;

a gate conductor disposed over the stepped gate dielectric; and,

source/drain regions formed in the semiconductor substrate at opposing ends of the stepped dielectric.

2. The non-volatile memory cell of claim 1 wherein the charge trapping dielectrics comprise multiple component layers of dielectric material.

3. The non-volatile memory cell of claim 2 wherein the charge trapping dielectrics comprise a first component layer of silicon dioxide and a second component layer of silicon nitride.

4. The non-volatile memory cell of claim 1 wherein the gate dielectric is at most the same thickness as the charge trapping dielectrics.

5. The non-volatile memory cell of claim 1 wherein the gate dielectric and the charge trapping dielectrics are fashioned of different materials.

6. The non-volatile memory cell of claim 1 wherein the gate dielectric and the charge trapping dielectrics are fashioned of the same materials and wherein the thickness of the gate dielectric and charge trapping dielectrics are different.

7. The non-volatile memory cell of claim 1 further comprising an etch stop layer disposed between the charge trapping dielectrics and the gate conductor.

8. The non-volatile memory cell of claim 1 wherein the non-volatile memory cell is adapted to store a single bit of data.

9. The non-volatile memory cell of claim 1 wherein the non-volatile memory cell is adapted to store multiple bits of data.

10. The non-volatile memory cell of claim 1 wherein the non-volatile memory cell is part of a NOR memory array.

11. The non-volatile memory cell of claim 1 wherein the non-volatile memory cell is part of a NAND memory array.

12. A method of fabricating a non-volatile memory cell, comprising:

forming a charge trapping dielectric layer on a semiconductor substrate;

forming a first sacrificial layer over the charge trapping dielectric layer;

applying a mask to the sacrificial layer to define the lateral boundaries of a groove;

removing that portion of the first sacrificial layer within the lateral boundaries defined by the mask to form the groove, the groove having a lower boundary that is substantially the upper surface of the charge trapping dielectric layer;

forming a second sacrificial layer over the first sacrificial layer and the exposed charge trapping dielectric layer;

forming a pair of spacers within the groove by anisotropically removing a portion of the second sacrificial layer, the pair of spacers being positioned against the respective lateral edges of the groove and defining therebetween the lateral boundaries of a trench within the groove;

removing the material of the charge trapping layer between the lateral boundaries defined by the spacers to form a trench, the trench having a lower boundary that is substantially the upper surface of the semiconductor substrate;

depositing a gate dielectric layer in the trench;

removing the spacers from the groove;

forming a control gate layer overlying the charge trapping dielectric layer and the gate dielectric layer within the groove formed in the first sacrificial layer; and,

patterning the control gate layer and the remainder of the charge trapping control layers that extend beyond the lateral edges of the control gate layer.

13. The method of fabricating a non-volatile memory cell of claim 12 further comprising the step of forming an etch stop layer over the charge trapping dielectric layer.

14. The method of fabricating a non-volatile memory cell of claim 13 wherein the etch stop layer is substantially removed during the formation of the groove in the first sacrificial layer.

15. The method of fabricating a non-volatile memory cell of claim 13 wherein at least a portion of the etch stop layer remains after the formation of the groove in the first sacrificial layer.

16. The method of fabricating a non-volatile memory cell of claim 12 wherein the charge trapping dielectric layer is comprised of a first component layer and a second component layer.

17. The method of fabricating a non-volatile memory cell of claim 16 wherein the first component layer of the charge trapping dielectric layer is of silicon dioxide and the second component layer of the charge trapping dielectric layer is of silicon nitride.

18. The method of fabricating a non-volatile memory cell of claim 12 wherein the gate dielectric layer is no thicker than the charge trapping dielectric layer.

19. A memory device, comprising:

an array of non-volatile memory cells; and

circuitry for control and/or access of the array of non-volatile memory cells;

wherein the at least one memory cell of the array of non-volatile memory cells comprises:

a stepped gate dielectric disposed on a semiconductor substrate, the stepped gate dielectric comprising:

two charge trapping dielectrics disposed on the semiconductor substrate, the charge trapping dielectrics being spaced apart from one another; and,

a distinct gate dielectric disposed on the semiconductor substrate between the charge trapping dielectrics so as to entirely separate the charge trapping dielectrics;

a gate conductor disposed over the stepped gate dielectric; and,

source/drain regions formed in the substrate at opposing ends of the stepped dielectric, the respective source/drain regions being in conductive contact with the respective charge trapping dielectrics.

20. An electronic system, comprising:

a processor; and

an array of non-volatile memory cells; and

circuitry for control and/or access of the array of non-volatile memory cells;

wherein the at least one memory cell of the array of non-volatile memory cells comprises:

a stepped gate dielectric disposed on a semiconductor substrate, the stepped gate dielectric comprising:

two charge trapping dielectrics disposed on the semiconductor substrate, the charge trapping dielectrics being spaced apart from one another; and,

a distinct gate dielectric disposed on the semiconductor substrate between the charge trapping dielectrics so as to entirely separate the charge trapping dielectrics;

a gate conductor disposed over the stepped gate dielectric; and,

source/drain regions formed in the substrate at opposing ends of the stepped dielectric, the respective source/drain regions being in conductive contact with the respective charge trapping dielectrics; and,

circuitry for control and/or access of the array of non-volatile memory cells.

21. A memory cell, comprising:

first and second charge trapping layers overlying a semiconductor substrate;

a gate dielectric layer overlying the semiconductor substrate and interposed between the first and second charge trapping layers, wherein the first and second charge trapping layers each extend above the gate dielectric layer; and

a control gate layer overlying the gate dielectric layer and the first and second charge trapping layers.

22. The memory cell of claim 21, wherein the first and second charge trapping layers comprise a dielectric material.

23. The memory cell of claim 22, wherein the dielectric material is selected from the group consisting of silicon dioxide, silicon nitride, Al_2O_3, HfO_2, HfON, HfOSiN, and Ta_2O_5.

24. The memory cell of claim 21, wherein the control gate layer comprises one or more layers of conductive material.

25. The memory cell of claim 21, further comprising one or more adhesion or barrier layers between the gate dielectric layer and the control gate layer.

26. The memory cell of claim 21, wherein the gate dielectric layer and the first and second charge trapping layers are overlying and adjoining the semiconductor substrate.

27. The memory cell of claim 21, wherein the control gate layer is overlying and adjoining the gate dielectric layer and the first and second charge trapping layers.

28. A memory cell, comprising:

first and second charge trapping layers overlying a semiconductor substrate;

a gate dielectric layer overlying the semiconductor substrate and interposed between the first and second charge trapping layers; and

a control gate layer overlying and adjoining the gate dielectric layer and the first and second charge trapping layers.

29. A method of forming a memory cell, comprising:

forming a first dielectric layer overlying a semiconductor substrate;

forming and patterning a hard mask layer overlying the first dielectric layer, thereby exposing a first portion of the first dielectric layer bounded by sidewalls of the hard mask layer;

forming spacers on the sidewalls of the hard mask layer, leaving a central portion of the first portion of the first dielectric layer exposed between the spacers;

removing the central portion of the first portion of the first dielectric layer, thereby exposing a portion of the substrate;

forming a second dielectric layer on the exposed portion of the substrate;

removing the spacers from the sidewalls of the hard mask layer;

forming a control gate layer overlying the first and second dielectric layers;

removing the hard mask layer; and,

forming source and drain regions in the substrate on opposing sides of the control gate layer.

30. The method of claim 29, wherein the method is performed in the order presented.

31. The method of claim 29, wherein forming the first dielectric layer further comprises:

forming a first layer of dielectric material overlying and adjoining the substrate; and

forming a second layer of dielectric material overlying and adjoining the first layer of dielectric material.

* * * * *