Title: HIGH PERFORMANCE DOUBLE-GATE LATCH

Abstract: A differential circuit to be used as a latch-up for asymmetric-double-gate complementary metal oxide semiconductor (DGCMOS) devices is provided. Specifically, the differential circuit comprises an asymmetric-DGCMOS device having the weak gates tied to input circuitry and strong gates that are used in cross-coupling.
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HIGH PERFORMANCE DOUBLE-GATE LATCH

Field of the Invention

The present invention relates to asymmetric-double-gate complementary metal oxide semiconductor (DGCMOS) devices, and more particularly to an asymmetric-DGCMOS device wherein a cross-coupled latch is employed which substantially reduces body-to-source/drain parasitic capacitances as well as structural body resistance parasitics of the asymmetric-DGCMOS device. The inventive DGCMOS device design provides a lower power, higher performance DGCMOS device than heretofore possible with prior art DGCMOS devices.

Background of the Invention

Asymmetric-double-gate complementary metal oxide semiconductor (DGCMOS) technology is considered to be the leading candidate to extend high-performance CMOS technology beyond 0.1 μm lithography and below 1.0 V power supply. Asymmetric-double-gate MOSFET (See, for example, T. Tanaka, et al., "Ultrafast Low-Power Operation of a p+-n+ Double-Gate SOI MOSFETS", 1994 Symposium on VLSI Technology Digest of Technical Papers, pp. 11-12) consists of a fully depleted double-gate MOSFET in which the two gate electrodes consist of dissimilar conductors, typically n+ and p+ doped polysilicon. A typical prior art asymmetric-double-gate device is shown, for example, in FIGS 1A and 1B. Since the two electrodes have differing Fermi levels, one of the two electrodes will prove more attractive to the channel inversion layer, when formed, and thus will exert stronger control of the conduction channel. The electrode which proves more attractive to the inversion carriers is referred to as the "strong" gate and the electrode which proves less attractive is referred to as the "weak" gate.

Conventional CMOS circuits in DGCMOS technology gain from increased effective $V_{ds}/V_t$ ratio due to the ideal sub-threshold swing and improved short-channel $V_t$ control compared to conventional CMOS. It is noted that the term "$V_{ds}$" is used herein to denote the power supply voltage of the device, whereas the term "$V_t$" denotes the threshold voltage of the device. Despite the above-mentioned improvements, the effective $V_{ds}/V_t$ ratio of prior art DGCMOS devices must degrade with $V_{ds}$ scaling.
Various attempts to further improve the effective $V_{th}/V_t$ ratio of DCGMOS devices to limits that are within conventional scaling expectations have been developed. One such attempt is disclosed, for example, in Fuse, et al., "0.5V SOI CMOS Pass-Gate Logic", Slide Supplement for the 1996 IEEE International Solid-State Circuits Conference, Page 71. Specifically, the Fuse, et al. publication discloses a DCGMOS design wherein a variant on dynamic threshold CMOS (DTCMOS) technology is employed. Specifically, the Fuse, et al. publication provides a DTCMOS design where the gates of the nFETs (field effect transistors) are connected to the bodies of the latch pFETs. The input-body connection scheme employed in Fuse, et al. is shown in FIGS 2-3. This prior art scheme includes an inverter with cross-coupled pull-up pMOSFETs. FIG 2 illustrates a prior art connection scheme without body-bias controlling, while FIG 3 shows a prior art connection scheme with body-bias controlling. In each of FIGS 2 and 3, reference numeral 10 is used to represent pMOSFETs, reference numeral 12 is used to represent an inverter, and reference numerals 14 and 16 are used to denote the point at which cross-coupling between adjacent pMOSFETs occurs.

Dynamic threshold complementary metal oxide semiconductor (DTCMOS) circuits, such as illustrated above and further described in the Fuse, et al. publication, unfortunately suffer from inherent body-to-source and body-to-drain parasitic capacitances as well as structural body resistance parasitics. These parasitics cause an undesirable increase in the gate input capacitance of the device since all the body of the MOSFET serves as a gate electrode. Moreover, in prior art DTCMOS devices, the source and drain regions are only isolated from the switched body by silicon depletion regions that have a high dielectric constant (on the order of about 11.7) associated therewith. A detailed discussion concerning the drawbacks associated with dynamic threshold CMOS circuits can be found, for example, in C. Wann, et al., "Channel Profile Optimization and Device Design for Low-Power High-Performance Dynamic-Threshold MOSFET". IEEE 96-113.

Due to the above-mentioned disadvantages of the DTCMOS devices, the use of these devices to improve the effective $V_{th}/V_t$ ratio presents significant shortcomings for power and delay reductions with $V_{th}$ scaling (reduction); therefore alternative solutions for improving effective $V_{th}/V_t$ ratio without causing any substantial body-to-source or body-to-drain parasitic capacitances nor body parasitic resistances are needed. Such a solution may lead to extending high-performance CMOS technology beyond 0.1 μm lithography and below 1.0 V power supply ranges.
Disclosure of the Invention

Brief Description of the Drawings

The invention will now be described by way of example only, with reference to the accompanying drawings, in which:

FIGS 1A (side view) and 1B (top view) are pictorial representations of a prior art asymmetric-double-gate device;

FIG 2 is a circuit diagram of a prior art input-body connection scheme without body-bias coupling, as described in the Fuse, et al. publication mentioned hereinabove;

FIG 3 is a circuit diagram of a prior art input-body connection scheme without body-bias coupling, as described in the Fuse, et al. publication mentioned hereinabove; and

FIG 4 is a circuit diagram of the inventive differential circuit of the present invention wherein the weak gates of the asymmetric-DGCMOS device are tied to input circuitry and the strong gates of the pFETs of the DGCMOS device are employed for cross-coupling.

Detailed Description of the Invention

As stated above, the present invention broadly provides a differential circuit which comprises an asymmetric-double-gate device containing a pair of series coupled pFETs and nFETs, each pFET and nFET having weak gates and strong gates associated therewith, wherein the weak gates of the nFETs and the pFETs are tied to input circuitry, and the strong gates of the pFETs are used for cross-coupling. The inventive circuit is shown, for example, in FIG 4 of the present invention.

Specifically, FIG 4 is a schematic diagram of inventive differential circuit 50 which includes pFET 52 tied in series to nFET 56 and pFET 54 tied in series to nFET 58. Both series coupled pFET and nFET form a DGCMOS device. As is shown in FIG 4, each pFET is also coupled to a Vdd power supply and each nFET is coupled to ground, Gnd. Moreover, in the illustrated circuit, each pFET and nFET includes a weak gate (60, 62, 64 and 66) and a strong gate (68, 70, 72 and 74).
Accordingly, the present invention provides a differential circuit which comprises an asymmetric-double-gate device having a pair of series coupled pFETs and nFETs, each pFET and nFET having weak gates and strong gates associated therewith, wherein the weak gates of the nFETs and the pFETs are tied to input circuitry, and the strong gates of said pFETs are used for cross-coupling.

The term "weak gate" is used herein to denote a gate of a FET (pFET or nFET) which has less influence on the FET channel portion by virtue of its less attractive (to the channel carriers) Fermi level with respect to the "strong gate", which, in turn, has a greater influence on the FET channel potential by virtue of its more attractive Fermi level (to the channel carriers). Specifically, and as shown in FIG 4, the gates facing outward (e.g., the right gates of the right hand side FETs and the left gates of the left hand side of the FETs) are the weak gates of the differential circuit. The strong gates, on the other hand, are those gates that are found in the interior region of the circuit between the two pair of series coupled nFETs and pFETs (e.g., the left gates of the right hand side FETs and the right gates of the left hand side FETs). It is noted that the above design is a feature uniquely suited to asymmetric-DGCMOS devices and suffers significant disadvantages with DTCMOS devices.

In differential circuit 50, the weak gates of the FETs, i.e., 60, 62, 64 and 66, are tied up to input circuitry which is referenced in FIG 4 by the term "Input". The strong gates of the nFETs are coupled to the corresponding weak gate of the pFET as well as the input circuitry. That is, strong gate 70 of nFET 56 is coupled to weak gate 60 of pFET 52 and strong gate 74 of nFET 58 is coupled to weak gate 64 of pFET 54. In FIG 4, reference numerals 76 and 78 represent the nodes wherein the weak gates (60, 62, 64 and 66) and strong gates (70 and 74) are coupled to the input circuitry.

Insofar as strong gate 66 of pFET 52 and strong gate 72 of pFET 54 are concerned, those strong gates are used as a cross-coupled latch as shown in FIG 4. Specifically, strong gate 66 of pFET 52 is cross-coupled to the adjacent coupled pFET and nFET through node 82, whereas strong gate 72 of pFET 54 is cross-coupled to the adjacent coupled pFET and nFET through node 80. Nodes 80 and 82 lead to output regions which are labeled simply as "output" in FIG 4.
It is noted that in the above-described differential circuit, the $V_t$ of each pFET is substantially modified by the input state. When 'input' is high, then the right hand side pFET has high $V_t$ and the left hand side pFET has low $V_t$ (since input is low). Moreover, the inventive differential circuit provides an improvement over the prior art DTCMOS solution described in the Fuse, et al. publication mentioned above because the DTCMOS solution of the prior art intrinsically has a much higher gate input capacitance than the inventive circuit since all the body serves as a gate electrode in DTCMOS. The increased capacitance obtained using the DTCMOS circuit disclosed in Fuse, et al. is caused by the source and drain being isolated from the switched body by silicon depletion regions having a dielectric constant of about 11.7, See, for example, the article to C. Wann, et al. mentioned supra.
CLAIMS

1. A differential circuit which comprises an asymmetric-double-gate device (50) having a pair of series coupled pFETs (52, 54) and nFETs (56, 58), each pFET and nFET having weak gates (60, 62, 64, 66) and strong gates (68, 70, 72, 74) associated therewith, wherein the weak gates (60, 62, 64, 66) of the nFETs and the pFETs are tied to input circuitry, and the strong gates (68, 72) of said pFETs are used for cross-coupling.

2. A differential circuit as claimed in Claim 1 wherein each of said nFETs (56, 59) are further coupled to ground.

3. The differential circuit as claimed in Claim 1 wherein each of said pFETs (52, 54) are further coupled to a power supply source.

4. A differential circuit as claimed in Claim 1 wherein the strong gates (70, 74) of said nFETs (56, 58) are coupled to input circuitry.

5. A differential circuit as claimed in Claim 1 wherein the strong gates (70, 74) of said nFETs (56, 58) are coupled to the weak gates of said series coupled pFET.

6. A differential circuit as claimed in Claim 1 wherein said cross-coupling occurs at a node on an adjacentely series coupled pFET and nFET.

7. A differential circuit as claimed in Claim 1 wherein said device is scalable to below about 0.1 µm.

8. A differential circuit as claimed in Claim 1 wherein said device operates at a voltage of below about 1 V.

9. A differential circuit as claimed in Claim 1 wherein said cross-coupling leads to output circuitry.
FIG. 1A
(PRIOR ART)

10nm Si body
p+ gate
n+ gate
Gate oxide
OXIDE

FIG. 1B
(PRIOR ART)

drain(n+ for nFET; p+ for pFET)
10nm Si body
Gate oxide
p+ gate
n+ gate
source(n+ for nFET; p+ for pFET)