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[21] Appl. No. 760,508
[22] Filed Sept. 18, 1968
[45] Patented Jan. 19, 1971
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[54] DIGITALLY CONTROLLED ANALOG
FUNCTION GENERATOR
21 Claims, 10 Drawing Figs.
[52] U.S. Cl. 235/150.53,
235/197
[51] Int. Cl. G06j 7/26,
G06j 1/00
[50] Field of Search. 235/197,
150.5, 150.51, 150.52, 150.53; 328/142, 144
[56] References Cited
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ABSTRACT: A function generator primarily adapted for use in hybrid computing systems, wherein method and apparatus are disclosed for producing an analog output signal as a digitally selected segmental function of an independent variable analog input signal. In particular, the system involves the generation of a fundamental or base signal having a digitally selected linear gain or slope relationship with the input signal and the concurrent generation of a plurality of modifier signals having individual digitally selected discontinuous breakpoint relationships with the same input signal. The base and modifier signals are thereupon electrically summed to produce an analog output signal having the desired segmental function relationship with the input signal.

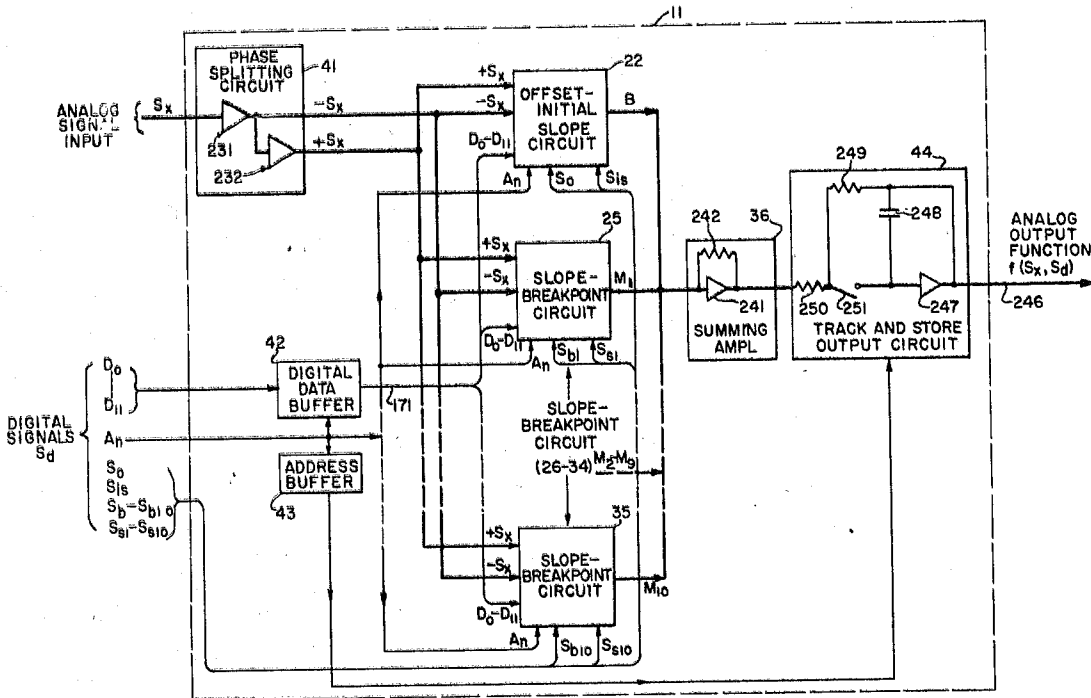


FIG. 1

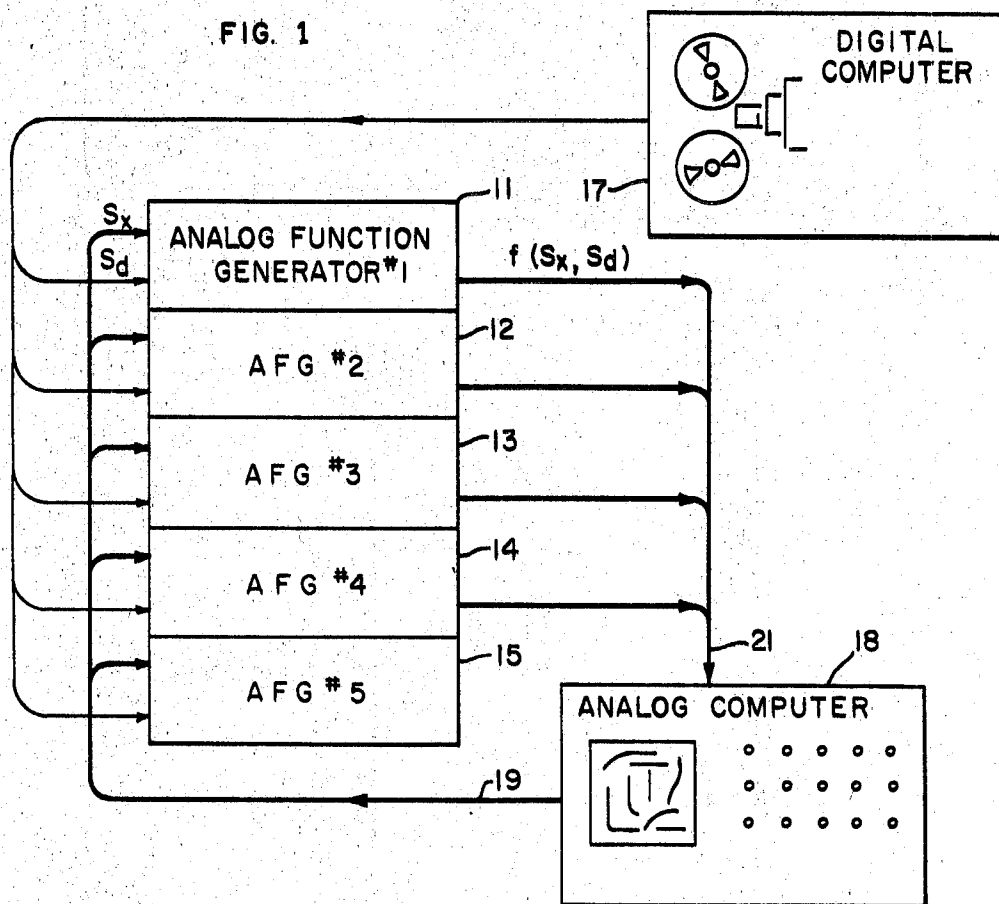
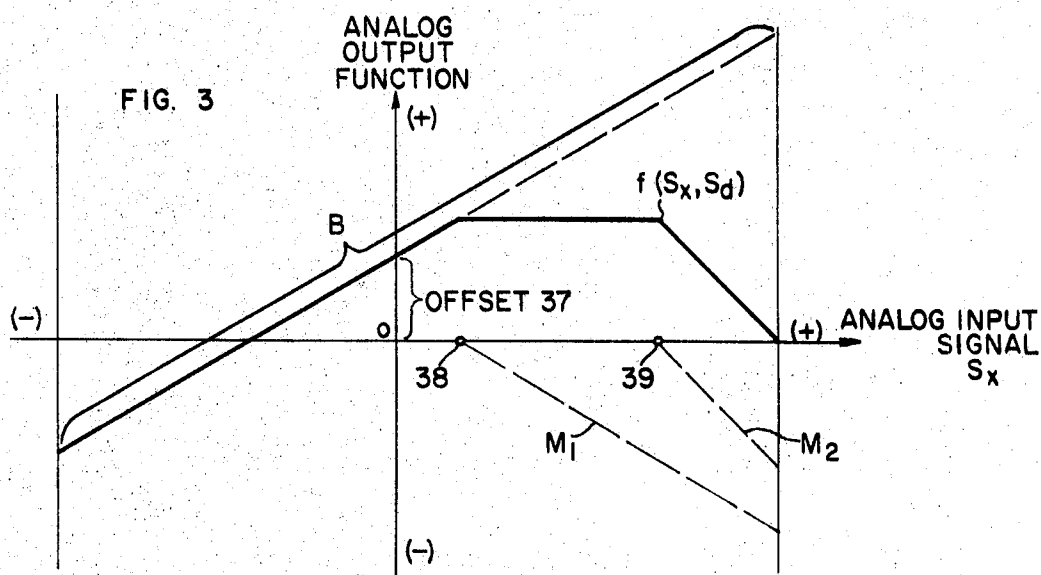
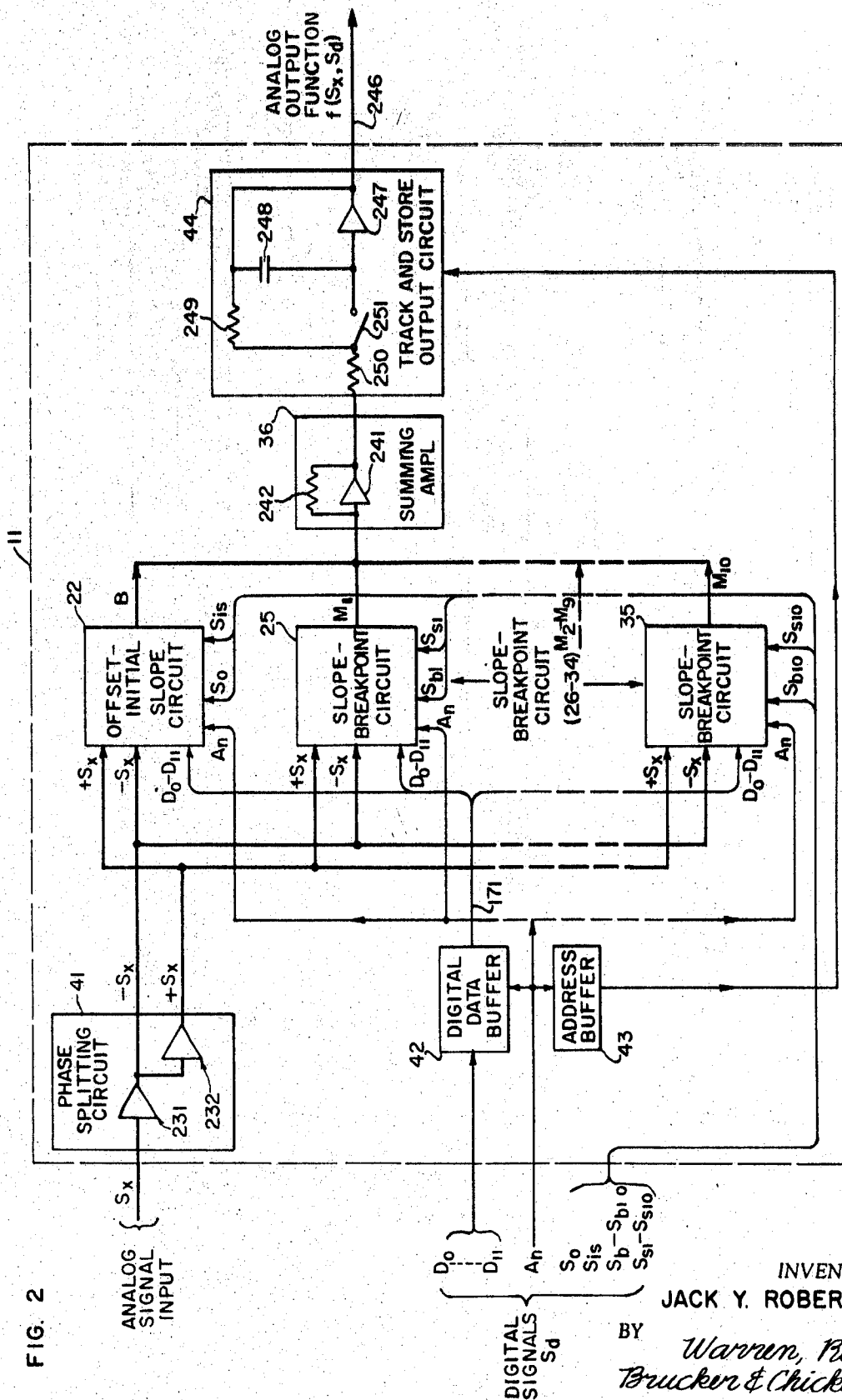


FIG. 3



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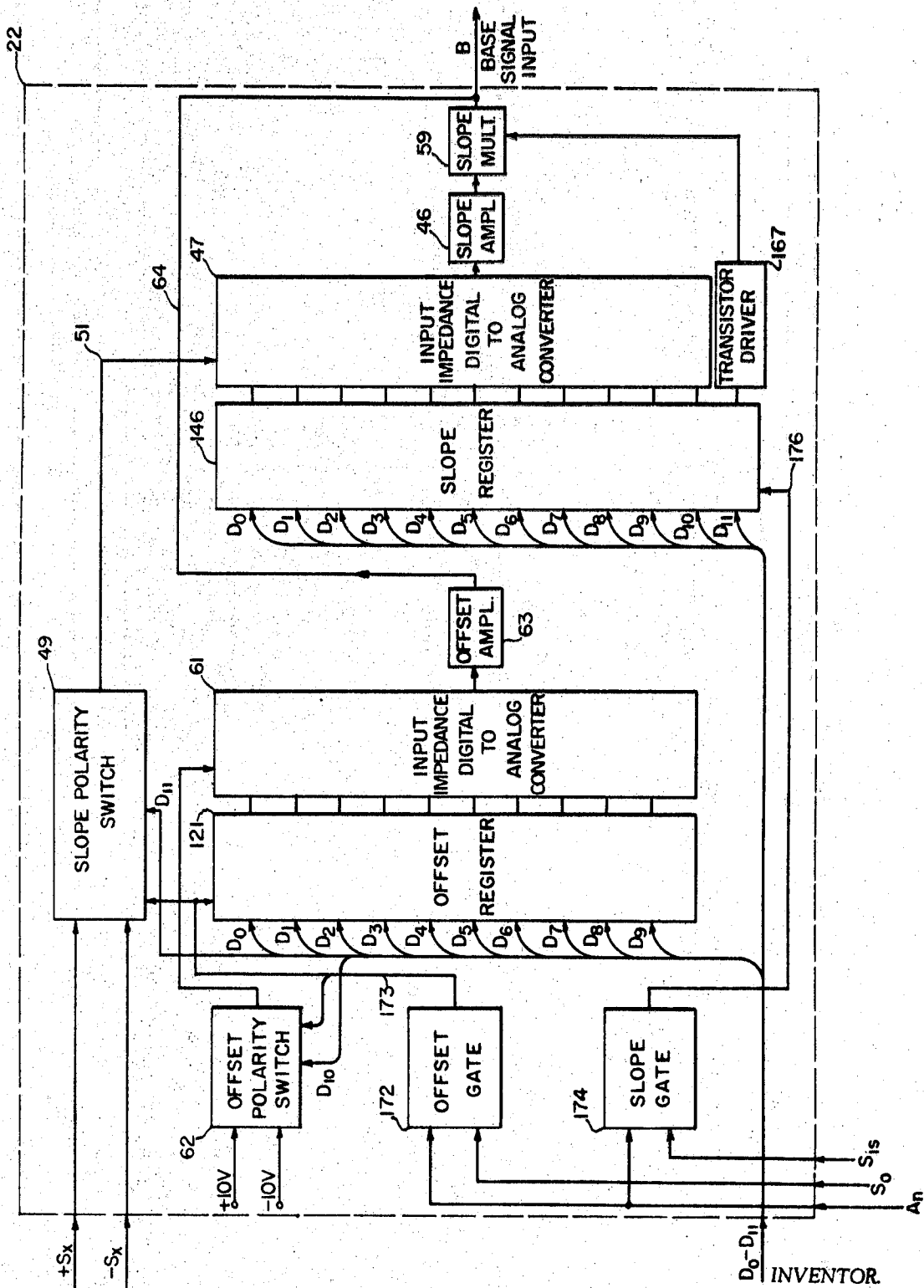


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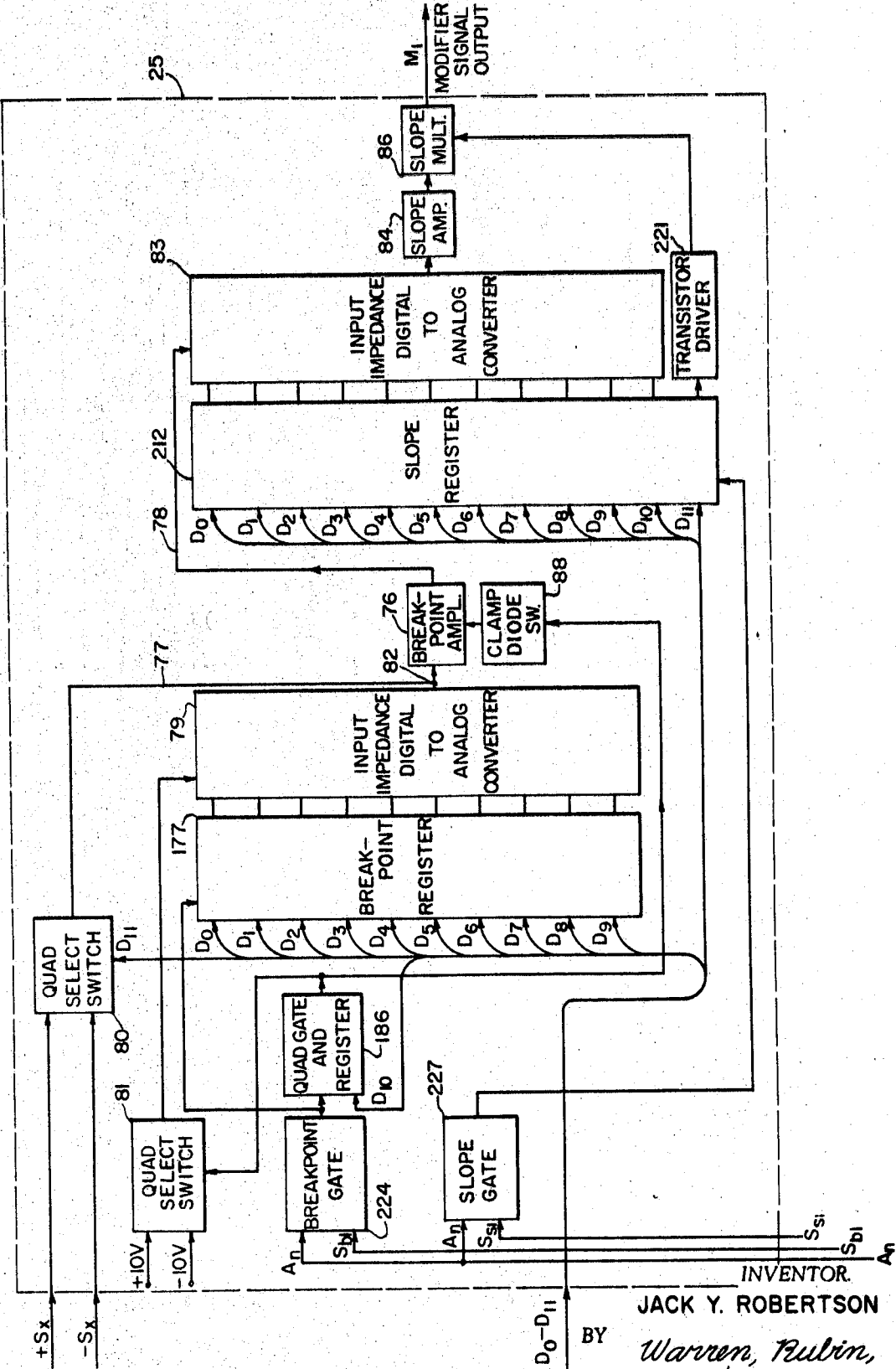
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FIG. 5



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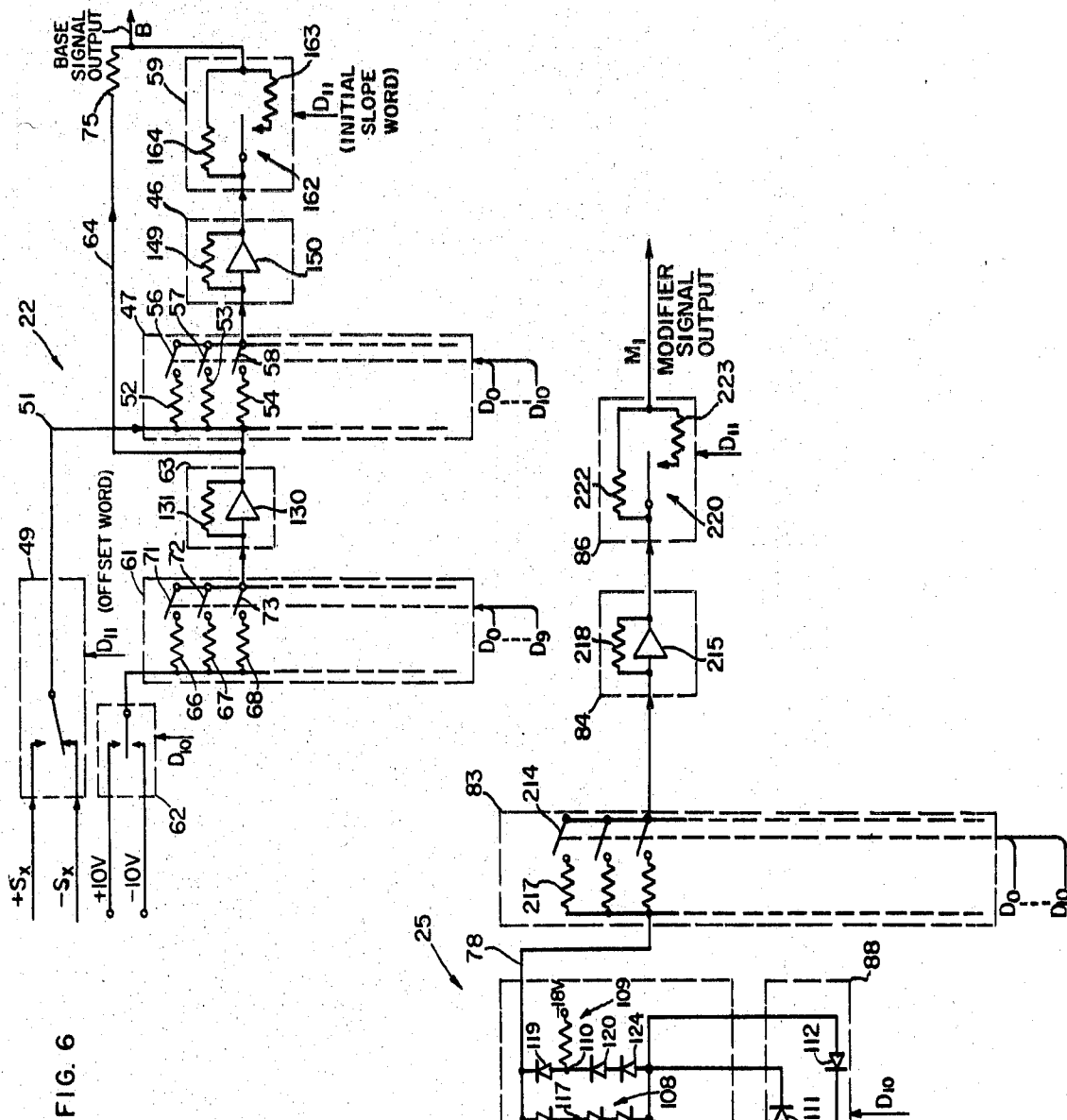
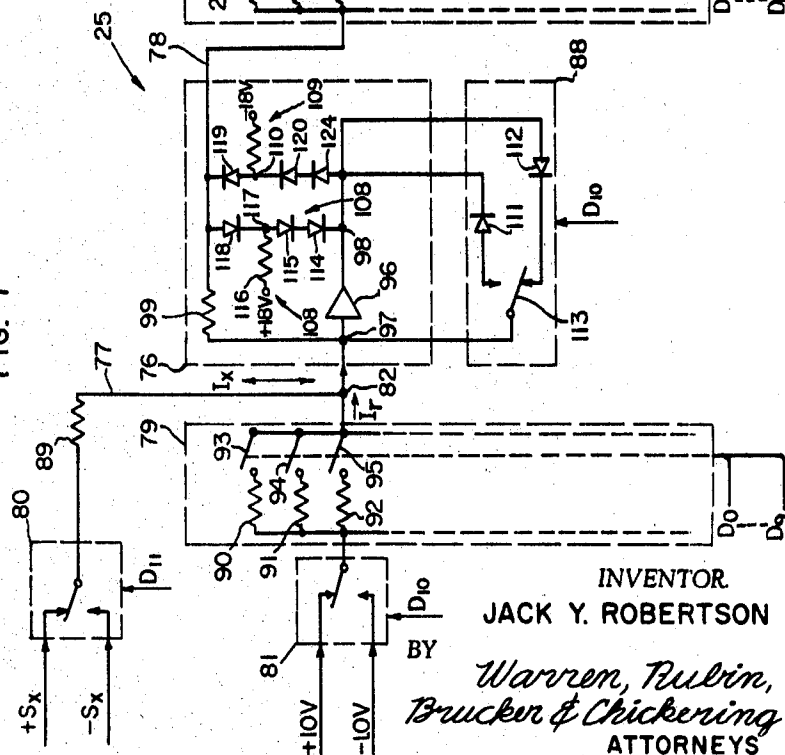


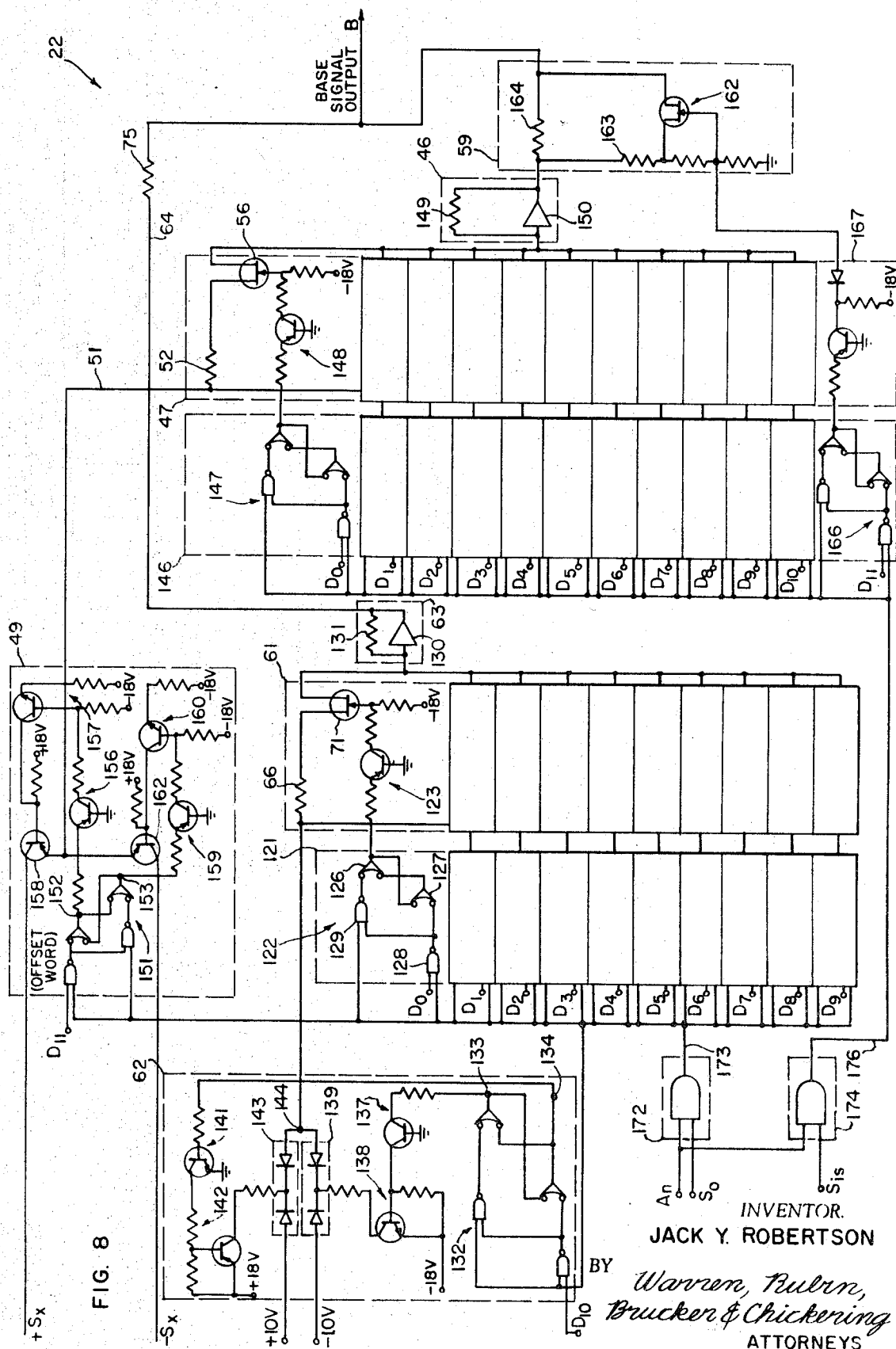
FIG. 6

FIG. 7



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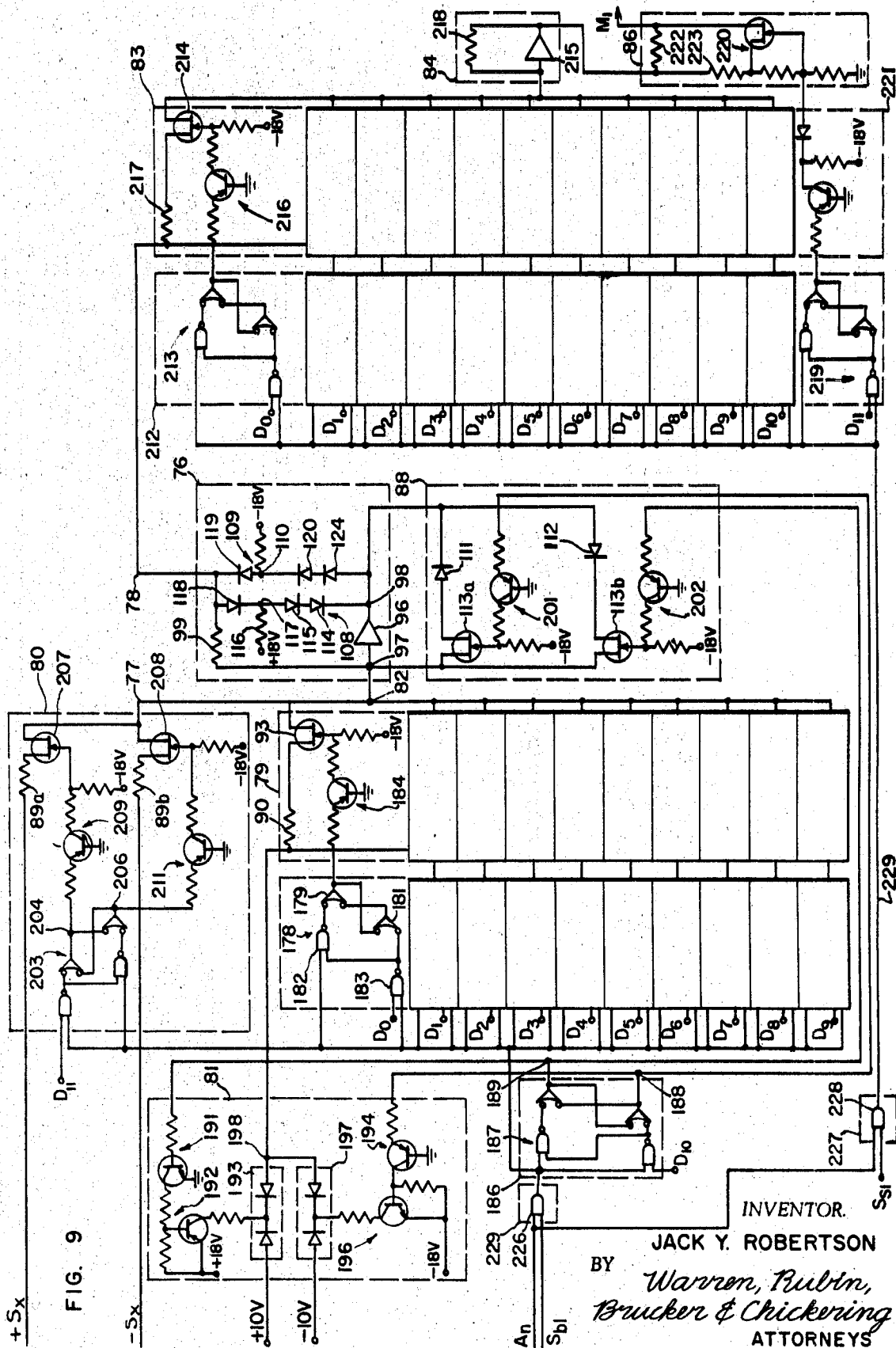
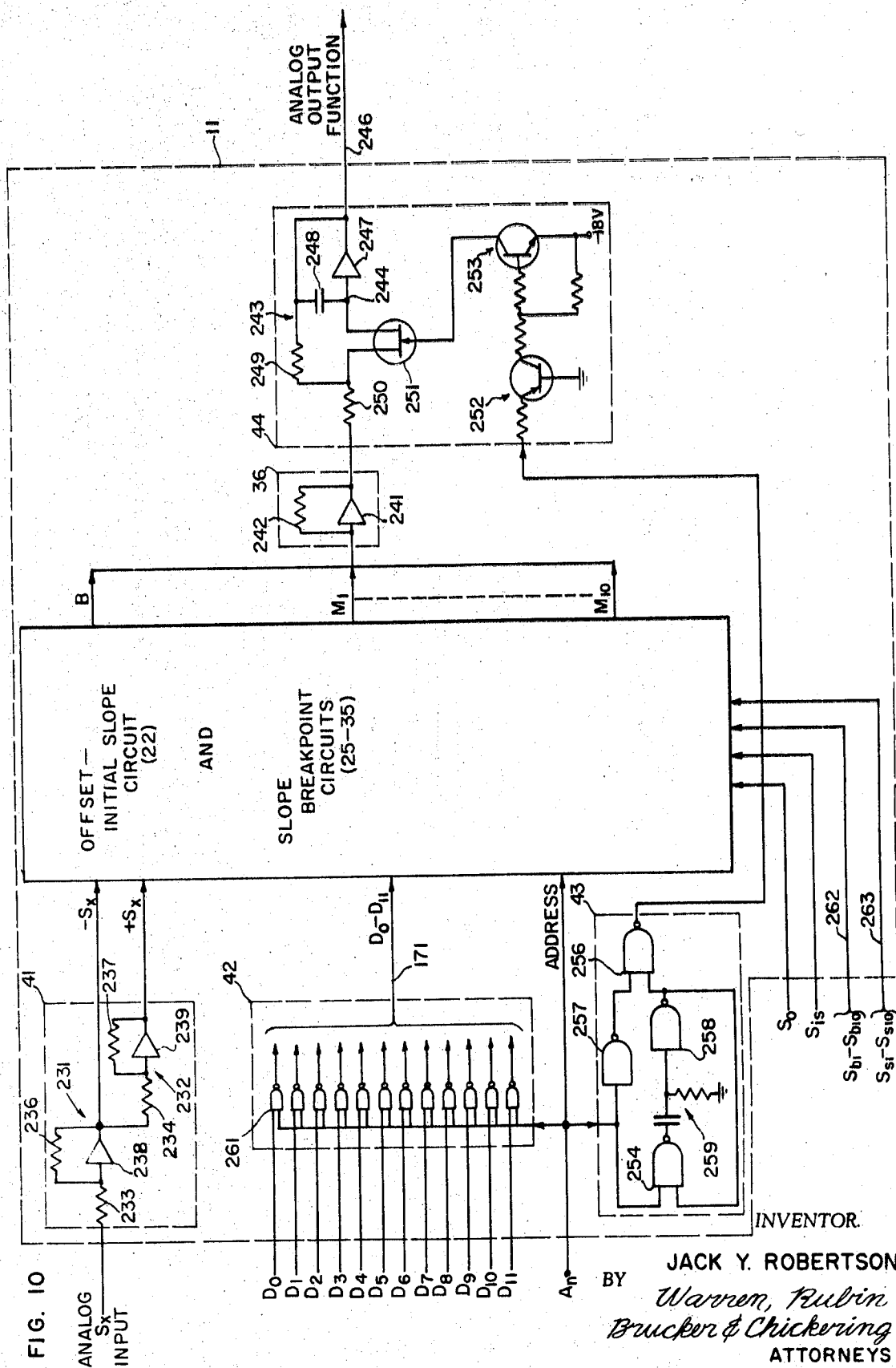


FIG. 9

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DIGITALLY CONTROLLED ANALOG FUNCTION GENERATOR

The invention relates in general to analogue methods and apparatus and particularly to a combined digital and analogue system for digitally controlling the electrical function provided by an analogue signal generator in response to an independently varying input signal.

In the computer art, it is desirable in many instances to employ the use of systems which have both digital and analogue computation capabilities. Such systems are popularly known as hybrid computer systems and permit the user to introduce both analogue data, i.e. data represented by the indiscrete amplitude of electrical signals, and digital data, i.e. data represented by a coded sequence or order of signals having only discrete states. In response to these two types of signal data, the hybrid computer concurrently performs both analogue and digital operations and at certain points in the computing sequence integrates these separate operations by means of analogue to digital and/or digital to analogue converting processes. The purpose and advantage of hybrid computing systems is to solve complex problems involving data or functions partially compatible with analogue operations and partially compatible with digital operations.

Another advantage of hybrid computers relates to their ability to solve problems involving empirical relationships which cannot be readily defined by known mathematical equations. In such cases, it is desirable to incorporate into the hybrid system, function generators which are capable of producing diverse preselected analogue output functions in response to an independently varying analogue input signal. In the past, function generators of this type have been largely noncompatible with the modern day high-speed hybrid systems, due to cumbersome and time-consuming methods for programming the desired function. As lost time in large computing systems can be extremely expensive even for minute durations, programming delays thus caused by existing analogue function generators are particularly undesirable.

In addition to the inconvenience and expensive time delays, the nonautomated programming characteristics of known function generators give rise to undesirable restraints on the full potential of hybrid computing systems. For example, due to the impracticality of changing the function output of available generators during computation, it has been necessary in the past to ignore the occurrence of slight to moderate variations in the desired function during computation. That is, the function generator is programmed to provide an approximate output which is thereafter used during the entire computing sequence. This results in a less than satisfactory approximation to the true solution.

Accordingly, it is an object of the present invention to provide a function generating method and apparatus particularly compatible with hybrid computing systems permitting faster and more accurate, dynamic solutions to complex analogue problems.

It is another object of the present invention to provide a function generating method and apparatus capable of providing an automatically and rapidly selectable analogue relationship between input and output signals.

It is a further object of the present invention to provide a digitally controlled dynamic analogue function generator exhibiting heretofore unobtainable accuracy, long term stability and wide band width and to do so at a reasonable cost.

It is still another object of the present invention to provide a method and apparatus for generating an analogue output signal having a universally selective functional relationship with an independently variable analogue input signal.

The invention possesses other objects and features of advantage, some of which of the foregoing will be set forth in the following description of the preferred form of the invention which is illustrated in the drawings accompanying and forming part of this specification. It is to be understood, however, that variations in the showing made by the drawings and description may be adopted within the scope of the invention as set forth in the claims.

FIG. 1 is a generalized block diagram showing a hybrid computing system incorporating a plurality of the digitally controlled function generators of the present invention;

FIG. 2 is a block diagram of the circuitry for one of the function generators shown in FIG. 1;

FIG. 3 is a simplified graph of the analogue signal input-output relationship provided by the function generator shown in FIG. 2;

FIG. 4 is a block diagram of one of the circuit components shown in FIG. 2;

FIG. 5 is a block diagram of another of the circuit components shown in FIG. 2;

FIGS. 6 and 7 are simplified schematic diagrams of the circuit components shown respectively in FIGS. 4 and 5;

FIG. 8 is a detailed schematic diagram of the block circuit diagram shown in FIG. 4;

FIG. 9 is a detailed schematic diagram of the block circuit diagram shown in FIG. 5; and

FIG. 10 is a combined schematic and block diagram detailing the input-output circuitry of the invention shown in block form in FIG. 2.

As the term is used herein, an analogue signal is a signal having a magnitude representative of a given or preselected quantity. A digital signal on the other hand and as used herein, refers to a signal comprised of one or more bit signals each having only discrete magnitude states. Also for the purposes of the following description, a digital signal includes any of a variety of signals generally associated with digital systems including binary words (a plurality of associated bit signals), address signals (generally a single bit signal used to drive a circuit component between one of two states) and strobe signals (generally a short duration pulse used to momentarily place a circuit component in one of two states).

In general and referring to FIG. 1, the present invention provides one or more analogue function generators, generators 11, 12, 13, 14 and 15 integrated in this instance into a hybrid computing system including a digital computer 17 and an analogue computer 18. Each of generators 11 through 15 is capable of providing an analogue output signal having a functional relationship with and in response to an input analogue signal wherein the relationship is controlled or selected by a digital signal. For example, in FIG. 1, generator 11 receives an input analogue signal S_x representing an independent variable from analogue computer 18. Generator 11 also receives a digital control signal S_d from digital computer 17. In response thereto, generator 11 issues an analogue output signal $f(S_x, S_d)$ as a function of signals S_x and S_d . The output signal is thereupon returned to analogue computer 18 for use in the analogue computation. As a brief example, assume that analogue computer 18 is programmed to calculate the vibration of an airplane wing as a function of aircraft speed. In setting up analogue computer 18 to provide such a solution, it is likely that one or more empirical relationships are involved in the computation. It is also probable that such an empirical relationship cannot be satisfactorily approximated by a known mathematical equation of the type which would permit direct analogue computation solely by computer 18. Accordingly, generator 11 may be rapidly programmed by digital computer 17 to provide a functional relationship between S_x and $f(S_x, S_d)$ approximating or equaling the empirical aerodynamic relationship. During computation computer 18 issues an independently varying analogue signal, representing the aircraft speed, over a signal path 19 and receives the desired analogue function output, representing the amplitude of wing vibration, from generator 11 over signal path 21.

As another advantageous feature of the present invention, digital computer 17 may be programmed to automatically adjust the functional relationship provided by generator 11 as the computation proceeds. For example, generator 11 may be set by digital signal S_d to provide a first empirical function for a given low range of aircraft speeds and automatically adjusts the generator to provide a different function as the simulated speed of the aircraft enters a higher range.

Referring to FIG. 2, each of function generators 11 through 15 constructed in accordance with the present invention comprises both digitally controlled linear and nonlinear circuit means responsive to the input analogue signal S_x and the digital signal S_d . For example, generator 11 comprises an offset-initial slope circuit 22 providing a digitally controlled linear circuit means responsive to S_x and S_d to produce a base analogue signal B having a digitally selected linear gain relationship with signal S_x . Additionally, generator 11 comprises a plurality of identical slope-breakpoint circuits 25, 26—34 (not shown) and 35, each providing a digitally controlled nonlinear circuit means responsive to S_x and S_d . The outputs of these slope-breakpoint circuits to produce a plurality of separate modifier signals $M_1, M_2—M_9$ (from circuits 26—34) and M_{10} , each having a digitally positioned breakpoint discontinuity with analogue signal input S_x . Each of these separate analogue signals B and $M_1—M_{10}$ are connected to the input of summing amplifier 36 providing a circuit means electronically summing the base and modifier signals to produce the analogue output signal $f(S_x, S_d)$ as a digitally selected segmental function of input signal S_x .

The result of the above operation is best illustrated in FIG. 3, wherein the analogue output signal $f(S_x, S_d)$ is plotted along the ordinate axis as a function of the input analogue signal S_x which is plotted along the abscissa axis. In this instance and by way of example, only two modifier signals shown by dotted lines M_1 and M_2 are generated and summed with base signal B.

It is noted that signal B exhibits a linear gain relationship for the entire range of $-S_x$ to $+S_x$. As described in more detail herein, circuit 22 provides for digitally selecting and controlling this linear gain or slope of base signal B. Additionally, circuit 22 provides for digitally selecting an ordinate offset 37 for base signal B which may take on a negative value or as shown in FIG. 3, a positive value measured from the origin of the axis. Thus, by operating on offset-initial slope circuit 22 by digital signal S_d , base signal B may be provided with any of a large range of positive or negative slopes and any of a large range of positive or negative ordinate offsets.

Each of slope-breakpoint circuits 25—35, produces a modifier signal such as signals M_1 and M_2 shown in FIG. 3 and produced by circuits 25 and 26. These modifier signals while being related to input signal S_x are nevertheless generated independently of one another such that each modifier signal may be individually controlled by digital signal S_d as hereinafter described. Moreover, circuits 25—35 provide a nonlinear relationship between S_x and the modifier signals evidenced in this instance by the breakpoint discontinuity between M_1, M_2 and S_x . Particularly, signal M_1 exhibits a breakpoint shown at 38 wherein M_1 is zero for all values of S_x up to breakpoint 38 and for positive values of S_x increasing beyond breakpoint 38, M_1 exhibits a linear and in this case negative slope relationship with S_x . In a similar manner, modifier signal M_2 produced by circuit 26 exhibits a breakpoint 39 for a positive value of S_x greater than breakpoint 38. Thereafter for increasing positive values of S_x , M_2 is provided with a negative linear slope relationship with S_x . While it is noted that signals M_1 and M_2 are linearly proportional to S_x for segments shown by the dotted lines and zero for other values of S_x , the overall relationship between the modifier signals and the analogue input signal is that of a nonlinear function characterized by a breakpoint discontinuity.

Having generated base signal B and each of modifier signals $M_1—M_{10}$, these signals are jointly fed to summing amplifier 36 and thereby electronically summed to produce the segmental analog output signal $f(S_x, S_d)$. The result of this operation is shown in FIG. 3, wherein the negative slope of M_1 and M_2 are added to the positive slope of B producing the segmental output signal $f(S_x, S_d)$ shown by the solid line. In the present example, the output analogue signal increases linearly from a negative value past the ordinate axis and levels off after reaching breakpoint 38 due to the addition at that point of modifier signal M_1 . The output signal plateau continues to breakpoint 39 at which point the negative slope of modifier

signal M_2 causes the function to decrease at the same rate as M_2 . It will be apparent that with the addition of all modifier signals $M_1—M_{10}$ a wide range of functions may be obtained by controlling the respective positions and slopes of the summed signals. In this regard, it is noted that while modifier signals M_1 and M_2 as illustrated in FIG. 3 appear in only one quadrant, the invention permits the positioning of any one or more of the modifier signals in any one or more of the four quadrants.

Referring again to FIG. 2, each of circuits 22 and 25—35 are responsive to input signal S_x through a phase splitting circuit 41 which provides opposing phases of input signal S_x , namely $+S_x$, in phase with the input signal and $-S_x$, 180° out of phase with the input signal. As described in further detail herein, the opposing phases of the input analogue signal facilitate the positioning of base signal B and each of the modifier signals $M_1—M_{10}$ to achieve the desired segmental function.

Digital signal S_d in the instant case, is comprised of a binary word provided by bit signals $D_0—D_{11}$; an address signal A_n ; and strobe signals $S_0, S_8, S_{b1}—S_{b10}$ and $S_{s1}—S_{s10}$. The word bits $D_0—D_{11}$ provide the data for setting each of circuits 22 and 25—35 while the address and strobe signals control the transmission of bits $D_0—D_{11}$ to the various circuits by means of digital data buffer 42 and address buffer 43.

Connected to the output of summing amplifier 36 is a track and store output circuit 44 providing a means for tracking the segmental signal output provided by amplifier 36 and storing the instantaneous value thereof in response to the digital signal S_d . As herein described, circuit 44 as the advantage of permitting a continuous and stable output during digital signal transitions.

OFFSET AND INITIAL SLOPE CIRCUIT CIRCUIT

Referring to FIGS. 4, 6 and 8, offset-initial slope circuit 22 comprises a slope amplifier 46 embodied in this instance by an operational amplifier best illustrated in FIGS. 6 and 8. Connected to and providing an input impedance for amplifier 46 is an input impedance digital to analogue converter 47 connecting the analogue input signal received through slope polarity switch 49 to amplifier 46. Particularly, switch 49 selects one of the opposing phases of analogue input signal S_x in response to a digital bit signal and issues the selected phase over connection 51 to an input of converter 47. As best illustrated in FIGS. 6 and 8, converter 47 comprises a plurality of preselected input resistors, for example, resistors 52, 53 and 54 shown in FIG. 6 which are selectively connected to slope amplifier 46 in response to digital bit signals $D_0—D_{10}$ by means of a equal plurality of switching devices, for example, devices 56, 57 and 58 also shown in FIG. 6. Thus, input impedance digital to analogue converter 47 provides a variable input impedance connecting the analogue signal to amplifier 46 and a digital to analogue conversion means responsive to the digital signal to selectively set this variable impedance input. As it is known in the art that the gain of an operational amplifier is inversely proportional to the input impedance thereof, this arrangement provides for digitally setting the gain and thus the relative slope between the analogue input signal and the output of amplifier 46. This output is transferred through a slope multiplier circuit 59 to the base signal output of circuit 22.

It is noted that the description thus far makes reference to both signal gain and signal slope. While the physical phenomenon involved in shaping and positioning each of the base and modifier signals relative to one another is provided by variable gain means, it is convenient to consider the characteristics of each signal segment in terms of relative slope. This facilitates the programming of the various circuits to provide the desired function between the input and output of the circuit. Thus, in FIG. 3, the base signal exhibits a positive slope somewhat less than 1. This is referred to as the initial or central slope of the function. Modifier signal M_1 is shown to have a relative slope equal to B but of negative value.

Modifier signal M_2 has a slope somewhat greater than M_1 and also of negative polarity. Thus, the operational amplifier circuits providing variable gain are referred to in terms of their function as slope amplifier and slope multiplier circuits.

In addition to the linear gain relationship provided by converter 47 and amplifier 46, circuit 22 provides the ordinate offset for base signal B. For this purpose, circuit 22 comprises an input impedance digital to analogue converter 61, an offset polarity switch 62, a voltage source therefor, and an offset amplifier 63. By this arrangement a digitally controlled bias generator means is provided which is responsive to the digital signal S_n and issues a digitally selected offset bias via connection 64 to the output of circuit 22 for biasing base signal B. As in the case of slope amplifier 46, offset amplifier 63 is embodied by an operational amplifier where converter 61 provides a variable input impedance therefor. However, converter 61 is best illustrated in FIG. 6, receives a constant plus or minus voltage source from switch 62, instead of the independently variable analogue input signal. Converter 61 including a plurality of resistors, for example, resistors 66, 67 and 68 and an equal number of switching devices, for example, devices 71, 72 and 73 responsive to digital bit signals D_0-D_n , thus provides a digitally selected variable impedance for amplifier 63. Offset amplifier 63 issues the bias signal over connection 64 and through summing resistor 75 for summation with the output of slope multiplier circuit 59 by means of summing amplifier 36 of FIG. 2. Offset polarity switch 62 provides a means selecting either a plus or minus, a 10-volt source in this instance, which determines the polarity of offset 37 as shown in FIG. 3.

SLOPE-BREAKPOINT CIRCUITS

Referring to FIGS. 5, 7 and 9, each slope-breakpoint circuit and in this instance circuit 25 comprises a breakpoint amplifier 76, including a nonlinear operational amplifier circuit, for receiving a selected phase of the analogue input signal S_x over connection 77 and issuing a nonlinear function thereof to connection 78. Particularly, and as described herein, the nonlinear function provided, results in a signal having a zero value for selected portions of the input analogue signal, and a gain or relative slope of plus or minus 1 for the remaining portions of the input signal. The discontinuity between these signal portions is referred to as the breakpoint such as breakpoint 38 or 39 in FIG. 3. The purpose and advantage of maintaining the slope or gain relationship at 1 for the nonzero signal portions issued by the breakpoint circuit is to facilitate subsequent slope shaping of the modifier signal. Specifically, the nonzero portion of the signal issued over connection 78 is preferably provided with a relative slope or gain by the combination of input impedance digital to analogue converter 83, slope amplifier 84 and slope multiplier 86. The operation of these latter circuits is similar to that described for converter 47, amplifier 46 and circuit 59 above, and results in the output of one of the modifier signals, in this instance M_1 .

To illustrate the operation of breakpoint amplifier 76 and its associated circuitry, let it be assumed that it is desired to generate modifier signal M_1 as graphically positioned in the diagram of FIG. 3. In this case M_1 is shown with a breakpoint 38 occurring at a preselected positive value of S_x and thereafter breaking into the lower right-hand quadrant with a negative slope. Because of the polarity inversion provided by slope amplifier 84, it will be necessary to generate a signal over connection 78 breaking into the upper right-hand coordinate with a positive slope. For this purpose, quadrant select switch 80, quadrant select switch 81 and clamping diode switch 88 are driven to the positions shown in FIG. 7 by digital bit signals D_{10} and D_{11} as hereinafter more fully described. Accordingly, amplifier 76 receives the inverted or negative phase, $-S_x$, of the input signal through connection 77 and resistor 89. The input signal thereby induces a current I_x as shown. Amplifier 76 also receives a plus voltage reference, in this instance 10 volts, through an input impedance digital to

analogue converter 79. Converter 79 operates in a manner similar to converter 61 and together with the reference voltage received through switch 81 functions to provide a digitally controlled bias generator means inducing a selected current flow I_r . This is accomplished by means of resistors 90, 91 and 92 and digitally operated switching devices 93, 94, and 95. The magnitude of current flow I_r positions the breakpoint of the modifier signal along the abscissa as shown by FIG. 3.

As noted above, breakpoint amplifier 76 is an operational amplifier circuit and includes a base amplifier 96 having an input 97 and an output 98. The feedback network of the operational amplifier circuit includes a pair of paralleled and oppositely poled blocking diode networks 108 and 109 jointly connected at one of their ends to output 98 and jointly connected at the other ends to connection 78 and through a feedback resistor 99 to input 97. Additionally, the feedback network of amplifier 96 includes clamping diode switch 88 which provides by means of switching device 113 selective connection of one of a pair of oppositely poled diodes 111 and 112 between output 98 and input 97. In this instance, diode 111 has been selected by the digital signal and switching device 113.

Assuming now that the input analogue signal S_x as shown in FIG. 3 varies from a maximum negative value to a maximum positive value or from left to right along the abscissa axis. For negative values of S_x , the opposing phase thereof, $-S_x$, will be positive. Accordingly, both I_r and I_x will flow toward a junction 82 and thus cause a negative polarity signal to appear at output 98 of base amplifier 96. The negative polarity at output 98 is caused by the inversion of the operational amplifier circuit of amplifier 76. With output 98 at a negative potential, the summation of currents I_r plus I_x is conducted through the now forward biased diode 111 to maintain input 97 at virtual ground in accordance with the known characteristics of operational amplifier circuits. Output 98 is thus slightly negative with respect to virtual ground due to the forward voltage drop across diode 111. This slight negative bias causes diodes 114 and 115 to conduct drawing current from a plus voltage reference, in this instance +18 volts, through resistor 116. This current flow maintains junction 117 at a slightly positive potential, thereby reverse biasing diode 118 with respect to virtual ground. In a similar manner diode 119 of network 109 is also reversed biased during this operation due to the appearance of a slight negative potential at junction 110 caused by forward biased conduction of diodes 120 and 124 to the associated negative voltage reference (-18v). Under these conditions, current cannot flow through resistor 99, and the output over connection 78 remains at zero volts. The zero output is maintained until $-S_x$ passes through zero and becomes sufficiently negative such that I_x is equal and opposite to reference current I_r . Thereupon, the current flow between junction 82 and input 97 and thus through diode 111 has been reduced to essentially zero. As $-S_x$ continues to increase in a negative direction, I_x exceeds I_r and output 98 tends to go slightly positive. When this occurs, diode 118 of network 109 becomes forward biased conducting the voltage at output 98 through resistor 99 and back to input 97. By selecting input resistor 89 and resistor 99 to be of equal value, the output issued over connection 78 is equal to the algebraic sum of inverted polarity value of $-S_x$ and the value of the bias signal defined by reference current I_r . With reference to FIG. 3, the output appearing on connection 78 in our example would occur with a breakpoint located at point 38 but at variance with FIG. 3 breaking into the upper right hand quadrant and with a slope of 1. The reason for this is that the signal on connection 78 is conducted through slope amplifier 84 which again inverts the signal and provides it with a digitally selected slope so as to appear as modifier signal M_1 as shown in FIG. 3. While the breakpoint amplifier of circuit 25 has been described in terms of a single operational mode, it will be apparent that modifier signal M_1 may be positioned to break into any one of the four possible quadrants by selective disposition of switches 80, 81 and 88. In a similar manner, each of modifier signals M_2-M_{10} are generated by circuits 26-35 respectively.

By virtue of the above operation, each of analogue function generators 11—15 may be digitally preset to produce a given function $f(S_r, S_d)$ of an independent variable S_r . As alluded to above, the output of each such generator has a maximum of 11 segments, wherein a first segment is provided by base signal B and whereas each of the remaining 10 segments are provided by the addition of modifier signals M_1 — M_{10} to base signal B. While 11 segments has been found sufficient for the approximation of most functions, it will be apparent that each of function generators 11—15 may be modified to provide any number of segments by varying the number of slope-breakpoint circuits thereof.

DIGITAL CONTROL

In order to set or control the offset and slope of the base signal and the breakpoints and slopes of each of the modifier signals, each of generators 11—15 employs a series of digital data words. These data words are introduced into each generator in series and comprise digital data bits D_0 — D_{11} of digital signal S_d . On the other hand, the digital bits forming each word are fed to the circuits in parallel. For example, generator 11 shown in FIG. 2 receives bits D_0 — D_{11} through digital data buffer 42 and distributes these bit signals in parallel to each of circuits 22 and 25—35.

Twenty-two data words are required to completely program or set the function of one generator in accordance with the following table:

One word base signal offset	} B
One word base signal slope	
Ten words modifier signal slopes	} M_1 — M_{10}
Ten words modifier signal breakpoints	

The 12 binary bits comprising each word determine the magnitude, polarity, and quadrant location of each of signals B and M_1 — M_{10} . For example, assuming that it is desired to set the polarity and amplitude of offset 37 provided by circuit 22, the logic states of data bits D_0 — D_{11} are appropriately set to form a desired offset word and introduced in parallel to all of circuits 22 and 25—35. However, only the offset portion of circuit 22 is enabled by means of the address and strobe signals of S_d to receive these data bit signals and thereby provide the desired offset for the base signal output. As a further example, if it is desired to set or alter slope of modifier signal M_1 , the states of data bits D_0 — D_{11} are varied to provide the desired slope word and the slope circuit portion of circuit 25 is appropriately addressed to receive bits D_0 — D_{11} , which in turn function to set the slope of M_1 . In a similar manner, the remaining parameters defining the output function may be programmed.

The following chart illustrates the various functions assigned to the data bits of each data word.

1 offset word	$D_0D_1D_2D_3D_4D_5D_6D_7D_8D_9$, determines magnitude of offset for B	$D_{10}D_{11}$, determines polarity of offset and initial slope.
1 initial slope word	D_0D_{10} , determines magnitude of initial slope for B	D_{11} , determines mult. factor $\times 1, \times 10$.
10 breakpoint words	D_2D_9 , determines magnitude of breakpoints for M_1 — M_{10}	$D_{10}D_{11}$, determines quadrant location.
10 slope words	D_0D_{10} , determines magnitude of slopes for M_1 — M_{10}	D_{11} , determines mult. factor $\times 1, \times 10$.

It is noted that D_{11} of the offset word is used in this instance to determine the polarity of the initial slope rather than one of the data bits of the initial slope word in order to make efficient use of available bit signals.

In programming or digitally setting the offset for base signal B digital bits D_0 — D_9 are fed into an offset register 121 of circuit 22 as shown in FIGS. 4 and 8. Offset register 121 is formed with a plurality of digital register circuits, one for each data bit, such as register circuit 122 for bit D_0 . Each register circuit provides a two-state signal at its output for operating an associated switching device of converter 61 between open and closed positions or states. For example, register circuit 122 has an output connected through a transistor driver 123 to operate switching device 71, which in this instance is a field effect transistor. Thus register circuit 122 may be digitally set to drive switching device 71 preferably a high speed field effect transistor switch as shown, to a high or low impedance condi-

tion providing controlled connection of resistor 66 between offset polarity switch 62 and offset amplifier 63.

Particularly, register circuit 122 is comprised of a pair of NOR gates 126 and 127 connected as shown to provide a bistable multivibrator providing a two-state signal at the output of circuit 122. Additionally, a pair of NAND gates 128 and 129 are connected to set gates 126 and 127 in one of their bistable states in response to digital bit D_0 . While NOR gates 126 and 127 have been herein distinguished from NAND gates 128 and 129 for the purpose of description, it is well known in the art that NOR and NAND gates are in fact constructed identically and form equivalent gating functions. Accordingly, in the actual construction of an embodiment of the invention, all of gates 126—129 may be structurally identical.

In a similar manner to the above operation, each of data bits D_1 — D_9 operates a separate register circuit identical to circuit 122 to provide connection of an associated resistor, such as resistors 66, 67 and 68 associated with bits D_0 , D_1 and D_2 , between switch 62 and amplifier 63 as indicated in FIG. 6.

The values of the resistors of converter 61 are functionally related to bits D_0 — D_9 of the offset word to provide a desired digitally coded variable analogue function gain between the voltage source from switch 81 and the bias signal output of offset amplifier 76. It is well known that the gain of an operational amplifier circuit is proportional to

$$\frac{r_f (\text{feedback impedance})}{r_{in} (\text{input impedance})}, \quad \text{where } r_f \text{ in this instance is}$$

provided by feedback resistor 131 connected across a base amplifier 130 and r_{in} is provided by one or more of the resistors of converter 61 such as resistor 66. Accordingly, the ratios of feedback resistor 131 to each of the resistors of converter 61 respectively associated with bits D_0 — D_9 , are selected to convert the offset digital word into a variable analogue gain and thus a variable magnitude of the bias signal output issued over connection 64. Particularly the ratio of resistor 131 to resistor 66 is selected in this instance to provide a gain of $-1/2$ between the source potential of switch 62 and connection 64. The resistor associated with digit bit D_1 , shown in FIG. 6 as resistor 67, is selected with a value twice that of resistor 66 to provide a gain equal to $-1/4$. The resistor of converter 61 associated with bit D_2 , shown in FIG. 6 as resistor 68, is selected to have a value four times that of resistor 66 to provide a gain of $-1/8$. It is noted that the gain provided by each resistor of converter 61 progressively decreases by a factor of 2^{-n} where $n = 1, 2, 3$, etc. This forms a binary basis for the conversion of the digital offset word into analogue gain function, in this instance the function being a variable bias. Accordingly, the remaining resistors (not shown) of converter 61 respectively associated with bits D_3 — D_9 are selected to provide ratios with resistor 131 progressively decreasing by the power of two. While this

code has proved satisfactory, any other desired coding may be employed such as binary-coded-decimal.

In the present embodiment, the offset or bias signal issued to connection 64 varies between 0 and ± 10 volts. Thus, for a ± 5 -volt offset for base signal B, the offset word is selected to connect only resistor 66 to the input of amplifier 63 by activating switching device 71 to its low impedance condition. This provides a gain of $-1/2$ between switch 62 and connection 64 and with the 10-volt reference issued by polarity switch 62, a ± 5 -volt offset signal is provided for the base signal. The polarity of the offset bias is dependent upon the selection of the plus or minus 10-volt reference by switch 62. For an offset or bias signal approaching 10 volts, digit bits D — D_9 of the offset word are selected to connect all of the resistors of the converter 61 to the input of the amplifier 63 thereby providing the summation of gains $-1/2, -1/4, -1/8$, etc. which approaches a gain of -1 . Intermediate values between 0 and ± 10 volts for the offset

signal are selected by an appropriate combination of the individual logic states of bits D_0 — D_9 in accordance with the above logic code. In this manner, 2^{10} or 1,024 bias levels are provided between 0 and 10 volts.

In addition to digit bits D_0 — D_9 , the offset word includes digit bits D_{10} and D_{11} respectively providing selection of the offset polarity and selection of the slope polarity for the base signal output B. The particular functioning of digit bit D_{11} will be discussed herein. As shown in FIGS. 4, 6 and 8, digit bit D_{10} is introduced into offset polarity switch 62, selectively disposing switch 62 to connect either the +10 volts or -10-volt reference source to converter 61. With reference to FIG. 8 switch 62 in this instance comprises a register circuit 132 similar to register circuit 122 discussed above but at variance therewith, providing a pair of outputs 133 and 134 forming two outputs of a bistable multivibrator. Output 133 is connected through a pair of transistor driver circuits 137 and 138 providing a means for gating diode switch 139 between an "on" or "off" condition. Output 134 is similarly connected through transistor driver circuits 141 and 142 for gating diode switch 143 between an "on" or "off" condition. Accordingly, register circuit 132 is responsive to digital bit D_{10} to provide at junction 144 the output of diode switches 143 and 139, either plus or minus 10 volts, depending upon the logic state of bit D_{10} . The polarity of the voltage reference thus selected is carried to converter 61 and thereafter inverted by amplifier 63 and issued to connection 64. Thus, if it is desired to have a positive offset for base signal B, the negative 10-volt reference is appropriately selected by switch 62 by means of data bit D_{10} .

In order to set the initial slope of the base signal, data bits D_0 — D_{11} of the initial slope word are introduced into register 146 as shown, while data bit D_{11} of the offset word is fed to slope polarity switch 49. Data bits D_0 — D_{10} of the initial slope word provide for operating the switching devices of converter 47 to connect selected input resistors to slope amplifier 46 and in this manner selectively set the slope of signal B. Register 146, as in the case of register 121, is comprised of a plurality of separate register circuits, one for each of bits D_0 — D_{10} , such as register circuit 147 for bit D_0 . Circuit 147 functions identically to circuit 122 and provides with transistor driver 148, operation of switching device 56 between low and high impedance conditions. Device 56 is preferably a field effect transistor as shown to permit high-speed switching operation responsive to an electrical signal. When switching device 56 is driven to its low impedance condition in response to data bit D_0 , resistor 52 of converter 47 is connected between switch 49 issuing the analogue input signal to the input of slope amplifier 46. Additionally, register 146 includes a separate register circuit, identical to circuit 147 for each of the remaining bits D_1 — D_{10} of the initial slope word. Likewise, converter 47 includes for each of D_1 — D_{10} a separate transistor drive, field effect transistor, switching device, and input resistor. The input resistors for digit bits D_0 , D_1 and D_2 are illustrated in FIG. 6 as resistors 52, 53, and 54 of converter 47. As discussed above, by selective connection of one or more of these input resistors to the input of amplifier 46, the slope of base signal B may be preset to a desired value.

As in the case of converter 61, each of the input resistors of converter 47 are selected to provide values in accordance with a binary code for converting digit bits D_0 — D_{10} into a selective gain for amplifier 46. In this instance, the ratios of feedback resistor 149 which is connected across a base amplifier 150 of slope amplifier 46 to each of the input resistors, such as resistor 52, of converter 47 are selected to provide progressively decreasing gain or slope. Particularly, the ratio of resistor 149 to input resistor 52 corresponding to digit bit D_0 is set at $\frac{1}{2}$ to provide a $\frac{1}{2}$ gain for the slope amplifier. The input resistor corresponding with digit bit D_1 shown in FIG. 6 as resistor 53 is selected to have a value twice that of resistor 52 to provide a gain of $\frac{1}{4}$. Input resistor 54 corresponding to data bit D_2 is selected to provide four times the value of resistor 52 thus providing a gain of $\frac{1}{8}$. The decreasing gain or slope provided individually by each of the input resistors of converter 47 is

thus seen to decrease by the factor 2^{-n} . In this manner and as discussed above in regard to converter 61, the digital to gain conversion provided by converter 47 forms the foundation for the digital to analogue conversion and provides the digitally selected relative slope for base signal B. Thus a slope range of 1 volt/volt to about 0.0005 volts/volt with 2^{11} or 2,048 available slope magnitudes. However, as in the case of converter 61, other desired codes may be utilized to achieve the slope selection.

In order to provide selection of the polarity of phase relationship of the base signal slope with respect to the analogue input signal S_r , digit bit D_{11} of the offset word is fed into slope polarity switch 49 shown in FIGS. 4, 6 and 8. Preferably and as best shown in FIG. 8, polarity switch 49 comprises a register circuit 151 identical to register circuit 132 and providing a bistable circuit having a pair of outputs 152 and 153 issuing mutually exclusive high and low signal conditions for selecting in response to digit bit D_{11} , either $+S_r$ or $-S_r$. Particularly, output 152 of register circuit 151 is fed through a pair of transistor drivers 156 and 157 to transistor switch 158, while output 153 is fed through transistor drivers 159 and 160 to transistor switch 162. Accordingly, register circuit 151 selectively drives either transistor switch 158 or 162 to a low impedance condition in response to the state of circuit 151 to effectively connect either $+S_r$ or $-S_r$ to connection 51. It will be apparent from this arrangement that the phase or polarity relationship between the slope of base signal B and analogue input signal S_r may be preset by the logic state of digit bit D_{11} of the offset word.

As a further feature of the present invention, the gain or slope of base signal B may be individually multiplied by a preselected factor, in this instance a factor of 10 has to be chosen. As noted above, this multiplication is accomplished in part by slope multiplier circuit 59 as shown in FIGS. 4, 6 and 8. Particularly as shown in FIG. 6, circuit 59 comprises a switching device 162, which is responsive to digit bit D_{11} of the initial slope word to connect resistor 163 in parallel with resistor 164. The total impedance provided by these resistors, which will be the value of resistor 164 with switch 162 in an open condition as shown and the value of the parallel impedance of resistors 164 and resistor 163 switch 162 in a closed condition, determines the gain or slope amplification at the output of summing amplifier 36 shown in FIG. 2. In other words, these resistors provide the input impedance for summing amplifier 36. By appropriate selection of the values of resistor 164 and 163, a gain or slope amplification factor of one or ten may be provided for base signal B.

Referring to FIG. 8, in order to drive switching device 162, which in this instance is a field effect transistor, a register circuit 166 is provided responsive to digit bit D_{11} of the initial slope word, and having an output connected to switching device 162 through transistor driver 167. Register circuit 166 operates in a manner similar to circuits 122 and 147 to respond to the logic state of bit D_{11} and issue a control signal through driver 167 to dispose switching device 162 in either a low impedance or a high impedance condition, whereupon the above-described slope multiplication factor is selected.

While reference has been made to digit bits D_0 — D_{11} of the offset word and digit bits D_0 — D_{11} of the initial slope word, it will be apparent that the digit bits in each case are fed into circuit 22 by means of a single set of 11 conductors. Particularly as illustrated in FIG. 2, digit bits D_0 — D_{11} are supplied from digital data buffer 42 by means of cable 171 which consists of 11 conductors and branches in parallel to each of the circuits 22 and 25—35. Accordingly, and as shown in FIG. 4 each of digit bits D_0 — D_{11} are fed simultaneously and as designated to offset register 121, slope register 146, offset polarity switch 62, and slope polarity switch 49. However, in order to segregate the information provided by the instantaneous states of bits D_0 — D_{11} into binary words, such as the offset word and the initial slope word, the present invention provides a series of addressing and strobing operations for commanding only selected circuits to respond to the instantaneous condition of

the bit signals. For example, referring to FIGS. 2 and 4, assume it is desired to select the offset for base signal B. Accordingly, digital bits D_0 — D_{11} of digital signal S_d are selected and introduced into data buffer 42 providing the selected offset information in digital form. Buffer 42 thereupon issues over cable 171 to circuit 22, the selected binary states of the digit bits which are in turn simultaneously fed to both the slope circuit and offset circuit portions of circuit 22. However, in addition to the introduction of digit bits D_0 — D_{11} , address signal A_n and strobe signals S_o and S_s of digital signal S_d are also fed to circuit 22 for actuating selected portions thereof. Particularly, address signal A_n is preassigned to address or enable the digital programming or setting of one of the analogue function generators, in this instance, generator 11. Strobe signals S_o and S_s , respectively enable the digital setting of the offset and slope portions of circuit 22. Accordingly, returning to our example, digit bits D_0 — D_{11} have been set to provide a desired offset and thus form the offset word described above. At the same time, address signal A_n and offset strobe signal S_o are issued by digital computer 17 to enable offset register 121, offset polarity switch 62 and slope polarity switch 49 to register and store the instantaneous states of digit bits D_0 — D_{11} . This is achieved by means of an offset gate 172 connected to receive A_n and S_o and having an output connection 173 feeding register 121, switch 62 and switch 49. Particularly, and with reference to FIG. 8, the occurrence of address signal A_n and strobe signal S_o , causes gate 172 to issue a signal over connection 173 conditioning the register circuits of register 121, register circuit 132 of switch 62 and register circuit 151 of switch 49 to respond to their associated input digit bits and store the instantaneous logic conditions thereof. Without the concurrent appearance of address signal A_n and offset strobe signal S_o , each of these register circuits remains unresponsive to the instantaneous condition of digit bits D_0 — D_{11} .

In a similar manner, digit bits D_0 — D_{11} may be selected by digital computer 17 to provide a desired slope for 0—base signal output of circuit 22. In this case, the concurrence of address signal A_n and initial slope strobe signal S_{is} is required. Again referring to FIGS. 4 and 8, A_n and S_{is} are introduced into a slope gate 174 which is responsive to the concurrence of these signals to issue over connection 176 a signal to slope register 146 enabling the individual register circuits thereof to respond to the instantaneous condition of digit bits D_0 — D_{11} .

Thus, the digital words, such as the offset and initial slope words are introduced into circuit 22 in parallel by consecutively selecting digit bits D_0 — D_{11} for the desired word and consecutively addressing and strobing the offset and slope portions of circuit 22 to digitally program the slope, phase, and offset relationship between analogue input signal S_r and base signal B.

In a manner similar to the foregoing, the individual slopes and breakpoints of circuits 25—35, best shown in FIG. 2 are digitally controlled by 10 slope words and 10 breakpoint words, each comprising selected logical states for digit bits D_0 — D_{11} . Particularly and referring to FIGS. 5, 7 and 9, digit bits D_0 — D_{11} of the breakpoint word function to actuate input impedance digital to analogue converter 79 by means of a breakpoint register 177. As in the case of registers 121 and 146 of circuit 22, register 177 comprises a plurality of register circuits such as circuit 178 best shown in FIG. 9. In this instance, register circuit 178 is constructed of a pair of NOR gates 179 and 181 interconnected with a pair of NAND gates 182 and 183 to provide a digitally preset bistable multivibrator. The output of register circuit 178 is connected to actuate switching device 93, in this instance a field effect transistor, through a transistor driver 184. Accordingly, register circuit 178 functions in response to digital bit D_0 and the address and strobe signals discussed herein to drive switching device 93 between a low or high impedance condition providing selective connection of input resistor 90 between quadrant select switch 81 and the input to the breakpoint amplifier 76. Likewise, register 177 and converter 79 provide an associated

register circuit, transistor driver, field effect switching device and input resistor for each of digit bits D_1 — D_9 .

The values of the input resistors associated with each of bits D_0 — D_9 of the breakpoint word are selected relative to feedback resistor 99 of amplifier 76 to provide a digitally coded variable bias current, shown in FIG. 7 as I_r , for digitally positioning the breakpoint of modifier signal M_1 . This is conveniently achieved in a manner similar to the selection of input resistors for converter 61 of the offset portion of circuit 22 as discussed above. Accordingly resistor 90 of converter 79 is selected at $\frac{1}{2}$ the value of the feedback 29 resistor 99, and the remaining input resistors associated respectively with digit bits D_1 — D_9 are provided with values progressively increasing by a factor of 2^n relatively to resistor 90. This again forms the binary code for performing the digital to analogue conversion operation of converter 79. As an example of this operation, assume only input resistor 90 is connected between switch 81 and amplifier 76, in response to digit bit D_0 of the breakpoint word.

With a 10-volt reference voltage provided by switch 81, and with resistor 90 equaling $\frac{1}{2}$ the value of resistor 99, a bias current I_r representative of 5 volts is achieved. Accordingly, modifier signal M_1 will break into a preselected quadrant as S_r reaches a magnitude of 5 volts. With the remaining input resistors selected according to the defined code 2^{10} or 1,024 breakpoint magnitude levels are available within a range of 0 to ± 10 volts.

As noted above, in the discussion of the breakpoint circuit, the present invention provides for placing each modifier signal, such as M_1 , in a digitally selected quadrant. For this purpose, digit bits D_{10} and D_{11} of the breakpoint word are respectively fed into quadrant gate and register 186 and quadrant select switch 80, first shown in FIGS. 5 and 9. The logic conditions of digit bits D_{10} and D_{11} of the breakpoint word provide in combination four states, one for each quadrant as exemplified by the following chart:

	Breakpoint words	
	D_{10}	D_{11}
Quadrant as shown in Figure 3:		
Upper right hand.....	0	0
Upper left hand.....	0	1
Lower left hand.....	1	0
Lower right hand.....	1	1

For example, if digit bits D_{10} and D_{11} of the breakpoint word are both in a logical one state, modifier signal M_1 will break into the lower right-hand quadrant as illustrated in FIG. 3. This operation follows from the above description in regard to selective disposition of switches 80, 81 and 88 discussed with reference to FIG. 7. Of course, other appropriate codes may be employed for this purpose, the above chart being one example.

As best shown in FIG. 9, digit bit D_{10} of the breakpoint word is fed to quadrant gate and register 186 embodied by a register circuit 187, similar to register circuit 178, but providing a pair of outputs 188 and 189 exhibiting mutually exclusive high and low bistable voltage conditions. Outputs 188 and 189 are connected to jointly control the disposition of switches 81 and 88 in response to digit bit D_{10} of the breakpoint word.

As quadrant select switch 81 provides for the issuance of either a plus or minus 10-volt reference, output 189 of register 186 is connected through a pair of transistor drivers 191 and 192 for biasing diode switch 193 to pass the plus 10-volt reference, while output 188 is connected through transistor drivers 194 and 196 to bias diode switch 197 for passing the minus 10-volt reference voltage. Thus, depending upon the logic condition of digit bit D_{10} outputs 189 and 188 assume selected but mutually exclusive high and low signal states for selectively biasing either diode switch 193 or 197, forming a floating switch, to pass a desired polarity of the 10-volt

reference voltage to junction 198 and to the input of converter 79. Simultaneously with the foregoing, outputs 188 and 189 of register 187 are fed to clamp diode switch 88 for positioning switching device 113, also shown in FIG. 7, in a selected mode. As shown in FIG. 9, switching device 113 is embodied by a pair of field effect transistors 113a and 113b respectively actuated by transistor drivers 201 and 202.

Accordingly the single bit D_{10} of the breakpoint word concurrently operates switches 81 and 88 to aid in the selection of a desired quadrant for modifier signal M_1 as discussed above.

Digit bit D_{11} of the breakpoint word functions to operate quadrant select switch 80 which is above noted performed the selection of one of the two phases of input signal S_r . As best shown in FIG. 9, quadrant selector switch 80 comprises a register circuit 203 identical to register circuit 187 and similar to the above described circuit 178, to provide at outputs 204 and 206 mutually exclusive bistable high and low signal conditions in response to the state of D_{11} of the breakpoint word. To achieve the switching function, diagrammatically illustrated by switch 80 of FIG. 7, a pair of field effect transistor switches 207 and 208 are respectively connected through a pair of transistor drivers 209 and 211 to outputs 204 and 206. By virtue of this circuitry, field effect switches 107 and 108 are selectively and mutually exclusively driven to their high and low impedance conditions in response to the logic state of digit bit D_{11} to connect either $+S_r$ or $-S_r$ to connection 77. It will be recalled that resistors 89a and 89b are identical in value and provide input resistor 89 as shown in FIG. 7 for feeding the analogue input signal to junction 82 of the breakpoint circuit.

Thus, switch 80 responsive to digit bit D_{11} cofunctions with switches 81 and 88 jointly responsive to digit bit D_{10} to position modifier signal M_1 and any one of the four available quadrants.

Referring to FIGS. 5, 7 and 9, each of modifier signals M_1 — M_{10} of circuits 25—35 is provided with a gain or slope relative to base signal B as discussed above in regard to FIG. 7. For this purpose, each of bits D_0 — D_{11} of the slope word functions to present converter 83 and slope multiplier 86 by means of a slope register D_{12} to provide the digitally selected modifier signal slope. As in the case of registers 121, 146 and 177, register 212 comprises a plurality of register circuits, such as circuit 213, one for each of digit bits D_0 — D_{11} . In operation, register circuit 213 functions in response to digit bit D_0 in conjunction with the address and strobe signals to assume one of two bistable electrical states at the output thereof. A switching device 214 in this instance a field effect transistor, is driven in response to the instantaneous state of circuit 213 to a high or low impedance condition by means of transistor driver 216 connected to the output of register circuit 213. Thus, an input resistor 217 of converter 83 may be selectively connected between connection 78 and the input of slope amplifier 84 in response to the mode of switching device 214 which in turn is determined by the logic state of digit D_0 . In a like manner, each of digit bits D_1 — D_{10} is provided with an associated register circuit, transistor driver, switching device, and input resistor for selectively connecting certain of such input resistors to amplifier 84. This construction as discussed above provides means for digitally controlling the relative slope of modifier signal M_1 which is issued by the output of slope amplifier 84 through multiplier circuit 86 to the output of circuit 25.

The values for the input resistors, such as resistors 217 of converter 83 are selected relative to the value of a feedback resistor 218 connected across a base amplifier 215 of slope amplifier 84 in accordance with the selection of input resistors for converter 47 of circuit 22. That is, the resistor values are selected to progressively increase by a factor 2^{-n} where $n=1, 2, 3$, etc. to provide a digital to analogue conversion between digit bits D_0 — D_{10} and the signal gain occurring between connection 78 and the output of slope amplifier 84.

In addition to the variable slope or gain provided by converter 83 in response to bits D_0 — D_{10} , the last bit D_{11} also of the slope word functions to operate slope multiplier circuit 86.

This is achieved by means of register circuit 219 of register 212, which is provided with an output connected through a transistor driver 221 to a switching device 220 in this instance a field effect transistor. As in the case of slope multiplier circuit 59 of 22, multiplier circuit 86 provides in response to the switching state of device 220 gain or slope multiplication of the output of the amplifier 84 by either factors of times 1 or 10. For this purpose, circuit 86 is provided with resistors 222 and 223 having a values selected as described above with regard to multiplier circuit 59 of circuit 22. Thus, depending upon the logic condition of digit bit D_{11} , the slope of modifier signal M_1 may be multiplied by a factor of 10. As each of circuits 22 and 25—35 are provided with this slope multiplication feature, the base signal B, or any one of modifier signals M_1 — M_{10} may be individually multiplied in slope to provide greater versatility and accuracy in generating the digitally selected function $f(S_r, S_d)$ output of the analogue function generator. To segregate the 10 breakpoint and 10 slope words used in digitally setting the breakpoint and slope circuits of each of the circuits 25—35, where the words in each case are provided by digit bits D_0 — D_{11} , a sequence of address and strobe signals are issued to analogue function generator 11 by digital computer 17. Address signal A_n is identified with function generator 11 and enables generator 11 to the exclusion of generators 12—15 to receive and respond to digital bit signaled D_0 — D_{11} . Breakpoint strobe signals S_{b1} — S_{b10} and slope strobe signals S_{s1} — S_{s10} are identified by their numerical subscripts with circuits 25—35 respectively and function to enable the individual slope and breakpoint networks of the circuits to respond to the slope and breakpoint words. In essence, operation of these breakpoint and slope strobe signals is the same as described in regard to offset and initial slope signals S_o and S_{10} . Thus, separate breakpoint and slope strobe signals are fed to individually to circuits 25—35, for example breakpoint strobe signal S_{b1} and slope strobe signal S_{s1} are fed to circuit 25 to enable the registering of the breakpoint and slope words associated with circuit 25.

Referring to FIGS. 5 and 9 the breakpoint word for circuit 25 is introduced and registered in accordance with the following operation: Address signal A_n and breakpoint signal S_{b1} are introduced into a breakpoint gate 224, which in this instance is provided by AND gate 226. The output of breakpoint gate 224 is in turn connected to register 186 and each of the register circuits of register 177 and register circuit 203 of switch 80. Thus, upon the concurrence of address signal A_n and breakpoint strobe signal S_{b1} , AND gate 226 issues an output signal to each of the above register circuits thereby enabling the instantaneous logic states of digit bits D_0 — D_{11} of the breakpoint word to be registered and thus stored. This operation sets a quadrant position and breakpoint magnitude of modifier signal M_1 as above described. Furthermore, this condition is maintained until a different breakpoint word is introduced into circuit 25 by address signal A_n and strobe signal S_{b1} .

In a similar manner, address signal A_n and slope strobe S_{s1} are introduced into a slope gate 227, which is comprised of an AND gate 228 and is identical AND gate 226. The output of slope gate 227 is fed over connection 229 to slope register 212 and jointly connected to each of the register circuits thereof, such as circuits 213 and 219. In operation, upon the concurrence of address signal A_n and slope strobe signal S_{s1} , a signal is issued by gate 228 to a connection 229 which enables each of the register circuits of register 212 to respond to and store the instantaneous logic states of digit bits D_0 — D_{11} of the slope word for modifier signal M_1 . The condition thus assumed by register 212 and thus converter 83 in response thereto is maintained until a difference slope word is introduced for circuit 25. Likewise, each of circuits 26—35 may be digitally programmed by separate breakpoint and slope words in response to address signal A_n and individual breakpoint strobe signals S_{b2} — S_{b10} and slope strobe signals S_{s2} and S_{s10} .

By virtue of the foregoing circuitry and operation, the base signal B and each of the modifier signals M_1 — M_{10} may be in-

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dividually digitally shaped to provide an infinite variety of signal functions between analogue input signal S_x and the output of analogue function generator 11, characterized in FIG. 1 as $f(S_x, S_d)$.

INPUT-OUTPUT CIRCUITRY

Referring to FIGS. 2 and 10, phase splitting circuit 41 provides an input, receiving analogue signal S_x and a pair of phase inverters 231 and 232 providing opposing phases $-S_x$ and $+S_x$ of the input analogue signal. Thus, circuit 41 facilitates the above described selection of a slope and breakpoint phase relationships provided by circuits 22 and 25—35. Particularly, inverters 231 and 232 comprise operational amplifier circuits wherein input resistors 233 and 234 thereto have values respectively equally feedback resistors 236 and 237 which are connected between the input and output of base amplifiers 238 and 239, respectively. By this arrangement, it will be apparent that inverter 231 issues a signal 180° out of phase with input signal S_x , wherein this out of phase signal is denoted $-S_x$. Similarly, inverter 232 having an input connected to the output of inverter 231, issues a signal 180° out of phase with $-S_x$ and thus in phase with analogue input S_x , or $+S_x$.

To achieve the summation of base signal B and modifier signals $M1-M_{10}$, summing amplifier 36 comprises an operational amplifier including a base amplifier 241 connected with its input jointly to the outputs of each of circuits 22 and 25—35 and having a feedback resistor 242 cofunctioning with such outputs to provide the desired summing operation. In this regard, reference is made to FIGS. 6 and 7 wherein it will be apparent that the resistors of multiplier circuits 59 and 86 provide the input summing resistors for summing amplifier 36. In accordance with the well-known characteristics of operational amplifiers, it is now seen that the resistor values for the multiplier circuit are selected relative to the value of feedback resistor 242 to provide the above-described multiplying operation. For example, and referring to FIG. 6, to provide the base signal B of offset-initial slope circuit 22 with optional times 1 or times 10 multiplication, resistor 164 of multiplier circuit 59 is selected to equal feedback resistor 242 of amplifier 36. On the other hand, resistor 163 of circuit 59 which is adapted to be connected in parallel with resistor 164 by switching device 162, is selected such that the parallel impedance of these two resistors is 1/10th of feedback resistor 242. Thus, as switching device 162 is disposed in its closed condition in response to digit bit D_{11} , a gain of times 10 is achieved for base signal B at the output of summing amplifier 36.

As an advantageous feature of the present invention, the output of each analogue function generator is continuously tracked and on command momentarily stored to permit modification of the output function by digital signal S_d without interrupting the stability of the output during analogue computation. This is achieved by track and storage circuit 44 which is responsive to address signal A_n of digital signal S_d .

Specifically, circuit 44 comprises an operational amplifier circuit 243 having an input junction 244 and an output 246 which also provided the output of the function generator. A base amplifier 247 is connected between junction 244 and output 246 in parallel with a feedback capacitor 248. Additionally, operational circuit 243 includes a resistor 249 connected between the output of summing amplifier 36 and output 246. A switching device 251, which is preferably a field effect transistor as shown, is connected between the output of summing amplifier 36 and junction 244 to provide a controlled impedance path therebetween. Switching device 251 has a normally closed or low impedance condition connecting resistor 249 in a feedback path between output 246 and junction 244 causing output 246 to track or in other words assume the instantaneous signal value issued by summing amplifier 36. In response to digital signal S_d , device 251 is disposed in an open or high impedance condition removing the resistor feedback loop provided by resistor 249 and leaving a capacitance feedback loop provided by capacitor 248. This latter or open

condition of device 251 allows capacitor 248 to assume and maintain output 246 at the instantaneous value of the signal provided by amplifier 36 immediately prior to opening of device 251.

In order to actuate circuit 44 between its track and store modes, address signal A_n of digital signal S_d is fed through address buffer 43 and a pair of transistor drivers 252 and 253 to switching device 251. Address buffer 43 operates as a delay circuit and by virtue of this construction, circuit 44 is automatically placed in its store mode in response to address signal A_n and is maintained in this mode for a preselected duration after a termination of address signal A_n . Thus, whenever digital data is entered into function generator 11 in response to address signal A_n , the output thereof is placed in its store mode allowing modification of the output function $f(S_x, S_d)$ without disturbing the output signal continuity. After the digital data has been entered address signal A_n is deactivated and after a short delay provided by address buffer 43, track and store output circuit 44 is returned to its track mode. The provided delay permits the circuitry of the generator to settle to the new function before output 246 begins tracking.

This feature is particularly advantageous in continuous computing operations where it is desired to vary or modify the function provided by generator 11 without interrupting the computation process. For example, this permits multivariate function generation by allowing digital computer 17 to automatically modify during computation the analogue function of generator 11 in accordance with a second independent variable. This is particularly desirable for accurately computing dynamic solutions to complex analogue problems.

As best shown by FIG. 10, address buffer 43 comprises a pair of NAND gates 254 and 256 interconnected with a pair of inverters 257 and 258 and a resistor-capacitor network 259. In this instance, a single input of a NAND gate is employed to provide inverters 257 and 258 and to achieve the phase inversion. In operation, gate 256 has a first input responsive to the output of inverter 257 and a second input responsive to a delay network consisting of gate 254, R-C network 259 and inverter 258. Thus, when function generator 11 is addressed by means of signal A_n , the output of gate 256 immediately assumes a condition driving switching device 251 to its open or high impedance condition providing the output store mode. However, when address signal A_n is removed, network 259 causes an electrical delay between the response of inverter 258 to a change in gate 254 and thus maintains gate 256 in a condition holding switching device 251 in the storage mode. This delay which is determined by the R-C time constant of network 259 is preferably on the order of 10 microseconds, provides a sufficient time to allow the circuitry of the function generator to register and set the function in response to the digital data. At the end of the delay provided by buffer 43, the output of gate 256 assumes its normal condition returning switching device 251 to its closed or low impedance condition and permitting output 246 to track the output of summing amplifier 36.

Digital data buffer 42 as shown in FIGS. 2 and 10, provides a means responsive to address signal A_n for gating each of digit bit signals D_0-D_{11} to circuits 22 and 25—35. As best shown in FIG. 10, buffer 42 comprises a plurality of NAND gate 261 for digit bit D_0 . Each of these gates includes a first input jointly connected to address signal A_n and a second input individually connected to an associated digit bit. Accordingly, in response to address signal A_n , addressing function generator 11, each of the NAND gates of buffer 42 are actuated to pass the instantaneous logic states of bits D_0-D_{11} to offset-initial slope circuit 22 and slope-breakpoint circuits 25—35 over cable 171.

The strobe signals of digital signal S_d , as shown in FIGS. 2 and 10, are introduced over individual conductors to circuits 22 and 25—35. Thus, breakpoint strobe signals $S_{b1}-S_{b10}$ are fed to circuits 25—35 over cable 262 consisting of 10 conductors, while slope strobe signals $S_{s1}-S_{s10}$ are introduced over cable 263 also consisting of 10 conductors.

In order to enhance the accuracy of the presently preferred circuitry of the invention as described herein, circuits 22 and 25—35 are constructed to operate at a ± 10 -volt analogue signal range. This relatively low level operation results in higher response speeds and low power consumption due to the lower values of impedance required. Additionally, the operational amplifier circuits used in forming the various slope and breakpoint functions which are preferred due to their accuracy and stability operate most advantageously in the 10-volt range.

On the other hand, many analogue computers such as computer 18 are designed to operate on a plus or minus 100-volt signal range. Accordingly, the function generator described herein has been adapted to receive and reduce 100-volt signals to a 10-volt range at the input thereof and at the output amplify the 10-volt range signal back to the 100-volt level. For this purpose, inverter 231 of circuit 41 as shown in FIG. 10 is constructed with its input and feedback resistors selected to provide a gain of -0.1 . That is, input resistor 233 is selected to have a value 10 times that of feedback resistor 236. Thus, the opposing phase signals $-S_x$ and $+S_x$ assume a value $1/10$ th of input analogue signal S_x .

Similarly, at the output of function generator 11, track and store output circuit 44 is constructed to amplify the 10-volt range signal issued by summing amplifier 36 back to the 100-volt range. This is achieved by selecting input resistor 250 of circuit 44 to equal $1/10$ th that of feedback resistor 249.

SUMMARY OF OPERATION

Consolidating all of the above individually described features of the invention, analogue function generator 11 operates in response to both an analogue signal S_x introduced into phase splitting circuit 41 and digital signal S_d (including digit bits D_0 — D_{11} , address signal A_n and strobe signals S_0 , S_{10} , S_{20} — S_{210} and S_{21} — S_{210}) to produce a digitally selected 11 segment electrical output function of input analogue signal S_x . For relatively smooth functions, the 11 segments provided by one base signal and 10 modifier signals in the instant embodiment have been found very satisfactory for approximating such a function. To achieve the closest possible match between a desired continuously varying function and the segmental function output of generator 11, digital computer programs have been developed for selecting the various slopes and breakpoints for base signal B and modifier signals M_1 — M_{10} . These programs, generally referred to as software in the computer art, compute the desired breakpoints and slopes according to the minimum mean square error deviation between a desired function or an empirical curve and the generated segmental signal. By virtue of the construction and operation of the present invention, digital computer 17 as shown in FIG. 1 may be programmed not only to digitally preset each of analogue function generators 11—15 but also compute the desired slopes and breakpoints required for a particular function. This results in a well integrated and efficient hybrid computation system.

In designing such a software program for use with the circuitry of the present invention, regard must be made to the various signal phase inversions occurring between the analogue input and output of generator 11. For example, with reference to FIGS. 2, 3, 6, and 7 in order to generate base signal B as it appears in FIG. 3 with a positive slope, the following conditions must be observed. Between the input to and output of offset-initial slope circuit 22, a phase inversion occurs, induced by slope amplifier 46. Accordingly, as shown in FIG. 6, the out-of-phase or $-S_x$ signal of the analogue input is selected to produce a positive slope or in-phase relationship between base signal B and the input analogue signal S_x . For each of the modifier signals, such as M_1 , polarity inversions are caused by breakpoint amplifier 76 and slope amplifier 81 of each of slope-breakpoint circuits 25—35. Thus, in order to produce modifier signal M_1 as it is shown in FIG. 3 breaking into the lower right-hand quadrant with a negative slope rela-

tionship with analogue input signal S_x , $-S_x$ is selected for the input to circuit 25. As the outputs from circuits 22 and 25—35 are inverted twice, respectively by amplifier 36 and output circuit 44 no resulting overall phase inversion occurs between base signal B, modifier signal M_1 — M_{10} and output 246.

I claim:

1. A function generator controlled by a digital signal for producing a segmental analogue output signal as a digitally selected function of an analogue input signal comprising:

10 digitally controlled linear circuit means for receiving the input and digital signals and issuing a base signal having a digitally selected linear gain relationship with the input signal;

15 digitally controlled nonlinear circuit means for receiving the input and digital signals and issuing a modifier signal having a digitally positioned breakpoint with the analogue input signal; and

20 summing circuit means connected to said linear and nonlinear circuit means summing the base and modifier signals to produce the segmental analogue output signal.

2. The function generator defined in claim 1 said linear circuit means further comprising, a digitally controlled bias generator means for receiving the digital signal and providing the base signal with a digitally selected offset bias with reference to the input signal.

3. The generator defined in claim 2, said bias generator means comprising, a direct current source, an operational amplifier having a variable impedance input connected to said source and an output selectively biasing the base signal in response to said variable impedance, and a digital to analogue conversion means for receiving the digital signal and selectively setting said variable impedance input.

4. The generator defined in claim 1, said linear circuit means comprising, an operational amplifier having a variable impedance input for receiving the input signal and an output issuing the base signal in response thereto, and digital to analogue conversion means for receiving the digital signal and selectively setting said variable impedance input to provide the aforesaid selective gain relationship.

5. The generator defined in claim 1 said linear circuit means further comprising, a gain multiplier circuit means for receiving the digital signal and providing the base signal with a digitally selected gain multiplication factor.

6. The function generator defined in claim 1 said nonlinear circuit means further comprising, a digitally controlled linear gain circuit means providing the modifier signal with a digitally selected linear gain.

7. The generator defined in claim 1 said nonlinear circuit means comprising, an operational amplifier circuit having an input for receiving the analogue input signal and a diode feedback network and an output issuing the modifier signal as a rectified nonlinear of function of the input signal, and a digitally controlled bias generator means for receiving the digital signal and being connected to said amplifier circuit input issuing a digitally selected bias signal thereto setting the aforesaid breakpoint position between the input and modifier signals.

8. The generator defined in claim 7 said bias generator means comprising, a direct current source, a variable impedance connected between said source and amplifier circuit input, and digital to analogue conversion means responsive to the digital signal selectively setting said impedance.

9. The function generator defined in claim 1 comprising, a plurality of said nonlinear circuit means each for receiving the analogue input and digital signals and each issuing a separate digitally selected modifier signal and said summing circuit means being connected to said plurality of nonlinear circuit means summing all of the modifier signals with the base signal to provide the segmental analogue output signal.

10. The function generator defined in claim 9, said nonlinear circuit means each comprising, a digitally controlled gain multiplier circuit means for receiving the digital signal and providing individual digitally selected gain multiplication factors for each modifier signal.

11. The function generator defined in claim 1 further comprising, signal track and storage circuit means for receiving the digital signal and being connected to said summing circuit means tracking the analogue output signal and storing the instantaneous value thereof in response to the digital signal.

12. The function generator defined in claim 11 said track and storage means comprising, an operational amplifier circuit having an input and an output and a capacitive feedback impedance connected therebetween, a resistor connected between said amplifier output and said summing circuit means and a switching device for receiving the digital signal and being connected between said summing circuit and amplifier input and having closed and open circuit conditions responsive to the digital signal respectively providing optional signal tracking or storing at said amplifier output.

13. The function generator defined in claim 1 further comprising, phase splitting circuit means for receiving the analogue input signal and being connected to said linear and nonlinear circuit means providing opposing phases of the input signal thereto, and said linear and nonlinear circuit means each selecting one of the opposing phase signals in response to the digital signal providing selective slope phase and breakpoint position phase relationships between the base and modifier signals and the analogue input signal.

14. A nonlinear function generator responsive to a digital signal for issuing an analogue output signal as a digitally selected nonlinear function of an analogue input signal comprising, an operational amplifier circuit having a nonlinearly conductive feedback network and an input for receiving the analogue input signal and an output for issuing the analogue output signal, and a digitally controlled bias generator for receiving the digital signal and being connected to said circuit input issuing a digitally selected bias signal thereto positioning the nonlinear relationship between the input and output analogue signals.

15. The function generator defined in claim 14, said operational amplifier circuit further comprising, phase splitting circuit means for receiving the analogue input signal and providing opposing phases thereof, switching means for receiving the digital signal and being connected between said phase splitting circuit means and said amplifier circuit input connecting a selected one of the input signal phases thereto in response to the digital signal providing a selective phase relationship between the analogue input and output signals.

16. The function generator defined in claim 14 wherein said

operational amplifier circuit includes a base amplifier having an input providing said amplifier circuit input and an output and said feedback network comprising, a pair of oppositely poled blocking diode networks connected in parallel between said base amplifier output and said amplifier circuit output, a resistor connected between said amplifier circuit output and said base amplifier input, a pair of oppositely poled diodes, and switching means for receiving the digital signal and responsive thereto connecting a selected one of said last named diodes between said base amplifier input and output to clamp a selected signal polarity appearing at said base amplifier output to said base amplifier input.

17. A method of generating an analogue output signal as a segmental function of an analogue input signal wherein such function is selected by a digital signal comprising, converting the input and digital signals into a base signal having a digitally selected linear gain relationship with the input signal, concurrently converting the input and digital signals into a modifier signal having a digitally selected breakpoint discontinuity with the input signal, and summing the base and modifier signals to provide the selected segmental function analogue output signal.

18. The method defined in claim 17 said first-named converting step further comprising, converting the digital signal into a digitally selected bias signal and adding the bias signal to the base signal to provide a digitally selected amplitude offset therefor.

19. The method defined in claim 17 said second converting step further comprising, converting the digital signal and modifier signal to provide the modifier signal with a digitally selected linear gain relative to the input analogue signal.

20. The method defined in claim 17 comprising, a plurality of said second-named converting steps each concurrently performed on said analogue input signal with said first named converting step to provide a plurality of separate modifier signals each having individual digitally selected breakpoint discontinuities with respect to the input signal and wherein said summing step consists in summing all of the modifier signals with the base signal to provide the analogue output signal.

21. The method of claim 17 further comprising, tracking the analogue output signal as the input signal varies and storing the instantaneous value of the output signal during transitions in the digital signal.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,557,347

January 19, 1971

Jack Y. Robertson

It is certified that error appears in the above identified patent and that said Letters Patent are hereby corrected as shown below:

Column 8, line 72, "D-D₉" should read -- D₀-D₉ --. Column line 72, "-1/4" should read -- -1/4. --. Column 10, line 10, "polarity of" should read -- polarity or --. Column 10, lines 61, 64 and 68, Column 11, lines 24, 38, 58 and 59, Column 13, lines 39 and 44, Column 14, lines 22, 49 and 66, Column 16, line 68 and Column 17, line 36, "DO-D₁₁", each occurrence, should read -- D₀-D₁₁ --. Column 11, line 10, "S_s" should read -- S_{is} --; line 39, "O-base" should read -- the base --; line 45, "DO-D₁" should read -- D₀-D₁ --. Column 12, line 2, "D1-D₉" should read -- D₁-D₉ -- line 4, "DO-D₉" should read -- D₀-D₉ --; line 11, after "feedback cancel "29"; line 13, "D1-D₉" should read -- D₁-D₉ --; line 14, "2+n" should read -- 2⁺ⁿ --. Column 13, line 27, "D₁₁ o" should read -- D₁₁ to --; line 36, "M1-" should read -- M₁- --; line 5 "D1-D₁₀" should read -- D₁-D₁₀--; line 69, "2+n" should read -- lines 71 and 74, "DO-D₁₀", each occurrence, should read -- D₀-D₁₀ --. Column 14, line 16, "M1-M₁₀" should read -- M₁-M₁₀ -- line 27, "signaled DO-D₁₁" should read -- signals D₀-D₁₁ --; line 63, "S₅₁'" should read -- S_{s1}/ --; line 73, "and S₁₀." should read -- S_{s10}. --; line 75, "M1-M₁₀" should read -- M₁-M₁₀ --. Column 15, line 25, "M1-M₁₀" should read -- M₁-M₁₀ --. Column lines 63 and 64, "gate 261 for digit D₀." should read -- gates,

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one for each digit bit, such as NAND gate 261 for digit bit D_0 . --. Column 18, line 5, " M_1-M_{10} " should read -- M_1-M_{10} -- line 72, "a digitally" should read -- digitally --.

Signed and sealed this 29th day of June 1971.

(SEAL)
Attest:

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