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H4J JGF
U1S S1947

(56) Documents Cited
GB 2317783 A **GB 0592917 A** **EP 0202016 A2**
US 5353347 A **US 4448074 A**

(58) Field of Search
UK CL (Edition Q) **H3P PCCB PCCG PCCX PDM , H4J JGF JGX**
INT CL[6] **H03K 17/16 , H04R 3/00**
Online: WPI,INSPEC

(54) Abstract Title
Telephone headset click-free muting circuit

(57) In a click-free muting circuit for a headset condenser microphone 13 connected to a telephone 1, actuation of mute switch 15 feeds base current to bipolar transistors Q1 and Q2, which gradually turn on and short-circuit the microphone 13. The gradual switching of the transistors, caused by capacitors C1 and C2, eliminates muting clicks. When Q1 and Q2 are on, series transistor Q3 no longer receives base current and turns off to provide hard muting. Resistor R23 ensures that the output of the headset detection circuit 25 has approximately the same duration as the actuation of switch 15 (figure 6), which may be located at the headset or at a headset interface box between the headset 7 and telephone set 1. Q1 and the diodes D1 may be eliminated.

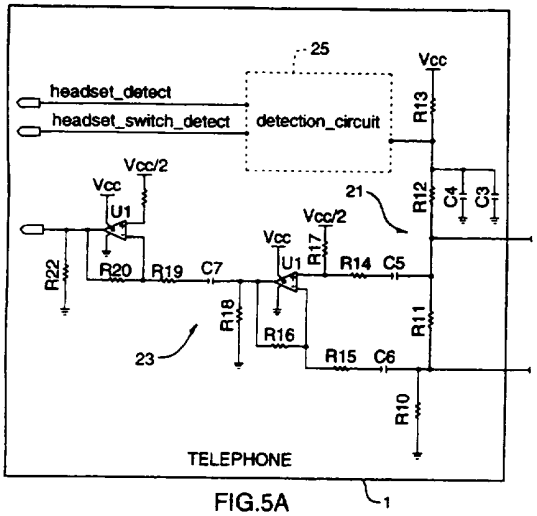

FIG.5A

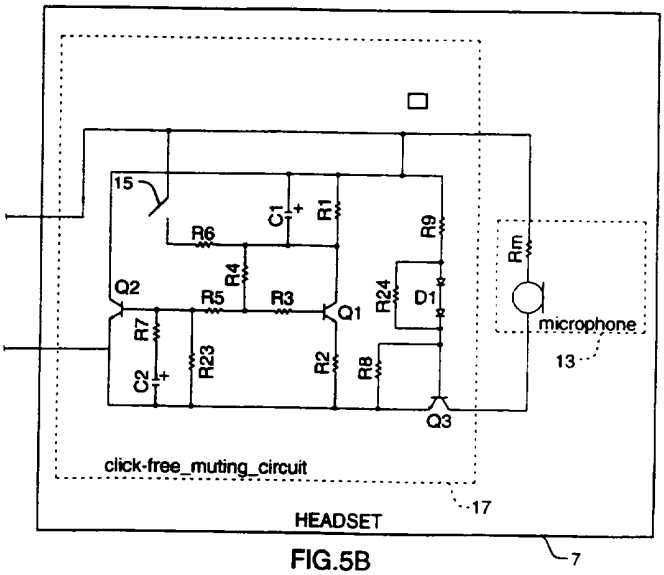

FIG.5B

GB 2 344 711 A

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

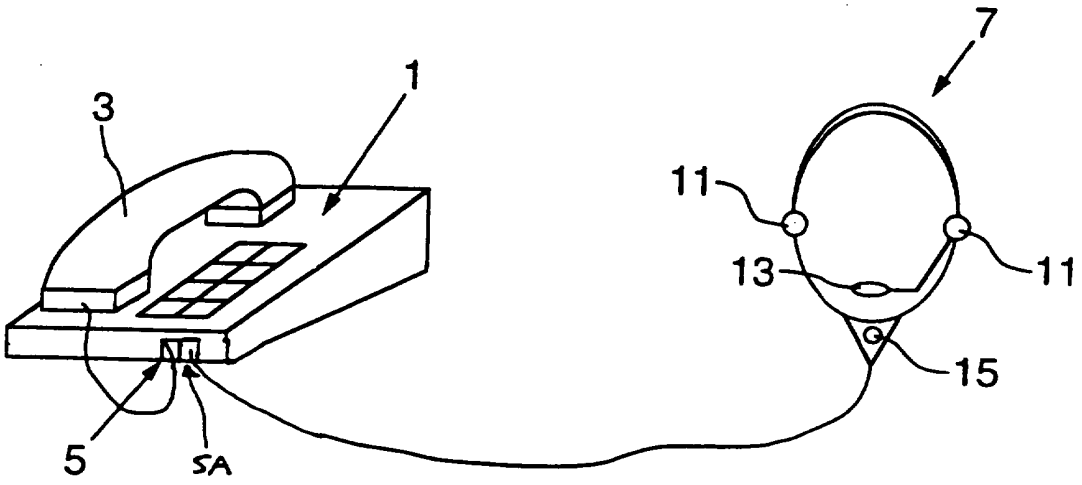

FIG.1

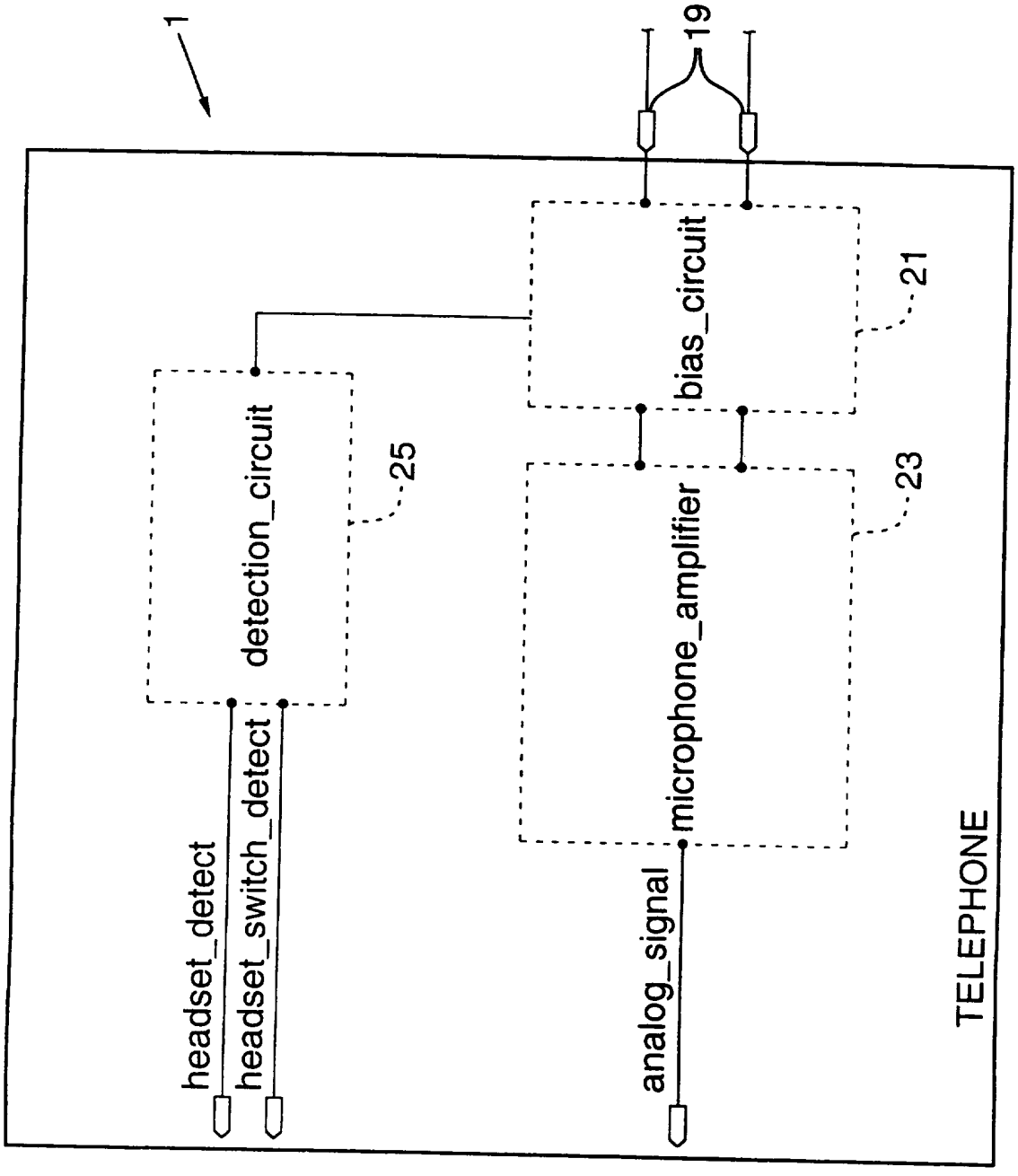
1
19
bias_circuit
21
detection_circuit
25
microphone_amplifier
23
headset_detect
headset_switch_detect
analog_signal
TELEPHONE

FIG.2A

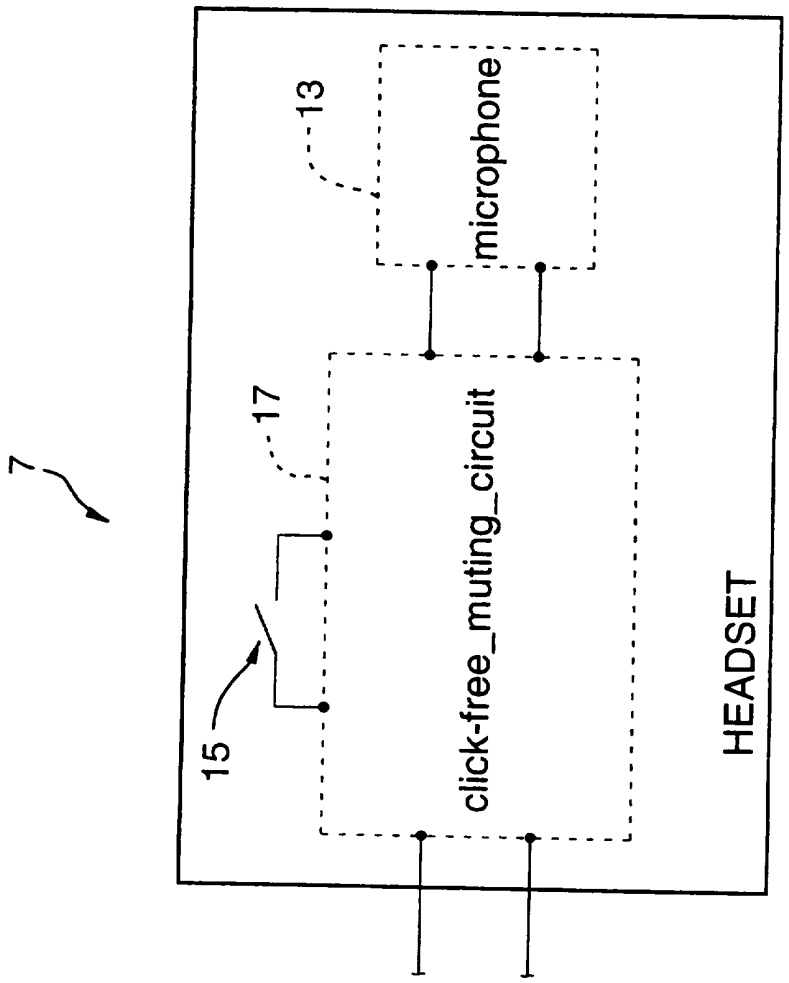

FIG.2B

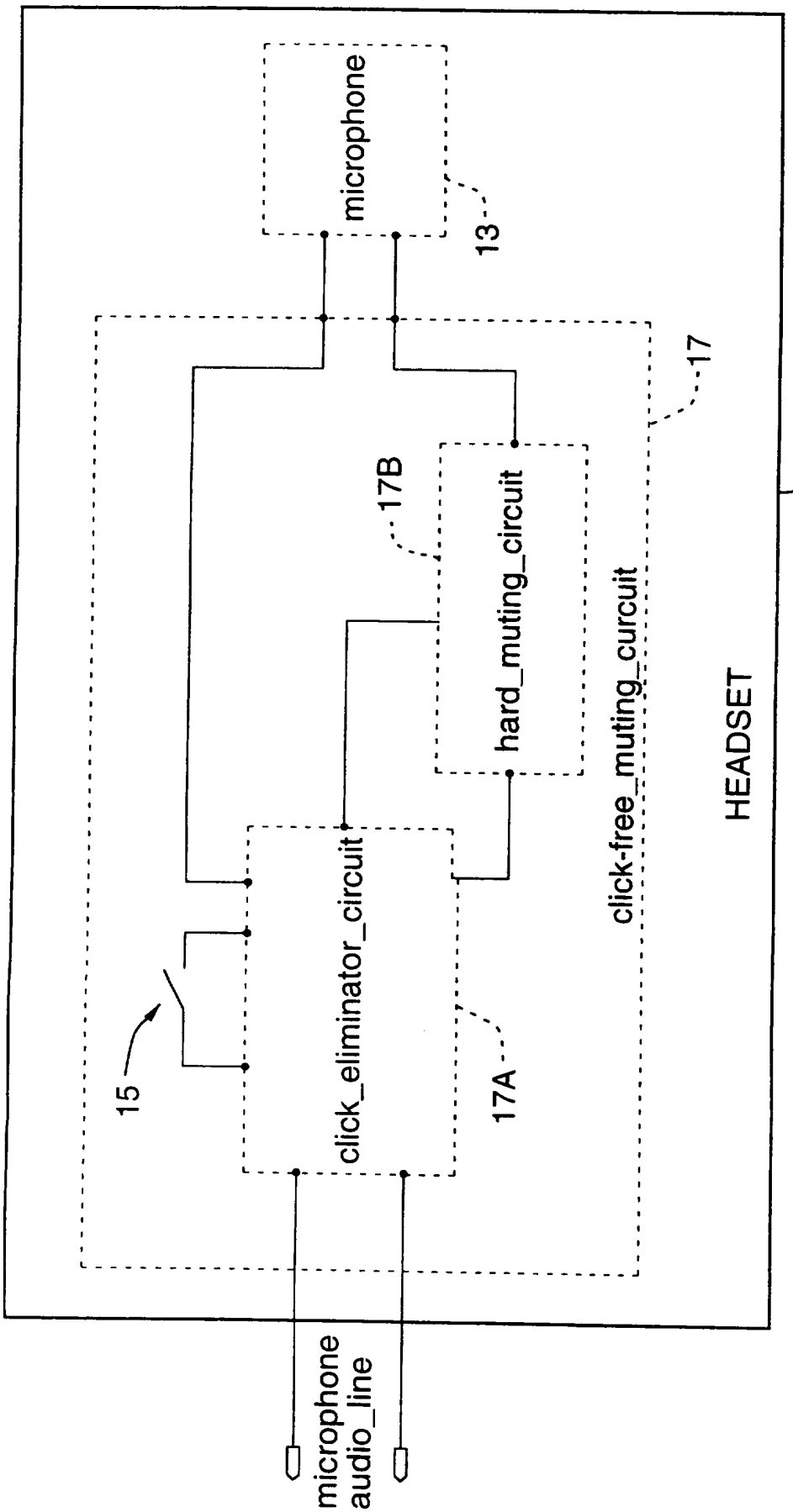
microphone
13
17
17B
hard_muting_circuit
click-free_muting_curcuit
HEADSET
7
15
click_eliminator_circuit
17A
microphone audio_line

FIG.3

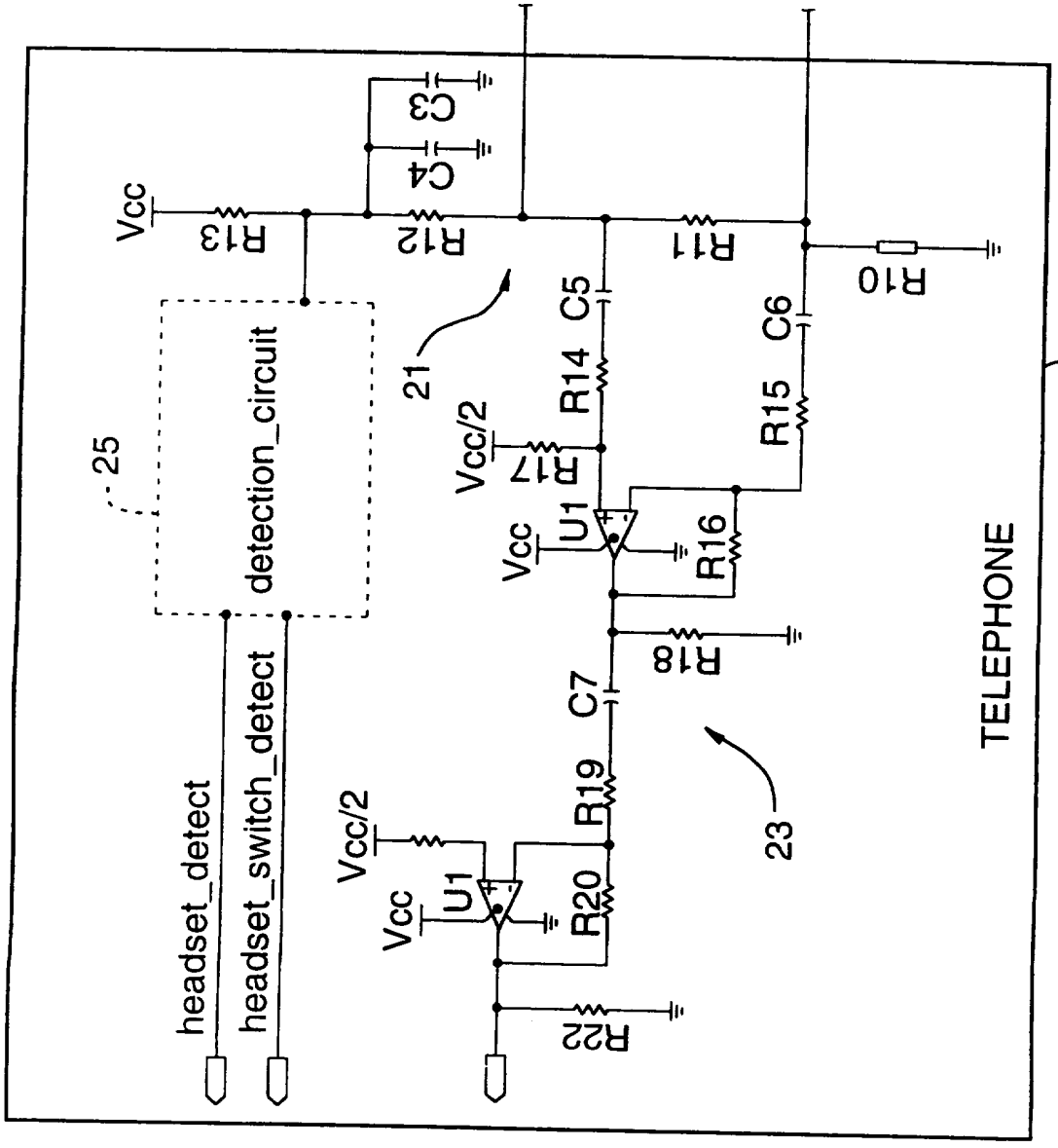
TELEPHONE
1
Vcc
R13
R12
R11
R10
C3
C4
C5
C6
R14
R15
21
Vcc/2
R17
U1
R16
R18
C7
R19
23
R20
R22
25
detection_circuit
headset_detect
headset_switch_detect

FIG.4A

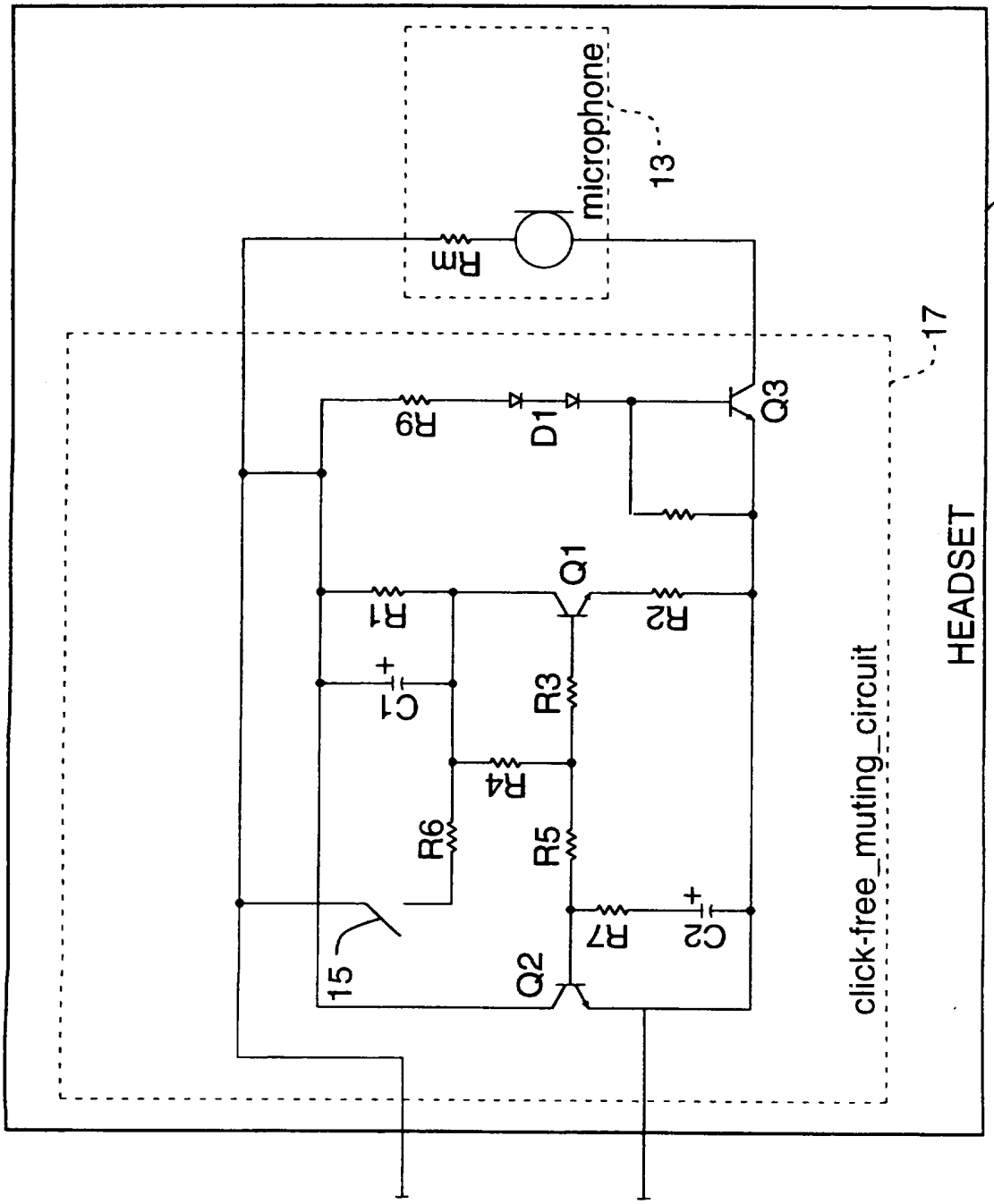
HEADSET
7
microphone
13
Rm
17
click-free_muting_circuit
R9
D1
Q3
Q1
R1
R2
C1
R3
R4
R6
R5
R7
C2
Q2
15

FIG.4B

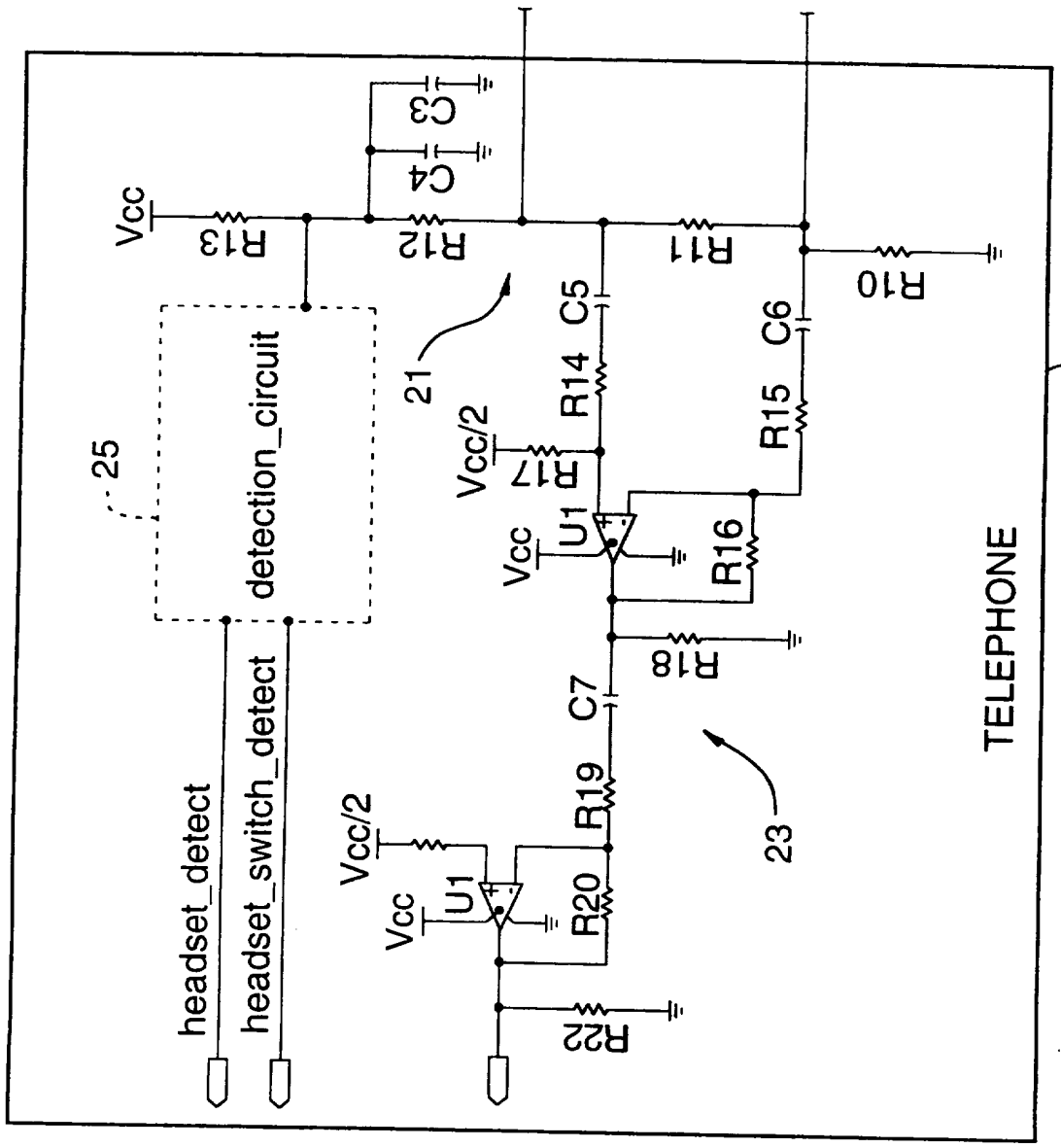
TELEPHONE
1
detection_circuit
25
headset_detect
headset_switch_detect
Vcc
R13
R12
R11
R10
C3
C4
C5
C6
21
R14
R15
Vcc/2
R17
U1
R16
R18
C7
R19
23
R20
R22

FIG.5A

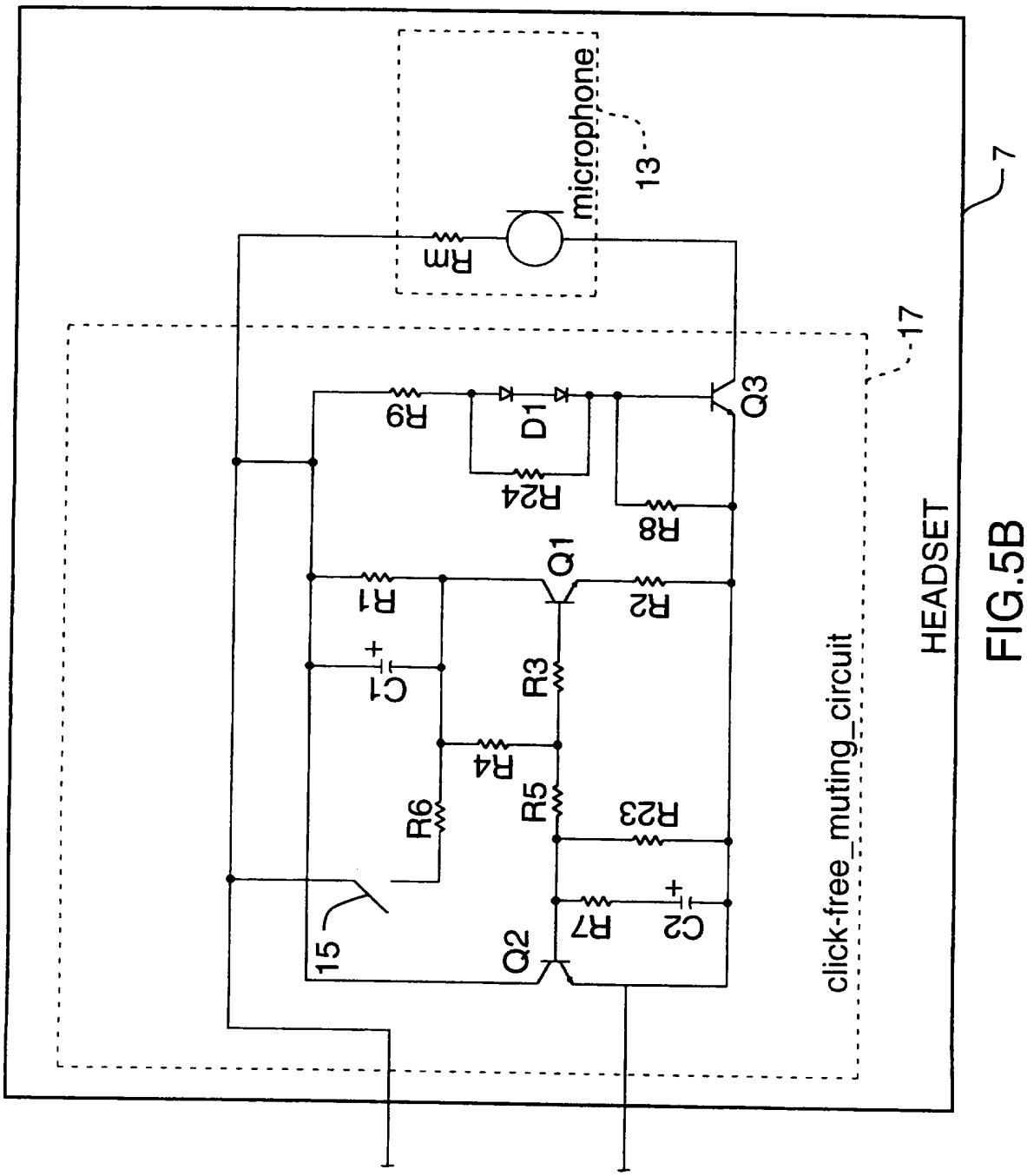
HEADSET
7
microphone
13
Rm
17
click-free_muting_circuit
Q3
R9
D1
R24
R8
Q1
R1
R2
C1
R3
R4
R6
R5
R23
15
Q2
R7
C2

FIG.5B

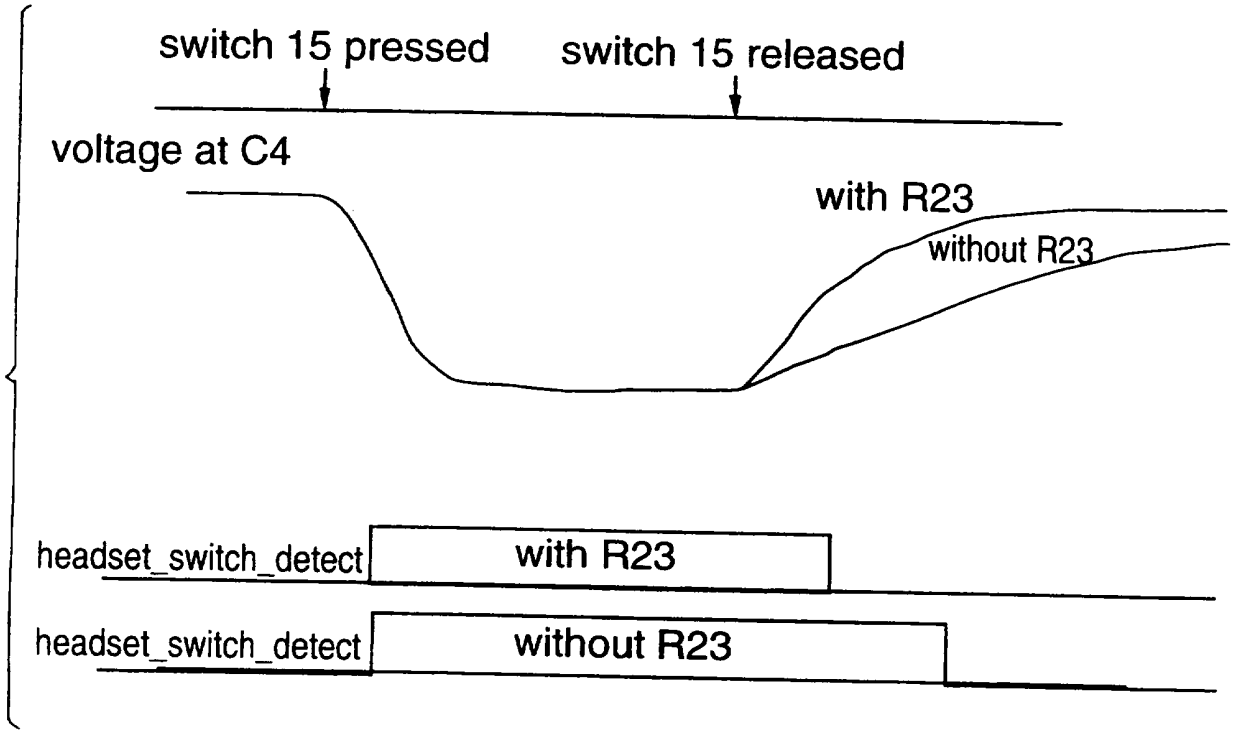
switch 15 pressed
switch 15 released
voltage at C4
with R23
without R23
headset_switch_detect
with R23
headset_switch_detect
without R23

FIG.6

CLICK-FREE MUTING CIRCUIT FOR HEADSET

Field of the Invention

The present invention relates in general to telephone headsets, and more particularly to a circuit for providing click-free muting of a telephone headset.

Background of the Invention

Headsets are useful for hands free telephony in circumstances in which a person requires the use of his or her hands for operation of a computer, switchboard, etc. Headsets are usually connected to the handset port of a telephone set through an interface box. The interface box allows the user to select whether the headset or the handset is activated. Prior art interface boxes vary greatly in complexity, but most boxes include a headset volume control. Some such boxes are battery operated while others steal current from the microphone bias circuit.

One common problem associated with the use of telephone headsets is the generation of unpleasant clicking noises which occur when a mute button for the headset microphone is depressed or released. Another problem is insufficient "hard" muting.

According to one prior art approach, an AC coupled mute switch has been used to provide headset microphone muting. Unfortunately, this approach generally fails to sufficiently attenuate the microphone signal (i.e. no "hard" muting) and is not capable of performing headset switch detection which is a desirable feature of telephone headsets which can function also using a regular handset. DC coupled mute switches overcome the problem of headset switch detection but produce the aforenoted unpleasant click noise. Another approach involves the use of expensive battery powered microphone amplifier muting circuits. These circuits are normally implemented within cumbersome interface boxes attached to the telephone, and often do not provide a hard muting function.

Summary of the Invention

According to the present invention, a circuit is provided which is capable of headset detection and microphone mute switch closure detection and which overcomes the above-discussed disadvantages of the prior art. The circuit provides click-free switching, 80 dB muting and is of inexpensive construction. No extra power supply is required, and the circuit is capable of providing headset detection.

Brief Introduction to the Drawings

A detailed description of the preferred embodiment is provided herein below, with reference to the following drawings, in which:

Figure 1 shows a telephone headset with mute switch connected to a telephone set, in accordance with the present invention;

Figure 2 is a block diagram showing connection of the headset with mute circuit to the telephone set of Figure 1;

Figure 3 is a block diagram of the click-free muting circuit according to the preferred embodiment;

Figure 4 is a circuit diagram of the click-free muting circuit according to a first embodiment connected to the telephone set;

Figure 5 is a circuit diagram of the click-free muting circuit according to a preferred embodiment of the invention; and

Figure 6 is a timing diagram showing differences in operation as between the embodiments of Figures 4 and 5.

Detailed Description of the Preferred Embodiment

In Figure 1, a standard telephone set 1 is shown with a handset 3 thereof resting in a handset cradle. The handset 3 is normally connected to the telephone set via a handset port 5 (e.g. RJ-11). In the illustrated embodiment, a headset 7 is connected to the telephone set 1 via headset port 5 A. The headset may also be connected to the handset port 5 and in that case, the bias circuit 21 (see below) must be designed in such a way that the bias circuit functions with both microphones; the handset microphone and the headset microphone. Headset 7 includes a pair of earpieces 11 and a microphone 13 (e.g. low voltage condenser microphone), in a usual manner.

With reference to Figure 2 in combination with Figure 1, according to the present invention, a switch 15 is connected to a click-free muting circuit 17 which, in turn, is connected across the terminals of microphone 13. Thus, the circuit 17 is connected between the microphone 13 and the microphone audio line connector 19 of the telephone set 1.

Headset microphone bias circuit 21 provides bias current for the microphone 13, in a well known manner. A microphone amplifier 23 is connected differentially to the bias circuit 21 for amplifying the low voltage output signals therefrom. An output of microphone amplifier 23 (analog_signal) is connectable to a phone chip (not shown) within the telephone set 1, in a well known manner. Although not shown, the earpieces 11 of the headset 7 and the earpiece of the handset 3 are normally connected together and to an output of the phone chip.

A headset detector circuit 25 is connected to the output of microphone bias circuit 21 for providing a signal (headset_detect) to the phone chip for indicating that headset 7 is connected to the set 1. Since many headsets are connected to telephones via a "quick-disconnect" plug, when the handset 3 is left in its cradle and the headset 7

is disconnected, it is still possible to use the telephone via the handset operation. The detector circuit 25 also generates a signal (headset_switch_detect) indicative of a momentary depression of the mute switch 15 for interpretation by the phone chip as a hookswitch event for invoking a telephone special feature (e.g. soft hold, call forward, etc.). The structure and operation of the circuit 25 is discussed in greater detail in co-assigned U.S. Patent No. 5832075 entitled "Off-Hook Detector for Headset", the contents of which are incorporated herein by reference.

With reference to Figure 3, the muting circuit 17 is shown comprising a click eliminator circuit 17A and a hard muting circuit 17B. An implementation of the circuit 17 is shown according to the preferred embodiment with reference to the schematic diagram of Figure 4.

In operation, circuit 17 steals current from the bias circuit 21, so that no extra power supply is required. When the switch 15 is closed, the click eliminator circuit 17A slowly creates a short circuit across the microphone 13, thereby suppressing any impulse click noise from being created. Once the click eliminator circuit 17A has fully short circuited the microphone 13, hard muting circuit 17B completely disconnects the microphone 13, thereby resulting in a hard mute (80dB). When the switch 15 is released, hard muting circuit 17B re-connects the microphone 13 and click eliminator circuit 17A slowly removes the short circuit across the microphone 13 , thereby again suppressing impulse switch noise during resumption of microphone operation after muting.

More particularly, having regard to the embodiment illustrated in Figure 4, transistor Q3 is normally on (i.e. saturated by the bias voltage applied across its base-emitter junction) as a result of the base-emitter voltage applied thereto via diodes D1, so that the microphone 13 is normally connected to the line. The use of dual diode D1 ensures two distinct states for operation of transistor Q3 (on and off), regardless of variations in parameters of the microphone and transistor Q3. The transistors Q1 and Q2 are normally off (i.e. the click eliminator circuit 17A does not normally short

circuit the microphone 13), capacitor C1 is normally charged to the voltage across R1 and capacitor C2 is normally charged to a low voltage which is insufficient to turn on transistor Q2. Upon closing switch 15, capacitor C2 begins to charge slowly through resistors R6, R4, R5 and R7 and capacitor C1 begins to discharge slowly thereby gradually turning on transistor Q2 so as to create a short circuit across the terminals of microphone 13. Shortly after the switch 15 is depressed, the voltage at the input of the detection circuit 21 begins to fall and the headset_switch_detect signal changes state so as to indicate mute switch detection. The duration of the headset_switch_detect signal is slightly longer than actual depression of the mute switch 15. The speed of the click elimination circuit 17A is governed by the choice of capacitors C1, C2 and resistors R1, R6, R5 and R7, and further regulated by the turning on of transistor Q1. More particularly, the equivalent resistance of transistor Q2 together with the remaining resistors forms a voltage divider with resistor R1. The current through transistor Q1 is small (in both on and off states) because resistor R1 is of high resistance (e.g. 510K ohm). Once the short circuit is fully established (i.e. the click eliminator circuit 17A is fully on), Q3 is no longer forward biased (as a result of the short circuit through transistor Q2) and turns off, thereby completely disconnecting the microphone 13 from the line and yielding a hard mute (80dB).

Turning to Figure 5, a preferred embodiment of the click-free muting circuit is shown. The circuit of Figure 5 is identical to the circuit of Figure 4 but includes a pair of additional resistors R23 and R24. Resistor R23 is connected between the base and emitter of transistor Q2, while resistor 24 is connected across the dual diode D1.

The addition of resistor 23 regulates the timing and duration of the headset_switch_detect signal generated by detection circuit 25 such that the duration of the signal becomes approximately the same as the duration of depression of the mute switch 15 but is delayed therefrom by a short amount (approximately 100ms in the preferred embodiment). The differences in timing of the headset_switch_detect signal with and without R23 is set forth in Figure 6. As a consequence of the addition of resistor R23, transistor Q1 and resistors R2 and R3 can be eliminated (not shown as

eliminated in Figure 5), resulting in a lower cost circuit. In this latter configuration operation is similar to the circuit of Figure 4 in that the duration of the headset_switch_detect signal becomes slightly longer than the actual duration of mute switch depression. Furthermore, the detection voltage range at the input of detection circuit 25 is somewhat smaller.

Resistor R24 is a zero Ohm resistance which can be used to replace the dual diode D1 (again, the elimination of diodes D1 is not shown in Figure 5), to reduce the cost of the circuit while providing essentially the same functionality. Since resistor R24 exhibits zero resistance (theoretically), it can be eliminated so that either only one diode D1 or no diode can be provided (not shown). If one or both diodes D1 are eliminated in favour of resistor R24 (or no resistor whatsoever) then care must be taken to choose a transistor Q3 having few variations in its stated operating parameters.

Although the switch 15 is shown located at the headset 7, it is also contemplated that the switch could be located at a headset interface box (not shown) between the headset 7 and telephone set 1. In either case, provision of the local switch 15 relieves the user from having to reach over to the set in order to mute the microphone 13. It is also contemplated that the switch 15 can be installed as a retrofit to existing headsets in the form of a series device which can dangle from the cable connecting the headset 7 to the telephone set 1 or interface box .

Other embodiments and variations are possible without departing from the sphere and scope of the invention as defined by the claims appended hereto.

I CLAIM:

1. A click-free muting circuit for a headset microphone connected to a telephone, comprising:

a user operated mute switch; and

a click eliminator circuit connected across said microphone for gradually creating a short circuit across said microphone in response to closure of said mute switch.

2. The click-free muting circuit of claim 1, further comprising a hard muting circuit connected in series with said microphone for disconnecting said microphone in response to said short circuit.

3. The click-free muting circuit of claim 1, wherein said click eliminator circuit further comprises at least one first transistor having a current conducting path connected across said microphone and a control terminal connected via a capacitance to said mute switch such that in response to said closure of the mute switch bias voltage on said control terminal gradually increases thereby turning on said transistor and causing current to flow through said current conducting path.

4. The click-free muting circuit of claim 3, further comprising an additional resistance connected in parallel to said capacitance.

5. The click-free muting circuit of claim 2, wherein said hard muting circuit comprises at least one further transistor having a current conduction path in series with said microphone and a control terminal connected to the current conducting path of said at least one first transistor such that current is drawn from said control terminal of said further transistor thereby turning off said further transistor and disconnecting said microphone via the current conduction path of said further transistor.

6. The click-free muting circuit of claim 3 wherein said at least one first

transistor is a bipolar junction transistor.

7. The click-free muting circuit of claim 5 wherein said further transistor is a bipolar junction transistor.

8. The click-free muting circuit of claim 5, further comprising at least one diode connected to a base terminal of said further transistor.

The Patent Office

9

Application No: GB 9827184.4
Claims searched: 1-8

Examiner: K. Sylvan
Date of search: 12 January 1999

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H3P (PDM,PCCG,PCCB,PCCX) H4J (JGF,JGX)

Int Cl (Ed.6): H03K (17/16) H04R (3/00)

Other: Online: WPI, INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	GB2317783 A	Mitel. See abstract.	-
A	GB0592917A	STC. See figure 3 and page 3 lines 21-37.	-
A	EP0202016 A2	Ampex. See figures 1 and 2.	-
A	US5353347	ACS. See column 11 lines 1-7.	-
A	US4448074	Bosch. See abstract.	-

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.