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(71) Applicant *(for all designated States except US)*: **SEMICONDUCTOR ENERGY LABORATORY CO., LTD.** [JP/JP]; 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **SUZAWA, Hideomi** [JP/JP]; c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD., 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP). **SASAGAWA, Shinya**.

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[Continued on next page]

(54) Title: MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

FIG. 2A

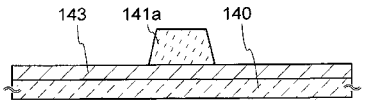


FIG. 2B

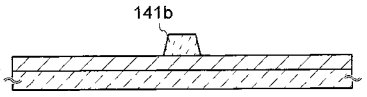


FIG. 2C

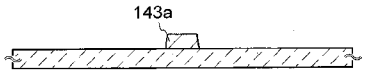


FIG. 2D

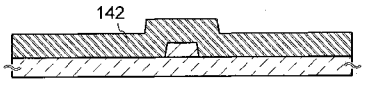


FIG. 2E

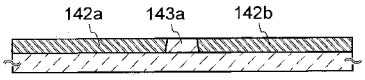


FIG. 2F

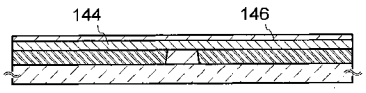
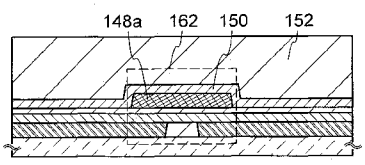


FIG. 2G



(57) Abstract: An embodiment is a manufacturing method of a semiconductor device including the steps of forming a first insulating film; forming a first mask over the first insulating film; performing a slimming process on the first mask to form a second mask; performing an etching process on the first insulating film using the second mask to form a second insulating film; forming a first conductive film covering the second insulating film; performing a polishing process on the first conductive film and the second insulating film to form a third insulating film, a source electrode, and a drain electrode having equal thicknesses; forming an oxide semiconductor film over the third insulating film, the source electrode, and the drain electrode; forming a gate insulating film over the oxide semiconductor film; and forming a gate electrode in a region which is over the gate insulating film and overlaps with the third insulating film.

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DESCRIPTION

MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001]

The technical field of the present invention relates to a semiconductor device and a manufacturing method of the semiconductor device. Here, semiconductor devices refer to general elements and devices which function utilizing semiconductor characteristics.

BACKGROUND ART

[0002]

There are a wide variety of metal oxides and such metal oxides are used for various applications. Indium oxide is a well-known material and has been used for transparent electrodes required in liquid crystal display devices or the like.

[0003]

Some metal oxides have semiconductor characteristics. Examples of such metal oxides having semiconductor characteristics are tungsten oxide, tin oxide, indium oxide, zinc oxide, and the like. Thin film transistors in which a channel formation region is formed using such metal oxides are already known (e.g., see Patent Documents 1 to 4, Non-Patent Document 1, and the like).

[0004]

As metal oxides, not only single-component oxides but also multi-component oxides are known. For example, $InGaO_3(ZnO)_m$ (m: natural number) having a homologous phase is known as a multi-component oxide semiconductor including In, Ga, and Zn (e.g., see Non-Patent Documents 2 to 4 and the like).

[0005]

Furthermore, it has been proved that an oxide semiconductor including such an In-Ga-Zn-based oxide is applicable to a channel formation region of a thin film transistor (e.g., see Patent Document 5, Non-Patent Documents 5 and 6, and the like).

[0006]

In order to achieve high speed operation of a transistor or the like, miniaturization of the transistor is needed. For example, in Patent Document 6, a thin film transistor including an oxide semiconductor used for a channel layer with a thickness of about 10 nm is disclosed. In Non-Patent Document 7, a thin film transistor including an oxide semiconductor whose channel length is 2 μm to 100 μm is disclosed.

[Reference]

[Patent Document]

[0007]

[Patent Document 1] Japanese Published Patent Application No. S60-198861

[Patent Document 2] Japanese Published Patent Application No. H8-264794

[Patent Document 3] Japanese Translation of PCT International Application No. H11-505377

[Patent Document 4] Japanese Published Patent Application No. 2000-150900

[Patent Document 5] Japanese Published Patent Application No. 2004-103957

[Patent Document 6] Japanese Published Patent Application No. 2010-21170

[Non-Patent Document]

[0008]

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[Non-Patent Document 2] M. Nakamura, N. Kimizuka, and T. Mohri, "The Phase Relations in the In_2O_3-Ga_2ZnO_4-ZnO System at 1350 °C," *J. Solid State Chem.*, 1991, Vol. 93, pp. 298-315

[Non-Patent Document 3] N. Kimizuka, M. Isobe, and M. Nakamura, "Syntheses and Single-Crystal Data of Homologous Compounds, $In_2O_3(ZnO)_m$ (m = 3, 4, and 5), $InGaO_3(ZnO)_3$, and $Ga_2O_3(ZnO)_m$ (m = 7, 8, 9, and 16) in the In_2O_3-$ZnGa_2O_4$-ZnO System," *J. Solid State Chem.*, 1995, Vol. 116, pp. 170-178

[Non-Patent Document 4] M. Nakamura, N. Kimizuka, T. Mohri, and M. Isobe, "Syntheses and crystal structures of new homologous compounds, indium iron zinc oxides ($InFeO_3(ZnO)_m$ (m: natural number) and related compounds," *KOTAI BUTSURI*

(SOLID STATE PHYSICS), 1993, Vol. 28, No. 5, pp. 317–327

[Non-Patent Document 5] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, "Thin-film transistor fabricated in single-crystalline transparent oxide semiconductor," *SCIENCE*, 2003, Vol. 300, pp. 1269-1272

[Non-Patent Document 6] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *NATURE*, 2004, Vol. 432, pp. 488-492

[Non-Patent Document 7] T. Kawamura, H. Uchiyama, S. Saito, H. Wakana, T. Mine, and M. Hatano, "Low-Voltage Operating Amorphous Oxide TFTs," IDW'09, pp. 1689-1692

DISCLOSURE OF INVENTION

[0009]

In order to make use of characteristics of an oxide semiconductor such as a light-transmitting property or an advantage that a transistor including an oxide semiconductor can easily have a large size, a glass substrate or the like is sometimes used as a substrate over which a transistor including an oxide semiconductor is formed. However, the difference in height of a surface of the glass substrate is about several tens of micrometers at a maximum, which is large as compared to the case of a silicon wafer or the like. Therefore, the accuracy of photomask projection exposure in semiconductor processing in the case of using a glass substrate is lower than that in the case of using a silicon wafer or the like, and the actual minimum feature size in the case of using a glass substrate is several micrometers at most.

[0010]

In the case of using an exposure apparatus for glass substrates (also referred to as a stepper), the above-described limit of the feature size makes it difficult to achieve sufficient miniaturization at submicron level. However, in order to fully utilize characteristics of an oxide semiconductor or an advantage attributed to the characteristics (e.g., an advantage of easily realizing large size), miniaturization is critical.

[0011]

In the case where a transistor is miniaturized, a defect generated in the

manufacturing process becomes a major problem. For example, in a transistor where a semiconductor layer is formed over a wiring functioning as a source or drain electrode, a gate electrode or the like, the wiring has a larger thickness than the semiconductor layer, which causes poor coverage with the semiconductor layer when the thickness of the semiconductor layer is reduced along with miniaturization. As a result, disconnection, a defective connection, or the like may occur.

[0012]

Further, in the case where the channel length of a transistor is short, another problem of a short channel effect arises. The short channel effect refers to degradation of electric characteristics which becomes obvious along with miniaturization of a transistor (a decrease in channel length (L)). The short channel effect results from the effect of an electric field of a drain on a source. Specific examples of the short channel effect are a decrease in threshold voltage, an increase in S value (subthreshold swing), an increase in leakage current, and the like. The short channel effect is likely to occur particularly in a transistor including an oxide semiconductor because the threshold voltage of such a transistor cannot be controlled by doping, unlike a transistor including silicon.

[0013]

In view of these problems, it is an object of one embodiment of the invention disclosed herein to provide a semiconductor device which suppresses a defect and achieves miniaturization. Further, it is another object of one embodiment of the invention disclosed herein to provide a semiconductor device which achieves miniaturization with favorable characteristics maintained.

[0014]

An embodiment of the invention disclosed herein is a manufacturing method of a semiconductor device, which includes the steps of forming a first insulating film over a flat surface; forming a first mask over the first insulating film; performing a slimming process on the first mask, so that a second mask is formed; performing an etching process on the first insulating film using the second mask, so that a second insulating film is formed; forming a first conductive film covering the second insulating film; performing a polishing process on the first conductive film and the second insulating film, so that a third insulating film, a source electrode, and a drain electrode having

equal thicknesses are formed; forming an oxide semiconductor film over the third insulating film, the source electrode, and the drain electrode; forming a gate insulating film over the oxide semiconductor film; and forming a gate electrode in a region which is over the gate insulating film and overlaps with the third insulating film.

[0015]

In the above-described structure, a difference in height between a part of a surface of the third insulating film and a surface of the source electrode or a difference in height between a part of a surface of the third insulating film and a surface of the drain electrode is preferably less than 5 nm.

[0016]

Another embodiment of the invention disclosed herein is a manufacturing method of a semiconductor device, which includes the steps of forming a first transistor including a channel formation region, a first gate insulating film over the channel formation region, a first gate electrode which is over the first gate insulating film and overlaps with the channel formation region, and a first source electrode and a first drain electrode which are electrically connected to the channel formation region; forming an interlayer insulating film having a flat surface and covering the first transistor; forming a first insulating film over the interlayer insulating film; forming a first mask over the first insulating film; performing a slimming process on the first mask, so that a second mask is formed; performing an etching process on the first insulating film using the second mask, so that a second insulating film is formed; forming a first conductive film covering the second insulating film; performing a polishing process on the first conductive film and the second insulating film, so that a third insulating film, a second source electrode, and a second drain electrode having equal thicknesses are formed; forming an oxide semiconductor film over the third insulating film, the second source electrode, and the second drain electrode; forming a second gate insulating film over the oxide semiconductor film; and forming a second gate electrode in a region which is over the second gate insulating film and overlaps with the third insulating film.

[0017]

In the above-described structure, it is preferable that the third insulating film have a thickness substantially equal to the thickness of the second insulating film. In addition, the flat surface preferably has a root-mean-square roughness of less than or

equal to 1 nm. Further, a difference in height between a part of a surface of the third insulating film and a surface of the second source electrode or a difference in height between a part of a surface of the third insulating film and a surface of the second drain electrode is less than 5 nm.

[0018]

In this specification and the like, the word concerning the thickness "substantially equal" means "almost equal" as well as "completely equal." For example, "substantially equal" refers to a case where, as compared to the "completely equal" thickness situation, there is a difference in thickness that causes a negligible influence on semiconductor device characteristics (a case where the influence on characteristics is 5 % or less), a case where the thickness is slightly reduced by polishing without intention (a case where the polishing amount is less than 5 nm), and the like.

[0019]

Note that in this specification and the like, the root-mean-square (RMS) roughness is obtained by three-dimensionally expanding the RMS roughness of a cross section curve so as to be able to apply it to the measurement surface. The RMS roughness is represented by the square root of the mean value of the square of the deviation from the reference surface to the specific surface, and is obtained by the following formula.

[0020]

[Formula 1]

$$R_{ms} = \sqrt{\frac{1}{S_0}\int_{Y_1}^{Y_2}\int_{X_1}^{X_2}\{F(X,Y) - Z_0\}^2 dXdY}$$

[0021]

Note that the measurement surface is a surface which is shown by all the measurement data, and is represented by the following formula.

[0022]

[Formula 2]

$$Z = F(X,Y)$$

[0023]

The specific surface is a surface which is a target of roughness measurement, and is a rectangular region which is surrounded by four points represented by the coordinates (X_1, Y_1), (X_1, Y_2), (X_2, Y_1), and (X_2, Y_2). The area of the specific surface when the specific surface is flat ideally is denoted by S_0. Note that S_0 can be obtained by the following formula.

[0024]

[Formula 3]

$$S_0 = |X_2 - X_1| \cdot |Y_2 - Y_1|$$

[0025]

In addition, the reference surface refers to a surface parallel to an X-Y surface at the average height of the specific surface. In short, when the average value of the height of the specific surface is denoted by Z_0, the height of the reference surface is also denoted by Z_0. Note that Z_0 can be obtained by the following formula.

[0026]

[Formula 4]

$$Z_0 = \frac{1}{S_0}\int_{Y_1}^{Y_2}\int_{X_1}^{X_2} F(X,Y)dXdY$$

[0027]

Note that in this specification and the like, the root-mean-square (RMS) roughness is calculated in a region of 10 nm × 10 nm, preferably 100 nm × 100 nm, further preferably 1 μm × 1 μm from an AFM image obtained using an atomic force microscope (AFM).

[0028]

In the above-described structure, the slimming process is performed using an ashing process using an oxygen radical. Further, the polishing process is preferably performed using chemical mechanical polishing.

[0029]

Further in the above-described structure, it is preferable that the first insulating film be formed by sputtering.

[0030]

The channel length L of the above-described transistor is preferably less than 2

μm, further preferably greater than or equal to 50 nm and less than or equal to 350 nm, and still further preferably greater than or equal to 100 nm and less than or equal to 150 nm. The thickness of the oxide semiconductor film is greater than or equal to 1 nm and less than or equal to 100 nm, preferably greater than or equal to 2 nm and less than or equal to 50 nm, and further preferably greater than or equal to 3 nm and less than or equal to 30 nm. This can realize a semiconductor device which operates at high speed and consumes low power. In addition, the gate insulating film is preferably formed using a high dielectric constant material such as hafnium oxide. For example, hafnium oxide has a relative permittivity of about 15, which is much higher than that of silicon oxide which is 3 to 4. Such a material facilitates miniaturization of a transistor. Further, the oxide semiconductor film includes an intrinsic oxide semiconductor which is obtained by purification. This enables the carrier density of the oxide semiconductor film to be lower than 1×10^{12} /cm^3, preferably lower than 1.45×10^{10} /cm^3, and the off-state current of the transistor to be smaller than or equal to 100 zA/μm (1 zA (zeptoampere) is 1×10^{-21} A), preferably smaller than or equal to 10 zA/μm, for example. In the case of employing the above-described structure, the off-state current of the transistor can be smaller than or equal to 10^{-21} A/μm and larger than or equal to 1×10^{-30} A/μm. The gate electrode may substantially correspond to a channel formation region between a source electrode and a drain electrode; alternatively, a part of the gate electrode may overlap with a part of a source electrode and a part of a drain electrode. Here, the above expression "the gate electrode corresponds to a channel formation region" means that the gate electrode overlaps with the channel formation region with an end portion and another end portion of the gate electrode aligning with an end portion of the source electrode and an end portion of the drain electrode, respectively, in the plane layout.

[0031]

Note that the semiconductor device in this specification indicates all the devices that can operate by utilizing semiconductor characteristics. For example, a display device, a memory device, an integrated circuit, and the like are included in the category of the semiconductor device.

[0032]

Note that in this specification and the like, the term such as "over" or "below" does not necessarily mean that a component is placed "directly on" or "directly under" another component. For example, the expression "a gate electrode over a gate insulating film" can mean the case where there is an additional component between the gate insulating film and the gate electrode.

[0033]

In addition, in this specification and the like, the term such as "electrode" or "wiring" does not limit the function of the component. For example, an "electrode" can be used as part of "wiring", and vice versa. Further, the term "electrode" or "wiring" can also mean a combination of a plurality of "electrodes" and "wirings" formed in an integrated manner.

[0034]

Functions of a "source" and a "drain" are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flow is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be used to denote the drain and the source, respectively, in this specification.

[0035]

Note that in this specification and the like, the term "electrically connected" includes the case where components are connected through an "object having any electric function." There is no particular limitation on the "object having any electric function" as long as electric signals can be transmitted and received between components that are connected through the object. Examples of the "object having any electric function" are a switching element such as a transistor, a resistor, an inductor, a capacitor, and an element with a variety of functions as well as an electrode and a wiring.

[0036]

In an embodiment of the invention disclosed herein, the channel length of the transistor can be sufficiently made short regardless of the kind of substrate. Therefore, it is possible to provide a semiconductor device which fully utilizes characteristics of an oxide semiconductor or an advantage attributed to the characteristics (e.g., an advantage of easily realizing large size).

[0037]

In an embodiment of the invention disclosed herein, a channel formation region of a transistor is provided over a highly flat region. This makes it possible to prevent a problem such as a short channel effect even under a situation where the channel length of a transistor is short; accordingly, a transistor having favorable characteristics can be provided.

[0038]

The increase in flatness of the surface over which the transistor is formed can make the thickness distribution of the oxide semiconductor film uniform; therefore, characteristics of the transistor can be improved. In addition, a decrease in coverage which may be caused by a large difference in height can be suppressed, and a break (disconnection) due to a step or a defective connection of the oxide semiconductor film can be prevented.

BRIEF DESCRIPTION OF DRAWINGS

[0039]

In the accompanying drawings:

FIG. 1 is a cross-sectional view illustrating an example of the structure of a semiconductor device;

FIGS. 2A to 2G are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 3A to 3C are a cross-sectional view, a plan view, and a circuit diagram of an example of the structure of a semiconductor device;

FIGS. 4A to 4D are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 5A to 5C are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 6A, 6B, and 6C show application examples of a semiconductor device;

FIGS. 7A and 7B show application examples of a semiconductor device;

FIGS. 8A to 8C show an application example of a semiconductor device;

FIG. 9 shows an application example of a semiconductor device;

FIGS. 10A and 10B show an application example of a semiconductor device;

FIGS. 11A to 11F each illustrate an electronic device including a semiconductor device;

FIGS. 12A and 12B illustrate models which were used for simulation;

FIGS. 13A and 13B show calculation results of electric characteristics of transistors which were obtained by simulation;

FIGS. 14A and 14B show calculation results of electric characteristics of transistors which were obtained by simulation;

FIG. 15 shows calculation results of electric characteristics of transistors which were obtained by simulation;

FIG. 16 shows calculation results of electric characteristics of a transistor which were obtained by simulation;

FIG. 17 shows calculation results of electric characteristics of a transistor which were obtained by simulation; and

FIG. 18 shows calculation results of electric characteristics of transistors which were obtained by simulation.

BEST MODE FOR CARRYING OUT THE INVENTION

[0040]

Hereinafter, embodiments of the present invention will be described with reference to the drawings. Note that the present invention is not limited to the following description and it will be easily understood by those skilled in the art that modes and details can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention should not be construed as being limited to the description of the following embodiments.

[0041]

Note that the position, the size, the range, or the like of each structure illustrated in drawings and the like is not accurately represented in some cases for easy understanding. Therefore, the invention disclosed herein is not necessarily limited to such position, size, range, and the like disclosed in the drawings and the like.

[0042]

In this specification and the like, ordinal numbers such as “first”, “second”, and “third” are used in order to avoid confusion among components, and the terms do not

limit the components numerically.

[0043]

(Embodiment 1)

In this embodiment, a structure and a manufacturing method of a semiconductor device according to an embodiment of the invention disclosed herein will be described with reference to FIG. 1 and FIGS. 2A to 2G.

[0044]

<Example of Structure of Semiconductor Device>

FIG. 1 illustrates an example of the structure of a semiconductor device.

[0045]

A transistor 162 in FIG. 1 includes an insulating film 143a over a substrate 140 having a surface over which components are formed, a source electrode 142a and a drain electrode 142b between which the insulating film 143a is sandwiched, an oxide semiconductor film 144 in contact with a part of an upper surface of the insulating film 143a, a part of an upper surface of the source electrode 142a, and a part of an upper surface of the drain electrode 142b, a gate insulating film 146 covering the oxide semiconductor film 144, and a gate electrode 148a over the gate insulating film 146.

[0046]

The channel length of the transistor 162 is preferably less than 2 μm, further preferably greater than or equal to 50 nm and less than or equal to 350 nm, and still further preferably greater than or equal to 100 nm and less than or equal to 150 nm. The thickness of the oxide semiconductor film is greater than or equal to 1 nm and less than or equal to 100 nm, preferably greater than or equal to 2 nm and less than or equal to 50 nm, and further preferably greater than or equal to 3 nm and less than or equal to 30 nm. This can realize a semiconductor device which operates at high speed and consumes low power.

[0047]

In the transistor 162, the insulating film 143a preferably has a tapered shape. The taper angle can be, for example, greater than or equal to 30° and less than or equal to 60°. Note that the "taper angle" means an angle formed by the side surface and the bottom surface of a layer having a tapered shape (e.g., the insulating film 143a) when

observed from a direction perpendicular to a cross section thereof (a plane perpendicular to a surface of the substrate 140).

[0048]

With the use of an oxide semiconductor for an active layer of the transistor illustrated in FIG. 1, favorable characteristics can be obtained. In addition, as illustrated in FIG. 1, the oxide semiconductor film used as an active layer of the transistor preferably has a flat shape.

[0049]

In addition, a part of the upper surface of the insulating film 143a (particularly referring to a region parallel to the surface over which components are formed), which is in contact with the oxide semiconductor film, has a root-mean-square (RMS) roughness of 1 nm or less. The difference in height between the part of the upper surface of the insulating film 143a and the upper surface of the source electrode 142a or the difference in height between the part of the upper surface of the insulating film 143a and the upper surface of the drain electrode 142b is less than 5 nm.

[0050]

As described above, in one embodiment of the invention disclosed herein, a channel formation region of the transistor 162 is provided over a highly flat region having a root-mean-square (RMS) roughness of 1 nm or less. This makes it possible to prevent a problem such as a short channel effect even under a situation where the channel length of the transistor 162 is short; accordingly, the transistor 162 having favorable characteristics can be obtained.

[0051]

The increase in flatness of the surface over which components are formed can make the thickness distribution of the oxide semiconductor film 144 uniform; therefore, characteristics of the transistor 162 can be improved. In addition, a decrease in coverage which may be caused by a large difference in height can be suppressed, and a break (disconnection) due to a step or a defective connection of the oxide semiconductor film 144 can be prevented.

[0052]

Here, the oxide semiconductor film 144 is preferably an oxide semiconductor film which is purified by sufficiently removing an impurity such as hydrogen therefrom

and/or by sufficiently supplying oxygen thereto. Specifically, the hydrogen concentration of the oxide semiconductor film 144 is 5×10^{19} atoms/cm^3 or less, preferably 5×10^{18} atoms/cm^3 or less, further preferably 5×10^{17} atoms/cm^3 or less, for example. Note that the above hydrogen concentration of the oxide semiconductor film 144 is measured by secondary ion mass spectrometry (SIMS). In the oxide semiconductor film 144 in which hydrogen is reduced to a sufficiently low concentration so that the oxide semiconductor film is purified and in which a defect level in an energy gap induced by oxygen deficiency is reduced by sufficiently supplying oxygen as described above, the density of carriers induced by a donor such as hydrogen is less than 1×10^{12} /cm^3, preferably less than 1×10^{11} /cm^3, and further preferably less than 1.45×10^{10} /cm^3. In addition, for example, the off-state current (per unit channel width (1 μm), here) at room temperature (25 °C) is 100 zA (1 zA (zeptoampere) is 1×10^{-21} A) or smaller, preferably 10 zA or smaller. In the case of employing the above-described structure, the off-state current of the transistor can be smaller than or equal to 10^{-21} A/μm and larger than or equal to 10^{-30} A/μm. In this manner, by using an i-type (intrinsic) or substantially i-type oxide semiconductor, the transistor 162 which has extremely favorable off-state current characteristics can be obtained. In addition, by using an i-type or substantially i-type oxide semiconductor, a problem with a transistor, which may be caused by the thickness of the oxide semiconductor film, can be prevented.

[0053]

<Example of Manufacturing Method of Semiconductor Device>

Next, an example of a manufacturing method of the semiconductor device will be described with reference to FIGS. 2A to 2G. Here, FIGS. 2A to 2G illustrate an example of a manufacturing method of the transistor 162 illustrated in FIG. 1.

[0054]

The following description is made with reference to FIGS. 2A to 2G. First, the insulating film 143 is formed over the substrate 140 having the surface over which components are formed, and then a mask 141a is formed (see FIG. 2A).

[0055]

Although there is no particular limitation on a substrate which can be used as

the substrate 140, it is necessary that the substrate 140 has at least heat resistance high enough to withstand heat treatment to be performed later. For example, the substrate may be a glass substrate, a ceramic substrate, a quartz substrate, a sapphire substrate, or the like. Alternatively, the substrate may be a single crystal semiconductor substrate or a polycrystalline semiconductor substrate of silicon, silicon carbide, or the like, a compound semiconductor substrate of silicon germanium or the like, an SOI substrate, or the like as long as the substrate has an insulating surface. Still alternatively, the substrate may be any of these substrates provided with a semiconductor element provided thereover. Further, a base film may be provided over the substrate 140.

[0056]

Note that the surface over which components are formed of the substrate 140 is preferably a sufficiently flat surface. For example, the surface over which components are formed of the substrate 140 may have a root-mean-square (RMS) roughness of 1 nm or less (preferably 0.5 nm or less). When the transistor 162 is formed over such a surface, the characteristics can be sufficiently improved. In the case where the surface over which components are formed of the substrate 140 has poor flatness, it is desirable that the surface be subjected to a chemical mechanical polishing (CMP) process, an etching process, or the like so as to have the above flatness. Note that, for the details of the CMP process, the later description of CMP process for a conductive film 142 can be referred to.

[0057]

The insulating film 143 can be formed using an inorganic insulating material such as silicon oxide, silicon oxynitride, silicon nitride, aluminum oxide, or gallium oxide. It is particularly preferable that the insulating film 143 be formed using silicon oxide because the oxide semiconductor film 144 formed later is in contact with the insulating film 143. Although there is no particular limitation on the formation method of the insulating film 143, in consideration of contact with the oxide semiconductor film 144, a method in which hydrogen is sufficiently reduced is preferably employed. As an example of such a method, a sputtering method and the like can be given. Needless to say, another deposition method such as a plasma CVD method may be used.

[0058]

The mask 141a can be formed by a photolithography technique using a material such as a photoresist. For light exposure at the time of forming the mask 141a, extreme ultraviolet light having a wavelength as short as several nanometers to several tens of nanometers is preferably used. The resolution of light exposure using extreme ultraviolet light is high and the depth of focus is large. Thus, the mask 141a can have a fine pattern.

[0059]

As long as it is possible to form the mask 141a having a sufficiently fine pattern, a different method such as an ink-jet method may be used to form the mask 141a. In this case, it is unnecessary to use a photosensitive material such as a photoresist as a material of the mask 141a.

[0060]

Next, a slimming process is performed on the mask 141a (see FIG. 2B). Through the slimming process on the mask 141a, a mask 141b having a dimension less than or equal to the resolution limit of lithography can be formed. The slimming process can be performed using an ashing process in which oxygen radicals are mainly used. Here, the line width of the mask 141b formed through the slimming process can be as narrow as less than or equal to half of the resolution limit, preferably less than or equal to one third of the resolution limit. For example, the line width can become more than or equal to 30 nm and less than or equal to 2000 nm (2 μm), preferably more than or equal to 50 nm and less than or equal to 350 nm, and further preferably more than or equal to 100 nm and less than or equal to 150 nm.

[0061]

Then, the insulating film 143 is etched using the mask 141b, so that the insulating film 143a is formed (see FIG. 2C).

[0062]

Although either dry etching or wet etching may be performed as the etching of the insulating film 143, dry etching with high controllability is preferably used for miniaturization. The etching may be performed so that the insulating film 143a to be formed have a tapered shape. The taper angle can be, for example, greater than or equal to 30° and less than or equal to 60°.

[0063]

Next, the conductive film 142 is formed so as to cover the substrate 140 and the insulating film 143a (see FIG. 2D).

[0064]

The above-described conductive film 142 can be formed by a PVD method such as a sputtering method, or a CVD method such as a plasma CVD method. As a material of the conductive film 142, an element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, and tungsten, an alloy including any of these elements as a component, or the like can be used. A material including one of manganese, magnesium, zirconium, beryllium, neodymium, or scandium or a combination of a plurality of these elements may be used.

[0065]

The conductive film 142 may have a single-layer structure or a stacked structure including two or more layers. For example, the conductive film 142 may have a single-layer structure of a titanium film or a titanium nitride film, a single-layer structure of an aluminum film including silicon, a two-layer structure in which a titanium film is stacked over an aluminum film, a two-layer structure in which a titanium film is stacked over a titanium nitride film, a two-layer structure in which a copper film is stacked over a copper-magnesium-aluminum alloy film, a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order, or the like.

[0066]

The conductive film 142 may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), an indium oxide-tin oxide alloy (In_2O_3-SnO_2, which is abbreviated to ITO in some cases), an indium oxide-zinc oxide alloy (In_2O_3-ZnO), or any of these metal oxide materials including silicon or silicon oxide can be used.

[0067]

Next, a CMP process is performed on the conductive film 142 (see FIG. 2E). Through the CMP process on the conductive film 142 under such conditions as to expose the surface of the insulating film 143a, the source electrode 142a and the drain electrode 142b can be formed.

[0068]

The CMP process is a method for planarizing a surface of an object with a combination of chemical and mechanical actions. More specifically, the CMP process is a method in which a polishing cloth is attached to a polishing stage, the polishing stage and an object are each rotated or swung while a slurry (an abrasive) is supplied between the object and the polishing cloth, and the surface of the object is polished by a chemical reaction between the slurry and the object and by a mechanical polishing action of the polishing cloth on the object.

[0069]

Through the CMP process, the root-mean-square (RMS) roughness of surfaces of the source electrode 142a and the drain electrode 142b can be 1 nm or less (preferably 0.5 nm or less). In some cases, the surface of the insulating film 143a may also be polished through the CMP process; in such a case, the root-mean-square (RMS) roughness of the surface of the insulating film 143a may also become 1 nm or less (preferably 0.5 nm or less). Needless to say, a polishing process for the purpose of polishing the surface of the insulating film 143a may also be employed. By the CMP process under theses conditions, the flatness of the surface over which the oxide semiconductor film 144 is formed later can be increased, and characteristics of the transistor 162 can be improved accordingly.

[0070]

Note that the CMP process may be performed only once or plural times. When the CMP process is performed in plural times, it is preferable that a first polishing step be performed at a high polishing rate and then a second polishing step be performed at a low polishing rate. By performing polishing steps with different polishing rates in combination, the flatness of the surfaces of the source electrode 142a, the drain electrode 142b, and the insulating film 143a can be further increased.

[0071]

Preferably, the thickness of the insulating film 143a and the thicknesses of the source electrode 142a and the drain electrode 142b become equal to each other by the CMP process. In addition, the difference in height between the part of the upper surface of the insulating film 143a and the upper surface of the source electrode 142a or the difference in height between the part of the upper surface of the insulating film 143a

and the upper surface of the drain electrode 142b is preferably set to less than 5 nm.

[0072]

Note that after the above-described etching process, another etching process may be performed to process the source electrode 142a and the drain electrode 142b into a desired pattern. Details of the etching process for processing the pattern are similar to those of the above-described etching process.

[0073]

The channel length (L) of the transistor is determined by a distance between an upper end portion of the source electrode 142a and an upper end portion of the drain electrode 142b. That is, the channel length is determined by the length of the insulating film 143a in the channel length direction of the transistor. Through the process of forming the conductive film 142 covering the insulating film 143a having a dimension less than or equal to the resolution limit of lithography and performing the polishing process on the conductive film 142, the distance between the upper end portion of the source electrode 142a and the upper end portion of the drain electrode 142b, which determines the channel length of the transistor, can be set short. In this manner, the channel length L of the transistor can be less than 2 μm, for example greater than or equal to 50 nm and less than or equal to 350 nm, and preferably greater than or equal to 100 nm and less than or equal to 150 nm, which enables miniaturization of the transistor. Therefore, a semiconductor device which operates at high speed and consumes low power can be realized.

[0074]

Next, the oxide semiconductor film 144 covering the above-described surfaces is formed in contact with a part of the source electrode 142a, a part of the drain electrode 142b, and a part of the insulating film 143a, and then the gate insulating film 146 is formed so as to cover the oxide semiconductor film 144 (see FIG. 2F).

[0075]

The oxide semiconductor film includes at least one element selected from In, Ga, Sn, and Zn. For example, a four-component metal oxide such as an In-Sn-Ga-Zn-O-based oxide semiconductor, a three-component metal oxide such as an In-Ga-Zn-O-based oxide semiconductor, an In-Sn-Zn-O-based oxide semiconductor, an In-Al-Zn-O-based oxide semiconductor, a Sn-Ga-Zn-O-based oxide semiconductor, an

Al-Ga-Zn-O-based oxide semiconductor, or a Sn-Al-Zn-O-based oxide semiconductor, a two-component metal oxide such as an In-Zn-O-based oxide semiconductor, a Sn-Zn-O-based oxide semiconductor, an Al-Zn-O-based oxide semiconductor, a Zn-Mg-O-based oxide semiconductor, a Sn-Mg-O-based oxide semiconductor, an In-Mg-O-based oxide semiconductor, or an In-Ga-O-based oxide semiconductor, a single-component metal oxide such as an In-O-based oxide semiconductor, a Sn-O-based oxide semiconductor, or a Zn-O-based oxide semiconductor, or the like can be used. The above oxide semiconductors may include an element other than In, Ga, Sn, and Zn, for example, SiO_2.

[0076]

For example, an In-Ga-Zn-O-based oxide semiconductor means an oxide semiconductor containing indium (In), gallium (Ga), and zinc (Zn), and there is no limitation on the composition ratio thereof.

[0077]

In particular, an In-Ga-Zn-O-based oxide semiconductor material has sufficiently high resistance when there is no electric field and thus off-state current can be sufficiently reduced. In addition, also having high field-effect mobility, the In-Ga-Zn-O-based oxide semiconductor material is suitable as a semiconductor material used in a semiconductor device.

[0078]

As a typical example of the In-Ga-Zn-O-based oxide semiconductor material, an oxide semiconductor material represented by $InGaO_3(ZnO)_m$ ($m > 0$) is given. Using M instead of Ga, there is an oxide semiconductor material represented by $InMO_3(ZnO)_m$ ($m > 0$). Here, M denotes one or more metal elements selected from gallium (Ga), aluminum (Al), iron (Fe), nickel (Ni), manganese (Mn), cobalt (Co), or the like. For example, M may be Ga, Ga and Al, Ga and Fe, Ga and Ni, Ga and Mn, Ga and Co, or the like. Note that the above-described compositions are derived from the crystal structures that the oxide semiconductor material can have, and are mere examples.

[0079]

As a target for forming the oxide semiconductor film using a sputtering method, a target having a composition ratio of In:Ga:Zn = 1:x:y (x is 0 or more and y is more

than or equal to 0.5 and less than or equal to 5) is preferably used. For example, a metal oxide target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:2 [molar ratio] or the like can be used. Furthermore, a metal oxide target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:1 [molar ratio], a metal oxide target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:4 [molar ratio], or a metal oxide target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:0:2 [molar ratio] can also be used.

[0080]

In the case where an In-Zn-O-based material is used as the oxide semiconductor, a target used has a composition ratio of In:Zn = 50:1 to 1:2 in an atomic ratio (In_2O_3:ZnO = 25:1 to 1:4 in a molar ratio), preferably In:Zn = 20:1 to 1:1 in an atomic ratio (In_2O_3:ZnO = 10:1 to 1:2 in a molar ratio), further preferably In:Zn = 15:1 to 1.5:1 (In_2O_3:ZnO = 15:2 to 3:4 in a molar ratio). For example, in a target used for forming an In-Zn-O-based oxide semiconductor which has an atomic ratio of In:Zn:O = X:Y:Z, the relation of $Z > 1.5X+Y$ is satisfied.

[0081]

In this embodiment, the oxide semiconductor film 144 having an amorphous structure is formed by a sputtering method with the use of an In-Ga-Zn-O-based metal oxide target. The thickness ranges from 1 nm to 50 nm, preferably from 2 nm to 20 nm, further preferably from 3 nm to 15 nm.

[0082]

The relative density of the metal oxide in the metal oxide target is 80 % or more, preferably 95 % or more, and further preferably 99.9 % or more. The use of the metal oxide target having high relative density makes it possible to form an oxide semiconductor film having a dense structure.

[0083]

The atmosphere in which the oxide semiconductor film 144 is formed is preferably a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere containing a rare gas (typically, argon) and oxygen. Specifically, it is preferable to use a high-purity gas atmosphere, for example, from which an impurity such as hydrogen, water, a hydroxyl group, or hydride is removed to a concentration of 1 ppm or less (preferably, 10 ppb or less).

[0084]

In forming the oxide semiconductor film 144, for example, an object to be processed is held in a treatment chamber that is maintained in reduced pressure, and the object is heated to a temperature higher than or equal to 100 °C and lower than 550 °C, preferably higher than or equal to 200 °C and lower than or equal to 400 °C. Alternatively, the temperature of an object to be processed in forming the oxide semiconductor film 144 may be room temperature (25 °C ± 10 °C). Then, moisture in the treatment chamber is removed, a sputtering gas from which hydrogen, water, or the like has been removed is introduced, and the above-described target is used; thus, the oxide semiconductor film 144 is formed. By forming the oxide semiconductor film 144 while heating the object, an impurity in the oxide semiconductor film 144 can be reduced. Moreover, damage due to sputtering can be reduced. In order to remove the moisture in the treatment chamber, it is preferable to use an entrapment vacuum pump. For example, a cryopump, an ion pump, a titanium sublimation pump, or the like can be used. A turbo pump provided with a cold trap may be used. Since it is possible to remove hydrogen, water, or the like from the treatment chamber by evacuating the treatment chamber with a cryopump or the like, the concentration of an impurity in the oxide semiconductor film can be reduced.

[0085]

For example, conditions for forming the oxide semiconductor film 144 can be set as follows: the distance between the object to be processed and the target is 170 mm, the pressure is 0.4 Pa, the direct current (DC) power is 0.5 kW, and the atmosphere is an oxygen (100 % oxygen) atmosphere, an argon (100 % argon) atmosphere, or a mixed atmosphere of oxygen and argon. Note that a pulsed direct current (DC) power supply is preferably used because powder substances (also referred to as particles or dust) formed at the time of the film formation can be reduced and the film thickness can be made uniform. The thickness of the oxide semiconductor film 144 is set in the range of 1 nm to 100 nm, preferably 2 nm to 50 nm, further preferably 3 nm to 30 nm. By employing a structure according to the invention disclosed herein, a short channel effect due to a decrease in channel length can be suppressed even in the case of using the oxide semiconductor film 144 having such a thickness. Note that the appropriate

thickness of the oxide semiconductor film differs depending on the oxide semiconductor material used, the intended use of the semiconductor device, or the like; therefore, the thickness can be determined as appropriate in accordance with the material, the intended use, or the like. Note that a surface over which the oxide semiconductor film 144 is formed is sufficiently planarized in one embodiment of the invention disclosed herein. Therefore, even an oxide semiconductor film having a small thickness can be favorably formed. In addition, in one embodiment of the invention disclosed herein, the oxide semiconductor film 144 preferably has a flat cross-sectional shape, as illustrated in FIG. 2F. In the case where the oxide semiconductor film 144 has a flat cross-sectional shape, leakage current can be reduced more, as compared to the case where the oxide semiconductor film 144 does not have a flat cross-sectional shape.

[0086]

Note that before the oxide semiconductor film 144 is formed by a sputtering method, reverse sputtering in which an argon gas is introduced and plasma is generated may be performed so that a material attached to a surface over which the oxide semiconductor film 144 is to be formed (e.g., the surface of the insulating film 143a) is removed. Here, the reverse sputtering is a method in which ions collide with a surface so that the surface is modified, in contrast to normal sputtering in which ions collide with a sputtering target. An example of a method for making ions collide with a surface is a method in which high-frequency voltage is applied to the surface side in an argon atmosphere so that plasma is generated near the object. Note that an atmosphere of nitrogen, helium, oxygen, or the like may be used instead of an argon atmosphere.

[0087]

After the oxide semiconductor film 144 is formed, heat treatment (first heat treatment) is preferably performed on the oxide semiconductor film 144. Through the first heat treatment, excess hydrogen (including water or a hydroxyl group) in the oxide semiconductor film 144 can be removed, the structure of the oxide semiconductor film 144 can be ordered, and a defect level in an energy gap can be reduced. For example, the temperature of the first heat treatment is set higher than or equal to 300 °C and lower than 550 °C, or higher than or equal to 400 °C and lower than or equal to 500 °C.

[0088]

For example, after an object to be processed is introduced into an electric furnace including a resistance heater or the like, heat treatment can be performed at 450 °C for one hour in a nitrogen atmosphere. The oxide semiconductor film 144 is not exposed to the air during the heat treatment so that entry of water or hydrogen can be prevented.

[0089]

The heat treatment apparatus is not limited to the electric furnace and may be an apparatus for heating an object by thermal radiation or thermal conduction from a medium such as a heated gas. For example, a rapid thermal annealing (RTA) apparatus such as a gas rapid thermal annealing (GRTA) apparatus or a lamp rapid thermal annealing (LRTA) apparatus can be used. The LRTA apparatus is an apparatus for heating an object by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. The GRTA apparatus is an apparatus for performing heat treatment using a high-temperature gas. As the gas, an inert gas that does not react with an object by heat treatment, for example, nitrogen or a rare gas such as argon, is used.

[0090]

For example, as the first heat treatment, a GRTA process may be performed as follows. The object to be processed is put in a heated inert gas atmosphere, heated for several minutes, and taken out of the inert gas atmosphere. The GRTA process enables high-temperature heat treatment in a short time. Moreover, the GRTA process can be employed even when the temperature exceeds the upper temperature limit of the object. Note that the inert gas may be switched to a gas including oxygen during the process. This is because a defect level in energy gap due to oxygen deficiency can be reduced by performing the first heat treatment in an atmosphere containing oxygen.

[0091]

Note that as the inert gas atmosphere, an atmosphere that contains nitrogen or a rare gas (e.g., helium, neon, or argon) as its main component and does not contain water, hydrogen, or the like is preferably used. For example, the purity of nitrogen or a rare gas such as helium, neon, or argon introduced into a heat treatment apparatus is greater

than or equal to 6 N (99.9999 %), preferably greater than or equal to 7 N (99.99999 %) (that is, the concentration of the impurities is 1 ppm or less, preferably 0.1 ppm or less).

[0092]

In any case, impurities are reduced by the first heat treatment so that an i-type (intrinsic) or substantially i-type oxide semiconductor film is obtained. Accordingly, a transistor having highly excellent characteristics can be realized. In addition, by using an i-type (intrinsic) or substantially i-type oxide semiconductor film, a problem with a transistor, which may be caused by the thickness of the oxide semiconductor film, can be prevented.

[0093]

The above heat treatment (the first heat treatment) can be referred to as dehydration treatment, dehydrogenation treatment, or the like because of its effect of removing hydrogen, water, or the like. The dehydration treatment or the dehydrogenation treatment can also be performed at the following timing: after the formation of the oxide semiconductor film 144, after the formation of the gate insulating film 146, after the formation of the gate electrode, or the like. Such dehydration treatment or dehydrogenation treatment may be conducted only once or plural times.

[0094]

After the oxide semiconductor film 144 is formed, the oxide semiconductor film 144 may be processed into an island-shaped oxide semiconductor film, for example, by etching. The etching of the oxide semiconductor film may be performed either before the heat treatment or after the heat treatment. Although dry etching is preferred in terms of element miniaturization, wet etching may be used. An etching gas and an etchant can be selected as appropriate depending on a material of the film to be etched.

[0095]

The gate insulating film 146 can be formed by a CVD method, a sputtering method, or the like. The gate insulating film 146 is preferably formed so as to contain gallium oxide, silicon oxide, silicon nitride, silicon oxynitride, aluminum oxide, gallium oxide, tantalum oxide, hafnium oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate to which nitrogen is added ($HfSi_xO_yN_z$ ($x > 0$, $y > 0$, $z > 0$)),

hafnium aluminate to which nitrogen is added ($HfAl_xO_yN_z$ ($x > 0$, $y > 0$, $z > 0$)), or the like. The gate insulating film 146 may have a single-layer structure or a stacked structure. There is no particular limitation on the thickness of the gate insulating film 146; the thickness is preferably small in order to ensure the operation of the transistor when the semiconductor device is miniaturized. For example, in the case of using silicon oxide, the thickness can be greater than or equal to 1 nm and less than or equal to 100 nm, preferably greater than or equal to 10 nm and less than or equal to 50 nm.

[0096]

When the gate insulating film 146 is thin as described above, gate leakage due to a tunnel effect or the like becomes a problem. In order to solve the problem of gate leakage, the gate insulating film 146 may be formed using a high dielectric constant (high-k) material such as hafnium oxide, tantalum oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate to which nitrogen is added ($HfSi_xO_yN_z$ ($x > 0$, $y > 0$, $z > 0$)), or hafnium aluminate to which nitrogen is added ($HfAl_xO_yN_z$ ($x > 0$, $y > 0$, $z > 0$)). The use of a high-k material for the gate insulating film 146 makes it possible to increase the thickness in order to suppress gate leakage as well as ensuring electric characteristics. For example, hafnium oxide is preferable as a material of the gate insulating film because the relative permittivity of hafnium oxide is approximately 15, which is much higher than that of silicon oxide which is 3 to 4. Note that a stacked structure of a film including a high-k material and a film including any of gallium oxide, silicon oxide, silicon nitride, silicon oxynitride, silicon nitride oxide, aluminum oxide, or the like may also be employed.

[0097]

After the gate insulating film 146 is formed, second heat treatment is preferably performed in an inert gas atmosphere or an oxygen atmosphere. The temperature of the heat treatment is set in the range of higher than or equal to 200 °C and lower than or equal to 450 °C, preferably higher than or equal to 250 °C and lower than or equal to 350 °C. For example, the heat treatment may be performed at 250 °C for one hour in a nitrogen atmosphere. By the second heat treatment, variation in electric characteristics of the transistor can be reduced. In the case where the gate insulating film 146 contains oxygen, oxygen can be supplied to the oxide semiconductor film 144 and

oxygen vacancies in the oxide semiconductor film 144 can be filled; thus, the oxide semiconductor film 144 which is i-type (intrinsic) or substantially i-type can be formed.

[0098]

In this embodiment, the second heat treatment is performed after the gate insulating film 146 is formed; however, the timing of the second heat treatment is not limited to this. For example, the second heat treatment may be performed after the gate electrode is formed. Alternatively, the first heat treatment and the second heat treatment may be performed in succession, or the first heat treatment may double as the second heat treatment, or the second heat treatment may double as the first heat treatment.

[0099]

By performing at least one of the first heat treatment and the second heat treatment as described above, the oxide semiconductor film 144 can be purified so as to contain impurities other than main components thereof as little as possible.

[0100]

Next, the gate electrode 148a is formed over the gate insulating film 146. Then, an insulating film 150 and an insulating film 152 are formed so as to cover the gate insulating film 146, the gate electrode 148a, and the like (see FIG. 2G).

[0101]

The gate electrode 148a can be formed by forming a conductive film over the gate insulating film 146 and then selectively etching the conductive film. The conductive film to be the gate electrode 148a can be formed by a PVD method such as a sputtering method, or a CVD method such as a plasma CVD method. The details are similar to those in the case of forming the conductive film 142; thus, the description thereof can be referred to. Note that although a part of the gate electrode 148a overlaps with the source electrode 142a and the drain electrode 142b in the structure employed here, the invention disclosed herein is not limited to this structure. It is possible to employ a structure in which an end portion of the gate electrode 148a and an end portion of the source electrode 142a overlap with each other, and an end portion of the gate electrode 148a and an end portion of the drain electrode 142b overlap with each other.

[0102]

The insulating film 150 and the insulating film 152 can be formed by a PVD method, a CVD method, or the like. The insulating film 150 and the insulating film 152 can be formed using a material including an inorganic insulating material such as silicon oxide, silicon oxynitride, silicon nitride, hafnium oxide, aluminum oxide, or gallium oxide.

[0103]

Note that the insulating film 150 and the insulating film 152 are preferably formed using a low dielectric constant material or to have a structure with low dielectric constant (e.g., a porous structure). When the dielectric constant of the insulating film 150 and the insulating film 152 is reduced, the capacitance generated between wirings or electrodes can be reduced, which results in higher speed operation.

[0104]

Note that, although a stacked structure of the insulating film 150 and the insulating film 152 is employed in this embodiment, one embodiment of the invention disclosed herein is not limited thereto. A single-layer structure or a stacked structure including three or more layers can also be used. Alternatively, the insulating film may be omitted.

[0105]

Note that the insulating film 152 is preferably formed so as to have a flat surface. By forming the insulating film 152 having a flat surface, an electrode, a wiring, or the like can be favorably formed over the insulating film 152 even in the case where the semiconductor device is miniaturized, for example. The insulating film 152 can be planarized by a method such as a chemical mechanical polishing (CMP) process.

[0106]

Through the above-described process, the transistor 162 including the purified oxide semiconductor film 144 is completed (see FIG. 2G).

[0107]

Note that after the above-described process, a variety of wirings, electrodes, or the like may be formed. The wirings or the electrodes can be formed by a so-called damascene method or dual damascene method in which a conductive film is formed and processed, or the like.

[0108]

By etching the insulating film 143 with the use of the mask 141b that is obtained by the slimming process in the above-described manner, the insulating film 143a having a dimension less than or equal to the resolution limit of lithography can be formed. Then, the conductive film 142 is formed so as to cover the insulating film 143a, and the conductive film 142 is subjected to the polishing process, whereby the distance between the upper end portion of the source electrode 142a and the upper end portion of the drain electrode 142b, which determines the channel length of the transistor, can be set short. In this manner, the channel length L of the transistor can be less than 2 μm, for example greater than or equal to 50 nm and less than or equal to 350 nm, and preferably greater than or equal to 100 nm and less than or equal to 150 nm, which enables miniaturization of the transistor. Therefore, a semiconductor device which operates at high speed and consumes low power can be realized. By the polishing process performed on the conductive film 142, the surfaces of the insulating film 143a and the source and drain electrodes 142a and 142b can be planarized.

[0109]

In addition, the channel formation region of the transistor 162 is provided over a highly flat region whose root-mean-square (RMS) roughness is 1 nm or less (preferably 0.5 nm or less); therefore, a problem such as a short channel effect can be prevented even under a situation where the channel length of the transistor 162 is short and thus the transistor 162 having favorable characteristics can be provided.

[0110]

The increase in flatness of the surface over which components are formed can make the thickness distribution of the oxide semiconductor film 144 uniform; therefore, characteristics of the transistor 162 can be improved. In addition, a decrease in coverage which may be caused by a large difference in height can be suppressed, and a break due to a step or a defective connection of the oxide semiconductor film 144 can be prevented.

[0111]

When the difference in height between the part of the upper surface of the insulating film 143a and the upper surface of the source electrode 142a or the difference in height between the part of the upper surface of the insulating film 143a and the upper surface of the drain electrode 142b is less than 5 nm as described above, leakage current

can be reduced, and the transistor 162 with favorable characteristics can be provided.

[0112]

In the transistor 162 described in this embodiment, the oxide semiconductor film 144 is purified and thus contains hydrogen at a concentration of 5×10^{19} atoms/cm^3 or less, preferably 5×10^{18} atoms/cm^3 or less, further preferably 5×10^{17} atoms/cm^3 or less. In addition, the density of carries generated due to a donor such as hydrogen in the oxide semiconductor film 144 is, for example, less than 1×10^{12} /cm^3, preferably less than 1.45×10^{10} /cm^3, which is sufficiently lower than the carrier density of a general silicon wafer (approximately 1×10^{14} /cm^3). In addition, the off-state current of the transistor 162 is sufficiently small. For example, the off-state current (per unit channel width (1 μm), here) of the transistor 162 at room temperature (25 °C) is 100 zA (1 zA (zeptoampere) is 1×10^{-21} A) or less, preferably 10 zA or less. When the above structure is employed, the off-state current of the transistor can be larger than or equal to 1×10^{-30} A/μm and smaller than or equal to 10^{-21} A/μm. In this manner, by using the oxide semiconductor film 144 which is purified to be intrinsic, it becomes easy to sufficiently reduce the off-state current of the transistor.

[0113]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0114]

(Embodiment 2)

In this embodiment, a structure and a manufacturing method of a semiconductor device according to another embodiment of the invention disclosed herein will be described with reference to FIGS. 3A to 3C, FIGS. 4A to 4D, and FIGS. 5A to 5C.

[0115]

<Example of Structure of Semiconductor Device>

FIGS. 3A to 3C illustrate an example of a structure of a semiconductor device. FIG. 3A is a cross-sectional view of the semiconductor device; FIG. 3B is a plan view of the semiconductor device; and FIG. 3C illustrates a circuit configuration of the

semiconductor device. Note that a structure of the semiconductor device is mainly described in this embodiment, and operation of the semiconductor device will be described in detail in the following embodiment. Note that the semiconductor device illustrated in FIGS. 3A to 3C is just an example of a semiconductor device having a predetermined function and does not exhaustively represent the semiconductor device of the invention disclosed herein. The semiconductor device according to the invention disclosed herein can have another function by changing connection of an electrode or the like as appropriate.

[0116]

FIG. 3A corresponds to a cross-sectional view along line A1-A2 and line B1-B2 in FIG. 3B. The semiconductor device illustrated in FIGS. 3A and 3B includes the transistor 162 described in the above embodiment, a transistor 160 below the transistor 162, and a capacitor 164.

[0117]

Here, a semiconductor material of the transistor 162 and a semiconductor material of the transistor 160 are preferably different materials. For example, the semiconductor material of the transistor 162 may be an oxide semiconductor, and the semiconductor material of the transistor 160 may be a semiconductor material (e.g., silicon) other than an oxide semiconductor. A transistor including an oxide semiconductor can hold charge for a long time owing to its characteristics. On the other hand, a transistor including a material other than an oxide semiconductor can operate at high speed easily.

[0118]

The transistor 160 in FIGS. 3A to 3C includes a channel formation region 116 provided in a substrate 100 including a semiconductor material (e.g., silicon), impurity regions 120 provided so that the channel formation region 116 is sandwiched therebetween, metal compound regions 124 in contact with the impurity regions 120, a gate insulating film 108 provided over the channel formation region 116, and a gate electrode 110 provided over the gate insulating film 108. Note that a transistor whose source electrode and drain electrode are not illustrated in a drawing may also be referred to as a transistor for the sake of convenience. Further, in such a case, in description of a connection of such a transistor, a source electrode and a drain electrode of the

transistor may be described in this specification.

[0119]

Further, an element isolation insulating film 106 is formed over the substrate 100 so as to surround the transistor 160, and an insulating film 130 is formed to cover the transistor 160. Note that in order to realize higher integration, the transistor 160 preferably has a structure without a sidewall insulating film as illustrated in FIGS. 3A and 3B. On the other hand, in the case where characteristics of the transistor 160 have priority, a sidewall insulating film may be provided on a side surface of the gate electrode 110, and the impurity regions 120 may include regions having different impurity concentrations.

[0120]

The structure of the transistor 162 in FIGS. 3A to 3C is similar to the structure of the transistor 162 in the above embodiment. Note that in this embodiment, the source electrode 142a (which may be the drain electrode) of the transistor 162 is connected to the gate electrode 110 of the transistor 160.

[0121]

The capacitor 164 in FIGS. 3A to 3C includes the source electrode 142a (which may be the drain electrode), the oxide semiconductor film 144, the gate insulating film 146, and an electrode 148b. In other words, the source electrode 142a functions as one electrode of the capacitor 164, and the electrode 148b functions as the other electrode of the capacitor 164. Note that the electrode 148b is formed in a process similar to that of the gate electrode 148a of the transistor 162.

[0122]

Note that in the capacitor 164 of FIGS. 3A to 3C, the oxide semiconductor film 144 and the gate insulating film 146 are stacked, whereby insulation between the source electrode 142a and the electrode 148b can be sufficiently secured. It is needless to say that the capacitor 164 without including the oxide semiconductor film 144 may be employed in order to secure sufficient capacitance. In addition, in the case where no capacitor is needed, a structure in which the capacitor 164 is not provided is also possible.

[0123]

In this embodiment, the transistor 162 and the capacitor 164 are provided so as

to overlap with the transistor 160. By employing such a planar layout, higher integration can be realized. For example, given that the minimum feature size is F, the area occupied by the semiconductor device can be 15 F^2 to 25 F^2.

[0124]

Note that the structure of a semiconductor device according to the invention disclosed herein is not limited to that illustrated in FIGS. 3A to 3C. Since the technical idea of an embodiment of the invention disclosed herein is to form a stacked structure of an oxide semiconductor and a semiconductor material other than an oxide semiconductor, the details such as a connection relationship of electrodes can be changed as appropriate.

[0125]

<Manufacturing Method of Semiconductor Device>

Next, an example of a manufacturing method of the semiconductor device will be described with reference to FIGS. 4A to 4D and FIGS. 5A to 5C. Note that FIGS. 4A to 4D and FIGS. 5A to 5C correspond to cross-sectional views along line A1-A2 and line B1-B2 of FIG. 3B. A manufacturing method of the transistor 162 is similar to that in the above embodiment; thus, a manufacturing method of the transistor 160 will be mainly described here.

[0126]

First, the substrate 100 including a semiconductor material is prepared (see FIG. 4A). A single crystal semiconductor substrate or a polycrystalline semiconductor substrate of silicon, silicon carbide, or the like, a compound semiconductor substrate of silicon germanium or the like, an SOI substrate, or the like can be used as the substrate 100 including a semiconductor material. Here, an example of the case where a single crystal silicon substrate is used as the substrate 100 including a semiconductor material is described. Note that the term "SOI substrate" generally means a substrate where a silicon semiconductor layer is provided over an insulating surface. In this specification and the like, the term "SOI substrate" also means a substrate where a semiconductor layer including a material other than silicon is provided over an insulating surface. That is, a semiconductor layer included in the "SOI substrate" is not limited to a silicon semiconductor layer. Moreover, the SOI substrate can be a substrate having a structure where a semiconductor layer is provided over an insulating

substrate such as a glass substrate with an insulating film interposed therebetween.

[0127]

It is preferable that a single crystal semiconductor substrate of silicon or the like be particularly used as the substrate 100 including a semiconductor material because the speed of reading operation of the semiconductor device can be increased.

[0128]

Note that an impurity element may be added to a region which later functions as the channel formation region 116 of the transistor 160, in order to control the threshold voltage of the transistor. Here, an impurity element imparting conductivity is added so that the threshold voltage of the transistor 160 becomes positive. When the semiconductor material is silicon, the impurity imparting conductivity may be boron, aluminum, gallium, or the like. Note that it is preferable to perform heat treatment after adding an impurity element, in order to activate the impurity element or reduce defects which may be generated during addition of the impurity element.

[0129]

Next, a protective layer 102 serving as a mask for forming an element isolation insulating film is formed over the substrate 100 (see FIG. 4A). As the protective layer 102, an insulating film including a material such as silicon oxide, silicon nitride, silicon oxynitride, or the like can be used, for example.

[0130]

Next, a part of the substrate 100 in a region not covered with the protective layer 102 (i.e., in an exposed region) is removed by etching using the protective layer 102 as a mask. Thus, a semiconductor region 104 isolated from other semiconductor regions is formed (see FIG. 4B). As the etching, dry etching is preferably performed, but wet etching may be performed. An etching gas or an etchant can be selected as appropriate depending on a material to be etched.

[0131]

Then, an insulating film is formed so as to cover the semiconductor region 104, and the insulating film in a region overlapping with the semiconductor region 104 is selectively removed; thus, the element isolation insulating film 106 is formed (see FIG. 4C). The insulating film is formed using silicon oxide, silicon nitride, silicon oxynitride, or the like. As a method for removing the insulating film, any of an

etching process, a polishing process such as a CMP process, and the like can be employed. Note that the protective layer 102 is removed after the formation of the semiconductor region 104 or after the formation of the element isolation insulating film 106.

[0132]

Next, an insulating film is formed over a surface of the semiconductor region 104, and a layer including a conductive material is formed over the insulating film.

[0133]

The insulating film is processed into a gate insulating film later and can be formed by heat treatment (thermal oxidation treatment, thermal nitridation treatment, or the like) of the surface of the semiconductor region 104, for example. Instead of heat treatment, high-density plasma treatment may be employed. The high-density plasma treatment can be performed using, for example, a mixed gas of any of a rare gas such as helium (He), argon (Ar), krypton (Kr), or xenon (Xe), oxygen, nitrogen oxide, ammonia, nitrogen, hydrogen, and the like. It is needless to say that the insulating film may be formed by a CVD method, a sputtering method, or the like. The insulating film preferably has a single-layer structure or a stacked structure including gallium oxide, silicon oxide, silicon oxynitride, silicon nitride, hafnium oxide, aluminum oxide, tantalum oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate to which nitrogen is added ($HfSi_xO_yN_z$ ($x > 0$, $y > 0$, $z > 0$)), hafnium aluminate to which nitrogen is added ($HfAl_xO_yN_z$ ($x > 0$, $y > 0$, $z > 0$)), or the like. The insulating film can have a thickness of greater than or equal to 1 nm and less than or equal to 100 nm, preferably, greater than or equal to 10 nm and less than or equal to 50 nm, for example.

[0134]

The layer including a conductive material can be formed using a metal material such as aluminum, copper, titanium, tantalum, or tungsten. The layer including a conductive material may be formed using a semiconductor material such as polycrystalline silicon. There is no particular limitation on the formation method of the layer including a conductive material, and a variety of film formation methods such as an evaporation method, a CVD method, a sputtering method, or a spin coating

method can be employed. Note that this embodiment shows an example of the case where the layer including a conductive material is formed using a metal material.

[0135]

After that, the insulating film and the layer including a conductive material are selectively etched; thus, the gate insulating film 108 and the gate electrode 110 are formed (see FIG. 4C).

[0136]

Next, phosphorus (P), arsenic (As), or the like is added to the semiconductor region 104, whereby the channel formation region 116 and the impurity regions 120 are formed (see FIG. 4D). Note that phosphorus or arsenic is added here in order to form an n-channel transistor; an impurity element such as boron (B) or aluminum (Al) may be added in the case of forming a p-channel transistor. Here, the concentration of the impurity added can be set as appropriate; the concentration is preferably set high when a semiconductor element is highly miniaturized.

[0137]

Note that a sidewall insulating film may be formed around the gate electrode 110, and impurity regions to which the impurity element is added at a different concentration may be formed.

[0138]

Next, a metal layer 122 is formed so as to cover the gate electrode 110, the impurity regions 120, and the like (see FIG. 5A). The metal layer 122 can be formed by any of a variety of film formation methods such as a vacuum evaporation method, a sputtering method, and a spin coating method. The metal layer 122 is preferably formed using a metal material which forms a low-resistance metal compound by reacting with the semiconductor material included in the semiconductor region 104. Examples of such a metal material are titanium, tantalum, tungsten, nickel, cobalt, platinum, and the like.

[0139]

Next, heat treatment is performed so that the metal layer 122 reacts with the semiconductor material. Thus, the metal compound regions 124 that are in contact with the impurity regions 120 are formed (see FIG. 5A). Note that when the gate electrode 110 is formed using polycrystalline silicon or the like, a metal compound

region is also formed in a portion of the gate electrode 110 which is in contact with the metal layer 122.

[0140]

As the heat treatment, irradiation with a flash lamp can be employed, for example. Although it is needless to say that another heat treatment method may be used, a method by which heat treatment can be achieved in an extremely short time is preferably used in order to improve the controllability of chemical reaction for formation of the metal compound. Note that the metal compound regions are formed by reaction of the metal material and the semiconductor material and have sufficiently high conductivity. The formation of the metal compound regions can properly reduce the electric resistance and improve element characteristics. Note that the metal layer 122 is removed after the metal compound regions 124 are formed.

[0141]

Next, the insulating film 130 is formed so as to cover the components formed in the above steps (see FIG. 5B). The insulating film 130 can be formed using an inorganic insulating material such as silicon oxide, silicon oxynitride, silicon nitride, or aluminum oxide. It is particularly preferable to use a low dielectric constant (low-k) material for the insulating film 130 because capacitance due to overlap of electrodes or wirings can be sufficiently reduced. Note that a porous insulating film including such a material may be employed as the insulating film 130. The porous insulating film has a lower dielectric constant than an insulating film with high density and thus makes it possible to further reduce capacitance due to electrodes or wirings. Alternatively, the insulating film 130 can be formed using an organic insulating material such as polyimide or acrylic. Note that although a single-layer structure of the insulating film 130 is used in this embodiment, an embodiment of the invention disclosed herein is not limited to this example. A stacked structure including two or more layers may be employed.

[0142]

Through the above-described process, the transistor 160 is formed with the use of the substrate 100 including a semiconductor material (see FIG. 5B). A feature of the transistor 160 is that it can operate at high speed. With the use of that transistor as a transistor for reading, data can be read at high speed.

[0143]

Then, as treatment performed before the transistor 162 and the capacitor 164 are formed, a CMP process is performed on the insulating film 130 so that an upper surface of the gate electrode 110 is exposed (see FIG. 5C). As treatment for exposing the upper surface of the gate electrode 110, an etching process or the like can also be employed instead of the CMP process; in order to improve characteristics of the transistor 162, a surface of the insulating film 130 is preferably made as flat as possible. The CMP process is preferably performed under such conditions that the root-mean-square (RMS) roughness of the surface of the insulating film 130 becomes 1 nm or less (preferably 0.5 nm or less).

[0144]

Note that before or after each of the above steps, a step of forming an electrode, a wiring, a semiconductor film, an insulating film, or the like may be further performed. For example, when the wiring has a multi-layer structure including a stack of insulating films and conductive films, a highly integrated semiconductor device can be realized.

[0145]

Then, the transistor 162 and the capacitor 164 are formed; thus, the semiconductor device is completed.

[0146]

The oxide semiconductor film 144 formed over the insulating film 130 can have a uniform thickness by increasing the flatness of the surface of the insulating film 130 by a CMP process or the like as described above; accordingly, the transistor 162 can have improved characteristics. In addition, a decrease in coverage which may be caused by a large difference in height can be suppressed, and a break due to a step or a defective connection of the oxide semiconductor film 144 can be prevented.

[0147]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0148]

(Embodiment 3)

In this embodiment, an example of application of a semiconductor device

according to one embodiment of the invention disclosed herein will be described with reference to FIGS. 6A, 6B, and 6C. Here, an example of a memory device will be described. Note that in some circuit diagrams, "OS" is written beside a transistor in order to indicate that the transistor includes an oxide semiconductor.

[0149]

In a semiconductor device which can be used as a memory device, which is illustrated in FIG. 6A, a first wiring (1st Line) is electrically connected to a source electrode (or a drain electrode) of a transistor 1000. A second wiring (2nd Line) is electrically connected to a drain electrode (or a source electrode) of the transistor 1000. A third wiring (3rd Line) is electrically connected to a source electrode (or a drain electrode) of a transistor 1010. A fourth wiring (4th Line) is electrically connected to a gate electrode of the transistor 1010. Furthermore, a gate electrode of the transistor 1000 and the drain electrode (or the source electrode) of the transistor 1010 are electrically connected to one electrode of a capacitor 1020. A fifth wiring (5th Line) is electrically connected to the other electrode of the capacitor 1020.

[0150]

Here, a transistor including an oxide semiconductor is used as the transistor 1010. Here, the transistor described in the above embodiment can be used as the transistor including an oxide semiconductor. A transistor including an oxide semiconductor has a characteristic of a significantly small off-state current. For that reason, a potential of the gate electrode of the transistor 1000 can be held for an extremely long period by turning off the transistor 1010. Furthermore, with the use of the transistor described in the above embodiment, a short channel effect of the transistor 1010 can be suppressed, and a decrease in channel length can be achieved. By providing the capacitor 1020, holding of charge applied to the gate electrode of the transistor 1000 and reading of the held data can be performed more easily. Here, the capacitor described in the above embodiment can be used as the capacitor 1020, for example.

[0151]

In addition, a transistor including a semiconductor material other than an oxide semiconductor is used as the transistor 1000. As the semiconductor material other than an oxide semiconductor, for example, silicon, germanium, silicon germanium,

silicon carbide, gallium arsenide, or the like can be used, and a single crystal semiconductor is preferably used. Alternatively, an organic semiconductor material or the like may be used. A transistor including such a semiconductor material can operate at high speed easily. Here, the transistor described in the above embodiment can be used as the transistor including a semiconductor material other than an oxide semiconductor, for example.

[0152]

Alternatively, a structure in which the capacitor 1020 is not provided is also possible as illustrated in FIG. 6B.

[0153]

The semiconductor device in FIG. 6A utilizes an advantage that the potential of the gate electrode of the transistor 1000 can be held, and can thus write, hold, and read data as follows.

[0154]

First of all, writing and holding of data will be described. First, the potential of the fourth wiring is set to a potential at which the transistor 1010 is on, so that the transistor 1010 is turned on. Accordingly, the potential of the third wiring is supplied to the gate electrode of the transistor 1000 and the capacitor 1020. That is, predetermined charge is supplied to the gate electrode of the transistor 1000 (writing). Here, one of two charges supplying different potentials (hereinafter, a charge supplying a low potential is referred to as charge Q_L and a charge supplying a high potential is referred to as charge Q_H) is given. Note that charges supplying three or more different potentials may be applied in order to improve storage capacity. After that, the potential of the fourth wiring is set to a potential at which the transistor 1010 is off, so that the transistor 1010 is turned off. Thus, the charge supplied to the gate electrode of the transistor 1000 is held (holding).

[0155]

Since the off-state current of the transistor 1010 is significantly small, the charge of the gate electrode of the transistor 1000 is held for a long time.

[0156]

Next, reading of data will be described. By supplying an appropriate potential (reading potential) to the fifth wiring while a predetermined potential (a constant

potential) is supplied to the first wiring, the potential of the second wiring varies depending on the amount of charge held in the gate electrode of the transistor 1000. This is generally because, when the transistor 1000 is an n-channel transistor, an apparent threshold voltage V_{th_H} in the case where Q_H is supplied to the gate electrode of the transistor 1000 is lower than an apparent threshold voltage V_{th_L} in the case where Q_L is supplied to the gate electrode of the transistor 1000. Here, an apparent threshold voltage refers to the potential of the fifth wiring, which is needed to turn on the transistor 1000. Thus, when the potential of the fifth wiring is set to a potential V_0 that is intermediate potential between V_{th_H} and V_{th_L}, charge supplied to the gate electrode of the transistor 1000 can be determined. For example, in the case where Q_H is supplied in writing, when the potential of the fifth wiring is V_0 ($> V_{th_H}$), the transistor 1000 is turned on. In the case where Q_L is supplied in writing, even when the potential of the fifth wiring is V_0 ($< V_{th_L}$), the transistor 1000 remains in an off state. Therefore, the held data can be read by measuring the potential of the second wiring.

[0157]

Note that in the case where memory cells are arrayed to be used, it is necessary to read data only from an intended memory cell. In the case where data of a predetermined memory cell are read and data of the other memory cells are not read, a potential at which the transistor 1000 is off regardless of the state of the gate electrode, that is, a potential lower than V_{th_H} may be supplied to fifth wirings of the memory cells that are not a target for reading. Alternatively, a potential at which the transistor 1000 is on regardless of the state of the gate electrode, that is, a potential higher than V_{th_L} may be supplied to the fifth wirings.

[0158]

Next, rewriting of data will be described. Rewriting of data is performed in a manner similar to that of the writing and holding of data. That is, the potential of the fourth wiring is set to a potential at which the transistor 1010 is on, so that the transistor 1010 is turned on. Accordingly, the potential of the third wiring (a potential for new data) is supplied to the gate electrode of the transistor 1000 and to the capacitor 1020. After that, the potential of the fourth wiring is set to a potential at which the transistor 1010 is off, so that the transistor 1010 is turned off. Accordingly, charge for new data

is supplied to the gate electrode of the transistor 1000.

[0159]

In the semiconductor device according to the invention disclosed herein, data can be directly rewritten by another writing of data as described above. Therefore, extraction of charge from a floating gate with the use of a high voltage which is necessary in a flash memory or the like is not needed, and thus a decrease in operation speed due to erasing operation can be suppressed. In other words, high-speed operation of the semiconductor device can be realized.

[0160]

Note that the drain electrode (or the source electrode) of the transistor 1010 is electrically connected to the gate electrode of the transistor 1000 and therefore has a function similar to that of a floating gate of a floating gate transistor used for a nonvolatile memory element. Therefore, in drawings, a portion where the drain electrode (or the source electrode) of the transistor 1010 is electrically connected to the gate electrode of the transistor 1000 is called a floating gate portion FG in some cases. When the transistor 1010 is off, the floating gate portion FG can be regarded as being embedded in an insulator and thus charge is held in the floating gate portion FG. The off-state current of the transistor 1010 including an oxide semiconductor is smaller than or equal to 1/100000 of the off-state current of a transistor including a silicon semiconductor or the like; thus, loss of the charge accumulated in the floating gate portion FG due to leakage of the transistor 1010 is negligible. That is, with the transistor 1010 including an oxide semiconductor, a nonvolatile memory device which can hold data without being supplied with power can be realized.

[0161]

For example, when the off-state current of the transistor 1010 at room temperature is 10 zA (1 zA (zeptoampere) is 1×10^{-21} A) or less and the capacitance of the capacitor 1020 is approximately 10 fF, data can be held for 10^4 seconds or longer. It is needless to say that the holding time depends on transistor characteristics and capacitance.

[0162]

Further, in that case, the problem of deterioration of a gate insulating film (tunnel insulating film), which has been a problem of a conventional floating gate

transistor, does not exist. That is, the problem of deterioration of a gate insulating film due to injection of electrons into a floating gate, which is a conventional problem, can be solved. This means that there is no limit on the number of writing times in principle. Furthermore, a high voltage needed for writing or erasing in a conventional floating gate transistor is not necessary.

[0163]

Components such as transistors in the semiconductor device in FIG. 6A can be regarded as including resistors and capacitors as illustrated in FIG. 6C. That is, in FIG. 6C, the transistor 1000 and the capacitor 1020 are each regarded as including a resistor and a capacitor. R1 and C1 denote the resistance and the capacitance of the capacitor 1020, respectively. The resistance R1 corresponds to the resistance of the insulating film included in the capacitor 1020. R2 and C2 denote the resistance and the capacitance of the transistor 1000, respectively. The resistance R2 corresponds to the resistance of the gate insulating film at the time when the transistor 1000 is on. The capacitance C2 corresponds to a so-called gate capacitance (capacitance formed between the gate electrode and the source or drain electrode, and capacitance formed between the gate electrode and the channel formation region).

[0164]

The value of resistance (also referred to as effective resistance) between the source electrode and the drain electrode in the case where the transistor 1010 is off is denoted by ROS. When R1 and R2 satisfy the following relations of $R1 \geq ROS$ (R1 is higher than or equal to ROS) and $R2 \geq ROS$ (R2 is higher than or equal to ROS) under the condition that gate leakage of the transistor 1010 is sufficiently small, a period for holding charge (also referred to as a data retention period) is determined mainly by the off-state current of the transistor 1010.

[0165]

On the other hand, when the above relations are not satisfied, it is difficult to secure a sufficient retention period even if the off-state current of the transistor 1010 is sufficiently small. This is because a leakage current other than the off-state current of the transistor 1010 (e.g., a leakage current generated between the source electrode and the gate electrode) is large. Thus, it is preferable that the semiconductor device

disclosed in this embodiment satisfy the above relations.

[0166]

Moreover, C1 and C2 preferably satisfy the relation: C1 ≥ C2 (C1 is larger than or equal to C2). This is because if C1 is large, the potential of the fifth wiring can be supplied to the floating gate portion FG efficiently at the time of controlling the potential of the floating gate portion FG by the fifth wiring, and a difference between potentials (e.g., the reading potential and a non-reading potential) supplied to the fifth wiring can be made small.

[0167]

When the above relation is satisfied, a more favorable semiconductor device can be realized. Note that R1 and R2 are controlled by the gate insulating film of the transistor 1000 and the insulating film of the capacitor 1020. The same can be said to C1 and C2. Therefore, it is preferable that the material, the thickness, and the like of the gate insulating film be set as appropriate to satisfy the above relations.

[0168]

In the semiconductor device of this embodiment, the floating gate portion FG has a function equivalent to that of a floating gate of a floating gate transistor in a flash memory or the like, but the floating gate portion FG of this embodiment has a feature essentially different from that of the floating gate of the flash memory or the like. In a flash memory, since a voltage applied to a control gate is high, it is necessary to keep a proper distance between cells in order to prevent the potential from adversely affecting a floating gate of the adjacent cell. This is one factor inhibiting higher integration of semiconductor devices. The factor is attributed to the following basic principle of a flash memory: a tunneling current is generated by application of a high electric field.

[0169]

Further, because of the above principle of a flash memory, deterioration of an insulating film proceeds and thus another problem of the limit on the number of rewriting times (approximately 10^4 to 10^5 times) arises.

[0170]

The semiconductor device according to the invention disclosed herein is operated by switching of a transistor including an oxide semiconductor and does not use the above-described principle of charge injection by a tunneling current. That is,

unlike a flash memory, a high electric field for injection of charge is not necessary. Accordingly, it is not necessary to consider an influence of a high electric field from a control gate on an adjacent cell, which facilitates high integration.

[0171]

Further, since charge injection by a tunneling current is not used, there is no cause for deterioration of a memory cell. In other words, the semiconductor device according to the invention disclosed herein has higher durability and reliability than a flash memory.

[0172]

In addition, the semiconductor device according to the invention has advantages over a flash memory in that a high electric field is unnecessary and a large peripheral circuit (such as a booster circuit) is unnecessary.

[0173]

In the case where the relative permittivity εr1 of the insulating film included in the capacitor 1020 is different from the relative permittivity εr2 of the gate insulating film included in the transistor 1000, it is easy to satisfy C1 ≥ C2 (C1 is larger than or equal to C2) while 2·S2 ≥ S1 (2·S2 is larger than or equal to S1), or preferably S2 ≥ S1 (S2 is larger than or equal to S1) is satisfied, where S1 is the area of the capacitor 1020 and S2 is the area having the gate capacitance in the transistor 1000. Specifically, for example, a film formed of a high-k material such as hafnium oxide or a stack including a film formed of a high-k material such as hafnium oxide and a film formed of an oxide semiconductor is used for the insulating film included in the capacitor 1020 so that εr1 can be set to 10 or more, preferably 15 or more, and silicon oxide is used for the gate insulating film included in the transistor 1000 so that εr2 can be set to higher than or equal to 3 and lower than or equal to 4.

[0174]

A combination of such structures enables higher integration of the semiconductor device according to the invention disclosed herein.

[0175]

Note that an n-channel transistor in which electrons are majority carriers is used in the above description; it is needless to say that a p-channel transistor in which

holes are majority carriers can be used instead of the n-channel transistor.

[0176]

As described above, the semiconductor device according to an embodiment of the invention disclosed herein has a non-volatile memory cell that includes a writing transistor in which a leakage current between a source and a drain in an off state (an off-state current) is small, a reading transistor including a semiconductor material different from that of the writing transistor, and a capacitor.

[0177]

With a normal silicon semiconductor, it is difficult to decrease the leakage current (the off-state current) to approximately 100 zA (1×10^{-19} A) or less at ambient temperature (e.g., 25 °C), whereas this can be achieved with a transistor including an oxide semiconductor which is processed under an appropriate condition. Therefore, a transistor including an oxide semiconductor is preferably used as the writing transistor.

[0178]

In addition, a transistor including an oxide semiconductor has a small subthreshold swing (S value), so that the switching rate can be sufficiently high even if mobility is comparatively low. Therefore, by using the transistor as the writing transistor, the rise of a writing pulse given to the floating gate portion FG can be very sharp. Further, since the off-state current is small, the amount of charge held in the floating gate portion FG can be reduced. That is, by using a transistor including an oxide semiconductor as the writing transistor, rewriting of data can be performed at high speed.

[0179]

Although there is no limitation on the off-state current of the reading transistor, a transistor that operates at high speed is preferably used as the reading transistor in order to increase the readout speed. For example, a transistor having a switching rate of 1 nanosecond or lower is preferably used as the reading transistor.

[0180]

In this manner, when a transistor including an oxide semiconductor is used as a writing transistor, and a transistor including a semiconductor material other than an oxide semiconductor is used as a reading transistor, a semiconductor device capable of

holding data for a long time and reading data at high speed, which can be used as a memory device, can be obtained.

[0181]

Furthermore, with the use of the transistor described in the above embodiment as a writing transistor, a short channel effect of the writing transistor can be suppressed, and a decrease in channel length can be achieved. Accordingly, a semiconductor device which can be used as a memory device can operate at higher speed.

[0182]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0183]

(Embodiment 4)

In this embodiment, an example of application of a semiconductor device according to one embodiment of the invention disclosed herein will be described with reference to FIGS. 7A and 7B and FIGS. 8A to 8C. Here, an example of a memory device will be described. Note that in some circuit diagrams, "OS" is written beside a transistor in order to indicate that the transistor includes an oxide semiconductor.

[0184]

FIGS. 7A and 7B are circuit diagrams of semiconductor devices, which can be used as memory devices, each including a plurality of semiconductor devices (hereinafter also referred to as memory cells 1050) illustrated in FIG. 6A. FIG. 7A is a circuit diagram of a so-called NAND semiconductor device in which the memory cells 1050 are connected in series, and FIG. 7B is a circuit diagram of a so-called NOR semiconductor device in which the memory cells 1050 are connected in parallel.

[0185]

The semiconductor device in FIG. 7A includes one source line SL, one bit line BL, one first signal line S1, m number of second signal lines S2, m number of word lines WL, and m number of memory cells 1050 (memory cells (1,1) to (m,1)). In FIG. 7A, one source line SL, one bit line BL, and one first signal line S1 are provided in the semiconductor device; however, an embodiment of the invention disclosed herein is not limited to this structure. A plurality of source lines SL, a plurality of bit lines BL, and

a plurality of first signal lines S1 may be provided.

[0186]

In each of the memory cells 1050, the gate electrode of the transistor 1000, the drain electrode (or the source electrode) of the transistor 1010, and one electrode of the capacitor 1020 are electrically connected to one another. The first signal line S1 and the source electrode (or the drain electrode) of the transistor 1010 are electrically connected to each other, and the second signal line S2 and the gate electrode of the transistor 1010 are electrically connected to each other. The word line WL and the other electrode of the capacitor 1020 are electrically connected to each other.

[0187]

Further, the source electrode of the transistor 1000 included in the memory cell 1050 is electrically connected to the drain electrode of the transistor 1000 in the adjacent memory cell 1050. The drain electrode of the transistor 1000 included in the memory cell 1050 is electrically connected to the source electrode of the transistor 1000 in the adjacent memory cell 1050. Note that the drain electrode of the transistor 1000 included in the memory cell 1050 at one end of the *m* number of memory cells connected in series is electrically connected to the bit line BL. The source electrode of the transistor 1000 included in the memory cell 1050 at the other end of the *m* number of memory cells connected in series is electrically connected to the source line SL.

[0188]

In the semiconductor device in FIG. 7A, writing operation and reading operation are performed for each row. The writing operation is performed as follows. A potential at which the transistor 1010 is on is supplied to the second signal line S2 of a row where writing is to be performed, so that the transistor 1010 of the row where writing is to be performed is turned on. Accordingly, a potential of the first signal line S1 is supplied to the gate electrode of the transistor 1000 of the specified row, so that predetermined charge is given to the gate electrode. Thus, data can be written to the memory cell of the specified row.

[0189]

Further, the reading operation is performed as follows. First, a potential at which the transistor 1000 is on regardless of charge of the gate electrode of the transistor 1000 is supplied to the word lines WL of the rows other than the row where

reading is to be performed, so that the transistors 1000 of the rows other than the row where reading is to be performed are turned on. Then, a potential (reading potential) at which an on state or an off state of the transistor 1000 is determined depending on charge of the gate electrode of the transistor 1000 is supplied to the word line WL of the row where reading is to be performed. After that, a constant potential is supplied to the source line SL so that a reading circuit (not illustrated) connected to the bit line BL is operated. Here, the plurality of transistors 1000 between the source line SL and the bit line BL are turned on except the transistor 1000 of the row where reading is to be performed; therefore, conductance between the source line SL and the bit line BL is determined by the state of the transistor 1000 (whether on or off) of the row where reading is to be performed. Since the conductance of the transistor varies depending on the charge in the gate electrode of the transistor 1000 of the row where reading is to be performed, a potential of the bit line BL also varies accordingly. By reading the potential of the bit line BL with the reading circuit, data can be read from the memory cell of the specified row.

[0190]

The semiconductor device in FIG. 7B includes n number of source lines SL, n number of bit lines BL, n number of first signal lines S1, m number of second signal lines S2, m number of word lines WL, and $m \times n$ memory cells 1050 (memory cells (1,1) to (m,n)). A gate electrode of the transistor 1000, the drain electrode (or the source electrode) of the transistor 1010, and one electrode of the capacitor 1020 are electrically connected to one another. The source line SL and the source electrode of the transistor 1000 are electrically connected to each other. The bit line BL and the drain electrode of the transistor 1000 are electrically connected to each other. The first signal line S1 and the source electrode (or the drain electrode) of the transistor 1010 are electrically connected to each other, and the second signal line S2 and the gate electrode of the transistor 1010 are electrically connected to each other. The word line WL and the other electrode of the capacitor 1020 are electrically connected to each other.

[0191]

In the semiconductor device in FIG. 7B, writing operation and reading operation are performed per row. The writing operation is performed in a manner similar to that of the semiconductor device in FIG. 7A. The reading operation is

performed as follows. First, a potential at which the transistor 1000 is off regardless of charge of the gate electrode of the transistor 1000 is supplied to the word lines WL of the rows other than the row where reading is to be performed, so that the transistors 1000 of the rows other than the row where reading is to be performed are turned off. Then, a potential (reading potential) at which an on state or an off state of the transistor 1000 is determined depending on charge of the gate electrode of the transistor 1000 is supplied to the word line WL of the row where reading is to be performed. After that, a constant potential is supplied to the source line SL so that a reading circuit (not illustrated) connected to the bit line BL is operated. Here, conductance between the source line SL and the bit line BL is determined by the state of the transistor 1000 (whether on or off) of the row where reading is to be performed. That is, a potential of the bit line BL depends on charge of the gate electrode of the transistor 1000 of the row where reading is to be performed. By reading the potential of the bit line BL with the reading circuit, data can be read from the memory cell of the specified row.

[0192]

Although the amount of data which can be stored in each of the memory cells 1050 is one bit in the above description, the structure of the semiconductor device of this embodiment is not limited to this example. The amount of data which is held in each of the memory cells 1050 may be increased by preparing three or more kinds of potentials to be supplied to the gate electrode of the transistor 1000. For example, in the case where four kinds of potentials are supplied to the gate electrode of the transistor 1000, data of two bits can be held in each of the memory cells.

[0193]

Next, an example of a reading circuit which can be used for the semiconductor devices illustrated in FIGS. 7A and 7B and the like will be described with reference to FIGS. 8A to 8C.

[0194]

FIG. 8A illustrates an outline of the reading circuit. The reading circuit includes a transistor and a sense amplifier circuit.

[0195]

At the time of reading data, a terminal A is connected to a bit line BL to which a memory cell from which data is to be read is connected. Further, a potential Vbias is

applied to a gate electrode of the transistor so that a potential of the terminal A is controlled.

[0196]

The resistance of the memory cell 1050 varies depending on stored data. Specifically, when the transistor 1000 of the selected memory cell 1050 is on, the memory cell 1050 has a low resistance, whereas when the transistor 1000 of the selected memory cell 1050 is off, the memory cell 1050 has a high resistance.

[0197]

When the memory cell has a high resistance, the potential of the terminal A is higher than a reference potential Vref and the sense amplifier circuit outputs a potential corresponding to the potential of the terminal A. On the other hand, when the memory cell has a low resistance, the potential of the terminal A is lower than the reference potential Vref and the sense amplifier circuit outputs a potential corresponding to the potential of the terminal A.

[0198]

In this manner, by using the reading circuit, data can be read from the memory cell. Note that the reading circuit of this embodiment is one example. Another circuit may be used. The reading circuit may further include a precharge circuit. Instead of the reference potential Vref, a reference bit line may be connected to the sense amplifier circuit.

[0199]

FIG. 8B illustrates a differential sense amplifier which is an example of sense amplifier circuits. The differential sense amplifier has input terminals Vin(+) and Vin(−) and an output terminal Vout, and amplifies a difference between Vin(+) and Vin(−). If Vin(+) > Vin(−), the output from Vout is relatively high, whereas if Vin(+) < Vin(−), the output from Vout is relatively low. In the case where the differential sense amplifier is used for the reading circuit, one of Vin(+) and Vin(−) is connected to the terminal A, and the reference potential Vref is supplied to the other of Vin(+) and Vin(−).

[0200]

FIG. 8C illustrates a latch sense amplifier which is an example of sense

amplifier circuits. The latch sense amplifier has input/output terminals V1 and V2 and input terminals for control signals Sp and Sn. First, the signal Sp is set high and the signal Sn is set low, and a power supply potential (Vdd) is interrupted. Then, potentials to be compared are supplied to V1 and V2. After that, the signal Sp is set low and the signal Sn is set high, and the power supply potential (Vdd) is supplied. If the potentials V1in and V2in to be compared satisfy V1in > V2in, the output from V1 is high and the output from V2 is low, whereas if the potentials satisfy V1in < V2in, the output from V1 is low and the output from V2 is high. By utilizing such a relationship, the difference between V1in and V2in can be amplified. In the case where the latch sense amplifier is used for the reading circuit, one of V1 and V2 is connected to the terminal A and an output terminal through a switch, and the reference potential Vref is supplied to the other of V1 and V2.

[0201]

With the use of the transistor described in the above embodiment as a writing transistor of a memory cell in the above-described semiconductor device which can be used as a memory device, a short channel effect of the writing transistor can be suppressed, and a decrease in channel length can be achieved. Accordingly, a semiconductor device which can be used as a memory device can operate at higher speed.

[0202]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0203]

(Embodiment 5)

In this embodiment, an example of application of a semiconductor device according to one embodiment of the invention disclosed herein will be described with reference to FIG. 9. Here, a central processing unit (CPU) will be described.

[0204]

FIG. 9 illustrates an example of a block diagram of a CPU. A CPU 1101 illustrated in FIG. 9 includes a timing control circuit 1102, an instruction decoder 1103,

a register array 1104, an address logic and buffer circuit 1105, a data bus interface 1106, an arithmetic logic unit (ALU) 1107, an instruction register 1108, and the like.

[0205]

These circuits are manufactured using the transistor described in the above embodiment, an inverter circuit, a resistor, a capacitor, and the like. Because the transistor described in the above embodiment can achieve an extremely small off-state current, a reduction in power consumption of the CPU 1101 can be realized. Furthermore, with the use of the transistor described in the above embodiment, a short channel effect of the transistor can be suppressed, and a decrease in channel length can be achieved.

[0206]

Circuits included in the CPU 1101 will be briefly described below. The timing control circuit 1102 receives instructions from the outside, converts the instructions into information for the inside, and transmits the information to another block. In addition, the timing control circuit 1102 gives directions such as reading and writing of memory data to the outside, according to internal operation. The instruction decoder 1103 functions to convert instructions from the outside into instructions for the inside. The register array 1104 functions to temporarily store data. The address logic and buffer circuit 1105 functions to specify the address of an external memory. The data bus interface 1106 functions to take data in and out of an external memory or a device such as a printer. The ALU 1107 functions to perform an operation. The instruction register 1108 functions to temporarily store instructions. The CPU includes such a combination of circuits.

[0207]

With the use of the transistor described in the above embodiment in at least a part of the CPU 1101, a short channel effect of the transistor can be suppressed, and a decrease in channel length can be achieved. Thus, the CPU 1101 can operate at higher speed.

[0208]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0209]

(Embodiment 6)

In this embodiment, an example of application of a semiconductor device according to one embodiment of the invention disclosed herein will be described with reference to FIGS. 10A and 10B. Here, an example of a semiconductor device having an image sensor function for reading information of an object will be described. Note that in some circuit diagrams, "OS" is written beside a transistor in order to indicate that the transistor includes an oxide semiconductor.

[0210]

FIG. 10A illustrates an example of a semiconductor device having an image sensor function. FIG. 10A is an equivalent circuit diagram of a photosensor, and FIG. 10B is a cross-sectional view of a part of the photosensor.

[0211]

One electrode of a photodiode 1202 is electrically connected to a photodiode reset signal line 1212, and the other electrode of the photodiode 1202 is electrically connected to a gate of a transistor 1204. One of a source electrode and a drain electrode of the transistor 1204 is electrically connected to a photosensor reference signal line 1218, and the other of the source electrode and the drain electrode of the transistor 1204 is electrically connected to one of a source electrode and a drain electrode of a transistor 1206. A gate electrode of the transistor 1206 is electrically connected to a gate signal line 1214, and the other of the source electrode and the drain electrode of the transistor 1206 is electrically connected to a photosensor output signal line 1216.

[0212]

Here, transistors including an oxide semiconductor are used as the transistor 1204 and the transistor 1206 illustrated in FIG. 10A. Here, the transistor described in the above embodiment can be used as the transistors including an oxide semiconductor. Because the transistor described in the above embodiment can achieve an extremely small leakage current in an off state, the photodetection accuracy of the photosensor can be improved. Furthermore, with the use of the transistor described in the above embodiment, a short channel effect of the transistor can be suppressed, and a decrease in channel length can be achieved. Thus, the area of the photodiode can be increased,

and the photodetection accuracy of the photosensor can be improved.

[0213]

FIG. 10B is a cross-sectional view illustrating the photodiode 1202 and the transistor 1204 in the photosensor. The photodiode 1202 functioning as a sensor and the transistor 1204 are provided over a substrate 1222 having an insulating surface (a TFT substrate). A substrate 1224 is provided over the photodiode 1202 and the transistor 1204 using an adhesive layer 1228. In addition, an insulating film 1234, an interlayer insulating film 1236, and an interlayer insulating film 1238 are provided over the transistor 1204.

[0214]

In addition, a gate electrode layer 1240 is provided in the same layer as the gate electrode of the transistor 1204 so as to be electrically connected to the gate electrode. The gate electrode layer 1240 is electrically connected to an electrode layer 1242 provided over the interlayer insulating film 1236, at an opening formed in the insulating film 1234 and the interlayer insulating film 1236. Because the photodiode 1202 is formed over the electrode layer 1242, the photodiode 1202 and the transistor 1204 are electrically connected to each other through the gate electrode layer 1240 and the electrode layer 1242.

[0215]

The photodiode 1202 has a structure in which a first semiconductor layer 1226a, a second semiconductor layer 1226b, and a third semiconductor layer 1226c are stacked in this order over the electrode layer 1242. In other words, the first semiconductor layer 1226a of the photodiode 1202 is electrically connected to the electrode layer 1242. In addition, the third semiconductor layer 1226c of the photodiode 1202 is electrically connected to an electrode layer 1244 provided over the interlayer insulating film 1238.

[0216]

Here, a PIN photodiode is given as an example, in which a semiconductor layer having n-type conductivity as the first semiconductor layer 1226a, a high-resistance semiconductor layer (an i-type semiconductor layer) as the second semiconductor layer 1226b, and a semiconductor layer having p-type conductivity as the third semiconductor layer 1226c are stacked.

[0217]

The first semiconductor layer 1226a is an n-type semiconductor layer and is formed from an amorphous silicon film containing an impurity element imparting n-type conductivity. In the formation of the first semiconductor layer 1226a, a plasma CVD method with the use of a semiconductor source gas containing an impurity element belonging to Group 15 (e.g., phosphorus (P)) is employed. As the semiconductor source gas, silane (SiH_4) may be used. Alternatively, disilane (Si_2H_6), dichlorosilane (SiH_2C1_2), trichlorosilane ($SiHCl_3$), silicon tetrachloride ($SiCl_4$), silicon tetrafluoride (SiF_4), or the like may be used. Alternatively, an amorphous silicon film which does not contain an impurity element may be formed, and then, an impurity element may be introduced into the amorphous silicon film by a diffusion method or an ion implantation method. After the impurity element is introduced by an ion implantation method or the like, heating or the like may be conducted in order to diffuse the impurity element. In this case, as a method for forming the amorphous silicon film, an LPCVD method, a vapor deposition method, a sputtering method, or the like may be used. The first semiconductor layer 1226a is preferably formed so as to have a thickness of greater than or equal to 20 nm and less than or equal to 200 nm.

[0218]

The second semiconductor layer 1226b is an i-type semiconductor layer (an intrinsic semiconductor layer) and is formed from an amorphous silicon film. In the formation of the second semiconductor layer 1226b, the amorphous silicon film is formed by a plasma CVD method with use of a semiconductor source gas. As the semiconductor source gas, silane (SiH_4) may be used. Alternatively, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, SiF_4, or the like may be used. The second semiconductor layer 1226b may alternatively be formed by an LPCVD method, a vapor deposition method, a sputtering method, or the like. The second semiconductor layer 1226b is preferably formed so as to have a thickness of greater than or equal to 200 nm and less than or equal to 1000 nm.

[0219]

The third semiconductor layer 1226c is a p-type semiconductor layer and is formed from an amorphous silicon film containing an impurity element imparting p-type conductivity. In the formation of the third semiconductor layer 1226c, a plasma

CVD method with the use of a semiconductor source gas containing an impurity element belonging to Group 13 (e.g., boron (B)) is employed. As the semiconductor source gas, silane (SiH_4) may be used. Alternatively, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, SiF_4, or the like may be used. Alternatively, an amorphous silicon film which does not contain an impurity element may be formed, and then, an impurity element may be introduced into the amorphous silicon film by a diffusion method or an ion implantation method. After the impurity element is introduced by an ion implantation method or the like, heating or the like may be performed in order to diffuse the impurity element. In this case, as a method for forming the amorphous silicon film, an LPCVD method, a vapor deposition method, a sputtering method, or the like may be used. The third semiconductor layer 1226c is preferably formed so as to have a thickness of greater than or equal to 10 nm and less than or equal to 50 nm.

[0220]

The first semiconductor layer 1226a, the second semiconductor layer 1226b, and the third semiconductor layer 1226c are not necessarily formed using an amorphous semiconductor, and they may be formed using a polycrystalline semiconductor or a microcrystalline semiconductor (or a semi-amorphous semiconductor (SAS)).

[0221]

The microcrystalline semiconductor belongs to a metastable state which is an intermediate state between an amorphous state and a single crystal state according to Gibbs free energy. That is, the microcrystalline semiconductor is a semiconductor having a third state which is stable in terms of free energy and has a short range order and lattice distortion. In the microcrystalline semiconductor, columnar or needle-like crystals grow in a normal direction with respect to a surface of a substrate. The Raman spectrum of microcrystalline silicon, which is a typical example of the microcrystalline semiconductor, is shifted to a smaller wavenumber region than 520 cm^{-1} which represents single crystal silicon. That is, the peak of the Raman spectrum of microcrystalline silicon exists between 520 cm^{-1} which represents single crystal silicon and 480 cm^{-1} which represents amorphous silicon. The microcrystalline semiconductor includes at least 1 at.% of hydrogen or halogen to terminate a dangling bond. Moreover, a rare gas element such as helium, argon, krypton, or neon may be included to further promote lattice distortion, so that a favorable microcrystalline

semiconductor film with enhanced stability can be obtained.

[0222]

This microcrystalline semiconductor film can be formed by a high-frequency plasma CVD method with a frequency of several tens to several hundreds of megahertz or a microwave plasma CVD method with a frequency of 1 GHz or more. Typically, the microcrystalline semiconductor film can be formed using a gas obtained by diluting a silicon hydride, such as SiH_4, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, or SiF_4, with hydrogen. Alternatively, the microcrystalline semiconductor film can be formed using a gas including a silicon hydride and hydrogen which is diluted with one or more rare gas elements selected from helium, argon, krypton, and neon. In this case, the flow rate of hydrogen is set 5 times to 200 times, preferably 50 times to 150 times, further preferably 100 times, as high as that of a silicon hydride. Furthermore, a gas including silicon may be mixed with a carbide gas such as methane (CH_4) or ethane (C_2H_6), a germanium gas such as germane (GeH_4) or germanium tetrafluoride (GeF_4), fluorine (F_2), or the like.

[0223]

In addition, the mobility of holes generated by the photoelectric effect is lower than the mobility of electrons. Therefore, a PIN photodiode has better characteristics when a surface on the p-type semiconductor layer side is used as a light-receiving plane. Here, an example where the photodiode 1202 receives incident light 1230 from the substrate 1224 side and converts it into electric signals is described. Further, light from a side on which the semiconductor layer having a conductivity type opposite to that of the semiconductor layer on the light-receiving plane side is disturbance light; therefore, the electrode layer 1242 is preferably formed using a light-blocking conductive film. Note that the n-type semiconductor layer side may alternatively be a light-receiving plane.

[0224]

In addition, when the incident light 1230 enters from the substrate 1224 side, the oxide semiconductor film of the transistor 1204 can be shielded from the incident light 1230 by the gate electrode of the transistor 1204.

[0225]

The insulating film 1234, the interlayer insulating film 1236, and the interlayer

insulating film 1238 can be formed using an insulating material by a method such as a sputtering method, an SOG method, a spin coating method, a dipping method, a spray coating method, or a droplet discharge method (e.g., an ink-jet method, screen printing, or offset printing), or with a tool such as a doctor knife, a roll coater, a curtain coater, or a knife coater, depending on the material.

[0226]

The insulating film 1234 may be a single layer or stacked layers of an inorganic insulating material, using any of oxide insulating films or nitride insulating films such as a gallium oxide layer, a silicon oxide layer, a silicon oxynitride layer, a silicon nitride layer, a silicon nitride oxide layer, an aluminum oxide layer, an aluminum oxynitride layer, an aluminum nitride layer, or an aluminum nitride oxide layer. In addition, a high-quality insulating film which is dense and has high withstand voltage can be formed by a high-density plasma CVD method using microwaves (2.45 GHz), which is preferable.

[0227]

For a reduction of surface roughness, an insulating film functioning as a planarization insulating film is preferably used as the interlayer insulating films 1236 and 1238. For example, the interlayer insulating films 1236 and 1238 can be formed using an organic insulating material having heat resistance such as polyimide, acrylic, benzocyclobutene, polyamide, or epoxy. Other than such organic insulating materials, it is possible to use a single layer or stacked layers of a low dielectric constant material (a low-k material), a siloxane-based resin, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), or the like.

[0228]

The photodiode 1202 can read information of an object by detecting the incident light 1230. Note that a light source such as a backlight can be used at the time of reading information of an object.

[0229]

In the photosensor described above, the transistor described in the above embodiment can be used as the transistor including an oxide semiconductor. Because the transistor described in the above embodiment can achieve an extremely small leakage current in an off state, the photodetection accuracy of the photosensor can be

improved. Furthermore, with the use of the transistor described in the above embodiment, a short channel effect of the transistor can be suppressed, and a decrease in channel length can be achieved. Thus, the area of the photodiode can be increased, and the photodetection accuracy of the photosensor can be improved.

[0230]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0231]

(Embodiment 7)

In this embodiment, the cases where any of the semiconductor devices described in the above embodiments is applied to electronic devices will be described with reference to FIGS. 11A to 11F. The cases where any of the above-described semiconductor devices is applied to electronic devices such as a computer, a mobile phone set (also referred to as a mobile phone or a mobile phone device), a portable information terminal (including a portable game machine, an audio reproducing device, and the like), a digital camera, a digital video camera, electronic paper, a television set (also referred to as a television or a television receiver), and the like will be described in this embodiment.

[0232]

FIG. 11A illustrates a laptop personal computer, which includes a housing 701, a housing 702, a display portion 703, a keyboard 704, and the like. At least one of the housings 701 and 702 is provided with any of the semiconductor devices described in the above embodiments. Thus, a laptop personal computer with sufficiently low power consumption, in which writing and reading of data can be performed at high speed and data can be stored for a long time, can be realized.

[0233]

FIG. 11B illustrates a portable information terminal (PDA). A main body 711 is provided with a display portion 713, an external interface 715, operation buttons 714, and the like. Further, a stylus 712 for operation of the portable information terminal, or the like is provided. The main body 711 is provided with any of the semiconductor devices described in the above embodiments. Thus, a portable information terminal

with sufficiently low power consumption, in which writing and reading of data can be performed at high speed and data can be stored for a long time, can be realized.

[0234]

FIG. 11C illustrates an electronic book reader 720 incorporating electronic paper, which includes two housings, a housing 721 and a housing 723. The housing 721 and the housing 723 include a display portion 725 and a display portion 727, respectively. The housing 721 is connected to the housing 723 by a hinge 737, so that the electronic book reader 720 can be opened and closed using the hinge 737 as an axis. In addition, the housing 721 is provided with a power switch 731, operation keys 733, a speaker 735, and the like. At least one of the housings 721 and 723 is provided with any of the semiconductor devices described in the above embodiments. Thus, an electronic book reader with sufficiently low power consumption, in which writing and reading of data can be performed at high speed and data can be stored for a long time, can be realized.

[0235]

FIG. 11D illustrates a mobile phone set, which includes two housings, a housing 740 and a housing 741. Moreover, the housings 740 and 741 in a state where they are developed as illustrated in FIG. 11D can be slid so that one is lapped over the other. Therefore, the size of the mobile phone set can be reduced, which makes the mobile phone set suitable for being carried around. The housing 741 includes a display panel 742, a speaker 743, a microphone 744, operation keys 745, a pointing device 746, a camera lens 747, an external connection terminal 748, and the like. The housing 740 includes a solar cell 749 for charging the mobile phone set, an external memory slot 750, and the like. An antenna is incorporated in the housing 741. At least one of the housings 740 and 741 is provided with any of the semiconductor devices described in the above embodiments. Thus, a mobile phone set with sufficiently low power consumption, in which writing and reading of data can be performed at high speed and data can be stored for a long time, can be realized.

[0236]

FIG. 11E illustrates a digital camera, which includes a main body 761, a display portion 767, an eyepiece 763, an operation switch 764, a display portion 765, a battery 766, and the like. The main body 761 is provided with any of the semiconductor

devices described in the above embodiments. Thus, a digital camera with sufficiently low power consumption, in which writing and reading of data can be performed at high speed and data can be stored for a long time, can be realized.

[0237]

FIG. 11F illustrates a television set 770, which includes a housing 771, a display portion 773, a stand 775, and the like. The television set 770 can be operated with a switch included in the housing 771 or with a remote controller 780. The housing 771 and the remote controller 780 are provided with any of the semiconductor devices described in the above embodiments. Thus, a television set with sufficiently low power consumption, in which writing and reading of data can be performed at high speed and data can be stored for a long time, can be realized.

[0238]

As described above, the electronic devices described in this embodiment each include any of the semiconductor devices according to the above embodiments. Thus, electronic devices with low power consumption can be realized.

[Example 1]

[0239]

In this example, results of computational verification of characteristics of a semiconductor device according to an embodiment of the invention will be described. Specifically, characteristics of transistors having different channel lengths L were compared. Note that device simulation software "Atlas" (produced by Silvaco Data Systems Inc.) was used for the calculation.

[0240]

FIGS. 12A and 12B illustrate the structures of transistors used for the calculation. A structure A illustrated in FIG. 12A is a structure according to one embodiment of the present invention, and a structure B illustrated in FIG. 12B is a comparative structure.

[0241]

The details of a transistor 562 used for the calculation will be described. The transistor having the structure A illustrated in FIG. 12A includes an insulating film 543a (material: silicon oxide), a source electrode 542a and a drain electrode 542b (material: titanium nitride, thickness: 100 nm), an oxide semiconductor layer 544 (material:

In-Ga-Zn-O-based oxide semiconductor, thickness: 10 nm) in contact with a part of an upper surface of the insulating film 543a, a part of an upper surface of the source electrode 542a, and a part of an upper surface of the drain electrode 542b, a gate insulating film 546 (material: hafnium oxide, thickness: 10 nm) covering the oxide semiconductor layer 544, and a gate electrode 548a (material: tungsten) over the gate insulating film 546.

[0242]

A transistor 662 having the structure B illustrated in FIG. 12B includes a source electrode 642a and a drain electrode 642b (material: titanium nitride, thickness: 100 nm), an oxide semiconductor layer 644 (material: In-Ga-Zn-O-based oxide semiconductor, thickness: 10 nm) over the source electrode 642a and the drain electrode 642b, a gate insulating film 646 (material: hafnium oxide, thickness: 10 nm) covering the oxide semiconductor layer 644, and a gate electrode 648a (material: tungsten) over the gate insulating film 646.

[0243]

In the structure A of FIG. 12A, the source electrode 542a and the drain electrode 542b are in contact with the insulating film 543a; thus, the oxide semiconductor layer 544 has a flat cross-sectional shape. In the structure B of FIG. 12B, the source electrode 642a and the drain electrode 642b are provided over a substrate (not illustrated); thus, the oxide semiconductor layer 644 is provided along the shape of the source electrode 642a and the drain electrode 642b and does not have a flat cross-sectional shape.

[0244]

By changing the channel length L in the above structures (the structure A and the structure B), how the threshold voltage V_{th} and the subthreshold swing (also referred to as the S value) of the transistors move was examined. As the channel length L, seven conditions of 50 nm, 70 nm, 80 nm, 100 nm, 200 nm, 300 nm, and 400 nm were adopted.

[0245]

Further, by changing the thickness of the gate insulating film, how the threshold voltage V_{th} of the transistors moves was examined. As the thickness of the gate insulating film, two conditions of 5 nm and 10 nm were adopted.

[0246]

The voltage V_{ds} between the source electrode and the drain electrode was set to 1 V.

[0247]

Parameters used for the calculation are as follows.

1. In-Ga-Zn-O-based oxide semiconductor (material of the oxide semiconductor layer)

Band gap E_g: 3.15 eV, electron affinity χ: 4.3 eV, relative permittivity: 15, electron mobility: 10 cm^2/Vs

2. Titanium nitride (material of the source electrode and the drain electrode)

Work function ϕ_M: 3.9 eV

3. Hafnium oxide (material of the gate insulating film)

Relative permittivity: 15

4. Tungsten (material of the gate electrode)

Work function ϕ_M: 4.9 eV

[0248]

FIGS. 13A and 13B and FIGS. 14A and 14B show results of calculation. In FIGS. 13A and 13B, the horizontal axis represents the channel length L (nm), and the vertical axis represents the amount of shift ΔV_{th} (V) in the threshold voltage V_{th}. Note that ΔV_{th} is calculated on the basis of the threshold voltage when the channel length L is 400 nm. In FIGS. 14A and 14B, the horizontal axis represents the channel length L (nm), and the vertical axis represents the S value (V/dec). FIG. 13A and FIG. 14A show the calculation results of the structure A, and FIG. 13B and FIG. 14B show the calculation results of the structure B.

[0249]

The results in FIG. 13B show that a negative shift in the threshold voltage V_{th} occurs in the structure B as the channel length L decreases. In addition, the results in FIG. 14B show that the S value increases in the structure B as the channel length L decreases. On the contrary, it can be perceived that a negative shift in the threshold voltage V_{th} is suppressed in the structure A even when the channel length L is decreased. In addition, it can also be perceived that an increase in the S value is suppressed. From the results in FIGS. 13A and 13B and FIGS. 14A and 14B, it can be understood that a

structure according to one embodiment of the present invention can prevent a negative shift in threshold voltage, an increase in S value, and the like which may be caused by the decrease in the channel length of a transistor.

[0250]

FIG. 15 shows current-voltage characteristics of the structure A and the structure B in the case where the channel length L is 50 nm and the gate insulating film is formed of hafnium oxide with a thickness of 10 nm. The horizontal axis represents the gate voltage V_G (V), and the vertical axis represents the drain current I_D (A/μm). In FIG. 15, a thicker line represents the calculation results in the case of the structure A, and a thinner line represents the calculation results in the case of the structure B. Note that the voltage V_{ds} between the source electrode and the drain electrode was set to 1 V. Furthermore, FIG. 16 and FIG. 17 show current density distributions of the structure A and the structure B when V_{gs} is 0 V and V_{ds} is 1 V, and diagrams of the structure A and the structure B.

[0251]

The current density distributions in FIG. 16 and FIG. 17 represent leakage currents at V_{gs} = 0 V. Here, attention is focused on a region where the leakage current is 10^4 A/cm^2. It can be seen that the distribution of leakage current in the structure A is limited to only the back channel side as shown in FIG. 16. On the other hand, it can be seen that the leakage current in the structure B is distributed to the inner side of the channel, as well as the back channel side as shown in FIG. 17, due to the presence of the source electrode and the drain electrode at the side of the channel. It can also be seen that electrons flowing into the channel from the upper side are also involved and thus leakage current is distributed to a wider range than in the structure A. This difference in the way that leakage current flows can be considered to be a cause of a difference in channel length dependence between the structure A and the structure B as shown in FIGS. 13A and 13B and FIGS. 14A and 14B. It can be seen from the results in FIG. 15, FIG. 16, and FIG. 17 that a structure according to one embodiment of the present invention can reduce leakage current.

[0252]

Next, electric characteristics of a transistor including an intrinsic oxide

semiconductor were calculated in more detail and the results will be described. Note that Sentaurus Device (TCAD software produced by Synopsys, Inc.) was used for the calculation. In addition, the Shockley-Read-Hall (SRH) model and the Auger recombination model were used as carrier recombination models.

[0253]

The structure of a transistor used for the calculation is the structure A illustrated in FIG. 12A. The details of the structure of the transistor are the same as the above. The calculation was based on the assumption that the oxide semiconductor was i-type and the donor density N_d was equal to the intrinsic carrier density n_i.

[0254]

In the above-described structure, how the off-state current I_{off} of the transistor moves when the channel length L is changed was also examined. As the channel length L, two conditions of 50 nm and 500 nm were adopted. The voltage V_{ds} between the source electrode 542a and the drain electrode 542b was set to 1 V.

[0255]

Parameters used for the calculation are as follows.

1. In-Ga-Zn-O-based oxide semiconductor (material of the oxide semiconductor layer)

Band gap E_g: 3.15 eV, electron affinity χ: 4.3 eV, relative permittivity: 15, electron mobility: 10 cm^2/Vs

2. Titanium nitride (material of the source electrode and the drain electrode)

Work function ϕ_M: 3.9 eV

3. Hafnium oxide (material of the gate insulating film)

Relative permittivity: 15

4. Tungsten (material of the gate electrode)

Work function ϕ_M: 4.9 eV

[0256]

The results of calculation are shown in FIG. 18. In FIG. 18, the horizontal axis represents the gate voltage V_G (V), and the vertical axis represents the drain current I_D (A/μm). In addition, in FIG. 18, a thicker line represents the calculation results in the case where the channel length L is 500 nm, and a thinner line represents the calculation results in the case where the channel length L is 50 μm.

[0257]

It can be seen from the calculation results in FIG. 18 that current-voltage characteristics in the case where the channel length L is 50 nm are negatively shifted as compared to those in the case where the channel length L is 500 nm. It can also be seen that leakage current is larger at V_{gs} = 0 V, but the off-state current can be reduced by applying a sufficient reverse bias to the gate. Furthermore, it can be seen from the calculation results in FIG. 18 that the lowest off-state current is 10^{-29} to 10^{-30} (A/μm) either when the channel length L is 50 nm or when the channel length L is 500 nm.

[0258]

The above-described results show that a structure according to one embodiment of the present invention can prevent a short channel effect such as a decrease in threshold voltage, an increase in S value, and an increase in leakage current which is caused by a decrease in the channel length of a transistor.

This application is based on Japanese Patent Application serial no. 2010-090283 filed with Japan Patent Office on April 9, 2010, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A manufacturing method of a semiconductor device comprising the steps of:

forming a first insulating film over a substrate;

forming a first mask over the first insulating film;

performing a slimming process on the first mask, so that a second mask is formed;

performing an etching process on the first insulating film by using the second mask, so that a second insulating film is formed;

forming a first conductive film over the second insulating film and the substrate;

performing a polishing process on the first conductive film and the second insulating film, so that a third insulating film, a source electrode, and a drain electrode are formed;

forming an oxide semiconductor film over the third insulating film, the source electrode, and the drain electrode;

forming a gate insulating film over the oxide semiconductor film; and

forming a gate electrode in a region which is over the gate insulating film and overlaps with the third insulating film.

2. The manufacturing method of a semiconductor device according to claim 1, wherein the polishing process is performed so that the third insulating film, the source electrode, and the drain electrode have substantially equal thicknesses.

3. The manufacturing method of a semiconductor device according to claim 1, wherein a difference in height between a part of a surface of the third insulating film and a surface of the source electrode or a difference in height between a part of a surface of the third insulating film and a surface of the drain electrode is less than 5 nm.

4. The manufacturing method of a semiconductor device according to claim 1, wherein the third insulating film has a thickness substantially equal to a thickness of the second insulating film.

5. The manufacturing method of a semiconductor device according to claim 1, wherein the first insulating film is formed on a flat surface having a root-mean-square roughness of less than or equal to 1 nm.

6. The manufacturing method of a semiconductor device according to claim 1, wherein the slimming process is performed using an ashing process using an oxygen radical.

7. The manufacturing method of a semiconductor device according to claim 1, wherein the polishing process is performed using chemical mechanical polishing.

8. The manufacturing method of a semiconductor device according to claim 1, wherein the first insulating film is formed by sputtering.

9. A manufacturing method of a semiconductor device comprising the steps of:

forming a first transistor including a channel formation region, a first gate electrode over the channel formation region with a first gate insulating film located between the channel formation region and the first gate electrode, and a first source electrode and a first drain electrode which are electrically connected to the channel formation region;

forming an interlayer insulating film over the first transistor;

forming a first insulating film over the interlayer insulating film;

forming a first mask over the first insulating film;

performing a slimming process on the first mask, so that a second mask is formed;

performing an etching process on the first insulating film by using the second mask, so that a second insulating film is formed;

forming a first conductive film over the second insulating film and the interlayer insulating film;

performing a polishing process on the first conductive film and the second insulating film, so that a third insulating film, a second source electrode, and a second drain electrode are formed;

forming an oxide semiconductor film over the third insulating film, the second source electrode, and the second drain electrode;

forming a second gate insulating film over the oxide semiconductor film; and

forming a second gate electrode in a region which is over the second gate insulating film and overlaps with the third insulating film.

10. The manufacturing method of a semiconductor device according to claim 9, wherein the polishing process is performed so that the third insulating film, the second source electrode, and the second drain electrode have substantially equal thicknesses.

11. The manufacturing method of a semiconductor device according to claim 9, wherein a difference in height between a part of a surface of the third insulating film and a surface of the second source electrode or a difference in height between a part of a surface of the third insulating film and a surface of the second drain electrode is less than 5 nm.

12. The manufacturing method of a semiconductor device according to claim 9, wherein the third insulating film has a thickness substantially equal to a thickness of the second insulating film.

13. The manufacturing method of a semiconductor device according to claim 9, wherein the interlayer insulating film has a flat surface having a root-mean-square roughness of less than or equal to 1 nm.

14. The manufacturing method of a semiconductor device according to claim 9, wherein the slimming process is performed using an ashing process using an oxygen radical.

15. The manufacturing method of a semiconductor device according to claim 9, wherein the polishing process is performed using chemical mechanical polishing.

16. The manufacturing method of a semiconductor device according to claim 9,

wherein the first insulating film is formed by sputtering.

17. A manufacturing method of a semiconductor device comprising the steps of:

forming a first gate electrode of a first transistor;

forming a first insulating film over the first gate electrode;

performing a first polishing process on the first insulating film;

forming a second insulating film over the first insulating film and the first gate electrode

forming a first mask over the second insulating film;

performing a slimming process on the first mask, so that a second mask is formed;

performing an etching process on the second insulating film by using the second mask, so that a third insulating film is formed;

forming a first conductive film over the third insulating film and the first insulating film;

performing a second polishing process on the first conductive film and the third insulating film, so that an electrode electrically connected to the first gate electrode and a fourth insulating film are formed;

forming an oxide semiconductor film over and in contact with the electrode and the fourth insulating film;

forming a second gate insulating film over the oxide semiconductor film; and

forming a second gate electrode in a region which is over the second gate insulating film and overlaps with the fourth insulating film.

18. The manufacturing method of a semiconductor device according to claim 17, wherein the second polishing process is performed so that the fourth insulating film and the electrode have substantially equal thicknesses.

19. The manufacturing method of a semiconductor device according to claim 17, wherein a difference in height between a part of a surface of the fourth insulating film and a surface of the electrode is less than 5 nm.

20. The manufacturing method of a semiconductor device according to claim 17, wherein the fourth insulating film has a thickness substantially equal to a thickness of the third insulating film.

21. The manufacturing method of a semiconductor device according to claim 17, wherein the second insulating film has a flat surface having a root-mean-square roughness of less than or equal to 1 nm.

22. The manufacturing method of a semiconductor device according to claim 17, wherein the slimming process is performed using an ashing process using an oxygen radical.

23. The manufacturing method of a semiconductor device according to claim 17, wherein the second polishing process is performed using chemical mechanical polishing.

24. The manufacturing method of a semiconductor device according to claim 17, wherein the second insulating film is formed by sputtering.

FIG. 1

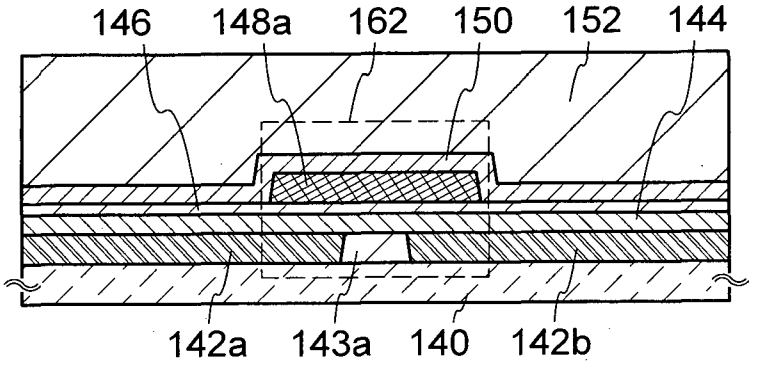


FIG. 2A

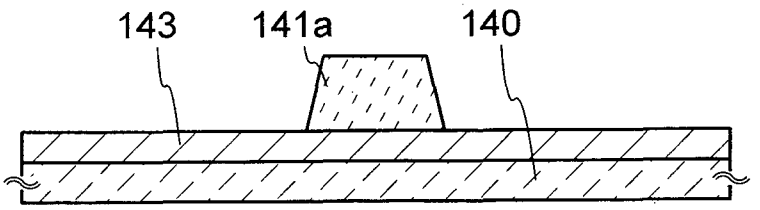


FIG. 2B

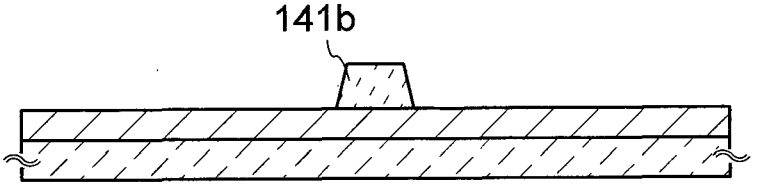


FIG. 2C

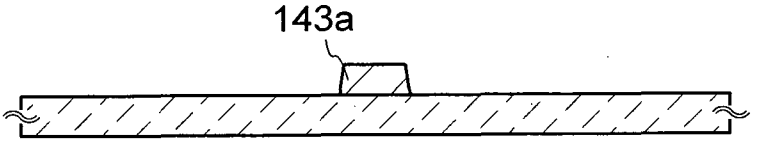


FIG. 2D

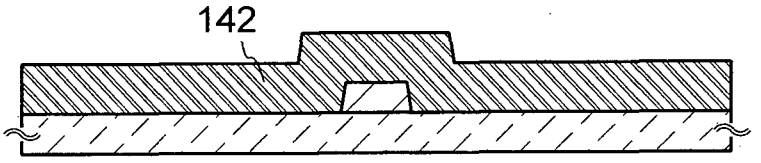


FIG. 2E

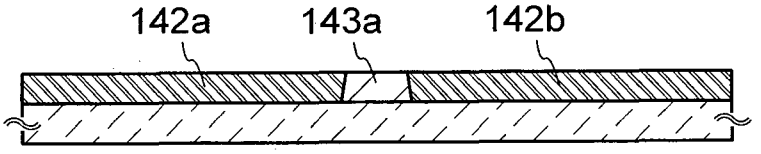


FIG. 2F

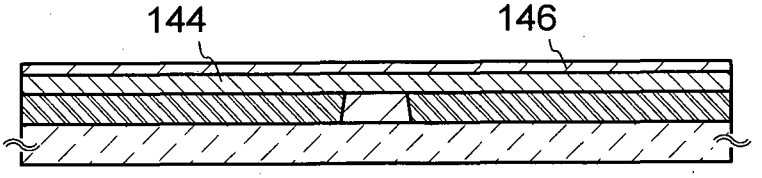


FIG. 2G

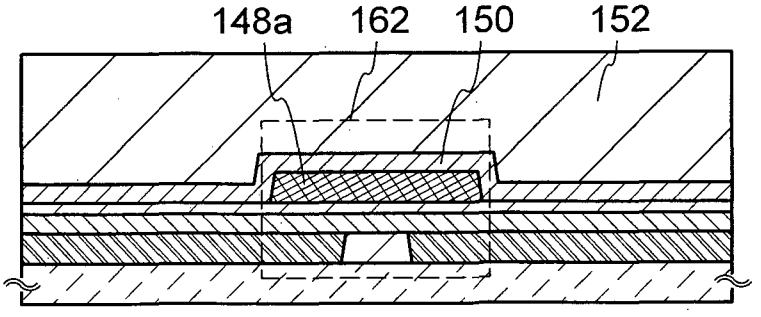


FIG. 3A

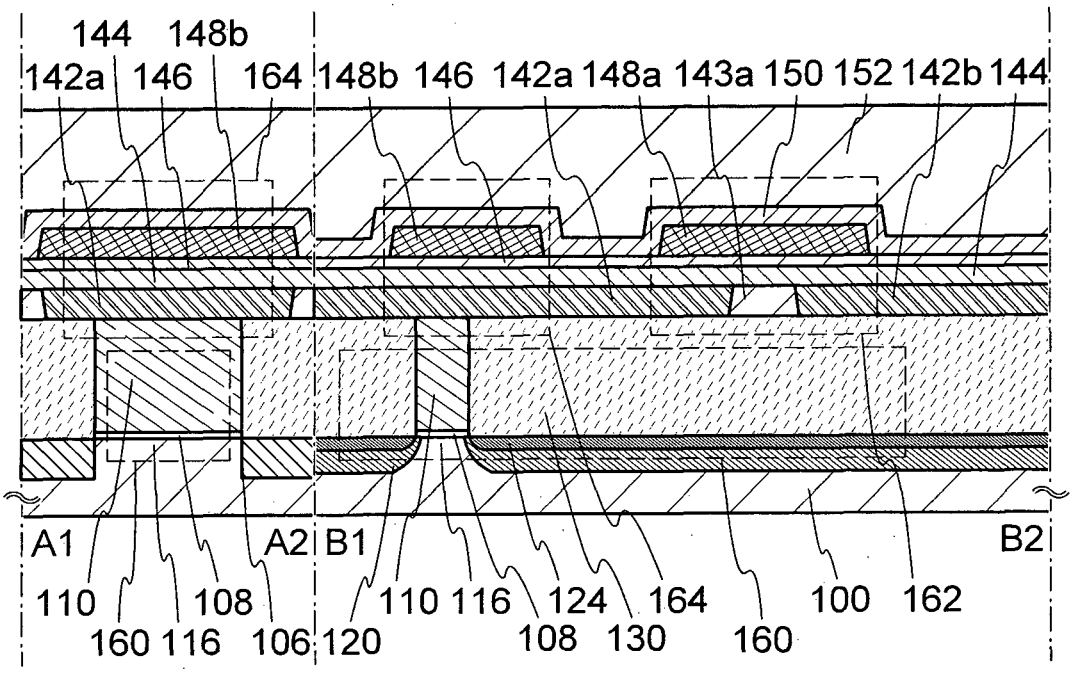


FIG. 3B

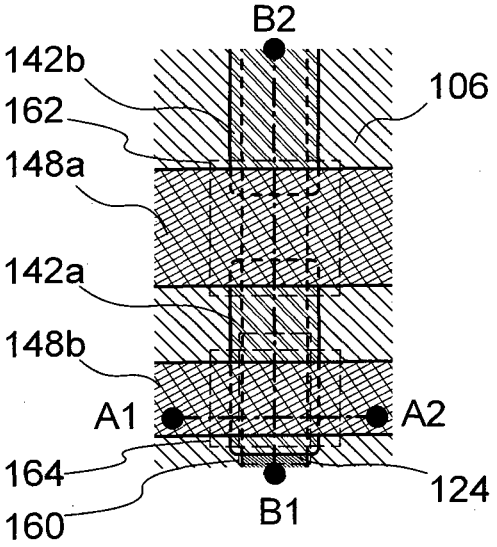


FIG. 3C

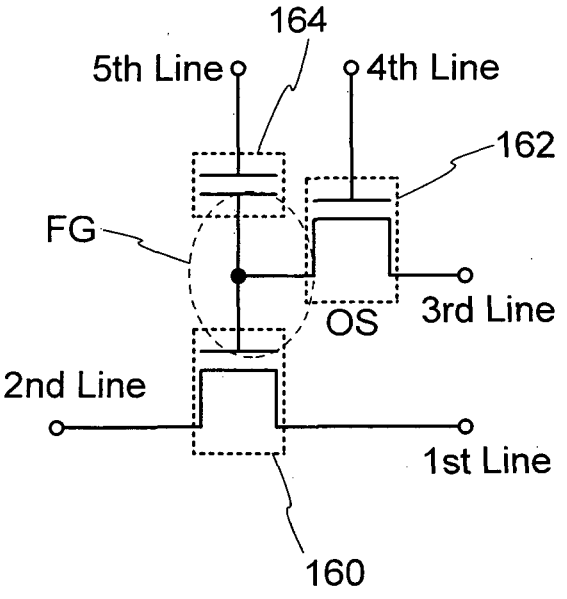


FIG. 4A

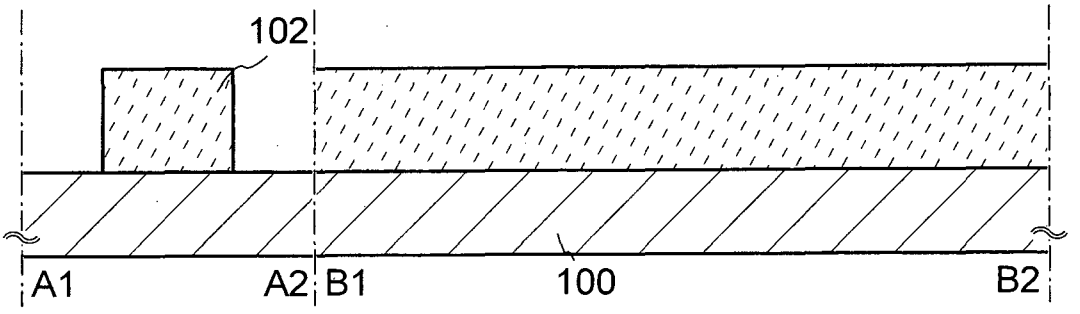


FIG. 4B

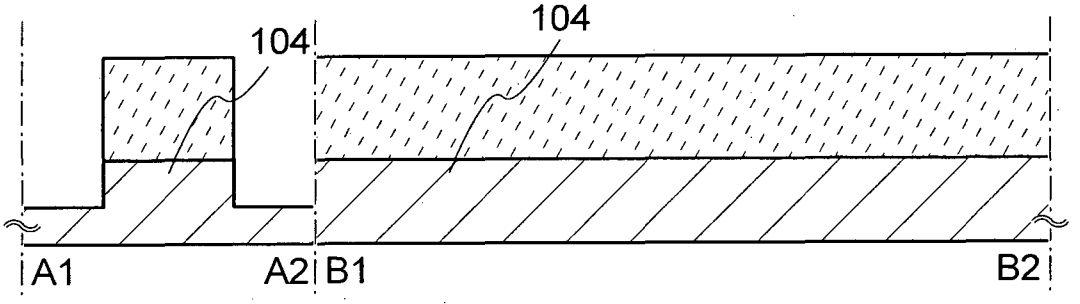


FIG. 4C

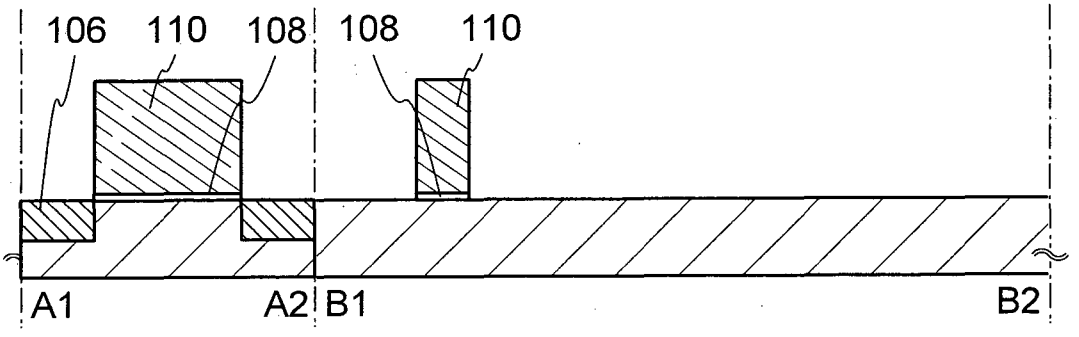


FIG. 4D

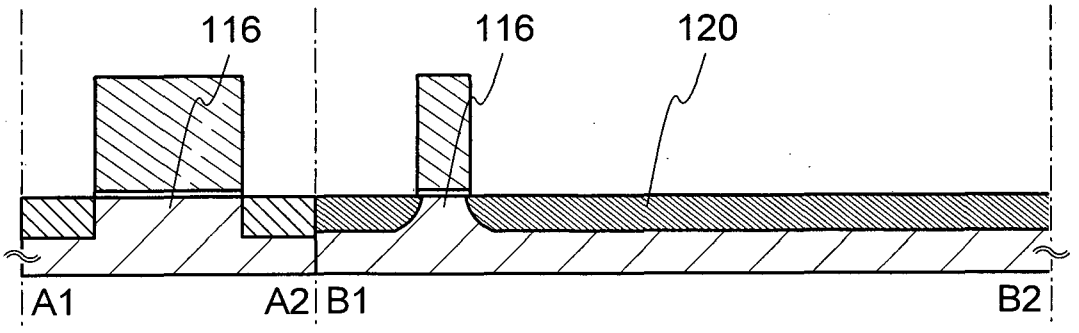


FIG. 5A

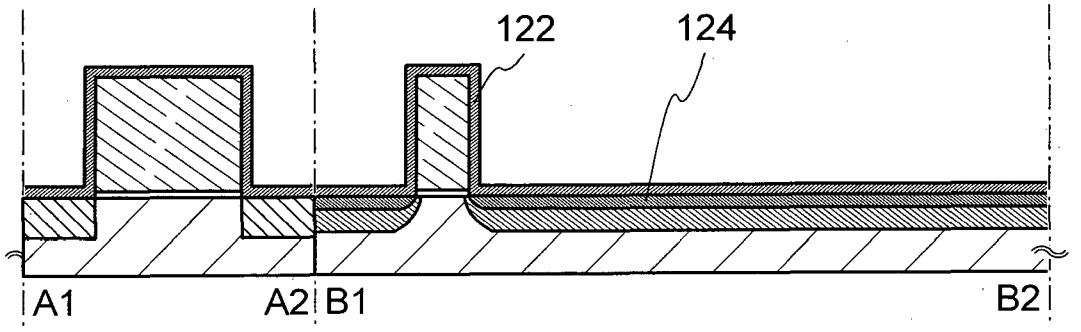


FIG. 5B

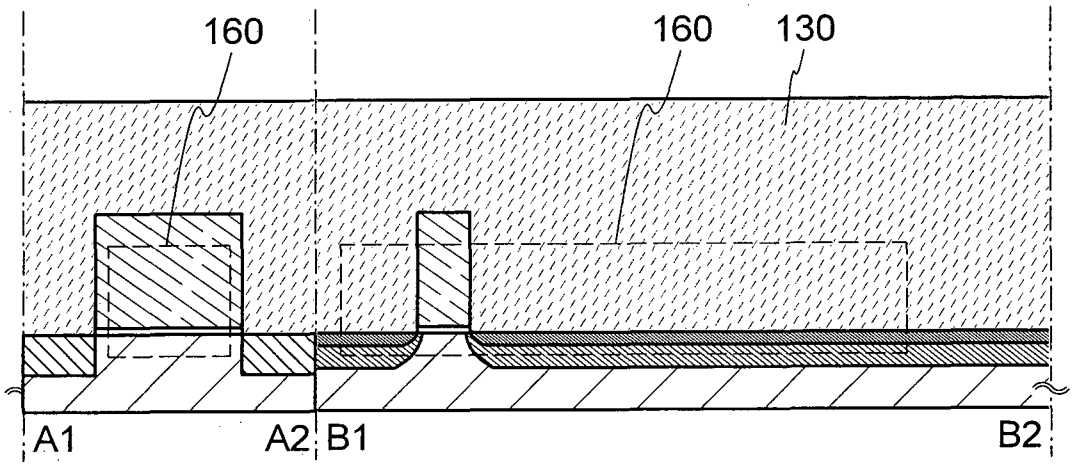


FIG. 5C

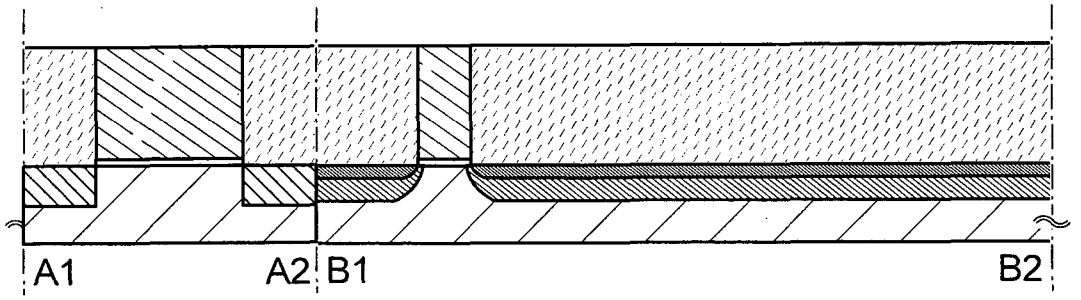


FIG. 6A

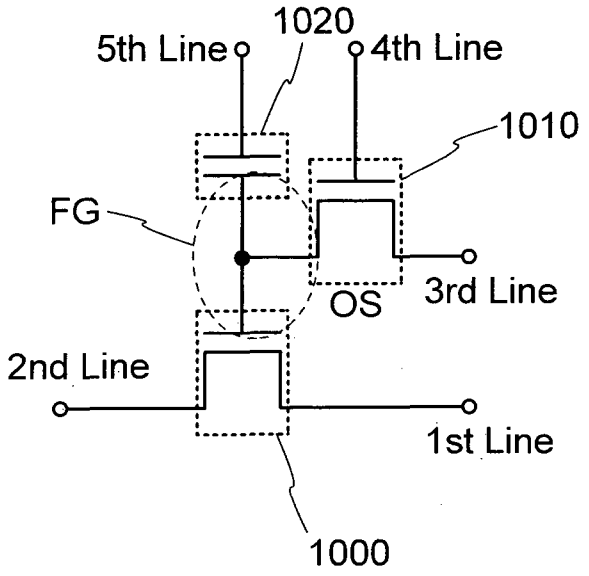


FIG. 6B

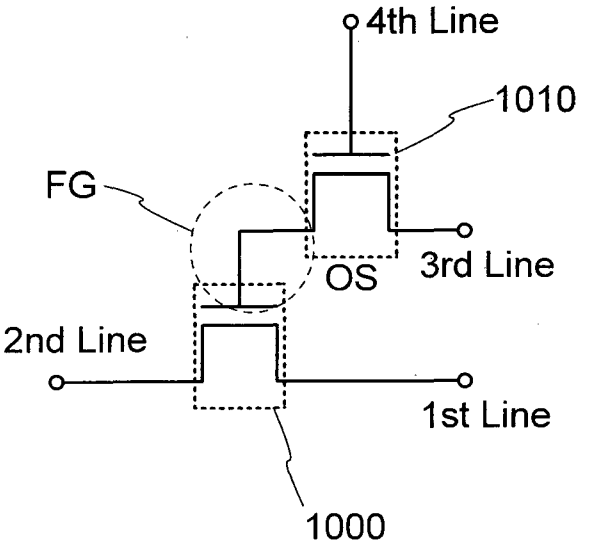


FIG. 6C

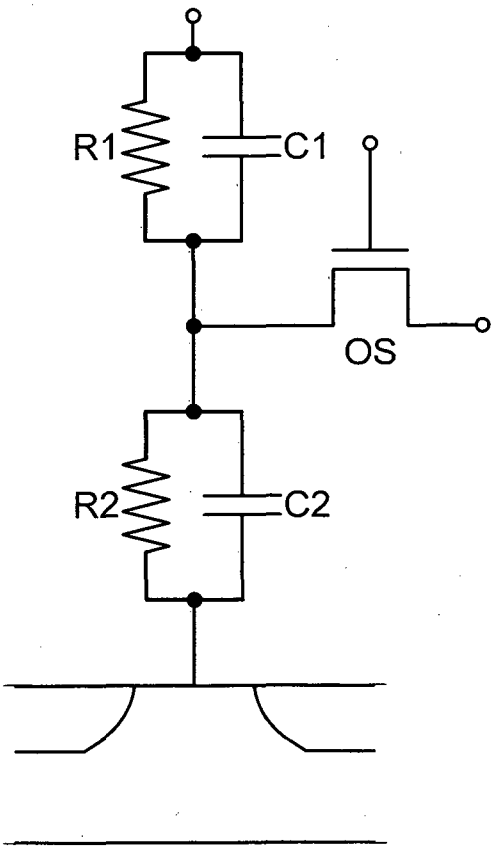


FIG. 7A

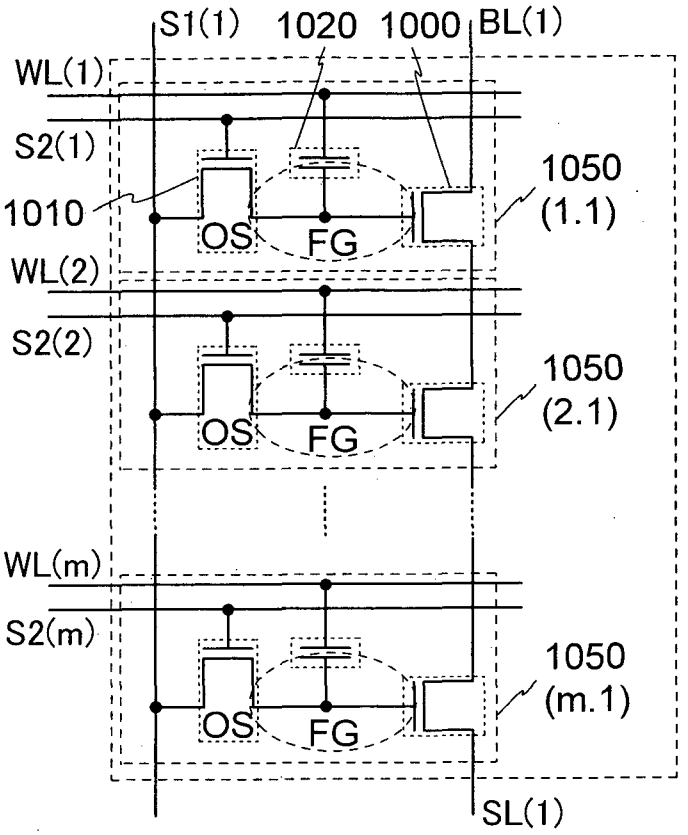

S1(1)
1020
1000
BL(1)
WL(1)
S2(1)
1010
OS
FG
1050
(1.1)
WL(2)
S2(2)
1050
(2.1)
WL(m)
S2(m)
1050
(m.1)
SL(1)

FIG. 7B

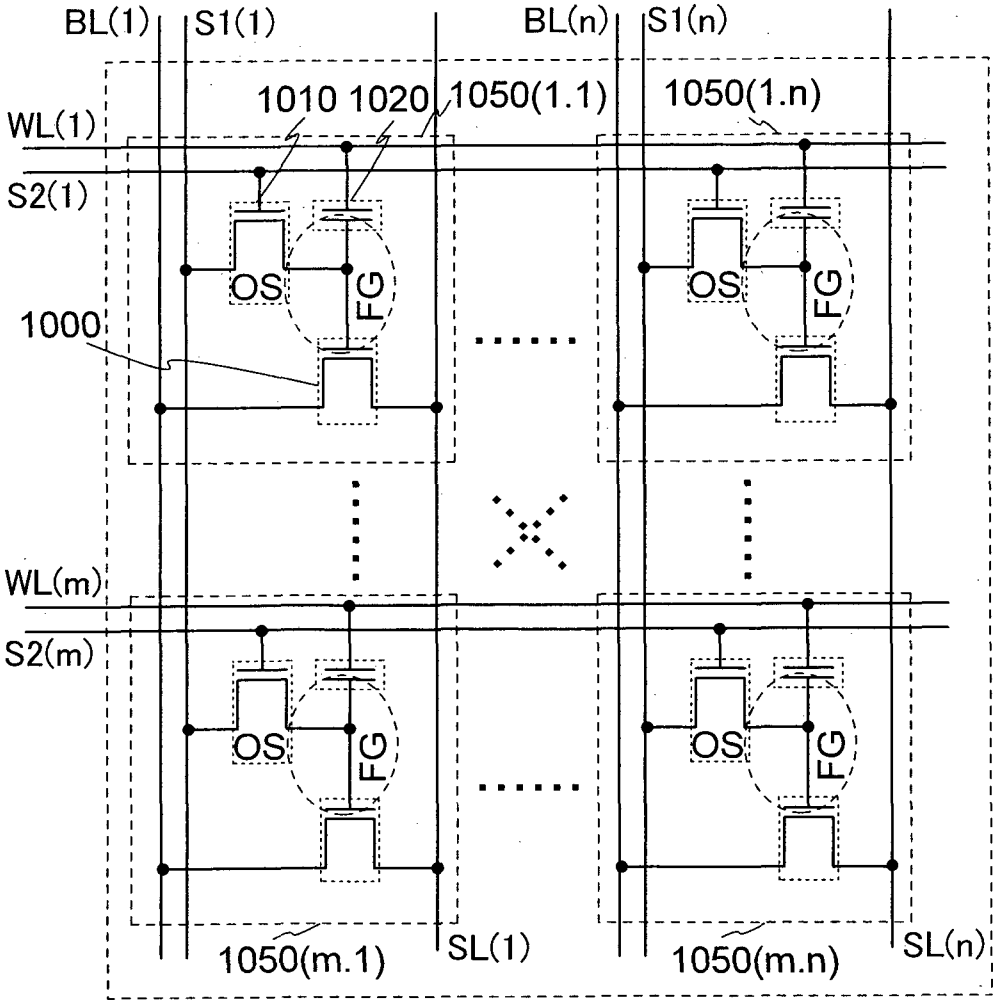

BL(1)
S1(1)
BL(n)
S1(n)
1010
1020
1050(1.1)
1050(1.n)
WL(1)
S2(1)
OS
FG
1000
WL(m)
S2(m)
1050(m.1)
SL(1)
1050(m.n)
SL(n)

FIG. 8A

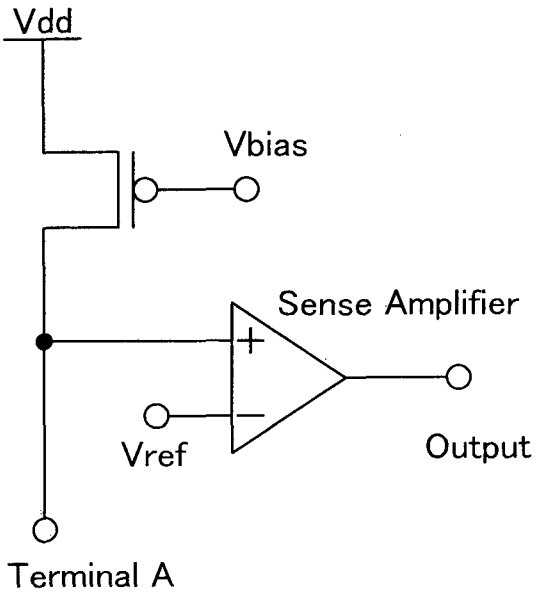


FIG. 8B

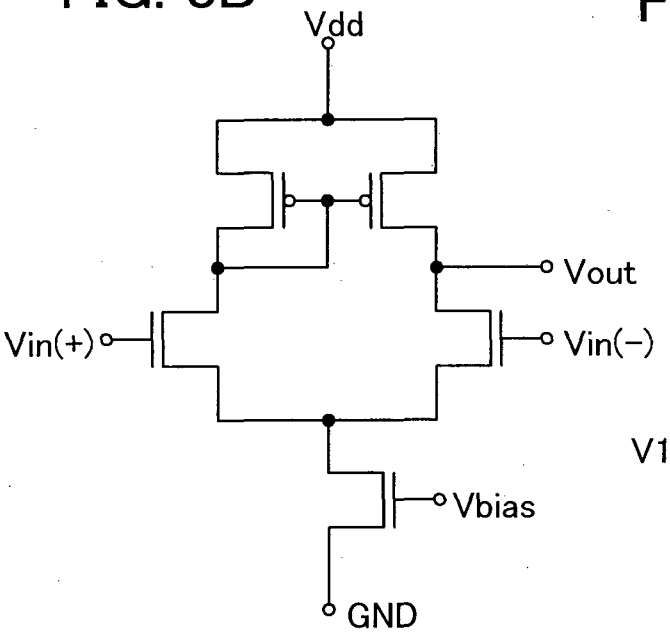
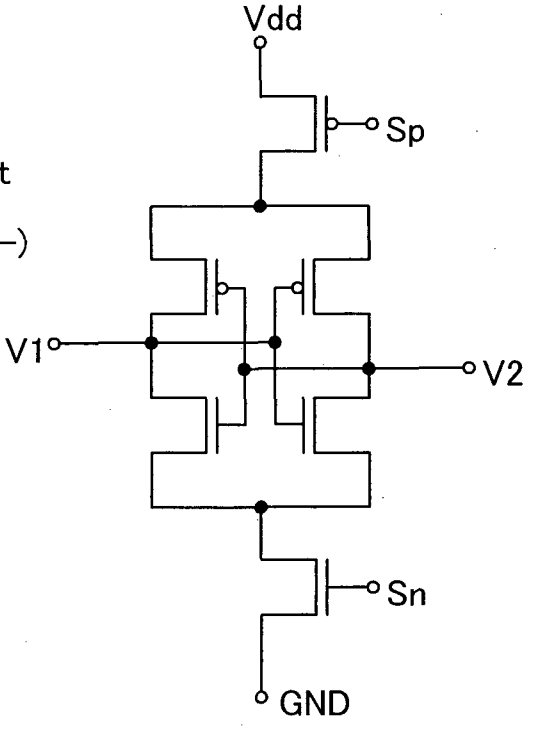


FIG. 8C



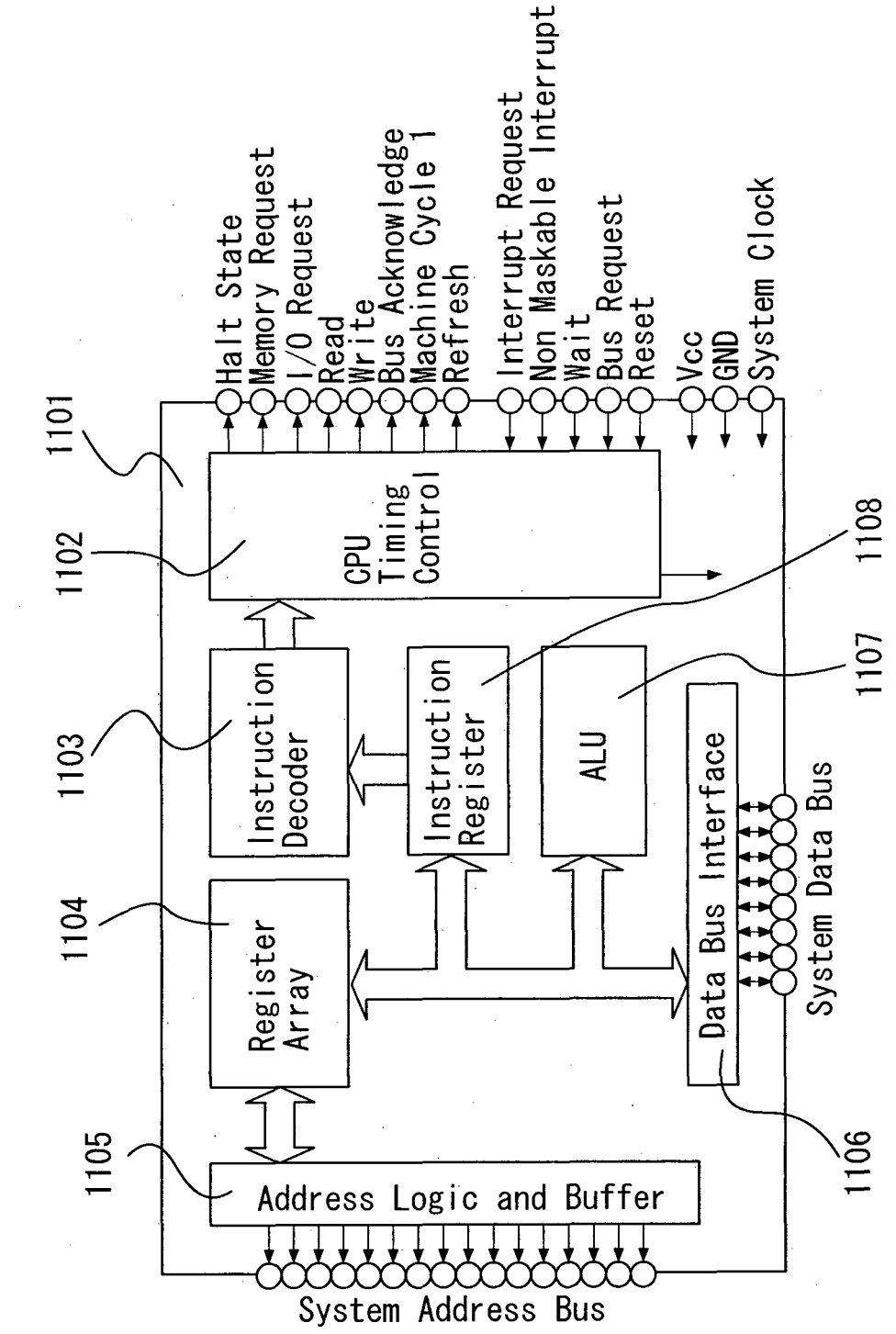

Halt State
Memory Request
I/O Request
Read
Write
Bus Acknowledge
Machine Cycle 1
Refresh
Interrupt Request
Non Maskable Interrupt
Wait
Bus Request
Reset
Vcc
GND
System Clock
1101
CPU Timing Control
1102
1103
Instruction Decoder
Instruction Register
1108
ALU
1107
1104
Register Array
Data Bus Interface
System Data Bus
1105
Address Logic and Buffer
1106
System Address Bus

FIG. 9

FIG. 10A

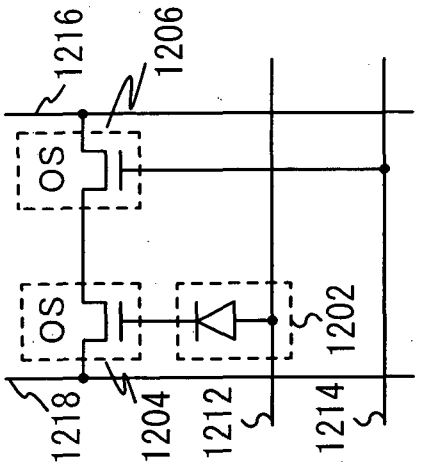


FIG. 10B

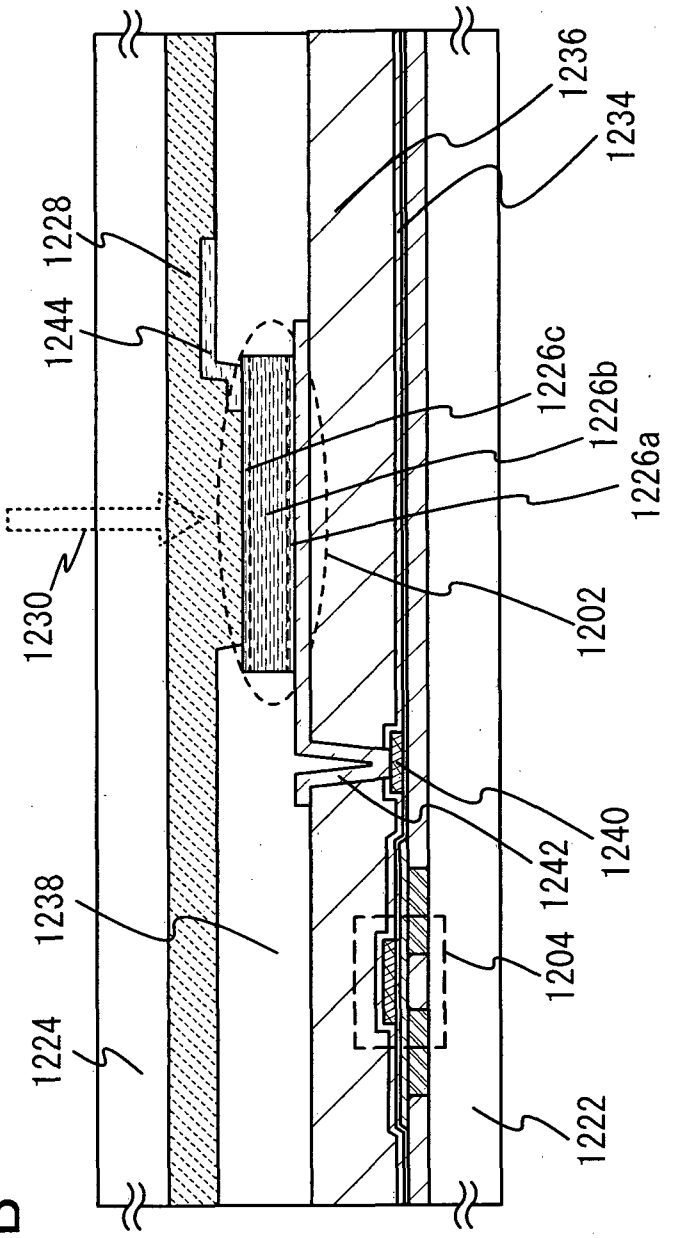


FIG. 11A

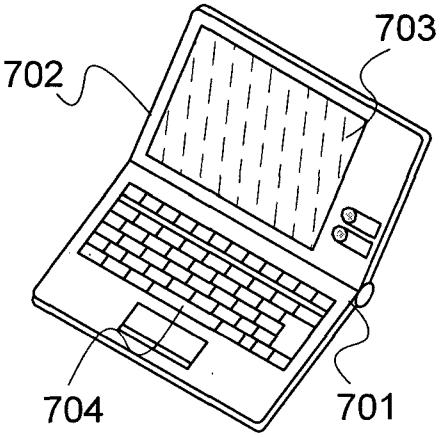


FIG. 11B

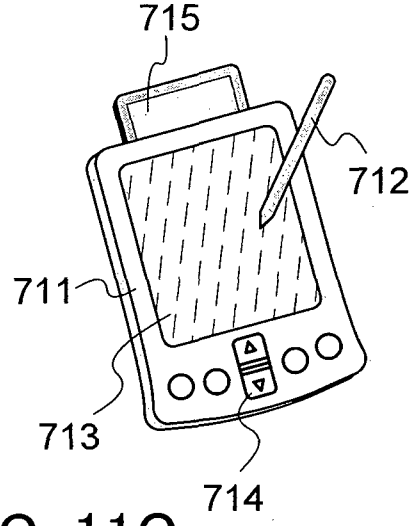


FIG. 11C

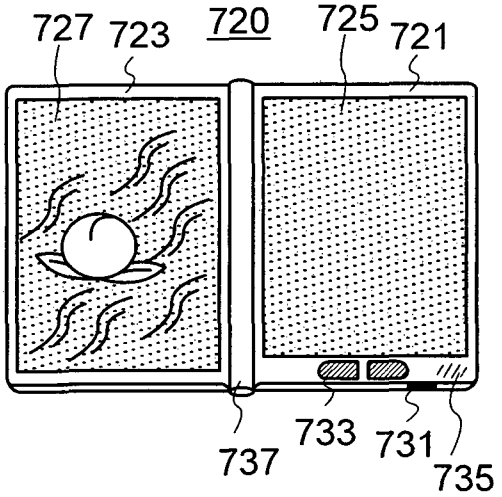


FIG. 11D

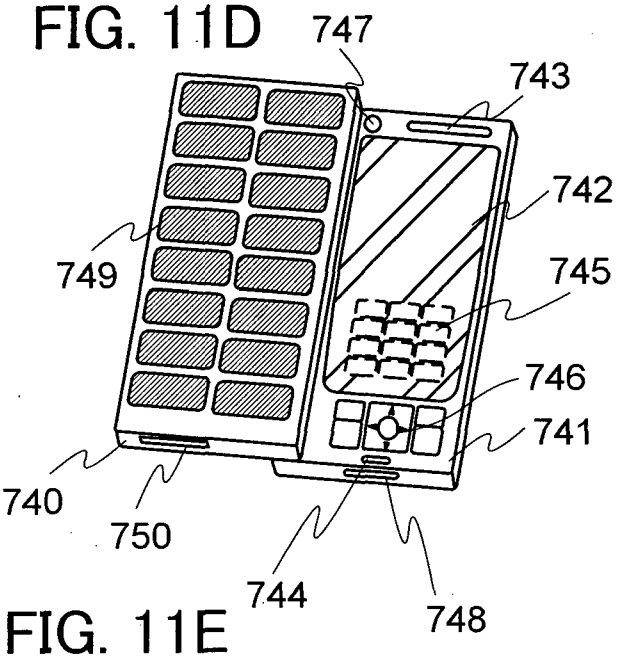


FIG. 11E

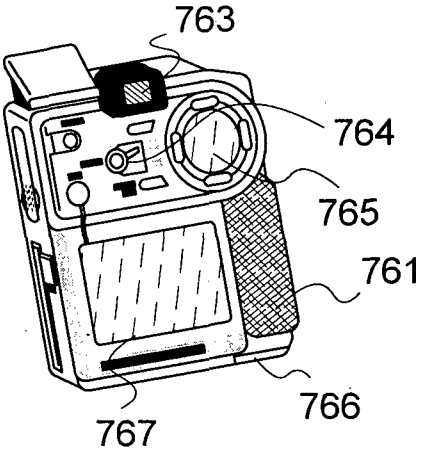


FIG. 11F

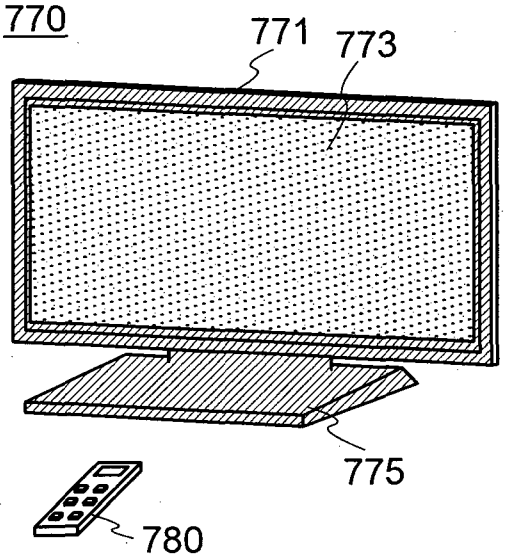


FIG. 12A

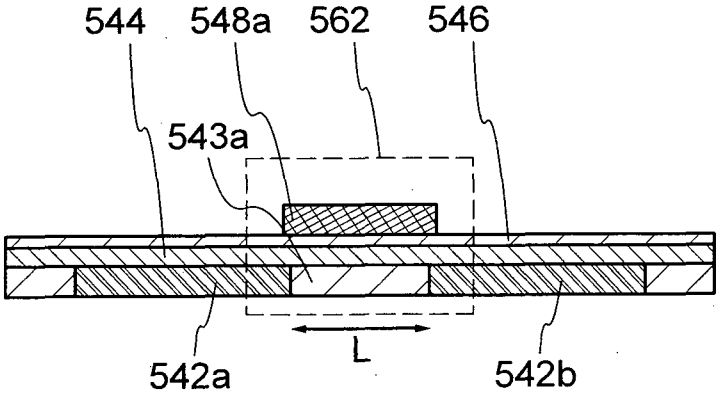


FIG. 12B

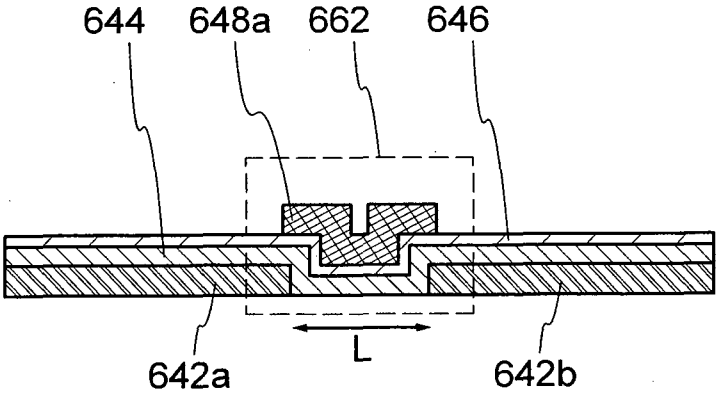


FIG. 13A

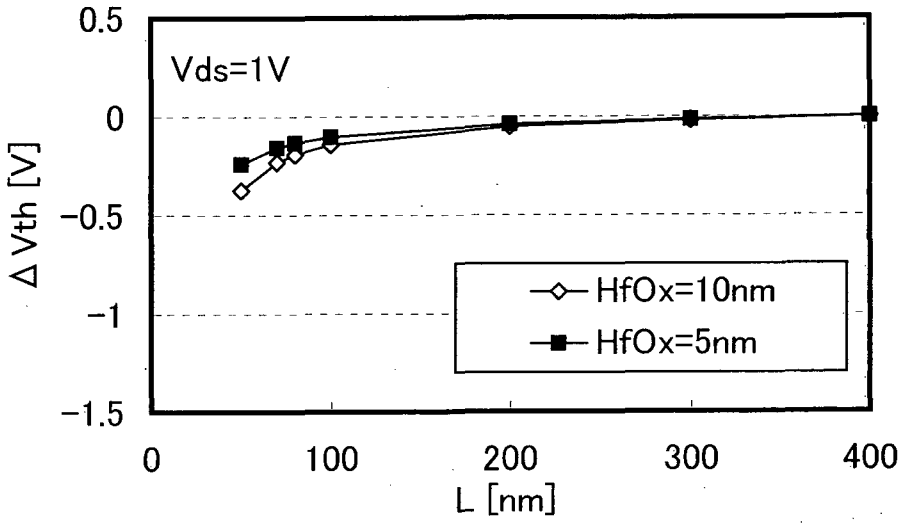


FIG. 13B

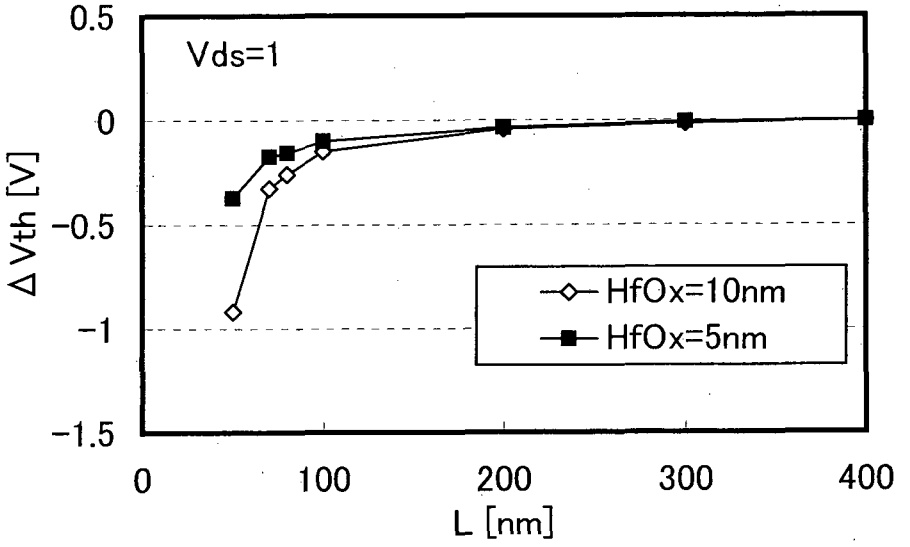


FIG. 14A

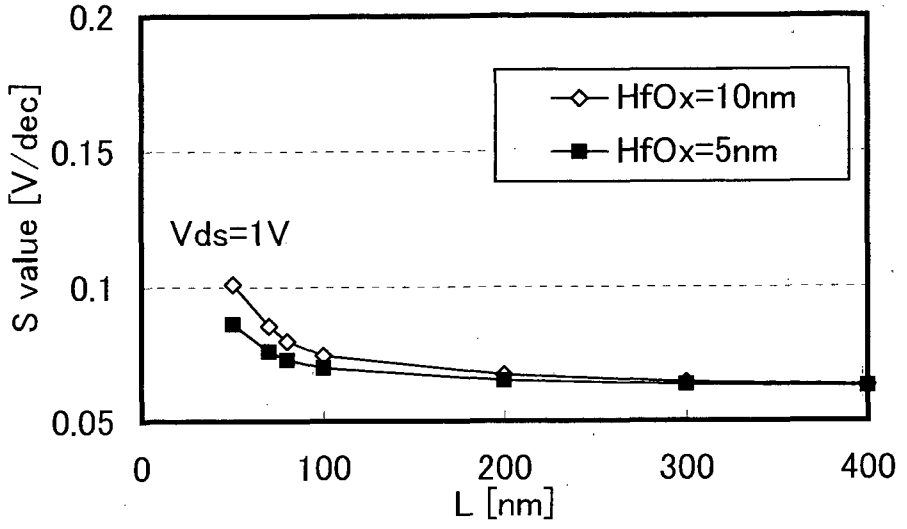


FIG. 14B

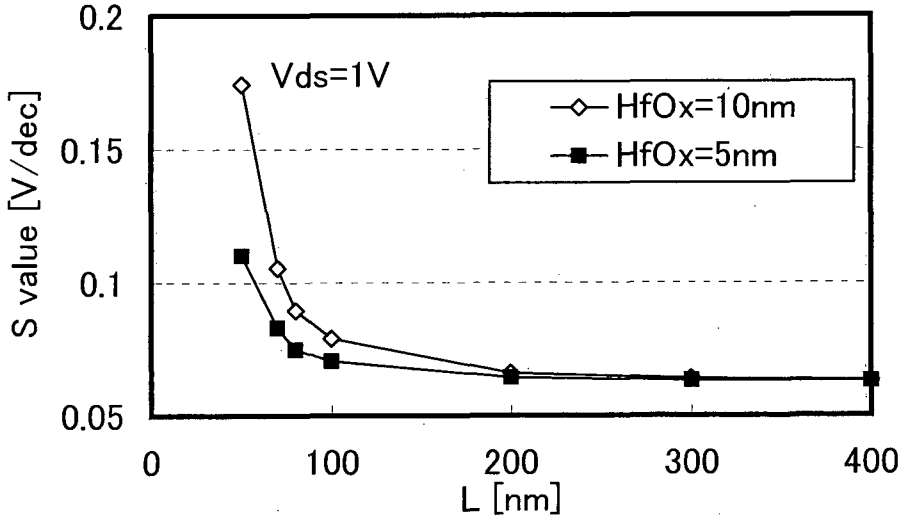


FIG. 15

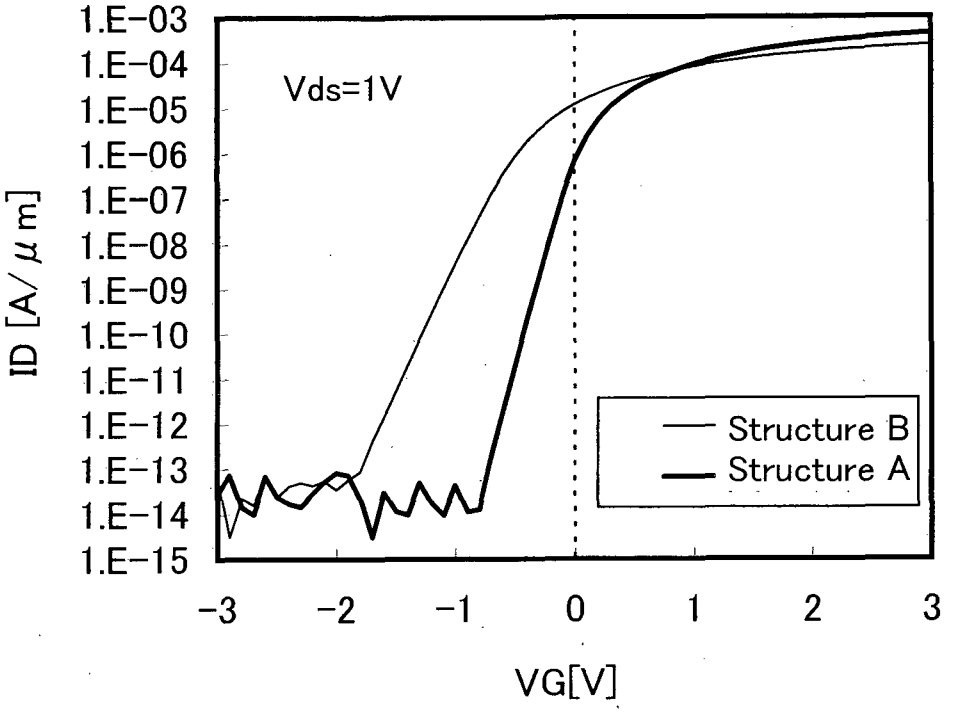

1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
1.E-10
1.E-11
1.E-12
1.E-13
1.E-14
1.E-15
ID [A/μm]
Vds=1V
Structure B
Structure A
-3
-2
-1
0
1
2
3
VG[V]

FIG. 16

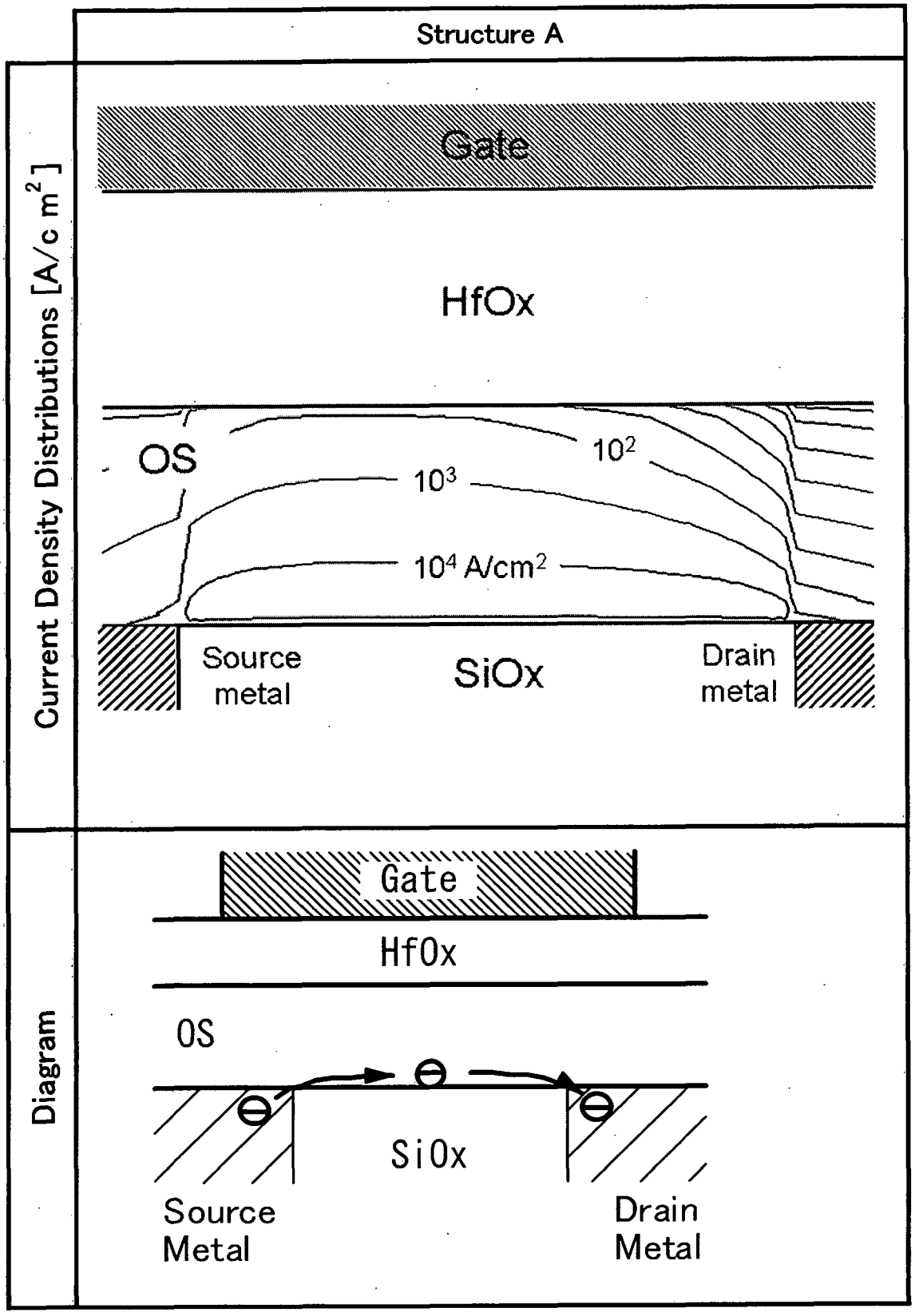

Structure A
Current Density Distributions [A/c m^2]
Gate
HfOx
OS
10^2
10^3
10^4 A/cm^2
Source metal
SiOx
Drain metal
Diagram
Gate
HfOx
OS
SiOx
Source Metal
Drain Metal

FIG. 17

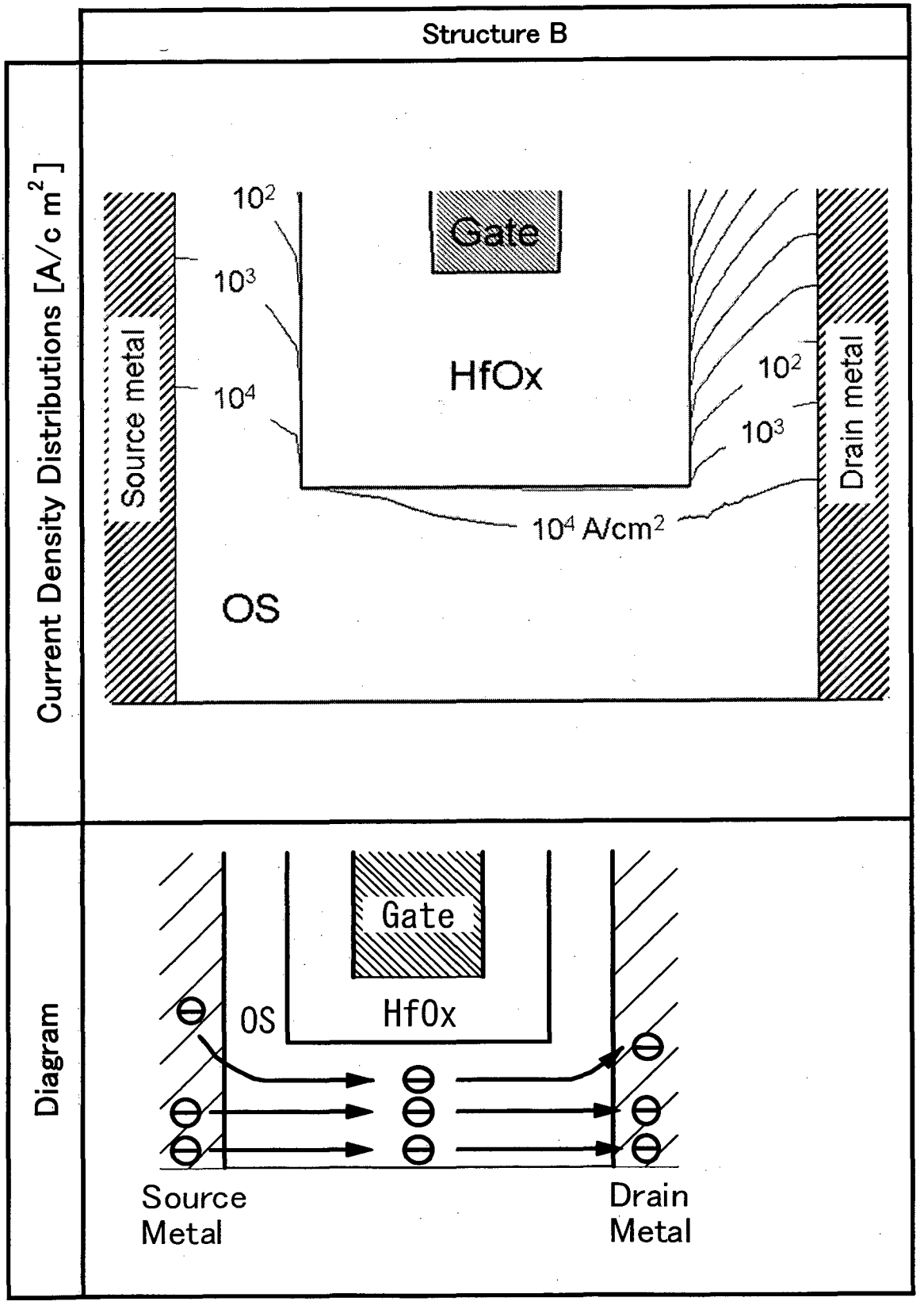
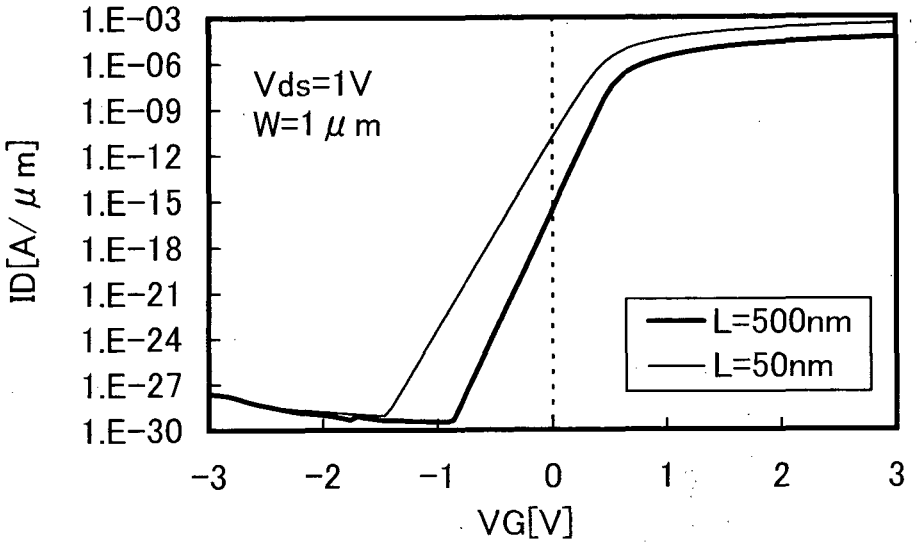

Structure B
Current Density Distributions [A/c m^2]
10^2
10^3
10^4
Source metal
Gate
HfOx
OS
10^2
10^3
Drain metal
10^4 A/cm^2
Diagram
Gate
OS
HfOx
Source Metal
Drain Metal

FIG. 18


1.E-03
1.E-06
1.E-09
1.E-12
1.E-15
1.E-18
1.E-21
1.E-24
1.E-27
1.E-30
ID[A/μm]
Vds=1V
W=1μm
L=500nm
L=50nm
-3
-2
-1
0
1
2
3
VG[V]

EXPLANATION OF REFERENCE

100: substrate, 102: protective layer, 104: semiconductor region, 106: element isolation insulating film, 108: gate insulating film, 110: gate electrode, 116: channel formation region, 120: impurity region, 122: metal layer, 124: metal compound region, 130: insulating film, 140: substrate, 141: mask, 141a: mask, 141b: mask, 142: conductive film, 142a: source electrode, 142b: drain electrode, 143: insulating film, 143a: insulating film, 144: oxide semiconductor film, 146: gate insulating film, 148a: gate electrode, 148b: electrode, 150: insulating film, 152: insulating film, 160: transistor, 162: transistor, 164: capacitor, 542a: source electrode, 542b: drain electrode, 543a: insulating film, 544: oxide semiconductor layer, 546: gate insulating film, 548a: gate electrode, 562: transistor, 642a: source electrode, 642b: drain electrode, 644: oxide semiconductor layer, 646: gate insulating film, 648a: gate electrode, 662: transistor, 701: housing, 702: housing, 703: display portion, 704: keyboard, 711: main body, 712: stylus, 713: display portion, 714: operation buttons, 715: external interface , 720: electronic book reader, 721: housing, 723: housing, 725: display portion, 727: display portion, 731: power switch, 733: operation keys, 735: speaker, 737: hinge, 740: housing, 741: housing, 742: display panel, 743: speaker, 744: microphone, 745: operation keys, 746: pointing device, 747: camera lens, 748: external connection terminal, 749: solar cell, 750: external memory slot, 761: main body, 763: eyepiece, 764: operation switch, 765: display portion, 766: battery, 767: display portion, 770: television device, 771: housing, 773: display portion, 775: stand, 780: remote controller, 1000: transistor, 1010: transistor, 1020: capacitor, 1050: memory cell, 1101: CPU, 1102: timing control circuit, 1103: instruction decoder, 1104: register array, 1105: address logic and buffer circuit, 1106: data bus interface, 1107: ALU, 1108: instruction register, 1202: photodiode, 1204: transistor, 1206: transistor, 1212: photodiode reset signal line, 1214: gate signal line, 1216: photosensor output signal line, 1218: photosensor reference signal line, 1222: substrate, 1224: substrate, 1226a: semiconductor layer, 1226b: semiconductor layer, 1226c: semiconductor layer, 1228: adhesive layer, 1230: incident light, 1234: insulating film, 1236: interlayer insulating film, 1238: interlayer insulating film, 1240: gate electrode layer, 1242: electrode layer, and 1244: electrode layer.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/058159

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L29/786(2006.01)i, H01L21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, H01L21/336

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2008-015487 A (AU Optronics Corp.) 2008.01.24, Paragraphs 0029-0042 & US 2008/0001232 A1	1-24
Y	JP 2009-059805 A (HITACHI HIGH-TECHNOLOGIES CORPORATION.) 2009.03.19, Paragraph 0005 (No Family)	1-24
Y	JP 2003-086808 A (MASASHI KAWASAKI) 2003.03.20, Paragraphs 0064-0080 & US 2003/0047785 A1 & KR 10-2003-0022692 A & CN 1405898 A	1-24
Y	JP 2009-094492 A (SEMICONDUCTOR ENERGY LABORATORY CO.,LTD.) 2009.04.30, Figs.15-18 (No Family)	9-24

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16.06.2011	28.06.2011

Name and mailing address of the ISA/JP	Authorized officer
Japan Patent Office 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	KAZUNARI TANADA Telephone No. +81-3-3581-1101 Ext. 3462

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