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(54) **SURFACE MOUNTED PACKAGE WITH DIE BOTTOM SPACED FROM SUPPORT BOARD**

GEHÄUSE ZUR OBERFLÄCHENANBRINGUNG MIT VON DER TRÄGERPLATTE BEABSTANDETEM CHIPBODEN

ENVELOPPE MONTEE SUR UNE SURFACE AVEC FOND DE PLAQUETTE ESPACE DE LA CARTE DE SUPPORT

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to a semiconductor package and more particularly to a semiconductor package for housing a power semiconductor die having a structure which reduces temperature cycling failures.

BACKGROUND OF THE INVENTION

[0002] Generally, thermal cycling causes frequent and repeated stress which in layered structures leads to cracks due to, for example, fatigue. Temperature cycling, therefore, is a material factor in causing failure in layered structures.

[0003] In semiconductor device packages, temperature cycling causes failures in die-underfill bonding, underfill-substrate bonding, solder bump attachment and passivation layers among other areas. This reduces the reliability of the package. It is, therefore, desirable to provide a means to reduce failure caused by temperature cycling.

[0004] Referring now to the drawings, in which like reference numerals refer to like elements, there is shown in Figs. 1 and 2 a semiconductor package 5 that is fully described in US 2001 048 116 A1. Figs. 1 and 2 show that semiconductor package 5 includes MOSFET 10 inside cup-shaped can 12 which functions as a drain clip. Can 12 is preferably made from a copper alloy and is silver-plated. Can 12 has internal dimensions that are greater than those of MOSFET 10; thus MOSFET 10 is readily received in the interior of can 12. The drain contact of MOSFET 10 is connected to the bottom of can 12 by a layer of silver-loaded conductive epoxy 14. A ring of low stress high adhesion epoxy 16 is applied around the edges of MOSFET 10 to seal and add extra structural strength to the package. Source contact 18 and gate contact 20 of MOSFET 10, which are disposed on a surface of MOSFET 10 opposing its drain contact, are exposed as shown in Fig. 1. Can 12 includes two rows of projections 22 disposed on two of its opposing edges. Projections are provided to make electrical contact with respective lands on a circuit board (not shown), such as an Insulated Metal Substrate or an ordinary circuit board, thereby electrically connecting the drain of MOSFET 10 to its place within a circuit. As shown in Fig. 1, source contact 18 of MOSFET 10 is flush with the contact surfaces of projections 22 of can 12. Therefore, source contact 18 and gate contact 20 of MOSFET 10 will be flush with the surface of the circuit board when package 5 is mounted thereon.

[0005] Document US-B1-6 262 489 is directed to mounting an IC semiconductor device to a substrate using flip chip technology. The assembly generally entails a flip chip having a first surface, an oppositely-disposed second surface, an integrated circuit that includes a vertical device on the first surface, and an electrical contact for the vertical device on the second surface. The flip chip is bonded with first solder connections to a first conductor pattern on a substrate, so that the first solder connections electrically and mechanically connect the flip chip to the substrate. The assembly further includes an electrical contact member that is positioned so that the flip chip is between the contact member and the substrate. The contact member is electrically and mechanically connected to a second conductor pattern on the substrate with second solder connections. A third solder connection electrically and mechanically connects the contact member to the electrical contact on the second surface of the flip chip.

[0006] Document US-A-4 392 151 is directed to a semiconductor element disposed in a recess at the bottom of a flanged metallic casing through a solder layer. An electrically insulating, molded plate is fixed to the casing by having protrusions fitted into holes disposed in opposite flanges of the casing and also two opposite L-shaped members abutting against adjacent lateral walls of the casing. Six strip-shaped leads buried in and extended from the molded plate are arranged to be soldered at first ends to associated solder electrodes on the exposed surface of the semiconductor element. The element and L-shaped members are buried in a resinous material molded within the casing.

[0007] The above-described package is subject to possible failure due to temperature cycling, as described above. It is desirable, therefore, to produce a package design having a similar structure as described above, such that substrate failure caused by thermal cycling is reduced.

SUMMARY OF THE INVENTION

[0008] A semiconductor device package according to the invention is provided having the features recited in claim 1.

[0009] In order to reduce substrate failure, for example, caused by thermal cycling a semiconductor device package is disclosed that comprises a semiconductor device die having a first surface substantially parallel to a second surface, and the first surface and second surface each have a solderable planar metal electrode. Further, a metal clip is disclosed that has a flat web portion comprising a first and second surface, wherein the second surface is electrically connected with the first surface of the semiconductor device die.

[0010] From the edge of flat web portion of the clip, at least one solderable planar metal post-shaped electrode extends over and spaced from an edge of the semiconductor device die. The die is disposed in the interior of the clip such that the die is inwardly recessed in the interior of the clip and the second surface of the die is not flush (or co-planar) with the at least one solderable planar metal post-shaped electrode. The interior of the solderable planar metal post-shaped electrode is removed to a parallel plane above the plane of the second surface of

the die.

[0011] The at least one solderable planar metal post-shaped electrode is mountable to a metallized pattern on a support surface, such as a circuit board and the second surface of the die is spaced from the metallized pattern on the support surface.

[0012] Therefore, the semiconductor package according to the present invention reduces the number of failures due to thermal cycling and, thus, adds to the reliability of the package. Furthermore, the semiconductor package according to the present invention includes a vertical conduction MOS-gated die such as a MOSFET having a first major surface on which a major electrode and a control electrode are disposed and another major surface opposing the first major surface on which another major electrode is disposed. Conventionally, the first major electrode in a vertical conduction MOSFET used in a package according to the present invention is the source electrode; while, its second major electrode is the drain electrode. The control electrode in a vertical conduction MOSFET is conventionally referred to as the gate electrode.

[0013] While the die is described herein as a power MOSFET, it will be apparent that the die may be any desired die, including any MOS-gated device (e.g., an IGBT), a thyristor or diode, or the like.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Fig. 1 shows a top view of a semiconductor package according to the prior art;

[0015] Fig. 2 shows a cross-section of semiconductor package of Fig. 1 looking in the direction of line 1-1; and

[0016] Fig. 3 shows a cross-section of a semiconductor package of Figs. 1 and 2 modified according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0017] Referring now to Fig. 3, in accordance with the present invention, semiconductor package 24 includes MOSFET 10 that is set back deeper into the interior of can 12 than in prior art packages as shown in Fig.1 and Fig. 2. Therefore, source contact 18 and gate contact 20 (not shown in Fig. 3) of MOSFET 10 are no longer flush with projections 22 of can 12. This arrangement is illustrated in Fig. 3 by the gap between broken lines A, A'. It has been found that when MOSFET 10 is set deeper within can 12 such that source 18 is offset from the plane of the circuit board (as represented by broken line A) by about 0.001 - 0.005 inches failure due to thermal cycling of the part when soldered down or affixed by an epoxy to a substrate is reduced.

[0018] In other words, a semiconductor package according to the present invention includes a metal can which receives in its interior space a MOSFET or other similar semiconductor type device die. The MOSFET so received is inwardly recessed in the can and oriented such that the MOSFET's drain electrode is facing the bottom of the can and is electrically connected to the same by a layer of conductive epoxy or a solder or the like. The edges of the MOSFET so placed are spaced from the walls of the can. The space between the edges of the MOSFET and the walls of the can is filled with an insulating layer. The can preferably includes two rows of posts on its opposing edges. The posts are connectable to appropriate conduction pads on a substrate, such as a circuit board, to connect the drain of the MOSFET to its appropriate place within a circuit. Moreover, in an alternative embodiment of the present invention, the posts can be a full or partial portion of the rim of the can.

[0019] As a result of this arrangement, the source and gate electrodes of the MOSFET face the substrate when the can is mounted thereon. It has been found that if the MOSFET is positioned within the can so that the source and gate electrodes of the MOSFET become sub-flush with the surface of the substrate, failure due to thermal cycling is improved. Thus, according to an aspect of the present invention, the bottom surface of the MOSFET is sub-flush below the plane of the substrate by 0.001 - 0.005 inches to reduce temperature cycling failures. The sub-flush volume is filled by the conductive attachment material such as solder, epoxy, and the like.

[0020] Variations of the disclosed invention are possible without diversion from its scope. It would thus be recognized by a skilled person in the art that materials other than the ones described with reference to the preferred embodiment of the invention may be used to accomplish the intended advantageous results of the present invention. For example, instead of MOSFET 10, an IGBT, a thyristor, a diode or any other suitable semiconductor device may be used in the package according to the invention. As further examples, other alloys may be used to form the can 12 and/or other conductive means other than silver-loaded epoxy 14 may be used to connect the semiconductor die to the can 12.

[0021] Thus, although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

Claims

1. A semiconductor device package (24) comprising:

a semiconductor device die (10) having a first surface substantially parallel to a second surface;

said first surface having a first solderable planar metal electrode;

said second surface having a second solderable

planar metal electrode (18, 20);
a metallic conductive clip (12) having a flat web portion, said web portion having a first surface and a second surface, said second surface of said web portion being electrically connected with said first electrode; and
at least one electrical connector (22) comprising a solderable planar metal post-shaped electrode extending from an edge of said web portion over and spaced form an edge of said semiconductor device die (10) and terminating at a connection surface, wherein
said semiconductor device die (10) is inwardly recessed in the interior of said clip such that said second electrode (18, 20) of said semiconductor device die (10) is not flush with said connection surface, and said connection surface is adapted to mount to a metallized pattern on a support surface,
wherein said semiconductor device die (10) is inwardly recessed between 0.001 and 0.005 inches (25.4 and 127 μm).

2. The semiconductor device package according to claim 1, wherein said first electrode is the drain contact of a MOSFET and said second electrode is the source contact of said MOSFET.

3. The semiconductor device package according to claim 1, wherein said clip (12) is unitary and cup-shaped.

4. The semiconductor device package according to claim 1, wherein said clip (12) is made from copper alloy and is silver plated.

5. The semiconductor device package according to claim 1, wherein said first electrode is electrically connected to said web portion by a layer of one of solder and conductive epoxy.

6. The semiconductor device package according to claim 1, wherein said clip (12) is cup-shaped and includes a peripheral portion being a continuous rim surrounding and spaced from said semiconductor device die (10).

7. The semiconductor device package according to claim 6, wherein said space between said semiconductor device die (10) and said peripheral rim is filled with insulation bead (16).

8. The semiconductor device package according to claim 1, wherein said semiconductor device die (10) is one of a MOSFET, an IGBT, a power diode, and a thyristor.

Patentansprüche

1. Halbleitervorrichtungsgehäuse (24), umfassend:

einen Halbleitervorrichtungschip (10) mit einer ersten Oberfläche, die im Wesentlichen parallel zu einer zweiten Oberfläche ist;
wobei die erste Oberfläche eine erste lötbare planare Metallelektrode aufweist;
wobei die zweite Oberfläche eine zweite lötbare planare Metallelektrode (18, 20) aufweist;
eine metallische leitfähige Klammer (12) mit einem flachen Stegabschnitt, wobei der Stegabschnitt eine erste Oberfläche und eine zweite Oberfläche aufweist, wobei die zweite Oberfläche des Stegabschnitts mit der ersten Elektrode elektrisch verbunden ist; und
wenigstens einen elektrischen Verbinder (22), umfassend eine lötbare planare metallstiftförmige Elektrode, die sich von einer Kante des Stegabschnitts herüber erstreckt und von einer Kante des Halbleitervorrichtungschips (10) beabstandet ist und an einer Verbindungsoberfläche endet, wobei der Halbleitervorrichtungschip (10) im Inneren der Klammer nach innen vertieft ist, so dass die zweite Elektrode (18, 20) des Halbleitervorrichtungschips (10) nicht bündig mit der Verbindungsoberfläche ist und die Verbindungsoberfläche angepasst ist, um auf einem metallisierten Muster auf einer Trägeroberfläche angebracht zu werden,
wobei der Halbleitervorrichtungschip (10) zwischen 0,001 und 0,005 Zoll (25,4 und 127 μm) nach innen vertieft ist.

2. Halbleitervorrichtungsgehäuse nach Anspruch 1, wobei die erste Elektrode der Drain-Kontakt eines MOSFET ist und die zweite Elektrode der Source-Kontakt des MOSFET ist.

3. Halbleitervorrichtungsgehäuse nach Anspruch 1, wobei die Klammer (12) einheitlich und becherförmig ist.

4. Halbleitervorrichtungsgehäuse nach Anspruch 1, wobei die Klammer (12) aus Kupferlegierung besteht und versilbert ist.

5. Halbleitervorrichtungsgehäuse nach Anspruch 1, wobei die erste Elektrode mit dem Stegabschnitt durch eine Schicht aus Lötmittel oder leitfähigem Epoxid elektrisch verbunden ist.

6. Halbleitervorrichtungsgehäuse nach Anspruch 1, wobei die Klammer (12) becherförmig ist und einen Umfangsabschnitt umfasst, der ein kontinuierlicher Rand ist, der den Halbleitervorrichtungschip (10) umgibt und von ihm beabstandet ist.

7. Halbleitervorrichtungsgehäuse nach Anspruch 6, wobei der Raum zwischen dem Halbleitervorrichtungschip (10) und dem Umfangsrand mit Isolierkugeln (16) gefüllt ist.

8. Halbleitervorrichtungsgehäuse nach Anspruch 1, wobei der Halbleitervorrichtungschip (10) eines von einem MOSFET, einem IGBT, einer Leistungsdiode und einem Thyristor ist.

Revendications

1. Boîtier (24) de dispositif à semi-conducteur comprenant :

   une puce (10) de dispositif à semi-conducteur ayant une première surface sensiblement parallèle à une deuxième surface ;
   la première surface ayant une première électrode métallique plane pouvant être soudée ;
   la deuxième surface ayant une deuxième électrode (18, 20) métallique plane pouvant être soudée ;
   une attache (12) métallique conductrice ayant une première partie plane en nappe, la partie en nappe ayant une première surface et une deuxième surface, la deuxième surface de la partie en nappe étant reliée électriquement à la première électrode et
   au moins un connecteur (22) électrique, comprenant une électrode post-formée métallique plane pouvant être soudée, s'étendant à partir d'un bord de la partie en nappe et à distance d'un bord de la puce (10) du dispositif à semi-conducteur et se terminant à une surface de connexion, dans lequel la puce (10) du dispositif à semi-conducteur est évidée vers l'intérieur à l'intérieur de l'attache, de manière à ce que la deuxième électrode (18, 20) de la puce (10) du dispositif à semi-conducteur ne soit pas à affleurement avec la surface de connexion et la surface de connexion est conçue pour se monter sur un motif métallisé sur une surface de support,
   dans lequel la puce (10) du dispositif à semi-conducteur est évidée vers l'intérieur, entre 0,001 et 0,005 pouces (25,4 et 127 μm).

2. Boîtier de dispositif à semi-conducteur suivant la revendication 1, dans lequel la première électrode est le contact de drain d'un MOSFET et la deuxième électrode est le contact de source du MOSFET.

3. Boîtier de dispositif à semi-conducteur suivant la revendication 1, dans lequel l'attache (12) est unitaire et conformée en coupelle.

4. Boîtier de dispositif à semi-conducteur suivant la revendication 1, dans lequel l'attache (12) est en alliage de cuivre et est plaquée d'argent.

5. Boîtier de dispositif à semi-conducteur suivant la revendication 1, dans lequel la première électrode est reliée électriquement à la partie en nappe par une couche de l'un d'une soudure et d'un époxy conducteur.

6. Boîtier de dispositif à semi-conducteur suivant la revendication 1, dans lequel l'attache (12) est en forme de coupelle et comprend une partie périphérique étant un rebord continu entourant la puce (10) du dispositif à semi-conducteur et à distance de celle-ci.

7. Boîtier de dispositif à semi-conducteur suivant la revendication 6, dans lequel l'espace entre la puce (10) du dispositif à semi-conducteur et le rebord périphérique est rempli d'une rondelle (16) isolante.

8. Boîtier de dispositif à semi-conducteur suivant la revendication 1, dans lequel la puce (10) du dispositif à semi-conducteur est l'un d'un MOSFET, d'un IGBT, d'une diode de puissance et d'un thyristor.

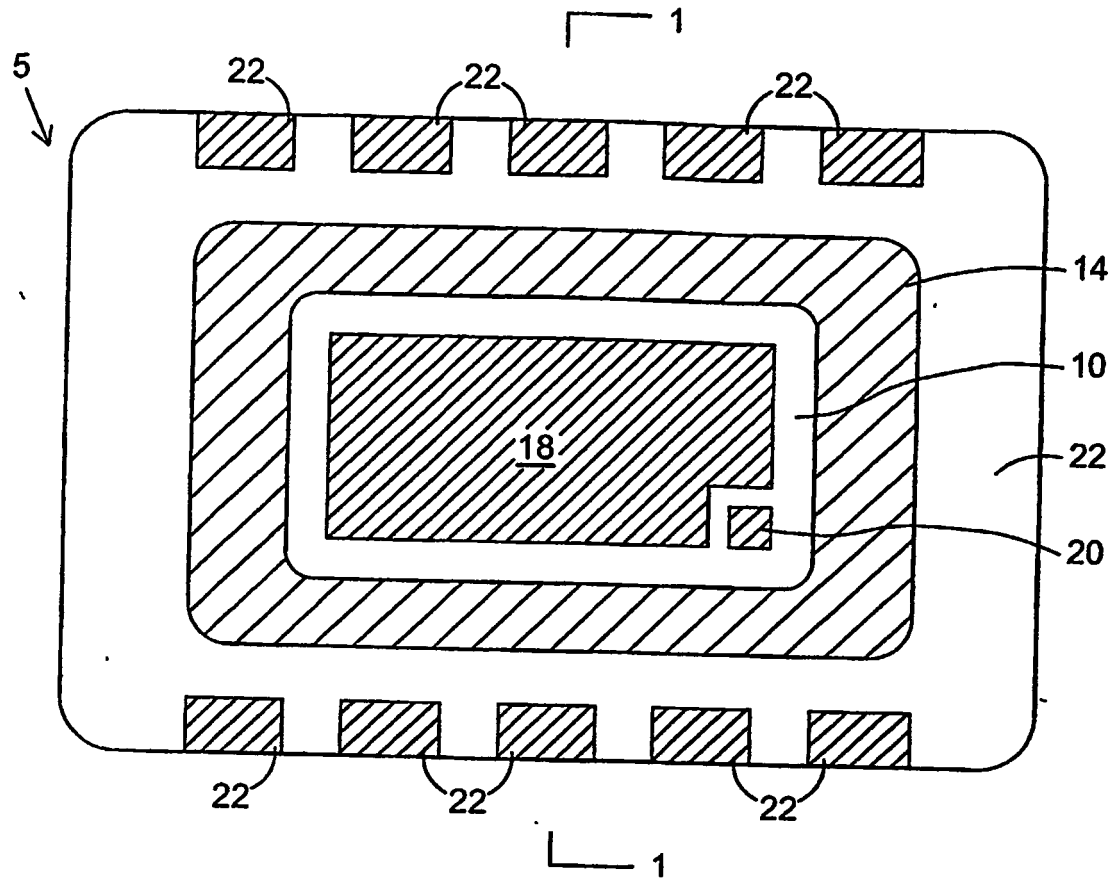

FIG. 1
PRIOR ART

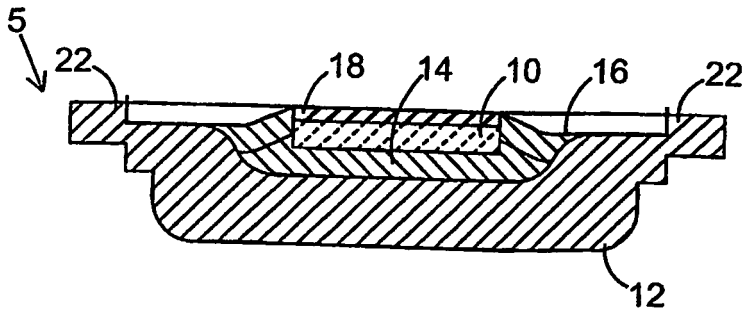

FIG. 2
PRIOR ART

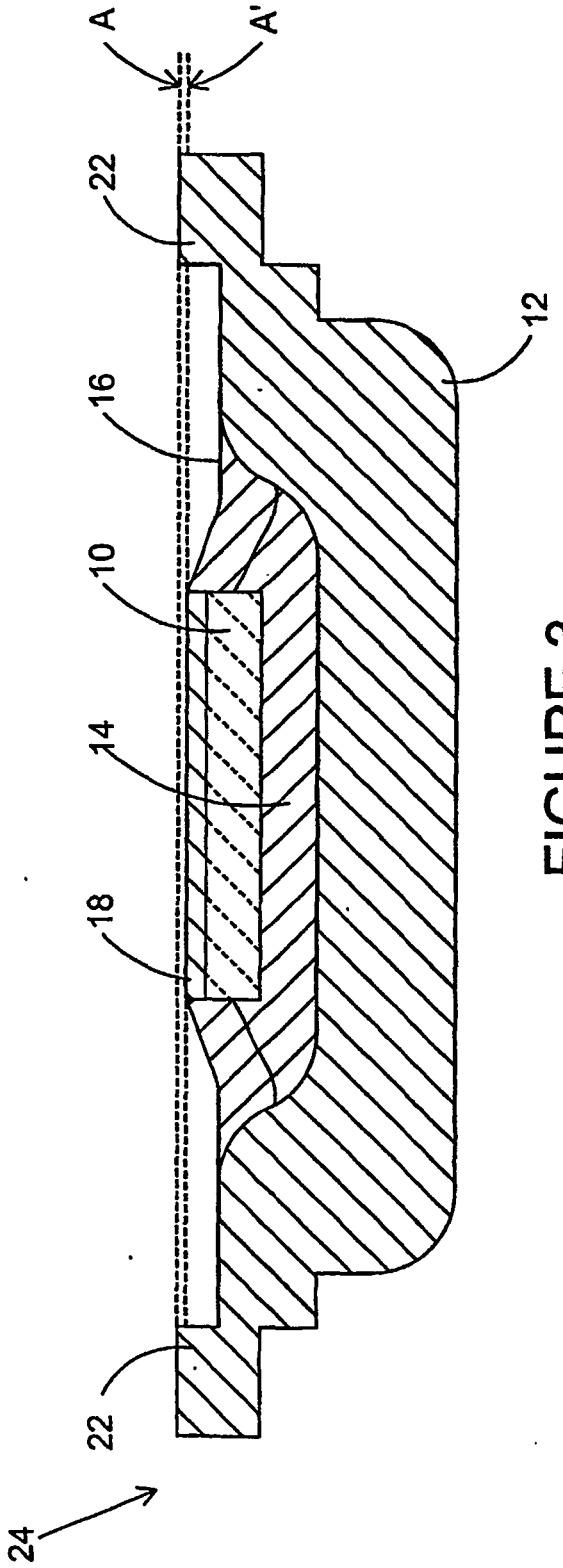

FIGURE 3

REFERENCES CITED IN THE DESCRIPTION

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