(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 December 2007 (06.12.2007)

PCT

(10) International Publication Number
WO 2007/138901 A1

(51) International Patent Classification:
H02J 7/00 (2006.01)

(21) International Application Number:
PCT/JP2007/060319

(22) International Filing Date: 15 May 2007 (15.05.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2006-153848 1 June 2006 (01.06.2006) JP

(71) Applicant *(for all designated States except US)*: **RICOH COMPANY, LTD.** [JP/JP]; 3-6, Nakamagome 1-chome, Ohta-ku, Tokyo, 1438555 (JP).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **YAMAMOTO, Norifumi** [JP/JP]; 1-1-432-434, Shinurashima-cho 1-chome, Kanagawa-kuYokohama-shi, Kanagawa, 2210031 (JP). **FUJIWARA, Akihiko** [JP/JP]; 1427-9-1102, Yamasakimachi, Machida-shi, Tokyo, 1950074 (JP).

(74) Agent: **ITOH, Tadahiko**; 32nd Floor, Yebisu Garden Place Tower, 20-3, Ebisu 4-chome, Shibuya-ku, Tokyo 1506032 (JP).

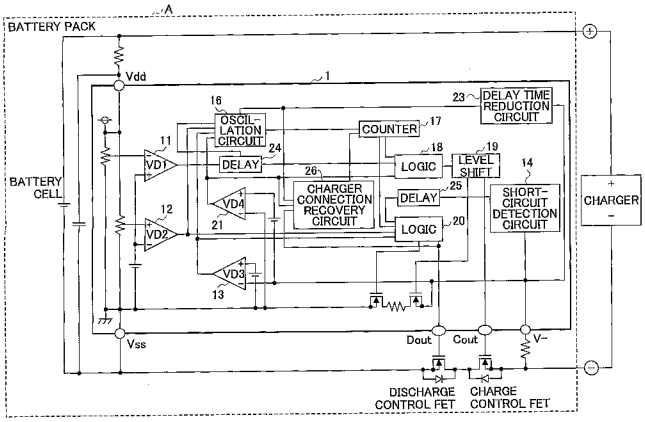
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) **Title:** CHARGE/DISCHARGE PROTECTION CIRCUIT, BATTERY PACK EMBEDDING THE CHARGE/DISCHARGE PROTECTION CIRCUIT, ELECTRONIC APPARATUS USING THE BATTERY PACK



(57) **Abstract:** A charge/discharge protection circuit that protects a secondary battery from overcharge, over-discharge, charge over-current, and discharge over-current is disclosed. The charge/discharge protection circuit includes an overcharge detection circuit, an over-discharge detection circuit, a charge over-current detection circuit, a discharge over- current detection circuit, a charge control FET that is turned off when overcharge is detected and when charge over-current is detected, a discharge control FET that is turned off when over-discharge is detected and when discharge over-current is detected, and a charger connection recovery circuit that controls on/off operations of the discharge control FET. When connection with a charger is established at a time over- discharge is detected and the discharge control FET is turned off, the discharge control FET is forcefully turned on after a first predetermined time elapses.

WO 2007/138901 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

DESCRIPTION

CHARGE/DISCHARGE PROTECTION CIRCUIT, BATTERY PACK EMBEDDING THE CHARGE/DISCHARGE PROTECTION CIRCUIT, ELECTRONIC APPARATUS USING THE BATTERY PACK

TECHNICAL FIELD

The present invention relates to a charge/discharge protection circuit of a lithium-ion secondary battery, for example, that is capable of reducing electric current consumption without increasing the chip size, preventing degradation of a discharge control FET, and reducing the battery charge time. The present invention also relates to a battery pack embedding such a charge/discharge protection circuit and various types of electronic apparatuses that use such a battery pack.

BACKGROUND ART

Various techniques related to a charge/discharge protection circuit of a lithium-ion secondary battery have been proposed. For example, Japanese Laid-Open Patent Publication No. 2002-176730 discloses a semiconductor device employed as a protection circuit of a battery pack as is shown in FIG. 5.

The illustrated semiconductor device

(charge/discharge protection circuit) 1 as a main component of a battery pack A includes an overcharge detection circuit 11, an over-discharge detection circuit 12, a discharge over-current detection circuit 13, a short-circuit detection circuit 14, an oscillation circuit 16, a counter circuit 17, logic circuits 18, 20, a level shift circuit 19, a charge over-current detection circuit 21, delay circuits 24, 25, and a delay time reduction circuit 23.

In the following, basic operations performed by the semiconductor device (charge/discharge protection circuit) 1 are described.

When overcharge, over-discharge, discharge over-current, charge over-current, or short-circuit is detected by the overcharge detection circuit 11, the over-discharge detection circuit 12, the discharge over-current detection circuit 13, the charge over-current detection circuit 21, or the short-circuit detection circuit 14, the oscillation circuit 16 is activated and the counter circuit 17 starts counting operations.

After the counter circuit 17 counts to a predetermined detection delay time that is set for a corresponding detection, in the case of overcharge or charge over-current detection, a Cout output is switched to low level "L" via the logic circuit (e.g., latch circuit) 18 and the level shift circuit 19 so that a charge control FET Q1 is

turned off; and in the case of over-discharge, discharge over-current, or short-circuit detection, a Dout output is switched to low level "L" via the logic circuit 20 so that a discharge control FET Q2 is turned off.

When a charger is connected to the battery pack A so that charge current flows into the battery pack A, the source voltage of the charge control FET Q1 becomes lower than the source voltage of the discharge control FET Q2. It is noted that the source voltage of the discharge control FET Q2 corresponds to the Vss terminal voltage of the semiconductor device 1, and although a resistance is connected to a V- terminal of the semiconductor device, since the V- terminal has high impedance, the source voltage of the charge control FET Q1 may be substantially equal to the V- terminal voltage of the semiconductor device 1.

Accordingly, when charge current is supplied, the V- terminal voltage becomes lower than the Vss terminal voltage. When the difference between the V- terminal voltage and the Vss terminal voltage reaches a predetermined voltage (charge over-current detection voltage), charge over-current is detected so that the output of terminal Cout is switched to low level "L" and the charge control FET Q1 is turned off. It is noted that the relationship between a charge over-current value I, a charge over-current detection voltage Vchgdet, the ON resistance Ron1 of the charge control FET Q1, and the ON

resistance Ron2 of the discharge control FET Q2 may be expressed by the following formula:

$$I = Vchgdet / (Ron1 + Ron2)$$

The above-described operations are basic operations performed by the charge/discharge protection circuit (semiconductor device) of FIG. 5 upon detecting overcharge, over-discharge, charge over-current, discharge over-current, or short-circuit.

In the following, the function and circuit configuration of the delay time reduction circuit 23 are briefly described.

Normally, the delay time set with respect to overcharge detection by the overcharge detection circuit 11 is at least 1 second so that a test time for testing the semiconductor device 1 may be relatively long.

In turn, when testing the semiconductor device 1 or a protection circuit substrate, a TEST terminal may be set to low level "L" so that the output frequency of the oscillation circuit 16 may be increased and the detection delay time may be decreased to enable reduction of the test time. It is noted that this scheme may also be applied to overcharge, over-discharge, or discharge over-current detection but is particularly advantageous when applied to overcharge detection

that requires a relatively long delay time.

The oscillation circuit 16 may be a ring oscillator that includes a constant current inverter and a condenser, for example. It is noted that the oscillation frequency of a ring oscillator is determined by a constant current value of a constant current source, a capacitor value, and a threshold value of the constant current inverter. Thus, a method for reducing the delay time may involve setting the signal of the test terminal to low level "L" to thereby (a) increase the constant current value of the constant current source; (b) substantially decrease the capacity value of a capacitor; or (c) change the threshold value of the constant current inverter of the ring oscillator, for example.

In another example, the position at which the output of the counter circuit 17 is obtained may be changed to reduce the delay time instead of changing the oscillation frequency of the oscillation circuit 16, the details of which are described in Japanese Laid-Open Patent Publication No. 2002-176730.

In the charge/discharge protection circuit shown in FIG. 5, recovery from over-discharge status to dischargeable status may be realized by establishing connection with a charger. In this case, if a Vdd terminal voltage is less than or equal to an over-discharge detection voltage when a charger is connected, a charge current is supplied via a parasitic

diode of the discharge control FET Q2, and then, after the Vdd terminal voltage becomes higher than the over-discharge detection voltage, the output of terminal Dout may be set to high level "H" to turn on the discharge control FET Q2 and switch to dischargeable status. On the other hand, if the Vdd terminal voltage is higher than the over-discharge detection voltage when the charger is connected, the Dout terminal may be immediately switched to high level "H".

It is noted that a PIN for recognizing charger connection or a comparator may be used to enable such charger connection recovery operations. However, the number of terminals has to be increased at the charger side as well as the IC side when the PIN is used, and in the case where the comparator is used, the chip size has to be increased so that current consumption may be increased.

Accordingly, there is a demand for a charge/discharge protection circuit that is capable of controlling on/off operations of a discharge control FET using existing PINs and circuits, preventing the current consumption and the chip size from increasing, preventing degradation of the discharge control FET when a charger is connected, and reducing a battery charge time. There is also a demand for a battery pack embedding such a charge/discharge protection circuit and an electronic apparatus using such a battery pack.

DISCLOSURE OF THE INVENTION

According to one embodiment of the present invention, a charge/discharge protection circuit that protects a secondary battery from overcharge, over-discharge, charge over-current, and discharge over-current is provided, the charge/discharge protection circuit including:

an overcharge detection circuit;

an over-discharge detection circuit;

a charge over-current detection circuit;

a discharge over-current detection circuit;

a charge control FET that is turned off when overcharge is detected by the overcharge detection circuit and when charge over-current is detected by the charge over-current detection circuit;

a discharge control FET that is turned off when over-discharge is detected by the over-discharge detection circuit and when discharge over-current is detected by the discharge over-current detection circuit; and

a charger connection recovery circuit that controls on/off operations of the discharge control FET such that when connection with a charger is established at a time over-discharge is detected and the discharge control FET is turned off, the discharge control FET is forcefully turned on after a first predetermined time elapses.

According to another embodiment of the present

invention, a battery pack is provided that includes a charge/discharge protection circuit according to an embodiment of the present invention.

According to another embodiment of the present invention, an electronic apparatus is provided that includes a battery pack according to an embodiment of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram showing a charge/discharge protection circuit according to an embodiment of the present invention that is embedded in a battery pack;

FIG. 2A is a diagram illustrating charger connection recovery control operations when no over-discharge, over-discharge, or over-current is detected, and no charger is connected;

FIG. 2B is a diagram illustrating charger connection recovery control operations when over-discharge is detected and a charger is not connected;

FIG. 2C is a diagram illustrating charger connection recovery control operations when over-discharge is detected and a charger is connected;

FIG. 3A is a diagram illustrating operations for controlling a discharge control FET in a case where a charger connection detection terminal is provided, the operations

being performed when over-discharge is not detected and a charger is not connected;

FIG. 3B is a diagram illustrating another set of operations for controlling the discharge control FET using the charger connection detection terminal, the operations being performed when over-discharge is detected and a charger is not connected;

FIG. 3C is a diagram illustrating another set of operations for controlling the discharge control FET using the charger connection detection terminal, the operations being performed when over-discharge is detected and a charger is connected;

FIG. 4 is a timing chart illustrating charge operations that are performed when a charger is connected; and

FIG. 5 is a diagram showing a charge/discharge protection circuit according to a prior art example.

BEST MODE FOR CARRYING OUT THE INVENTION

In the following, preferred embodiments of the present invention are described with reference to the accompanying drawings.

FIG. 1 is a diagram showing a charge/discharge protection circuit (semiconductor device) according to an embodiment of the present invention.

The illustrated charge/discharge protection circuit

of FIG. 1 differs from the circuit shown in FIG. 5 in that it does not include a TEST terminal and includes a charger connection recovery circuit 26. It is noted that components of the charge/discharge protection circuit of the present embodiment that are identical to those shown in FIG. 5 are given the same reference numbers.

The charge/discharge protection circuit 1 of the present embodiment includes an overcharge detection circuit 11, an over-discharge detection circuit 12, a discharge over-current detection circuit 13, a short-circuit detection circuit 14, an oscillation circuit 16, a counter circuit 17, logic circuits 18, 20, a level shift circuit 19, a charge over-current detection circuit 21, delay circuits 24, 25, a delay time reduction circuit 23, and the charger connection recovery circuit 26.

As is described above, the TEST terminal is not provided in the semiconductor device (charge/discharge detection circuit) 1 of FIG. 1 so that the number of terminals may be reduced compared to the semiconductor device 1 of FIG. 5. In the present embodiment, during test mode operations, instead of applying a low level "L" signal to the TEST terminal, a signal with a predetermined value (e.g., -3 V) that is normally not applied to the V- terminal is applied to the delay time reduction circuit 23 to reduce the delay time in the manner described in relation to FIG. 5 (e.g.,

increasing the constant current value of the constant current source, substantially decreasing the capacity of the capacitor, or changing the threshold value of the constant current inverter).

It is noted that basic charge/discharge protection operations performed within the semiconductor device 1 of FIG. 1 may be similar to the operations performed in the semiconductor device 1 shown in FIG. 5; however, according to an aspect of the present embodiment, by providing the charger connection recovery circuit 26 in the semiconductor device 1, on/off operations of the discharge control FET Q2 may be controlled in the manner described below.

In the charger connection recovery circuit 26, a charger connection signal corresponding to an internal circuit signal of the charge over-current detection circuit 21, a delay time reduction signal corresponding to an internal circuit signal of the delay time reduction circuit 23, an over-discharge detection signal corresponding to a detection signal from the over-discharge detection circuit 12, and an over-discharge confirmation signal that is inverted after the elapse of an over-discharge recovery delay time or an over-discharge detection delay time are used to control on/off operations of the discharge control FET Q2. In a case where a charger is connected at the time over-discharge is detected, the discharge control FET Q2 is forcefully turned on after the

elapse of the over-discharge recovery delay time (first predetermined time) and then forcefully turned off after the elapse of the over-discharge detection delay time (second predetermined time). Further, in a case where a battery cell voltage is still less than or equal to an over-discharge detection voltage, the operations of turning on the discharge control FET Q2 after the elapse of the over-discharge recovery delay time and turning off the discharge control FET Q2 after the elapse of the over-discharge detection delay time are repeated. In one preferred embodiment, the over-discharge recovery delay time and the over-discharge detection delay time may be determined based on variations in internal circuit temperature characteristics, charger temperature characteristics, over-discharge recovery delay time temperature characteristics, and over-discharge detection delay time temperature characteristics, for example.

In the following, specific operations performed within the charger connection recovery circuit 26 are described.

The charger connection signal corresponding to an internal signal of the charge over-current detection circuit 21 is set to high level "H" when a charger is connected and is set to low level "L" when a charger is not connected.

The delay time reduction signal corresponding to an internal signal of the delay time reduction circuit 23 is set

to low level "L" when the delay time is being reduced and is set to high level "H" when the delay time is not reduced.

The over-discharge detection signal corresponding to an internal signal of the over-discharge detection circuit (VD2) 12 is set to high level "H" when over-discharge is detected and is set to low level "L" when over-discharge is not detected.

The over-discharge confirmation signal that is obtained from an internal signal of the over-discharge detection circuit (VD2) 12 is set to high level "H" after the elapse of the over-discharge detection delay time (second predetermined time: "tVdet2" of FIG. 4) from the time over-discharge is detected, and is set to low level "L" when over-discharge is not detected.

In the following, exemplary charger connection recovery control operations performed by the charger connection recovery circuit 26 are described with reference to FIGS. 2A-2C.

[FIG. 2A: overcharge undetected, over-discharge undetected, over-current undetected, charger not connected]

When no overcharge, over-discharge, or over-current is detected and a charger is not connected (i.e., normal operations mode), the charge control FET Q1 and the discharge control FET Q2 are both turned on. In this case, the charger connection signal is at "L" level since the charger is not

connected.

The delay time reduction signal is at "H" level since operations are not in test mode (delay time reduction mode). Accordingly, "H" level and "L" level inputs are supplied to NAND gate M1 so that an "H" level output is obtained at M1.

Since over-discharge is not detected in the present case, the over-discharge detection signal is at low level "L", and the "H" level output of M1 and the over-discharge detection signal at "L" level are input to NAND gate M2 so that an "H" level output is obtained at M2.

The "H" level output of M2 is input to inverter M3 so that an "L" level output is obtained at M3.

Since the over-discharge detection confirmation signal is at low level "L" when over-discharge is not detected, the "L" level output of M3 and the over-discharge detection confirmation signal at "L" level are input to EXNOR gate M4 so that an "H" level output is obtained at M4. The "H" level output of M4 is then input to a counter, and in this case, the counter is not activated. Thus, in normal operations mode, both the charge control FET Q1 and the discharge control FET Q2 are turned on.

[FIG. 2B: over-discharge detected and charger not connected]

When over-discharge is detected and a charger is

not connected, the charger connection signal is at "L" level since a charger is not connected and the delay time reduction signal is at "H" level since operations are not in test mode (delay time reduction mode). Accordingly, "L" level and "H" level inputs are supplied to NAND gate M1 so that an "H" level output is obtained at M1.

Since over-discharge is detected in the present case, the over-discharge detection signal is at "H" level. Accordingly, the "H" level output of M1 and the over-discharge detection signal at "H" level are input to NAND gate M2 so that an "L" level output is obtained at M2.

The "L" level output of M2 is input to inverter M3 so that an "H" level output is obtained at M3. The "H" level output of M3 and the over-discharge detection confirmation signal at "L" level are input to EXNOR gate M4 so that an "L" level output is obtained at M4. The "L" level output of M4 is input to the counter so that counting operations of the counter are activated. Then, after a predetermined time (over-discharge detection delay time) elapses from the time counting operations are started, the over-discharge detection confirmation signal is switched to "H" level. In turn, the output of M4 is switched to "H" level so that counting operations of the counter are stopped and the discharge control FET Q2 is turned off. In one embodiment, the over-discharge detection confirmation signal may be inverted after

the elapse of the predetermined time (over-discharge detection delay time) by inverting a flip flop that outputs the over-discharge detection confirmation signal at the time the counter counts to the predetermined time (over-discharge detection delay time).

[FIG. 2C: over-discharge detected and charger connected]

When over-discharge is detected and a charger is connected, the charger connection signal is set to "H" level and the delay time reduction signal is set to "H" level. The charger connection signal at "H" level and the delay time reduction signal at "H" level are input to NAND gate M1 so that an "L" level output is obtained at M1.

Since over-discharge is detected in the present case, the over-discharge detection signal is set to "H" level. Accordingly the "L" level output of M1 and the over-discharge detection signal at "H" level are input to NAND gate M2 so that an "H" level output is obtained at M2. The "H" level output of M2 is input to inverter M3 so that an "L" level output is obtained at M3.

Since over-discharge is detected in the present case, the over-discharge detection confirmation signal is set to "H" level. Accordingly, the "L" level output of M3 and the over-discharge detection confirmation signal at "H" level are input to EXNOR gate M4 so that an "L" level output is obtained

at M4. The "L" level output of M4 is input to the counter so that counting operations of the counter are activated. Then, after a first predetermined time (over-discharge recovery delay time) elapses from the time counting operations are started, the discharge control FET Q2 may be forcefully turned on. In one embodiment, the over-discharge detection confirmation signal may be inverted after the elapse of the first predetermined time (over-discharge recovery delay time) by inverting a flip flop that outputs the over-discharge detection confirmation signal at the time the counter counts to the first predetermined time (over-discharge recovery time).

It is noted that in the case where the battery cell voltage is less than or equal to the over-discharge detection voltage, the discharge control FET Q2 is turned off after the elapse of the over-discharge detection delay time. However, when the charger is connected as in the example described above, the discharge control FET Q2 is forcefully turned on after the elapse of the over-discharge recovery delay time.

Thus, when a charger is connected at the time the battery cell voltage is less than or equal to the over-discharge detection voltage, pulse charge operations are performed by repeating the operations of turning off the discharge control FET Q2 after the elapse of the over-discharge detection delay time and turning on the discharge control FET Q2 after the elapse of the over-discharge recovery

delay time. It is noted that the pulse width of the charge pulse may be adjusted by changing the over-discharge detection delay time and the over-discharge recovery delay time according to variations in temperature characteristics of the internal circuits, the charger and the IC, for example.

FIG. 4 is a timing chart illustrating charge operations performed when a charger is connected.

As is shown in FIG. 4, when the level of Vdd is higher than the over-discharge detection voltage (Vdet2) but lower than an overcharge detection voltage, the output of Dout is set to "H" level. When the output of Dout is at "H" level, the discharge control FET Q2 that is connected to Dout is turned on so that charge/discharge operations are enabled.

When the level of Vdd falls to the over-discharge detection voltage (Vdet2) or lower, the internal counter 17 counts to the over-discharge detection delay time (tVdet2) after which the output of Dout is switched to "L" level. When the output of Dout is switched to "L" level, the discharge control FET Q2 that is connected to Dout is turned off so that discharge operations are disabled. When the charger is not connected at the time over-discharge is detected, the level of the V- terminal is raised to equal the level of Vdd by the internal circuits.

When the charger is connected under such conditions, the V- terminal temporarily falls to a charge over-current

detection voltage (Vdet4) or lower. When the charge over-current (Vdet4) is detected, recovery from the over-discharge detection status to dischargeable status may be enabled by the charge over-current detection signal, the delay time reduction signal, the over-discharge detection signal, and the over-discharge detection confirmation signal, for example.

In this case, the discharge control FET Q2 is turned on after the elapse of the over-discharge recovery delay time (tVrel2). When the level of Vdd does not rise above the over-discharge detection voltage (Vdet2) even after the elapse of the over-discharge detection delay time (tVdet2), the discharge control FET Q2 is turned off (Dout is switched to "L" level) after the elapse of the over-discharge detection delay time (tVdet2).

When the charger is connected at the time Dout is switched to "L" level, the above-described on/off operations of the discharge control FET Q2 may be repeated. Thus, the discharge control FET Q2 is turned back on after the elapse of the over-discharge recovery delay time (tVrel2).

By repeating the above described on/off operations, pulse charge operations controlled by the over-discharge recovery delay time (tVrel2) and the over-discharge detection delay time (tVdet2) are performed until the level of Vdd rises above the over-discharge detection voltage.

It is noted that according to an exemplary charge

operation scheme, initial charge operations may be started in response to the connection of a charger. Then, the battery cell voltage may be checked by temporarily halting the charge operations (see "halt charge" of FIG. 4), and the charge operations may be resumed after the battery cell voltage is checked.

However, when the level of Vdd is less than or equal to the over-discharge detection voltage (Vdet2) so that the discharge control FET Q2 is turned off and charge operations are not performed, it may not be possible to monitor the battery cell voltage.

Thus, according to an embodiment of the present invention, the discharge control FET Q2 that is turned off may be forcefully turned on after the elapse of a first predetermined time (over-discharge recovery delay time "tVrel2") so that the battery cell voltage may be monitored. In one preferred embodiment, the first predetermined time may be determined based on variations in internal circuit temperature characteristics, charger temperature characteristics, over-discharge recovery delay time temperature characteristics, and over-discharge detection delay time temperature characteristic, for example.

It is noted that embodiments of the present invention may be widely used in a variety of applications. For example, a charge/discharge protection circuit according

to an embodiment of the present invention may be embedded in a battery pack, and the battery pack may be installed in various types of electronic apparatuses such as a mobile phone, a portable game apparatus, a digital camera, or a portable audio apparatus.

In the following, another exemplary method for controlling on/off operations of the discharge control FET Q2 is described. In this example, a charger connection detection terminal for detecting connection of a charger is provided to enable charger connection recovery control operations. FIGS. 3A-3C are diagrams illustrating operations for controlling the discharge control FET Q2 under various conditions in the present example where such a charger connection detection terminal for detecting connection of a charger is used.

[FIG. 3A: over-discharge undetected, charger not connected]

The charger connection signal may normally be at "L" level, and may be switched to "H" level when a signal from a battery pack positive (+) side of a charger is input and the charger is connected. In this case, when a source voltage is below an overcharge detection level and above an over-discharge detection level, a non-over-discharge detection signal that is set to "H" level when over-discharge is not detected and is set to "L" level when over-discharge is detected may be at "H" level.

When a charger is not connected, the charger connection signal is set to "L" level so that an "L" level output is obtained at NAND gate M1. The "L" level output of M1 is input to inverter M2 so that an "L" level output is obtained at M2. When the output of M2 is at "L" level, the discharge control FET Q2 corresponding to an N-channel FET may be turned on.

[FIG. 3B: over-discharge detected and charger unconnected]

When over-discharge is detected, the non-over-discharge detection signal at "L" level is output, and when a charger is not connected, the charger connection signal at "L" level is output. The above "L" level outputs are input to NAND gate M1 so that an "H" level output may be obtained at M1. The "H" level output of M1 is input to inverter M2 so that an "L" level output may be obtained at M2. When the output of M2 is at "L" level the discharge control FET Q2 is turned off.

[FIG. 3C: over-discharge detected and charger connected]

When a charger is connected at the time over-discharge is detected, the non-over-discharge detection signal at "L" level is output and the charger connection signal at "H" level is output. The above "L" level output and "H" level output are input to NAND gate M1 so that an "L" level output is obtained at M1. The "L" level output of M1 is input to

inverter M2 so that an "H" level output is obtained at M2. When the output of M2 is at "H" level, the discharge control FET is turned on.

In the following, exemplary advantages that may be realized by embodiments of the present invention are described.

According to one aspect of the present invention, a charge/discharge protection circuit with low current consumption and a relatively small chip size that is capable of preventing degradation of a discharge control FET when a charger is connected and reducing a battery charge time may be provided.

Specifically, in a charge/discharge protection circuit according to an embodiment of the present invention, even when a battery cell voltage is less than or equal to an over-discharge detection voltage so that the discharge control FET is turned off, the discharge control FET may be forcefully turned on when a charger is connected. It is noted that in a conventional charge/discharge protection circuit, when a charger is connected to perform charge operations at the time a discharge control FET is turned off, first, charge operations are performed using a parasitic diode of the discharge control FET. However, when such a parasitic diode is used in the charge operations, the discharge control FET may be prone to degradation. In view of such a problem in the conventional charge/discharge protection circuit, a

charge/discharge protection circuit according to an embodiment of the present invention controls the discharge control FET to be forcefully turned on when a charger is connected at the time the discharge control FET is turned off to thereby prevent degradation of the discharge control FET and enable efficient charge operations in a short period of time, for example. Also, a charge/discharge protection circuit according to one preferred embodiment of the present invention does not have to include an additional terminal for detecting connection of a charger so that an increase in current consumption and chip size may be prevented, for example.

According to another aspect of the present invention, the charge/discharge protection circuit according to an embodiment of the present invention may be embedded in a battery pack that is widely used in a variety of electronic apparatuses such as a mobile phone, a portable game apparatus, a digital camera, and a portable audio apparatus.

Although the present invention is shown and described with respect to certain preferred embodiments, it is obvious that equivalents and modifications will occur to others skilled in the art upon reading and understanding the specification. The present invention includes all such equivalents and modifications, and is limited only by the scope of the claims.

The present application is based on and claims the

benefit of the earlier filing date of Japanese Patent Application No. 2006-153848 filed on June 1, 2006, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A charge/discharge protection circuit that protects a secondary battery from overcharge, over-discharge, charge over-current, and discharge over-current, said charge/discharge protection circuit comprising:

an overcharge detection circuit;

an over-discharge detection circuit;

a charge over-current detection circuit;

a discharge over-current detection circuit;

a charge control FET that is turned off when overcharge is detected by the overcharge detection circuit and when charge over-current is detected by the charge over-current detection circuit;

a discharge control FET that is turned off when over-discharge is detected by the over-discharge detection circuit and when discharge over-current is detected by the discharge over-current detection circuit; and

a charger connection recovery circuit that controls on/off operations of the discharge control FET such that when connection with a charger is established at a time over-discharge is detected and the discharge control FET is turned off, the discharge control FET is forcefully turned on after a first predetermined time elapses.

2. The charge/discharge protection circuit as claimed in claim 1, wherein

the discharge control FET is turned off after a second predetermined time elapses from the time the discharge control FET is forcefully turned on.

3. The charge/discharge protection circuit as claimed in claim 2, wherein

when a battery cell voltage is less than or equal to an over-discharge detection voltage, operations of turning on the discharge control FET after the elapse of the first predetermined time and turning off the discharge control FET after the elapse of the second predetermined time are repeated.

4. The charge/discharge protection circuit as claimed in claim 2, wherein

the first predetermined time and the second predetermined time are determined according to variations in internal circuit temperature characteristics, charger temperature characteristics, over-discharge recovery delay time temperature characteristics, and over-discharge detection delay time temperature characteristics..

5. A battery pack comprising the charge/discharge protection circuit as claimed in any one of claims 1 through 4.

6. An electronic apparatus comprising the battery pack as claimed in claim 5.

7. A mobile phone comprising the battery pack as claimed in claim 5.

8. A portable game apparatus comprising the battery pack as claimed in claim 5.

9. A digital camera comprising the battery pack as claimed in claim 5.

10. A portable audio apparatus comprising the battery pack as claimed in claim 5.

FIG.1

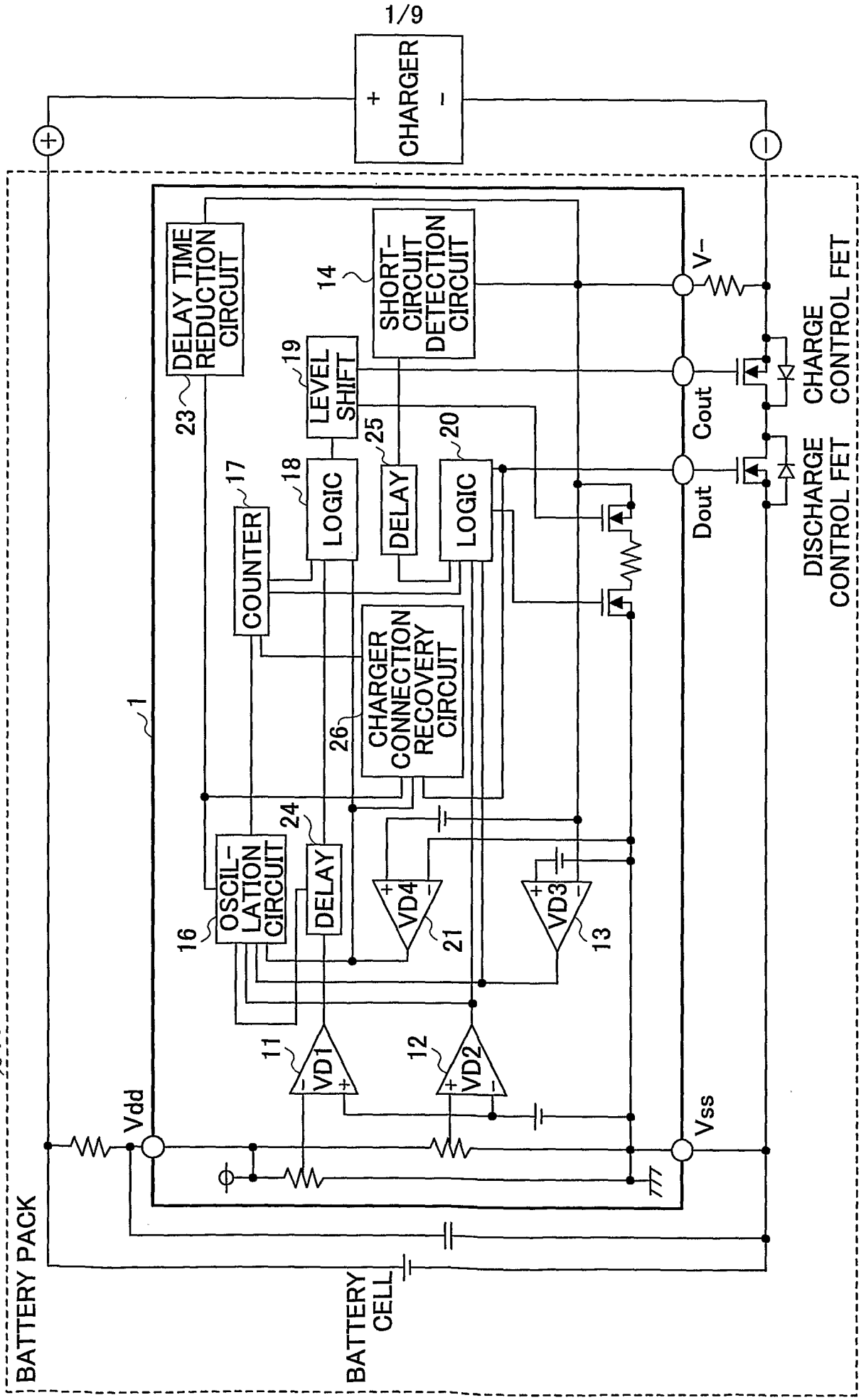

CHARGER
+
-
BATTERY PACK
A
BATTERY CELL
Vdd
Vss
V-
Cout
Dout
DISCHARGE CONTROL FET
CHARGE CONTROL FET
1
DELAY TIME REDUCTION CIRCUIT
23
SHORT-CIRCUIT DETECTION CIRCUIT
14
LEVEL SHIFT
19
COUNTER
17
LOGIC
18
DELAY
25
LOGIC
20
CHARGER CONNECTION RECOVERY CIRCUIT
26
OSCIL-LATION CIRCUIT
16
DELAY
24
VD1
11
VD2
12
VD3
13
VD4
21

FIG.2A

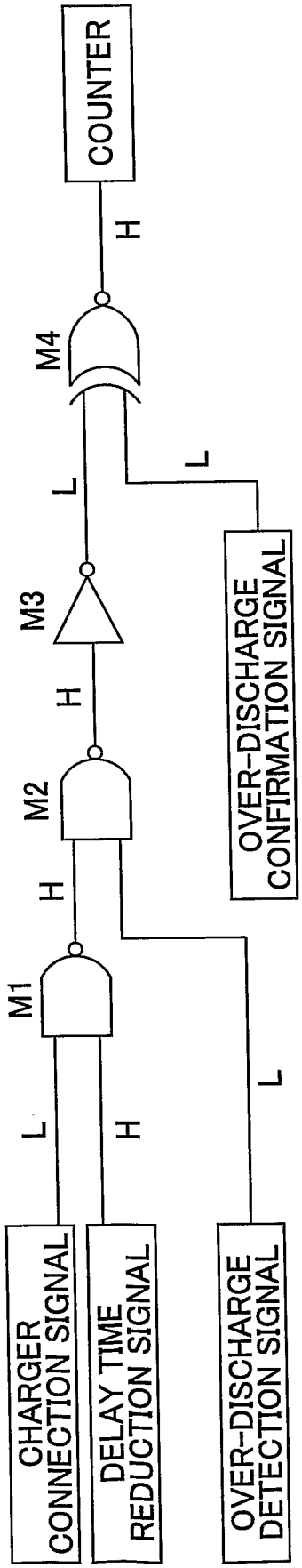

COUNTER
H
M4
L
L
M3
H
M2
H
M1
L
H
L
CHARGER CONNECTION SIGNAL
DELAY TIME REDUCTION SIGNAL
OVER-DISCHARGE DETECTION SIGNAL
OVER-DISCHARGE CONFIRMATION SIGNAL

FIG.2B

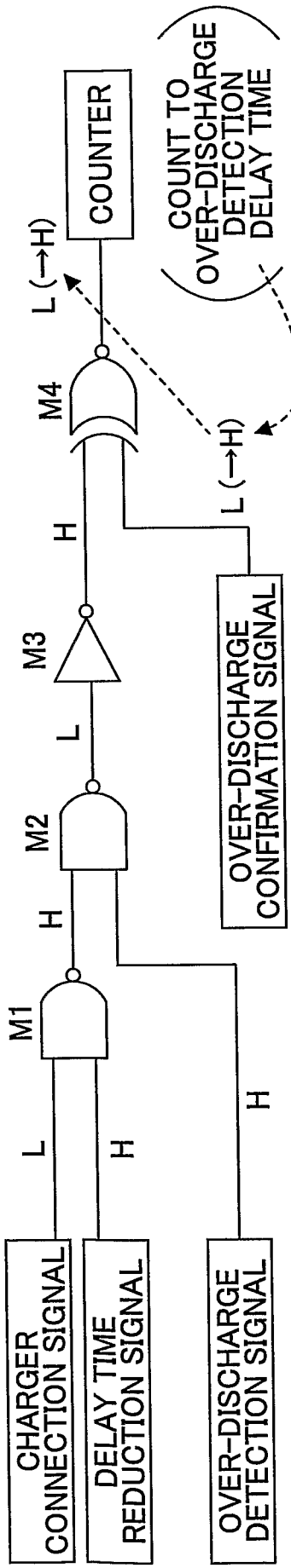

CHARGER CONNECTION SIGNAL
DELAY TIME REDUCTION SIGNAL
OVER-DISCHARGE DETECTION SIGNAL
OVER-DISCHARGE CONFIRMATION SIGNAL
COUNTER
COUNT TO OVER-DISCHARGE DETECTION DELAY TIME
M1
M2
M3
M4
L
H
H
L
H
L
H
L (→H)
L (→H)

FIG.2C

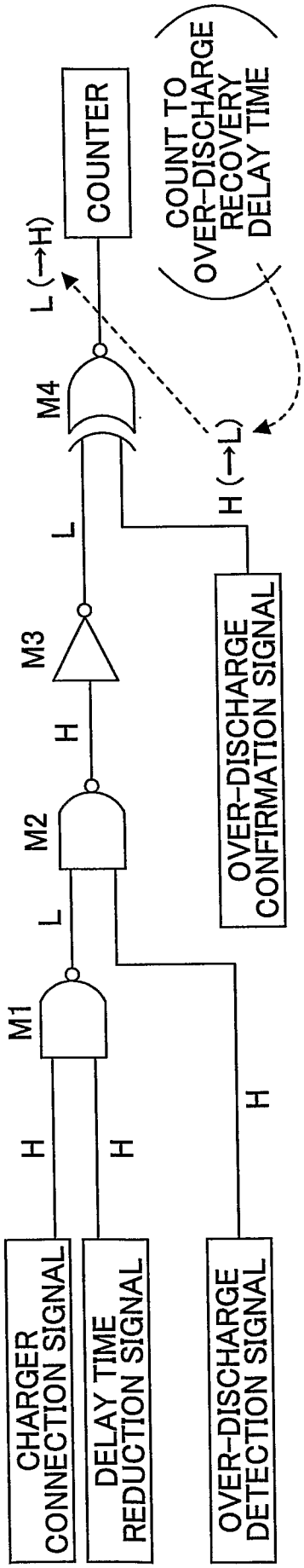

CHARGER CONNECTION SIGNAL
DELAY TIME REDUCTION SIGNAL
OVER-DISCHARGE DETECTION SIGNAL
H
H
H
M1
L
M2
H
M3
L
M4
L (→H)
H (→L)
COUNTER
COUNT TO OVER-DISCHARGE RECOVERY DELAY TIME
OVER-DISCHARGE CONFIRMATION SIGNAL

FIG.3A

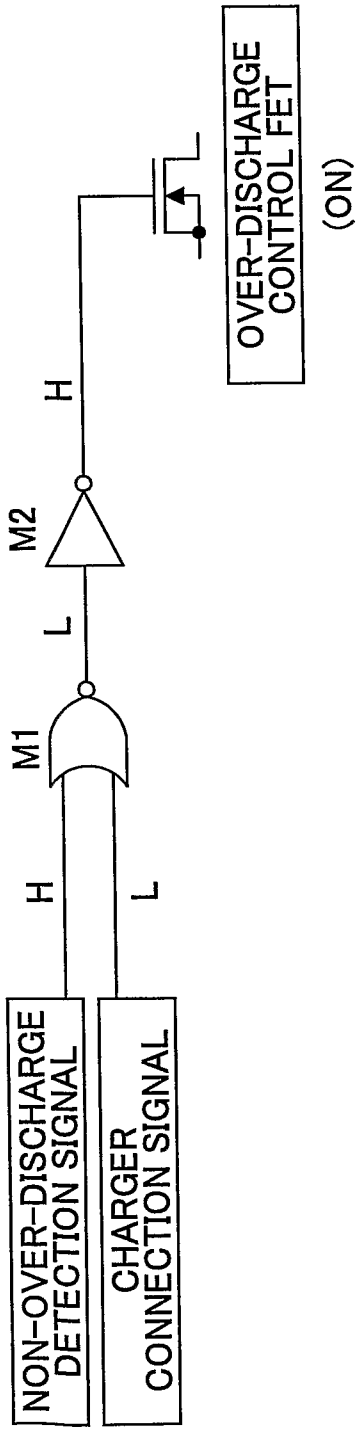

NON-OVER-DISCHARGE DETECTION SIGNAL
CHARGER CONNECTION SIGNAL
H
L
M1
L
M2
H
L
OVER-DISCHARGE CONTROL FET
(ON)

FIG.3B

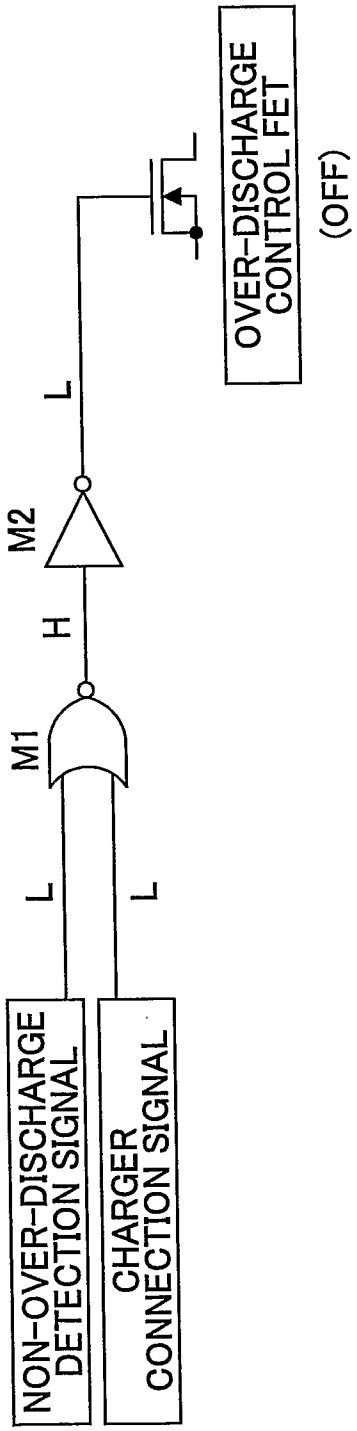
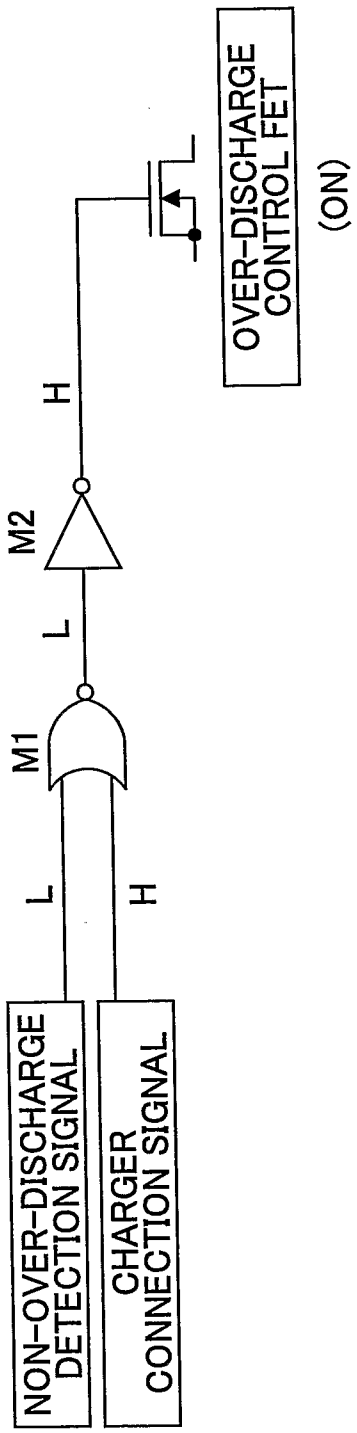

NON-OVER-DISCHARGE DETECTION SIGNAL
CHARGER CONNECTION SIGNAL
L
L
M1
H
M2
L
OVER-DISCHARGE CONTROL FET
(OFF)

FIG.3C


NON-OVER-DISCHARGE DETECTION SIGNAL
CHARGER CONNECTION SIGNAL
L
H
M1
L
M2
H
OVER-DISCHARGE CONTROL FET
(ON)

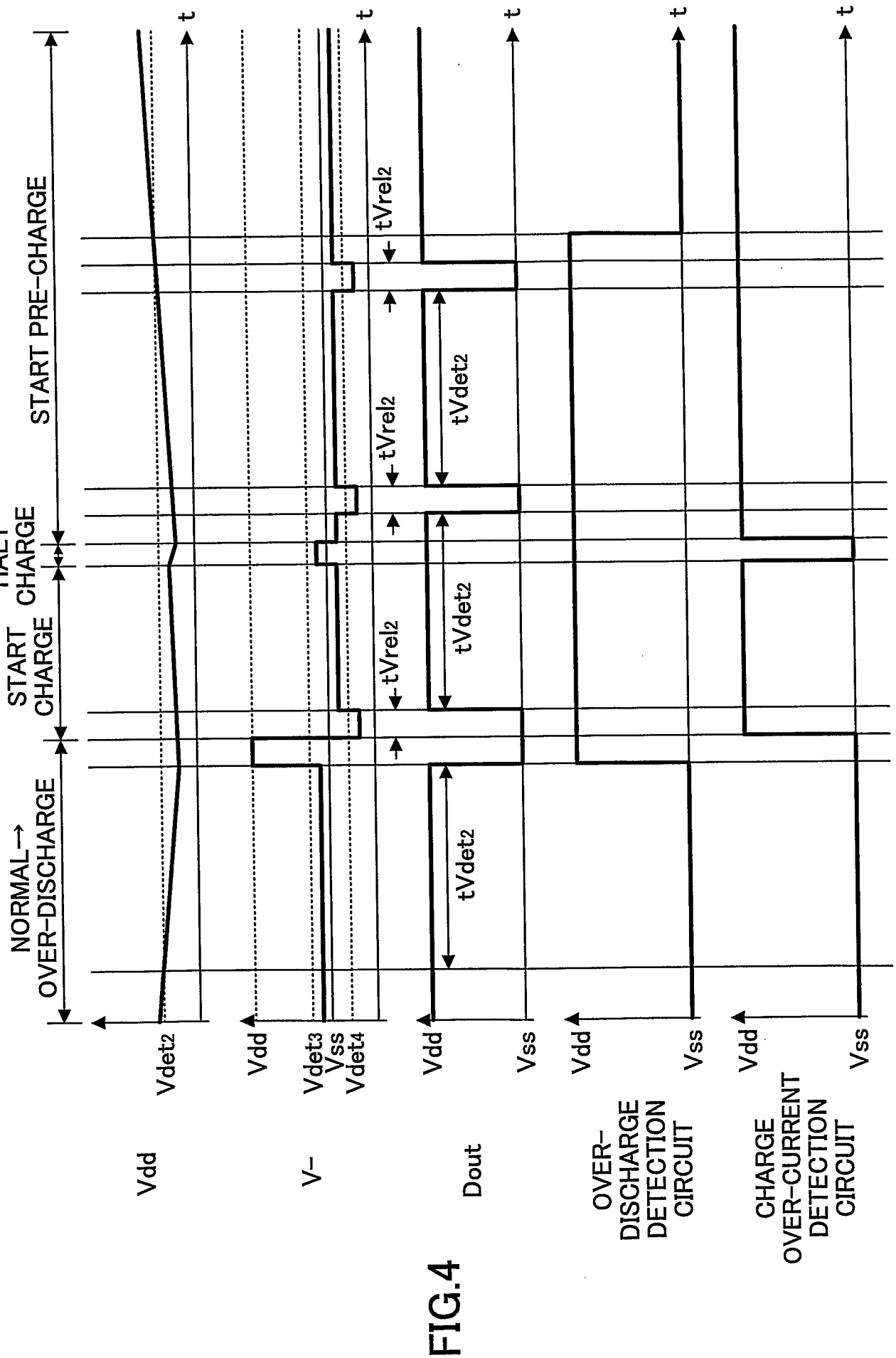
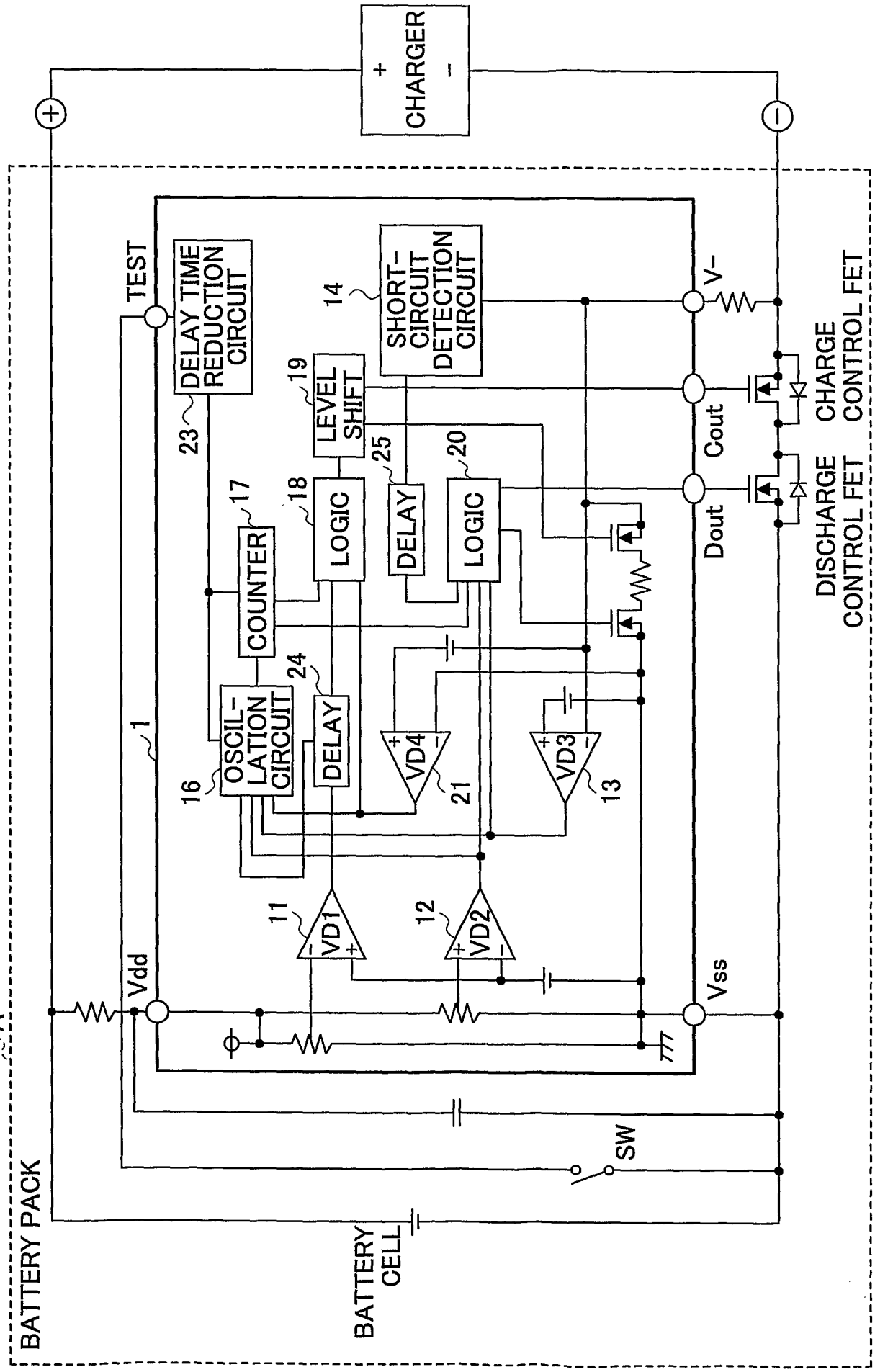

NORMAL→
OVER-DISCHARGE
START
CHARGE
HALT
CHARGE
START PRE-CHARGE
tVrel2
tVdet2
Vdet2
Vdd
Vdet3
Vss
Vdet4
Vss
Vdd
Vss
Vdd
Vss
Vdd
Vss
t
Vdd
V-
Dout
OVER-
DISCHARGE
DETECTION
CIRCUIT
CHARGE
OVER-CURRENT
DETECTION
CIRCUIT

FIG.4

FIG.5 PRIOR ART



INTERNATIONALSEARCHREPORT

International application No.
PCT/JP2007/060319

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H02J7/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H02J7/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2007
Registered utility model specifications of Japan 1996-2007
Published registered utility model applications of Japan 1994-2007

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	JP 2002-176730 A (RICOH COMPANY, LTD.) 2002.06.21, Par. No. [0012]; Fig. 1 & US 2002/0050806 A1 & US 2003/0141847 A1	1,5-10 2-4
Y A	JP 10-285810 A (Seiko Instruments Inc.) 1998.10.23, Par. Nos. [0006], [0011] to [0016], [0021] to [0024]; Figs. 1 to 7 (Family: none)	1,5-10 2-4
A	JP 11-215716 A (Matsushita Electric Industrial Co., Ltd.) 1999.08.06, Par. Nos. [0076] to [0081]; Figs. 1, 5(b) (Family: none)	1-10

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31.05.2007	12.06.2007

Name and mailing address of the ISA/JP	Authorized officer
Japan Patent Office 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	Shin-ichi Yajima 5T 9060 Telephone No. +81-3-3581-1101 Ext. 3568

Form PCT/ISA/210 (second sheet) (April 2005)