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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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(54) **Title**: INTEGRATED CIRCUIT WITH ZERO TEMPERATURE COEFFICIENT CAPACITOR

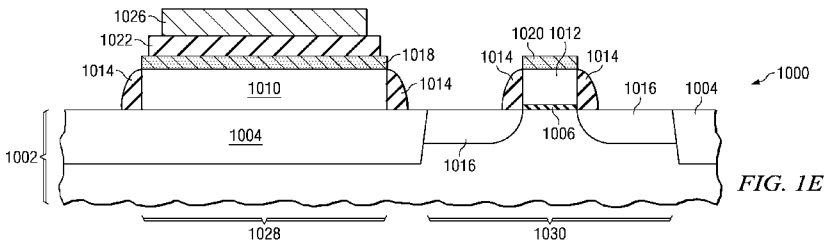

FIG. 1E

(57) **Abstract**: An integrated circuit (1000) has a zero temperature coefficient (ZTC) capacitor formed together with a metal oxide semiconductor (MOS) transistor. The capacitor has a capacitor lower plate (1010) formed in a same layer with a MOS electrode (1012), a capacitor dielectric layer (1022) implanted to have a phosphorus density of $1.7\chi\ 10^{20}$ to $2.3\chi\ 10^{20}$ atoms/cm3, and a capacitor upper plate (1026).

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INTEGRATED CIRCUIT WITH ZERO TEMPERATURE COEFFICIENT CAPACITOR

[0001] This invention relates to the field of electronic capacitors.

BACKGROUND

[0002] Electronic capacitors may operate over a range of temperatures. It may be desirable to form a capacitor which exhibits substantially constant capacitance over an operational temperature range.

SUMMARY

[0003] A zero temperature coefficient (ZTC) capacitor may be formed by forming a silicon dioxide capacitor dielectric layer, followed by placing phosphorus into the dielectric layer to obtain a phosphorus density between 1.7×10^{20} atoms/cm^3 and 2.3×10^{20} atoms/cm^3. The phosphorus may be ion implanted, provided from a diffusion source, or provided by other means. A temperature coefficient of the ZTC capacitor may be between -1 parts per million per degree Centigrade (ppm/°C) and 1 ppm/°C. The ZTC capacitor may be formed as part of an integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIGS. 1A through 1H are cross-sectional views of an integrated circuit having ZTC capacitors formed according to embodiments, depicted in successive stages of fabrication.

[0005] FIG. 2 is a chart of measured temperature coefficients of capacitors as a function of phosphorus density in dielectric layers of the capacitors.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0006] A zero temperature coefficient (ZTC) capacitor may include a lower conducting plate, a capacitor dielectric layer and an upper conducting plate. A

capacitance of the ZTC capacitor may vary over a temperature range. A temperature coefficient K_T of the ZTC capacitor may be estimated by fitting measured capacitance values of the ZTC capacitor at more than one temperature in the temperature range to the expression of Equation 1:

$$C(T) = C(T_{REF}) \times [\, 1 + (K_T \times (T - T_{REF})]] \; ; \qquad \text{Equation 1}$$

wherein C (T) is a capacitance value at a temperature T, and T_{REF} is a reference temperature, for example 27 °C.

[0007] Phosphorus may be placed into the capacitor dielectric layer to obtain a phosphorus atom density between 1.7×10^{20} atoms/cm^3 and 2.3×10^{20} atoms/cm^3. Work performed in association with the instant invention indicate the temperature coefficient K_T of the ZTC capacitor may be between -1 ppm/°C and 1 ppm/°C.

[0008] The ZTC capacitor may be formed as part of an integrated circuit. In one embodiment, the bottom plate may include gate material used to form a gate of a metal oxide semiconductor (MOS) transistor in the integrated circuit. In another embodiment, the bottom plate may include metal used to form interconnects in the integrated circuit.

[0009] For the purposes of this description, terms describing elemental formulas of materials without subscripts do not imply a particular stoichiometry of the elements. For example, the term TiSiN describes a material containing titanium (Ti), silicon (Si) and nitrogen (N), not necessarily having a Ti:Si:N atomic ratio of 1:1:1. Terms describing elemental formulas of materials with subscripts imply a stoichiometry given by the subscripts. For example, the term SiO_2 describes a material containing silicon and oxygen (O) having a Si:O atomic ratio substantially equal to 1:2.

[0010] In some instances of integrated circuits containing a ZTC capacitor, substantially the entire integrated circuit is dedicated to the ZTC capacitor. In other instances of integrated circuits containing a ZTC capacitor, such as analog integrated circuits, the integrated circuits may contain another active component such as a metal oxide semiconductor (MOS) transistor.

[0011] FIGS. 1A-1H illustrate an integrated circuit containing ZTC capacitors formed according to embodiments, depicted in successive stages of fabrication.

[0012] Referring to FIG. 1A, the integrated circuit 1000 is formed in and on a substrate 1002, which may be a single crystal silicon wafer, but may be a silicon-on-

insulator (SOI) wafer, a hybrid orientation technology (HOT) wafer with regions of different crystal orientations, a semiconductor wafer of another material such as gallium arsenide, or other material appropriate for fabrication of the IC 1000. In one realization of the instant embodiment, the substrate 1002 may include an electrically insulating layer such as ceramic, crystalline aluminum oxide, glass, plastic or other non-conducting material.

[0013] One or more elements of field oxide 1004 may be formed at a top surface of the substrate 1002, for example of silicon dioxide between 250 and 600 nanometers thick. The field oxide elements 1004 may be formed by shallow trench isolation (STI) or local oxidation of silicon (LOCOS) processes. In STI processes, silicon dioxide may be deposited by high density plasma (HDP) or high aspect ratio process (HARP). In one realization of the instant embodiment, a gate dielectric layer 1006 for a MOS transistor may be formed at the top surface of the substrate 1002.

[0014] A first electrically conducting layer 1008 is formed on the substrate 1002, possibly contacting the field oxide elements 1004 if present and possibly contacting the gate dielectric layer 1006 if present. In a realization of the instant embodiment which includes a MOS transistor in the integrated circuit 1000, the first electrically conducting layer 1008 may include material such as polycrystalline silicon for forming a gate of the MOS transistor.

[0015] Referring to FIG. 1B, the first electrically conducting layer 1008 of FIG. 1A is patterned and etched to form a first capacitor lower plate 1010. In a realization of the instant embodiment which includes a MOS transistor in the integrated circuit 1000, a MOS gate 1012 may be formed from the first electrically conducting layer 1008 of FIG. 1A, concurrently with the first capacitor lower plate 1010.

[0016] Referring to FIG. 1C, sidewall spacers 1014 may be formed, for example of silicon nitride or layers of silicon nitride and silicon dioxide, on lateral surfaces of the first capacitor lower plate 1010, and on lateral surfaces of the MOS gate 1012 if formed. In a realization of the instant embodiment which includes a MOS transistor in the integrated circuit 1000, source and drain regions 1016 may be formed in the substrate 1002 adjacent to the MOS gate 1012. In realizations of the instant embodiment in which the first capacitor lower plate 1010 includes polycrystalline silicon, an optional metal

silicide layer 1018 may be formed at a top surface of the first capacitor lower plate 1010. In a realization of the instant embodiment which includes a MOS transistor in the integrated circuit 1000, a metal silicide layer 1020 may be formed at a top surface of the MOS gate 1012. The metal silicide layers 1018 and 1020 if present may be formed by depositing a layer of metal, such as nickel, cobalt or titanium, on a top surface of the integrated circuit 1000, heating the integrated circuit 1000 to react a portion of the metal with exposed polycrystalline silicon, and selectively removing unreacted metal from the integrated circuit 1000 surface, for example by exposing the integrated circuit 1000 to wet etchants including a mixture of an acid and hydrogen peroxide.

[0017] Referring to FIG. 1D, a first capacitor dielectric layer 1022 is formed on the integrated circuit 1000. The first capacitor dielectric layer 1022 is composed of silicon dioxide, possibly including other elements such as carbon or fluorine. A total density of atoms in the first capacitor dielectric layer 1022 other than silicon and oxygen is less than 1×10^{18} atoms/cm^3. The first capacitor dielectric layer 1022 may be between 10 and 200 nanometers thick. In one realization of the instant embodiment, the first capacitor dielectric layer 1022 may be between 45 and 55 nanometers thick. The first capacitor dielectric layer 1022 may be formed by chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), atmospheric pressure chemical vapor deposition (APCVD), high density plasma (HDP), an ozone based thermal chemical vapor deposition (CVD) process, also known as the high aspect ratio process (HARP), or other suitable silicon dioxide layer formation process deposition. The first capacitor dielectric layer 1022 may be formed by decomposition of tetraethyl orthosilicate, also known as tetraethoxysilane or TEOS, or deposition of methylsilsesquioxane (MSQ).

[0018] A first phosphorus placement process 1024 is performed which places phosphorus atoms in the first capacitor dielectric layer 1022. The first phosphorus placement process 1024 is adjusted to provide an average density of phosphorus atoms in the first capacitor dielectric layer 1022 of 1.7×10^{20} to 2.3×10^{20} atoms/cm^3. For example, in a realization of the instant embodiment in which the first capacitor dielectric layer 1022 is 50 nanometers thick, the first phosphorus placement process 1024 is performed to provide a dose between 8.5×10^{14} atoms/cm^2 and 1.15×10^{14} atoms/cm^2. In one realization

of the instant embodiment, the first phosphorus placement process 1024 may be an ion implantation process; an implantation energy of the first phosphorus placement process 1024 may be adjusted to place a peak of a distribution of the implanted phosphorus atoms approximately in a center of the first capacitor dielectric layer 1022. For example, in a realization of the instant embodiment in which the first capacitor dielectric layer 1022 is 50 nanometers thick, the implantation energy of the first phosphorus placement process 1024 may be set between 10 and 20 kiloelectron-volts (keV). In an alternate realization of the instant embodiment, the first phosphorus placement process 1024 may include exposing the integrated circuit 1000 to a phosphorus containing gas at a temperature above 300 C. In another realization, the first phosphorus placement process 1024 may include exposing the integrated circuit 1000 to a phosphorus containing plasma. In a further realization, phosphorus may be placed in the first capacitor dielectric layer 1022 by other means.

[0019] Referring to FIG. 1E, the first capacitor dielectric layer 1022 may optionally be patterned and etched to form a boundary proximate to a boundary of the first capacitor lower plate 1010, as depicted in FIG. 1E. A first capacitor upper plate 1026 is formed on the first capacitor dielectric layer 1022. The first capacitor upper plate 1026 is formed of electrically conducting material, such as metal or doped semiconductor material. In one realization of the instant embodiment, the first capacitor upper plate 1026 may include Ti, TiN, TiSiN, Ta, TaN, TaSiN, W, WN, WSiN, or any combination thereof, between 50 and 400 nanometers thick. In another realization, the first capacitor upper plate 1026 may include aluminum, copper, gold or other metal used for interconnects in the integrated circuit 1000, between 50 and 500 nanometers thick.

[0020] The first capacitor lower plate 1010, the first capacitor dielectric layer 1022 with a phosphorus density between 1.7×10^{20} atoms/cm^3 and 2.3×10^{20} atoms/cm^3 and the first capacitor upper plate 1026 form a first ZTC capacitor 1028. The gate dielectric layer 1006, MOS gate 1012 and source and drain regions 1016, if present, are part of a MOS transistor 1030 formed in and on the substrate 1002.

[0021] A second ZTC capacitor may be formed in the integrated circuit 1000 in an interconnect region above the substrate 1002, as described in reference to FIG. 1F through FIG. 1H. Referring to FIG. 1F, a first interconnect dielectric layer 1032 is

formed on the integrated circuit 1000. The first interconnect dielectric layer 1032 may include one or more layers of silicon dioxide, silicon nitride, organo-silicate glass (OSG), carbon-doped silicon oxides (SiCO or CDO), fluorosilicate glass (FSG), or other dielectric material. The first interconnect dielectric layer 1032 may include one or more layers of metal interconnect elements such as metal lines of aluminum, copper and/or gold, and vias of aluminum, copper, gold, and/or tungsten. Metal interconnect elements in the first interconnect dielectric layer 1032 are not shown in FIG. 1F.

[0022] A second capacitor lower plate 1034 is formed on the first interconnect dielectric layer 1032. The second capacitor lower plate 1034 is formed of electrically conductive material, such as metal or doped semiconductor material. An optional metal interconnect line 1036 may be formed on the first interconnect dielectric layer 1032. In one realization of the instant embodiment, the second capacitor lower plate 1034 may be formed concurrently with the metal interconnect line 1036. The second capacitor lower plate 1034 and metal interconnect line 1036 if formed may include aluminum, copper and/or gold.

[0023] Referring to FIG. 1G, a second capacitor dielectric layer 1038 is formed on the integrated circuit 1000 as described in reference to FIG. 1D. Material properties and possible formation processes of the second capacitor dielectric layer 1038 are as described in reference to FIG. 1D. In one realization of the instant embodiment, a thickness of the second capacitor dielectric layer 1038 may be different from the thickness of the first capacitor dielectric layer 1022. In an alternate realization, the thickness of the second capacitor dielectric layer 1038 may substantially equal to the thickness of the first capacitor dielectric layer 1022. In one realization of the instant embodiment, the formation process of the second capacitor dielectric layer 1038 may use process parameters different from those of the first capacitor dielectric layer 1022.

[0024] A second phosphorus placement process 1040 is performed which places phosphorus atoms into the second capacitor dielectric layer 1038. The second phosphorus placement process 1040 is adjusted to provide a phosphorus density as described in reference to FIG. 1D. In one realization of the instant embodiment, the second phosphorus placement process 1040 may be an ion implantation process, as described in reference to FIG. 1D. In an alternate realization, the second phosphorus

placement process 1040 may be a diffusion process from a phosphorus containing gas as described in reference to FIG. 1D. In another realization, the second phosphorus placement process 1040 may be include exposure to a phosphorus containing plasma, as described in reference to FIG. 1D. In a further realization, the phosphorus may be placed in the second capacitor dielectric layer 1038 by other means.

[0025] Referring to FIG. 1H, the second capacitor dielectric layer 1038 may optionally be patterned and etched to form a boundary proximate to a boundary of the second capacitor lower plate 1034, as depicted in FIG. 1H. A second capacitor upper plate 1042 is formed on the second capacitor dielectric layer 1038. The second capacitor upper plate 1042 is formed of electrically conductive material such as metal or doped semiconductor material. In one realization of the instant embodiment, the second capacitor upper plate 1042 may include Ti, TiN, TiSiN, Ta, TaN, TaSiN, W, WN, WSiN, or any combination thereof, between 50 and 400 nanometers thick. In another realization, the second capacitor upper plate 1042 may include aluminum, copper, gold or other metal used for interconnects in the integrated circuit 1000, between 100 and 2000 nanometers thick.

[0026] The second capacitor lower plate 1034, the second capacitor dielectric layer 1038 with a phosphorus density between 1.7×10^{20} atoms/cm^3 and 2.3×10^{20} atoms/cm^3 and the second capacitor upper plate 1042 form a second ZTC capacitor 1044.

[0027] An optional second interconnect dielectric layer 1046 may be formed over the second ZTC capacitor 1044. The second interconnect dielectric layer 1046 if formed may include materials described in reference to the first interconnect dielectric layer 1032. The second interconnect dielectric layer 1046 may include one or more layers of metal interconnect elements such as metal lines of aluminum, copper and/or gold, and vias of aluminum, copper, gold, and/or tungsten. Metal interconnect elements are not shown in FIG. 1H.

[0028] In one realization of the instant embodiment, the integrated circuit 1000 may include only the first ZTC capacitor 1028 and not the second ZTC capacitor 1044. In another realization of the instant embodiment, the integrated circuit 1000 may include both the first ZTC capacitor 1028 and the second ZTC capacitor 1044. In an alternate embodiment, an integrated circuit may contain only an instance of a ZTC capacitor

formed above an interconnect dielectric layer, as described in reference to the second ZTC capacitor 1044 of FIG. 1H.

[0029] FIG. 2 is a chart of measured temperature coefficients of capacitors as a function of phosphorus density in dielectric layers of the capacitors. Data in FIG. 2 are from work performed in association with the instant invention, using a capacitor dielectric layer approximately 50 nanometers thick, and ion implanted with phosphorus at an ion implant energy of 16 keV. It will be recognized by one familiar with fabricating capacitors, having reference to the data shown in FIG. 2, that providing a phosphorus density between 1.7×10^{20} atoms/cm^3 and 2.3×10^{20} atoms/cm^3 may provide a temperature coefficient between -1 ppm/°C and 1 ppm/°C.

[0030] Those skilled in the art to which the invention relates will appreciate that modifications may be made to the described example embodiments, and other embodiments realizes, within the scope of the claimed invention.

What is claimed is:

1. A capacitor, comprising:

a capacitor lower plate, the capacitor lower plate including electrically conductive material;

a capacitor dielectric layer of silicon dioxide formed over the capacitor lower plate, the capacitor dielectric layer having a phosphorus density of 1.7×10^{20} to 2.3×10^{20} atoms/cm^3, such that a total density of atoms in the capacitor dielectric layer other than phosphorus, silicon and oxygen is less than 1×10^{18} atoms/cm^3; and

a capacitor upper plate formed over the capacitor dielectric layer, the capacitor upper plate including electrically conductive material.

2. The capacitor of claim 1, wherein the capacitor dielectric layer is between 45 and 55 nanometers thick.

3. The capacitor of claim 1, wherein the capacitor lower plate includes polycrystalline silicon.

4. The capacitor of claim 3, wherein the capacitor upper plate includes material selected from the group consisting of Ti, TiN, TiSiN, Ta, TaN, TaSiN, W, WN, WSiN, and any combination thereof.

5. The capacitor of claim 1, wherein the capacitor lower plate includes metal selected from the group consisting of aluminum, copper, and gold.

6. An integrated circuit, comprising:

a substrate; and

a capacitor formed over the substrate, the capacitor including:

a capacitor lower plate formed over the substrate, the capacitor lower plate including electrically conductive material;

a capacitor dielectric layer of silicon dioxide formed over the capacitor lower plate, the capacitor dielectric layer having a phosphorus density between 1.7×10^{20} atoms/cm^3 and 2.3×10^{20} atoms/cm^3, such that a total density of atoms in the capacitor dielectric layer other than phosphorus, silicon and oxygen is less than 1×10^{18} atoms/cm^3; and

a capacitor upper plate formed over the capacitor dielectric layer, the capacitor upper plate including electrically conductive material.

7. The circuit of claim 6, further comprising a metal oxide semiconductor (MOS) transistor formed over the substrate, including a transistor gate electrode formed of the same material as the capacitor lower plate.

8. The circuit of claim 6, in which the capacitor dielectric layer is between 45 and 55 nanometers thick.

9. The circuit of claim 6, further including an element of field oxide formed at a top surface of the substrate; and wherein the capacitor lower plate is formed on the field oxide element; and the capacitor lower plate includes polycrystalline silicon.

10. The circuit of claim 9, wherein the capacitor upper plate includes material selected from the group consisting of Ti, TiN, TiSiN, Ta, TaN, TaSiN, W, WN, WSiN, and any combination thereof.

11. The circuit of claim 6, in which:

the integrated circuit further includes an interconnect dielectric layer formed over the substrate,

a metal interconnect line formed on the interconnect dielectric layer;

the capacitor lower plate is formed on the interconnect dielectric layer concurrently with the metal interconnect line; and

the capacitor lower plate includes metal selected from the group consisting of aluminum, copper, and gold.

12. A process of forming an integrated circuit, comprising;

providing a substrate; and

forming a capacitor over the substrate, by a process including steps:

forming a capacitor lower plate over the substrate, the capacitor lower plate including electrically conductive material;

forming a capacitor dielectric layer of silicon dioxide over the capacitor lower plate, such that a total density of atoms in the capacitor dielectric layer other than silicon and oxygen is less than 1×10^{18} atoms/cm^3;

placing phosphorus into the capacitor dielectric layer so as to provide a phosphorus density between 1.7×10^{20} atoms/cm^3 and 2.3×10^{20} atoms/cm^3 in the capacitor dielectric layer; and

forming a capacitor upper plate over the capacitor dielectric layer, the capacitor upper plate including electrically conductive material.

13. The process of claim 12, wherein the step of forming a capacitor lower plate simultaneously forms a gate electrode of a transistor.

14. The process of claim 13, in the step of placing phosphorus is performed by an ion implantation process so that a total dose of phosphorus in the capacitor dielectric layer is between 8.5×10^{14} atoms/cm^2 and 1.15×10^{14} atoms/cm^2, and so that a peak of a distribution of the implanted phosphorus is approximately in a center of the capacitor dielectric layer.

15. The process of claim 14, in which:

the process of forming the integrated circuit further includes a step of forming an element of field oxide at a top surface of the substrate; and

the step of forming the capacitor lower plate is performed so that the capacitor lower plate is formed of polycrystalline silicon on the field oxide element.

16. The process of claim 12, further comprising:

forming an interconnect dielectric layer over the substrate; and

forming a metal interconnect line on the interconnect dielectric layer;

wherein the capacitor lower plate is formed on the interconnect dielectric layer concurrently with the metal interconnect line; and

wherein the capacitor lower plate includes metal selected from the group consisting of aluminum, copper, and gold.

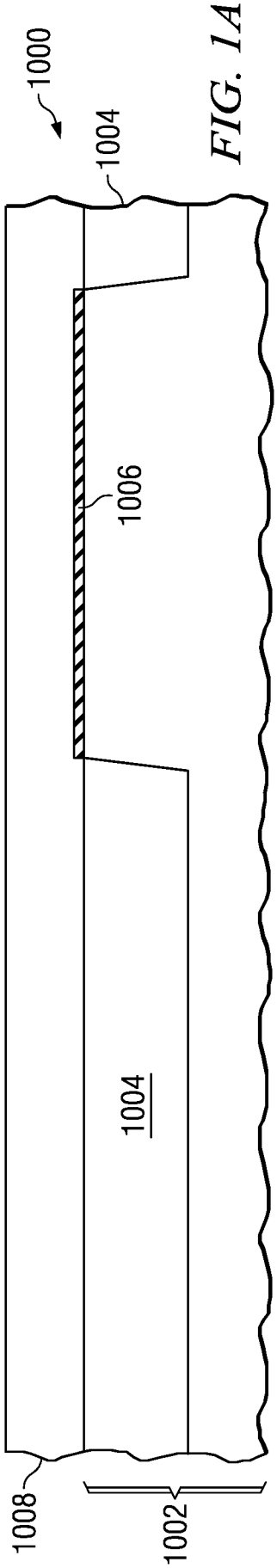

FIG. 1A

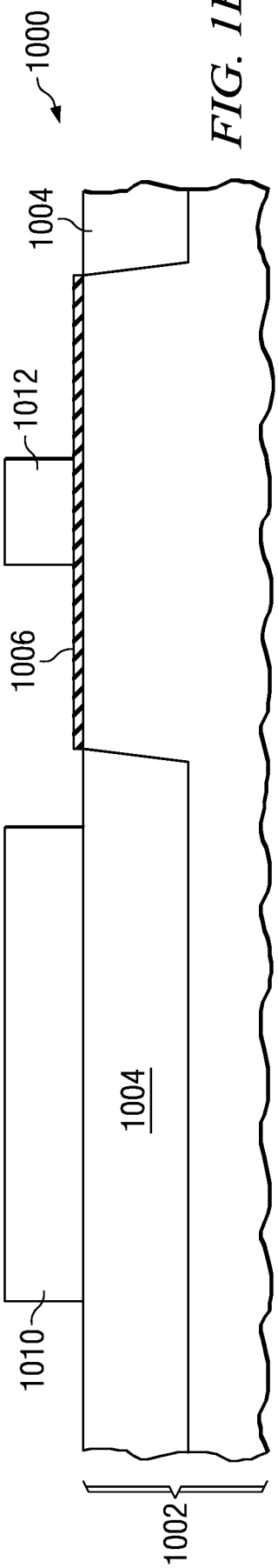

FIG. 1B

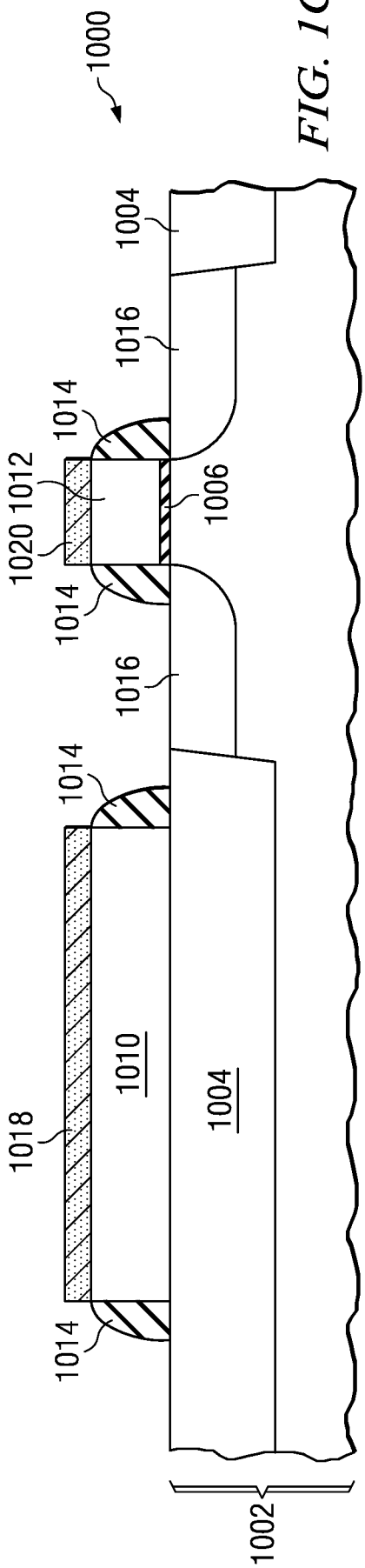

FIG. 1C

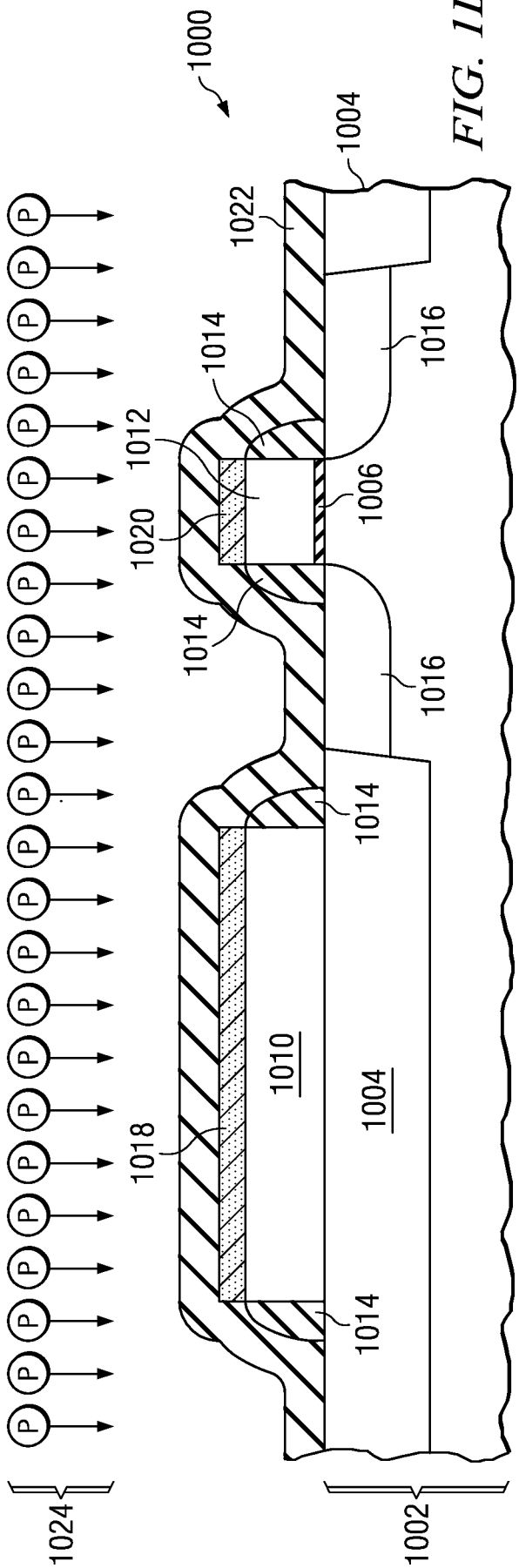
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FIG. 1D

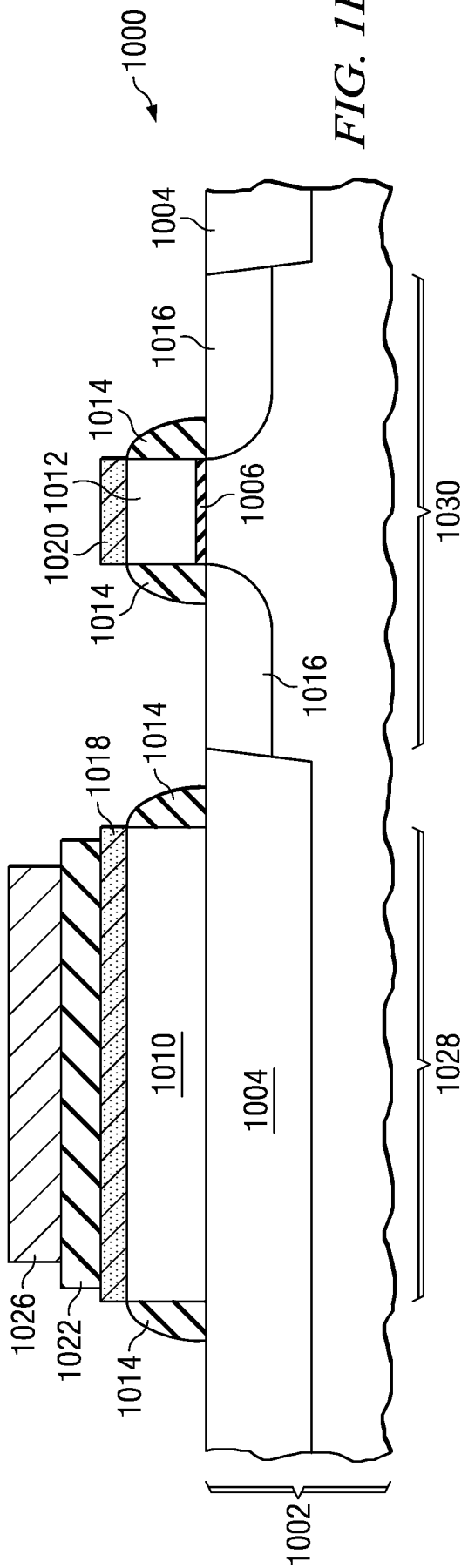
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FIG. 1E

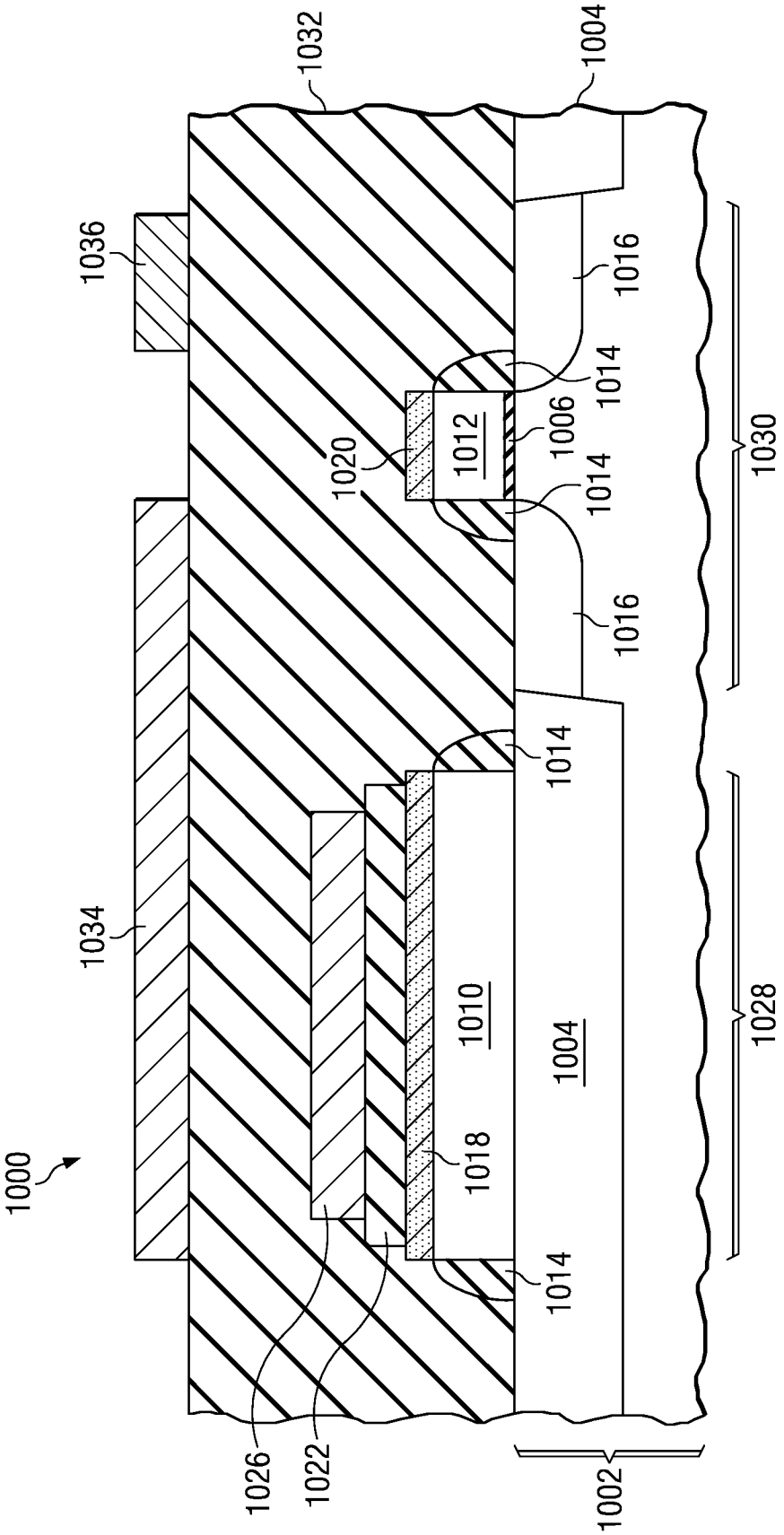
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FIG. 1F

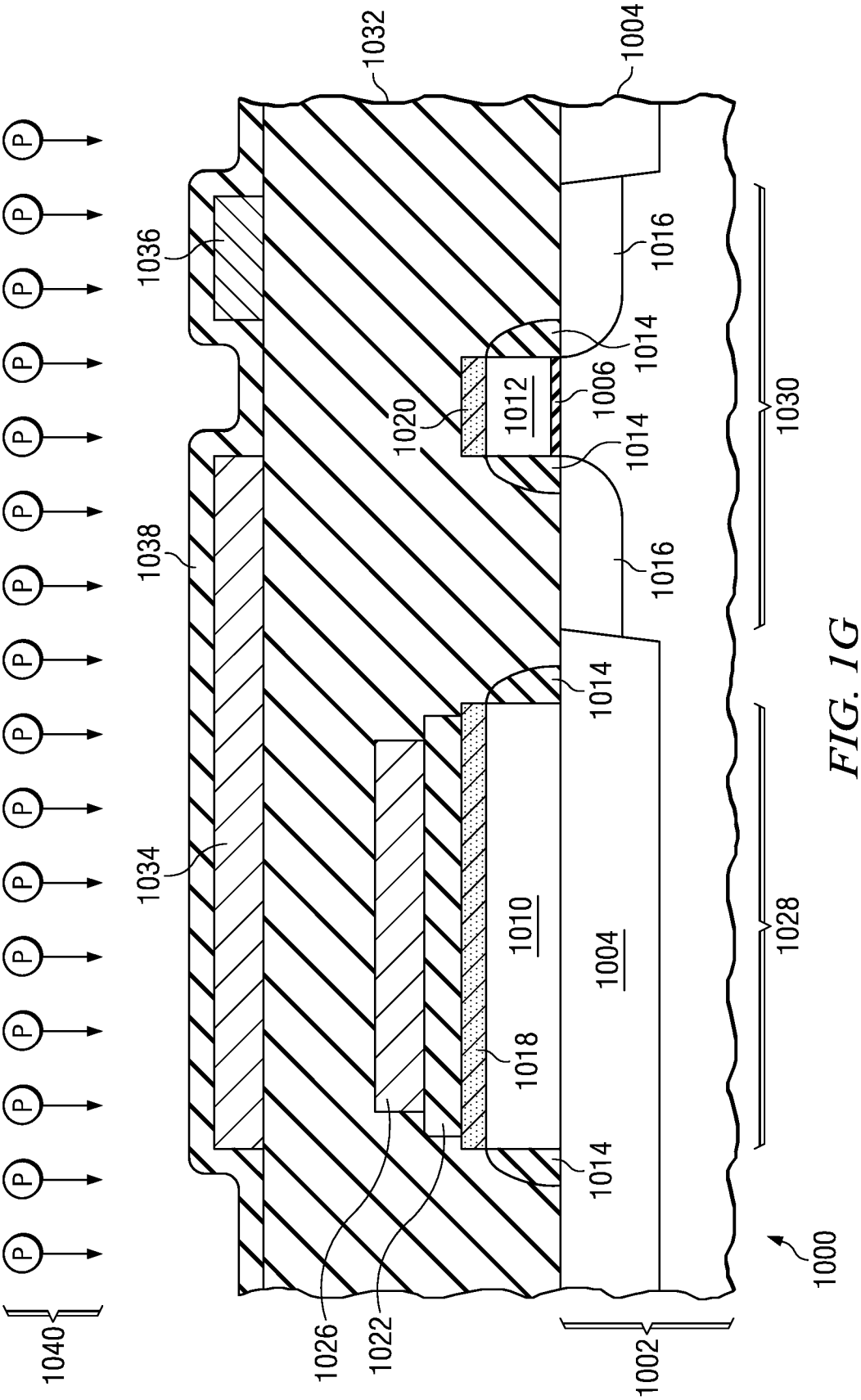
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FIG. 1G

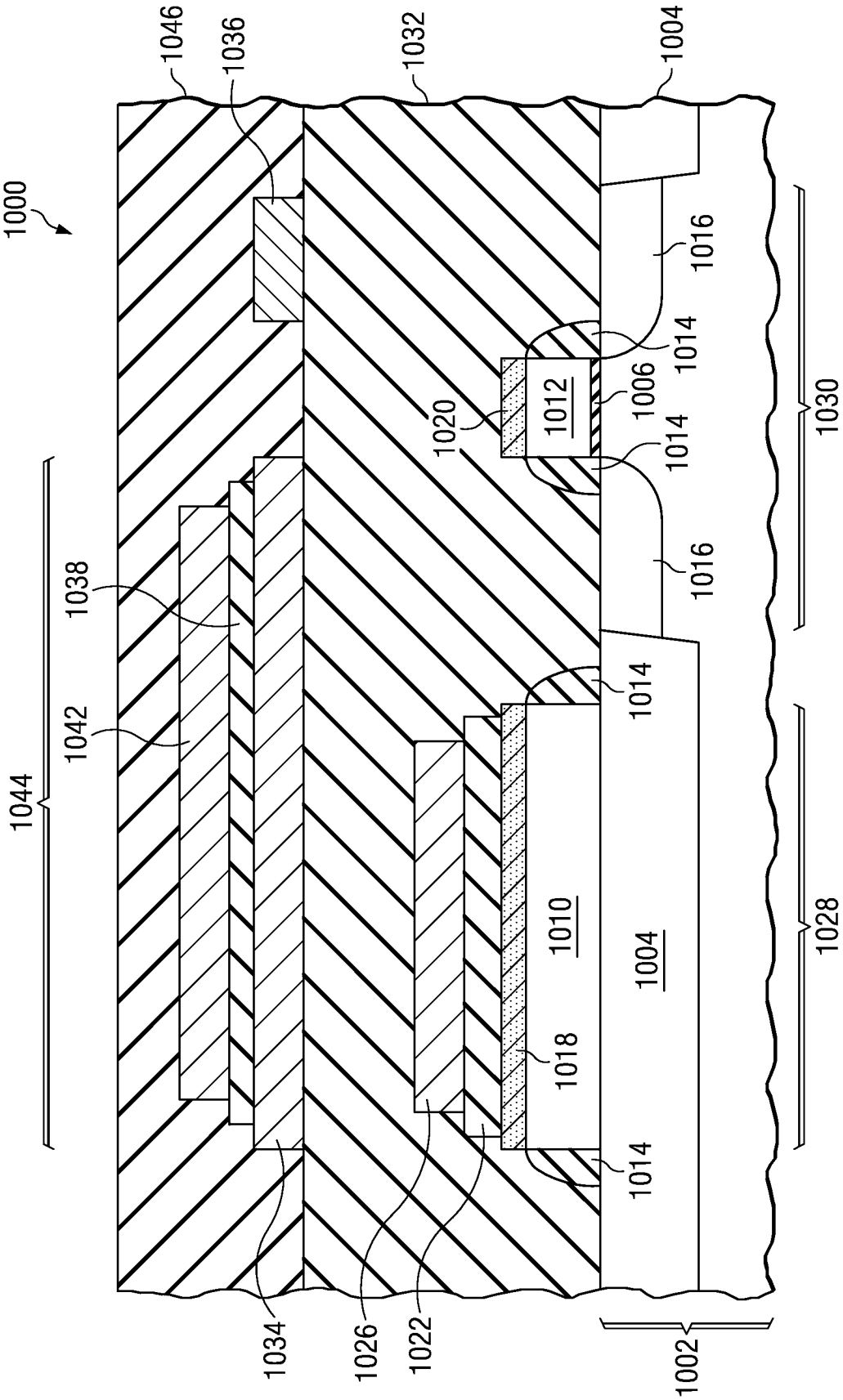
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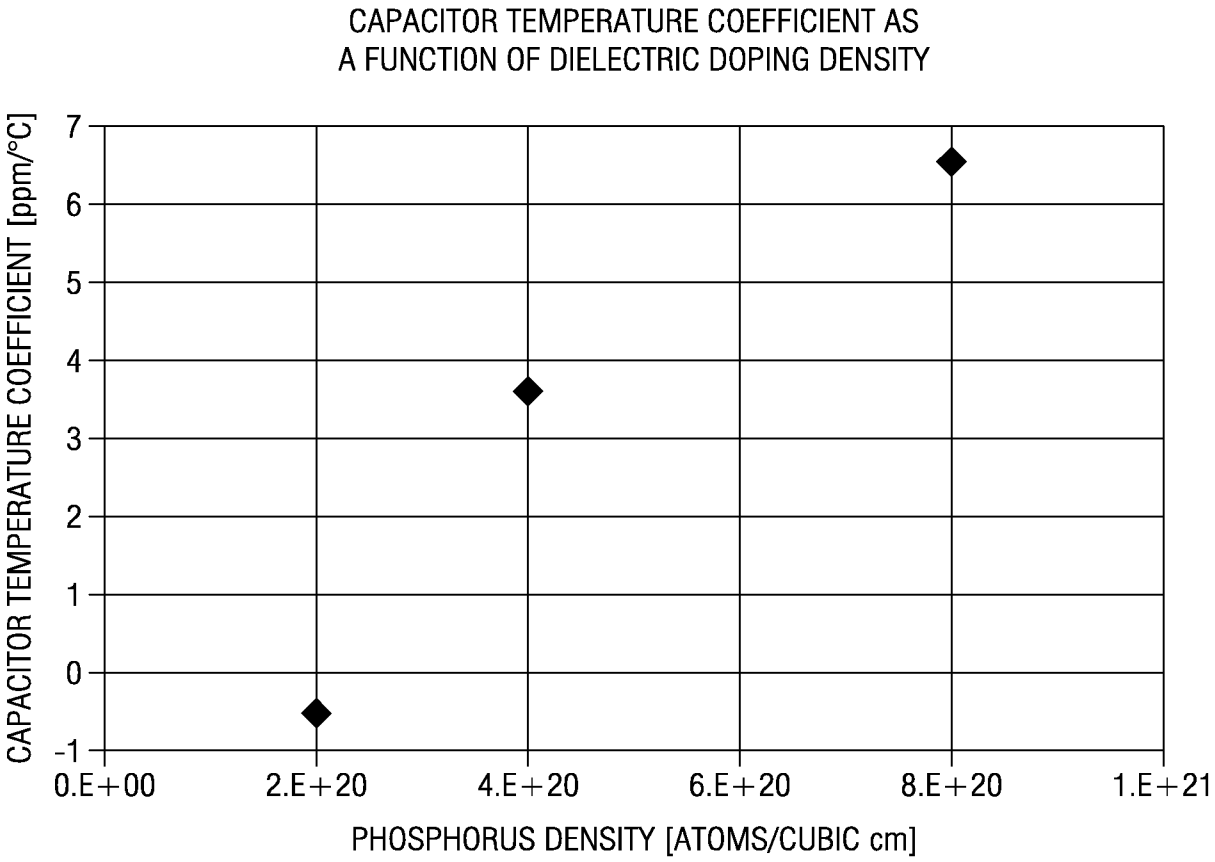
FIG. 1H


CAPACITOR TEMPERATURE COEFFICIENT AS
A FUNCTION OF DIELECTRIC DOPING DENSITY
CAPACITOR TEMPERATURE COEFFICIENT [ppm/°C]
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5
4
3
2
1
0
-1
0.E+00
2.E+20
4.E+20
6.E+20
8.E+20
1.E+21
PHOSPHORUS DENSITY [ATOMS/CUBIC cm]

FIG. 2