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Gicca et al.

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[54] **DISPLAY SYSTEM WITH GRAPHIC FILL-IN**

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[73] Assignee: **GTE Sylvania Incorporated,** Stamford, Conn.

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[52] **U.S. Cl.** ..... **340/324 AD,** 178/30

[51] **Int. Cl.** **G06f 3/14**

[58] **Field of Search** ..... 340/324 A, 324 AD; 178/15, 30

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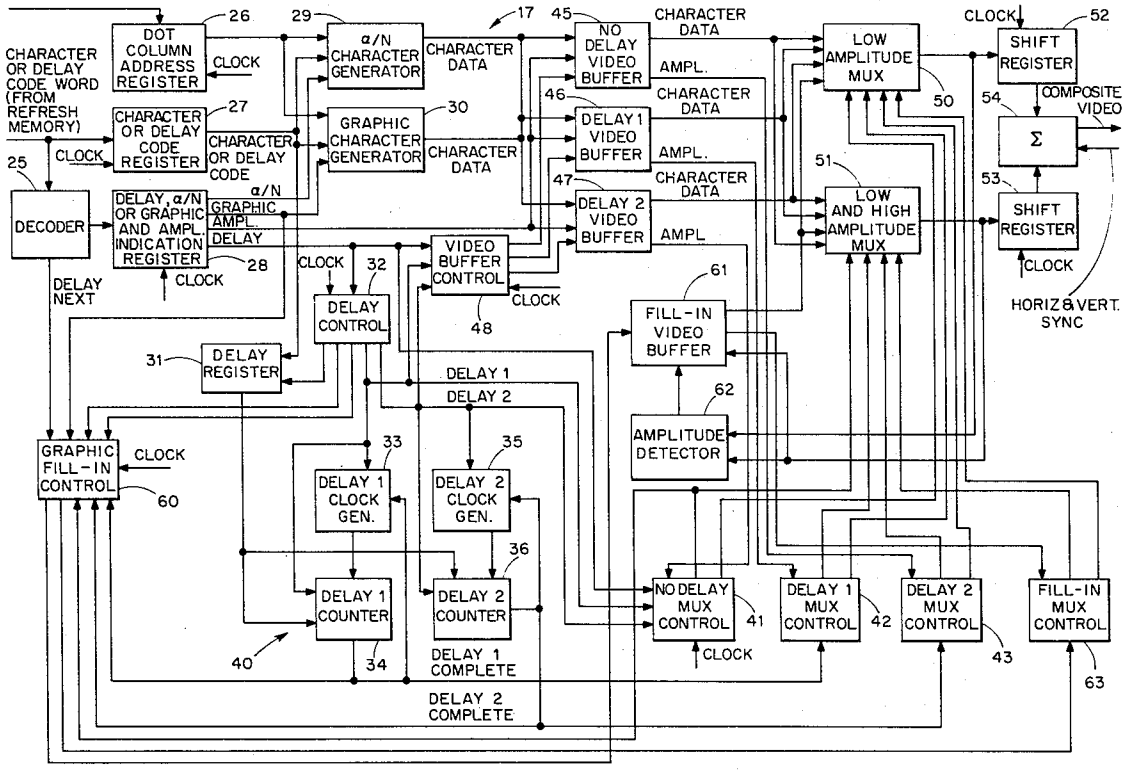
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Assistant Examiner—Marshall M. Curtis
Attorney—Norman J. O'Malley et al.

[57] **ABSTRACT**

Television-type display system for displaying information in the form of bargraphs. Code words designating individual characters of bargraphs are read out of a random access memory and the characters are displayed at fixed normal locations on the display surface of the display device. Delay code words designating amounts of delay for fine positioning the top edges of the bars may be associated with the uppermost character of each bar. The system provides for filling in certain portions of the bars in the display of overlapping bargraphs to produce continuous, uniform bars.

11 Claims, 12 Drawing Figures



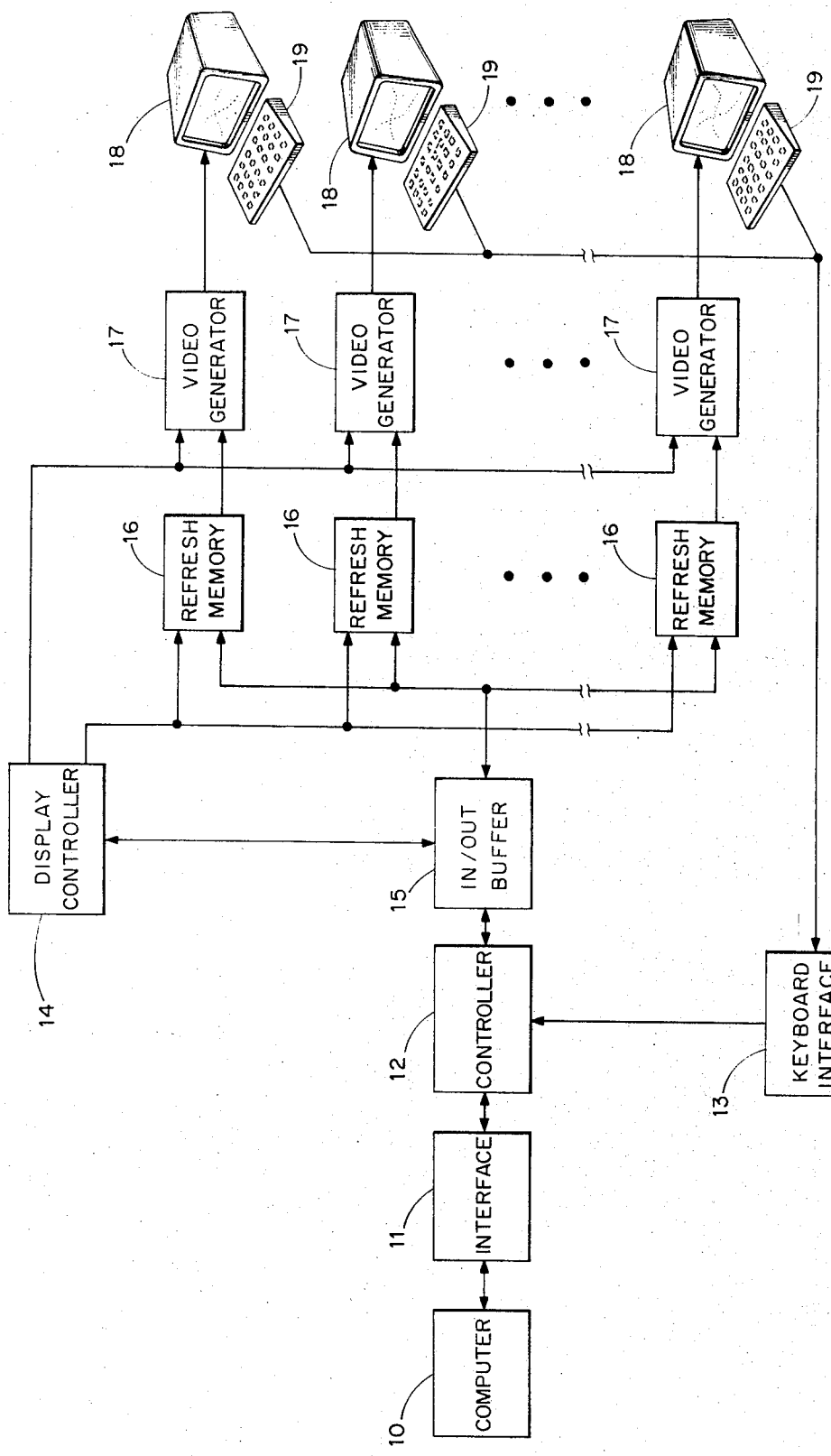

18
19
VIDEO GENERATOR
17
REFRESH MEMORY
16
DISPLAY CONTROLLER
14
IN/OUT BUFFER
15
CONTROLLER
12
KEYBOARD INTERFACE
13
INTERFACE
11
COMPUTER
10

Fig. 1.

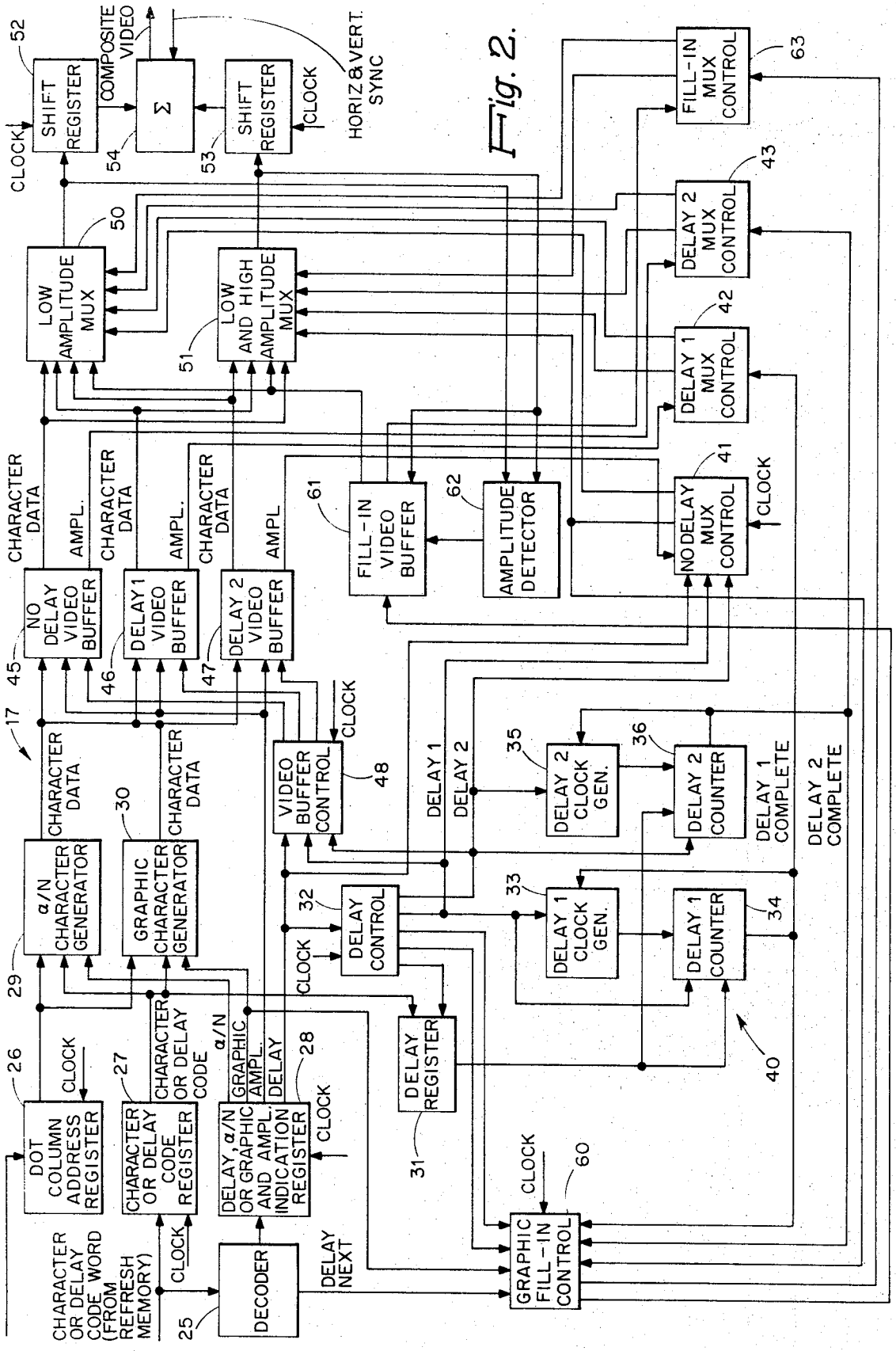

SHIFT REGISTER
COMPOSITE VIDEO
Σ
SHIFT REGISTER
CLOCK
HORIZ & VERT. SYNC
CLOCK
FILL-IN MUX CONTROL
DELAY 2 MUX CONTROL
LOW AMPLITUDE MUX
LOW AND HIGH AMPLITUDE MUX
DELAY 1 MUX CONTROL
CHARACTER DATA
AMPL.
FILL-IN VIDEO BUFFER
AMPLITUDE DETECTOR
NO DELAY MUX CONTROL
CLOCK
NO DELAY VIDEO BUFFER
DELAY 1 VIDEO BUFFER
DELAY 2 VIDEO BUFFER
VIDEO BUFFER CONTROL
CLOCK
DELAY 1
DELAY 2
DELAY 2 CLOCK GEN.
DELAY 2 COUNTER
DELAY 1 COMPLETE
DELAY 2 COMPLETE
α/N CHARACTER GENERATOR
GRAPHIC CHARACTER GENERATOR
DELAY CONTROL
DELAY 1 CLOCK GEN.
DELAY 1 COUNTER
DOT COLUMN ADDRESS REGISTER
CHARACTER OR DELAY CODE REGISTER
DELAY, α/N OR GRAPHIC AND AMPL. INDICATION REGISTER
DELAY REGISTER
CHARACTER OR DELAY CODE
α/N GRAPHIC AMPL. DELAY
CLOCK
CHARACTER OR DELAY CODE WORD (FROM REFRESH MEMORY)
DECODER
DELAY NEXT
GRAPHIC FILL-IN CONTROL
CLOCK

Fig. 2.

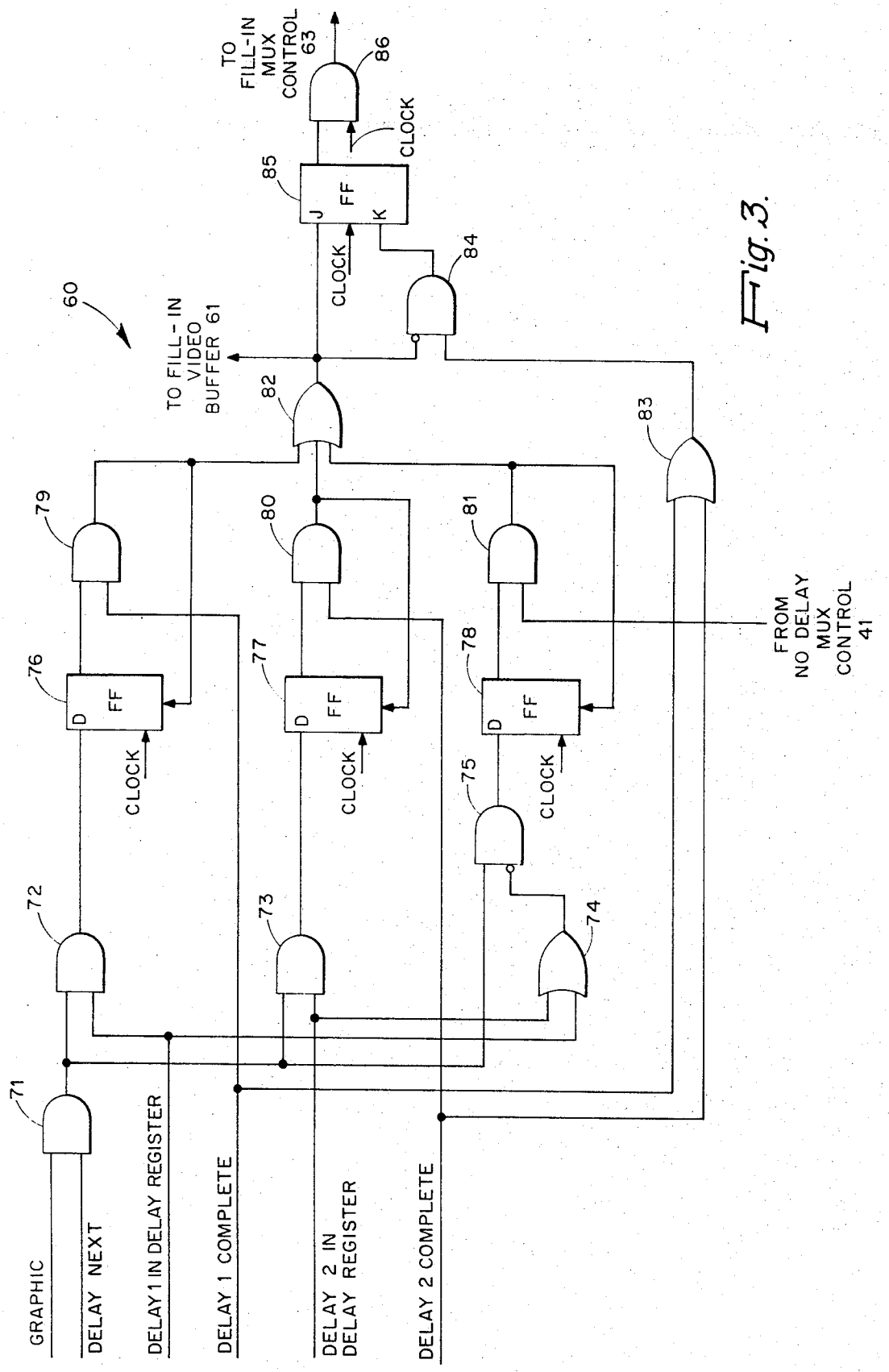

TO FILL-IN MUX CONTROL 63
86
CLOCK
85
J
FF
K
CLOCK
84
60
TO FILL-IN VIDEO BUFFER 61
82
83
79
80
81
76
77
78
D
FF
CLOCK
75
72
73
74
FROM NO DELAY MUX CONTROL 41
71
GRAPHIC
DELAY NEXT
DELAY1 IN DELAY REGISTER
DELAY 1 COMPLETE
DELAY 2 IN DELAY REGISTER
DELAY 2 COMPLETE

Fig. 3.

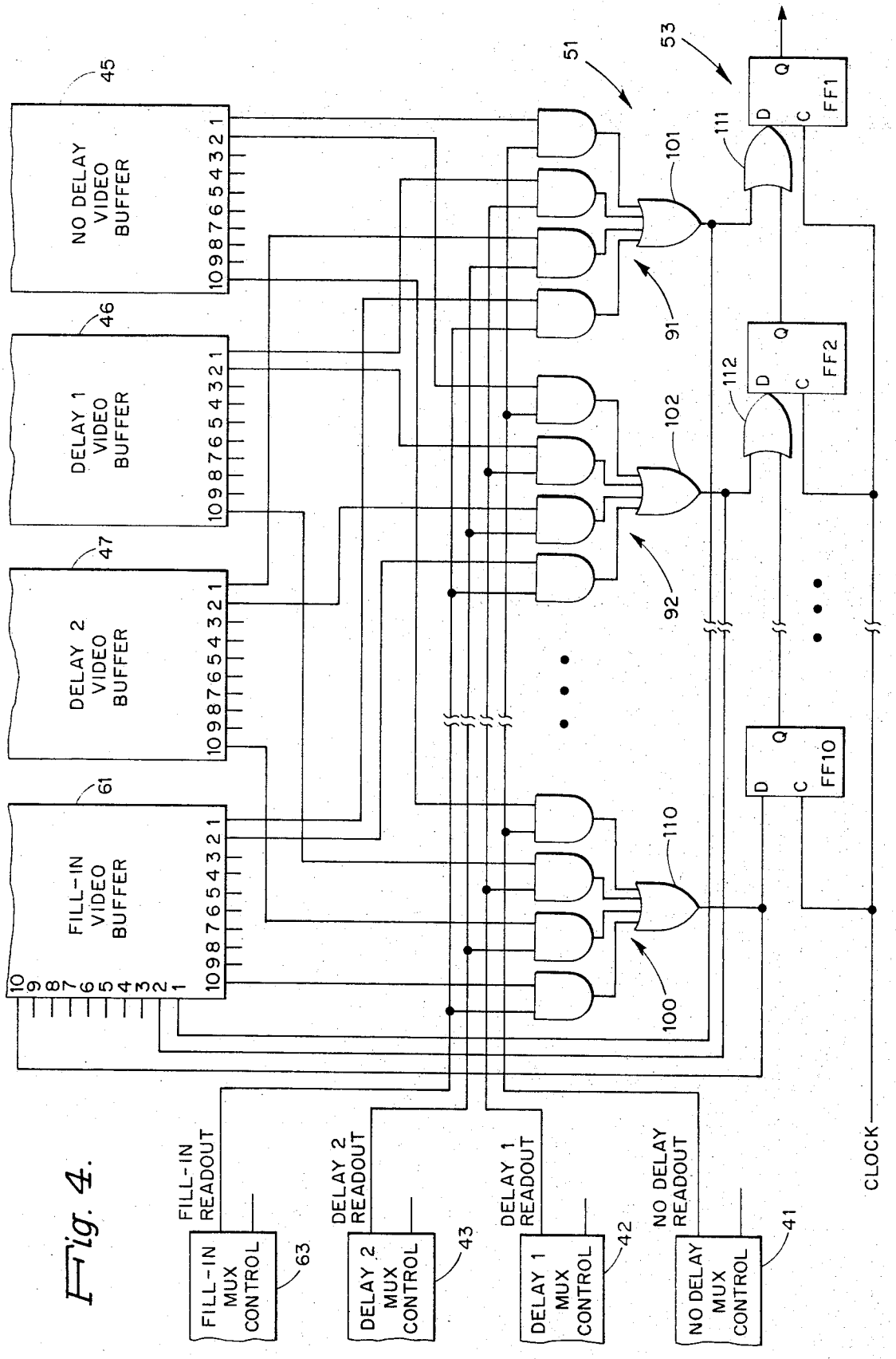

NO DELAY VIDEO BUFFER
DELAY 1 VIDEO BUFFER
DELAY 2 VIDEO BUFFER
FILL-IN VIDEO BUFFER
10 9 8 7 6 5 4 3 2 1
45
46
47
61
51
53
101
102
110
100
91
92
111
112
FF1
FF2
FF10
D
C
Q
CLOCK
FILL-IN READOUT
DELAY 2 READOUT
DELAY 1 READOUT
NO DELAY READOUT
FILL-IN MUX CONTROL
DELAY 2 MUX CONTROL
DELAY 1 MUX CONTROL
NO DELAY MUX CONTROL
63
43
42
41

Fig. 4.

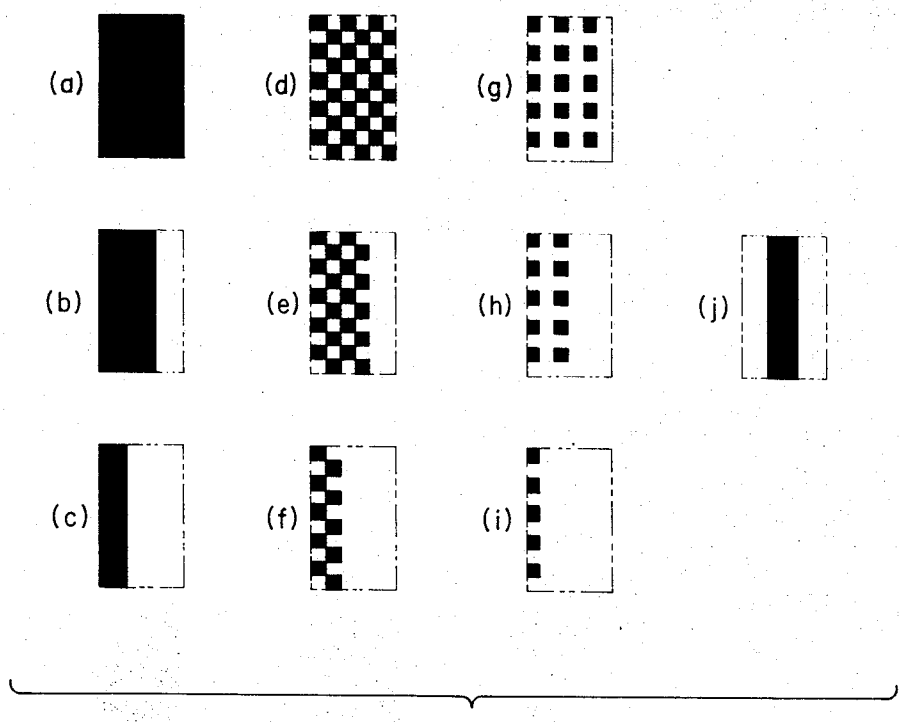


Fig. 5.

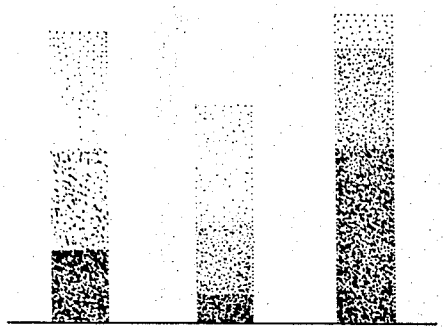


Fig. 8.

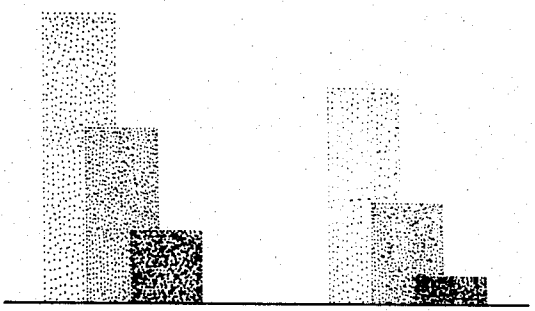


Fig. 9.

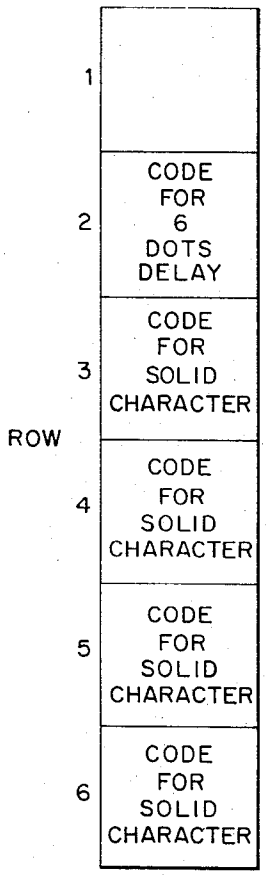

ROW
1
2
CODE FOR 6 DOTS DELAY
3
CODE FOR SOLID CHARACTER
4
CODE FOR SOLID CHARACTER
5
CODE FOR SOLID CHARACTER
6
CODE FOR SOLID CHARACTER

Fig. 6A.

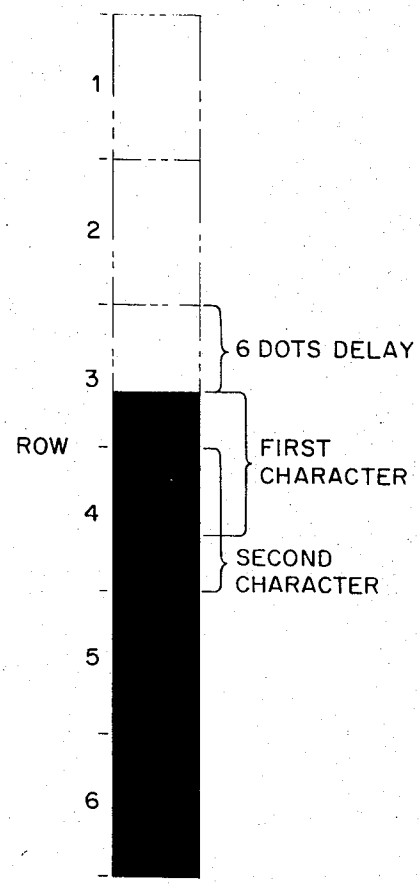

ROW
1
2
3
4
5
6
6 DOTS DELAY
FIRST CHARACTER
SECOND CHARACTER

Fig. 6B.

Fig. 7C.

Fig. 7B.

Fig. 7A.

DISPLAY SYSTEM WITH GRAPHIC FILL-IN

BACKGROUND OF THE INVENTION

This invention relates to display systems. More particularly, it is concerned with apparatus for producing television-like displays of information in graphical form.

Terminal display systems of the type for displaying business data from a computer on television monitors are well-known. These systems are generally similar. A controller is employed to communicate message to and from a host computer in which data processing tasks are performed. Information to be displayed is transmitted from the controller to refresh memories which store the information being displayed in binary code format. The display stations each employ a standard closed-circuit television monitor and keyboard which permits the operator to communicate with the host computer.

Typically display systems of this general type display information in alphanumeric form. Alphanumeric codes representing the characters to be displayed are loaded from the host computer through the controller and into a refresh memory associated with a display device at the display station. The alphanumeric code words are placed in particular storage positions in the refresh memory. Each storage position designates a specific row and column character location on the face of the display device. Each display station includes a video generator which receives the code words as they are repeatedly read out of the associated refresh memory in timed relationship with the sweeping of the raster scanline pattern. The code words read out for each scanline are converted into a series of data bits. These bits are gated into the video stream to the display device to cause the image of each character to be constructed of several series of dots written during several scanlines. The character represented by a code word is displayed on the face of the displayed device in the normal location designated by its storage position in the refresh memory.

Although display terminals of this type are satisfactory for displaying alphanumeric characters in a regular row and column array of text, they do not permit the display of true curves, histograms, or bargraphs. Since characters may be positioned only in normal locations, graphical displays of information are relatively crude. High quality graphic presentations may be obtained by the use of random access display devices of the type in which deflection amplifiers guide the beam of a cathode ray tube through a pattern of movement permitting characters to be displayed at almost any position on the display surface. However, high-speed, high-quality random access display terminals of this type which permit complete freedom of beam movement and character location are considered inordinately expensive for use in routine business applications.

An improved display system which provides high quality displays of graphical information on standard television displays is described and claimed in application Ser. No. 264,970 filed concurrently herewith and entitled "Television Type Display System for Displaying Information in the Form of Curves or Graphs." Systems in accordance with this invention may be employed to display the information in the form of bargraphs and curves which are esthetically pleasing and exhibit a high degree of accuracy. The system also permits the display of sets of curves which maintain their continuity and smoothness throughout, including at crossover points. In addition, the system is capable of producing bargraphs of uniform appearance and with their upper edges accurately positioned.

However, it is sometimes desirable in displaying graphical information in bargraph form to utilize composite or overlapping bargraphs of different density. The system as described in the aforementioned application while providing for the display of information in bargraph form is limited in its capability of producing overlapping bargraphs. Since portions of the refresh memory which usually designate specific row and column display locations on the display device are also needed to contain information for accurate positioning of the upper edge of each bargraph, the refresh memory lacks sufficient storage positions to contain data for all the required characters and also all the necessary positioning information.

SUMMARY OF THE INVENTION

Display systems in accordance with the present invention permit the high quality display of overlapping or composite bargraphs. A system displays characters so as to produce overlapping bargraphs on a video display means of the type producing images on a display surface by selectively writing on the display surface while repeatedly sweeping a raster scanline pattern over the display surface. The system includes character data memory means for storing character data in a plurality of storage positions. An addressing means causes character data to be read out of the character data memory means by addressing the storage positions in a predetermined sequence.

A video signal generating means is coupled to the character data memory means and in response to character data being read out of the character data memory means generates video signals for producing images related to the character data on the display surface so that images related to the character data are produced in a predetermined location on the display surface. The system also includes a fill-in means which is coupled to the video signal generating means. The fill-in means causes the video signal generating means to repeat generating the video signals for producing images related to the character data so that images relating to the character data are also produced in one or more other locations on the display surface.

The system thus provides the capability for repeating the display of images related to the character data in more than one location on the display surface even though only a single storage position is used to store the character data. Storage capability is thus made available for containing necessary information to permit accurate positioning of certain of the character images as required in the construction of high quality overlapping or composite bargraphs.

BRIEF DESCRIPTION OF THE DRAWINGS

Additional objects, features, and advantages of display systems in accordance with the present invention will be apparent from the following detailed discussion together with the accompanying drawings wherein:

FIG. 1 is a block diagram of a display system employed in the present invention;

FIG. 2 is a block diagram of a video generator in accordance with the present invention for use in the system illustrated in FIG. 1;

FIG. 3 is a detailed block diagram of a graphic fill-in control section of the apparatus;

FIG. 4 is a detailed block diagram of a multiplexer and shift register section of the apparatus;

FIG. 5 illustrates several graphic characters which may be employed in the display systems of FIG. 1 in the construction of bargraphs;

FIG. 6A is a chart or map of a portion of a random access digital storage type refresh memory employed in the system of FIG. 1;

FIG. 6B is a representation of a portion of the display surface of a display device illustrating the resulting display produced from the data encoded in the refresh memory of FIG. 6A;

FIG. 7A is also a map of a portion of a refresh memory;

FIG. 7B is a representation of a portion of the display surface illustrating the resulting display produced from the data encoded in the refresh memory of FIG. 7A in the absence of the fill-in capability in accordance with the present invention;

FIG. 7C is a representation of a portion of the display surface illustrating the resulting display produced from the data encoded in the refresh memory of FIG. 7A employing apparatus in accordance with the present invention;

FIG. 8 is a representation of a portion of a display surface illustrating the display of several overlapping bargraphs constructed by apparatus in accordance with the present invention; and

FIG. 9 is another representation of a portion of a display surface illustrating the display of a different form of overlapping bargraphs.

DETAILED DESCRIPTION OF THE INVENTION

General

FIG. 1 is a block diagram of an entire display system which at the level of detail shown resembles many known systems as well as systems in accordance with the present invention. FIG. 2 is a detailed block diagram of a video generator in accordance with the present invention which is employed in the system of FIG. 1. The system includes a host computer **10** together with associated peripheral equipment and software and a controller **12** which communicates with the computer through a suitable interface arrangement **11**. The system may contain several display stations each including a refresh memory **16**, a video generator **17**, a video display device **18**, and a keyboard **19**. Data is transferred to th refresh memories **16** through an input/output buffer **15**. The refresh memories **16** and video generators **17** are controlled by a display controller **14** which is also connected to the input/output buffer **15**. The keyboards **19** of the individual display stations are connected to the computer **10** through a keyboard interface **13** and the controller **12**.

Apparatus of the type shown generally in FIG. 1 typically is employed to display alphanumeric characters in text row-column locations, or "normal" locations, on the face of the television display device **18** at a display station. More specifically, the refresh memory **16** is divided into an array of storage positions each corresponding to a normal location within a row and column arrangement on the display surface. Each storage position stores a single code word representing an alphanumeric character and each location provides space for displaying a single character. For example, the storage positions in the memory and the character locations on the display surface may be arranged in 100 vertical columns and 40 horizontal rows to provide for displaying up to 4,000 characters of text on the surface of the display device.

Heretofore, when systems of this general type have been employed to display graphical information, the limitation of positioning characters only in normal locations severely limited the accuracy and the esthetics of the resulting display. Each character was limited to being displayed in its appropriate normal location by row and column. In contrast, systems in accordance with the aforementioned application being filed concurrently herewith permit shifting of individual characters from their normal locations, thus providing a display of graphical information which more clearly represents a curve. This system also permits shifting the location of a character to permit the construction of bargraphs in which the top edges are precisely located to within a fraction of the dimension of a character location, as illustrated in FIG. 6B. Because of limitations in the memory and the manner in which it is addressed, as will be explained in detail hereinbelow, this system does not permit the construction of overlapping or composite bargraphs with precisely positioned upper edges. Systems in accordance with the present invention do permit the display of overlapping bargraphs with the uppr edges of each portion accurately located to provide displays as illustrated by FIGS. **8** and **9**.

As an example of a specific embodiment for purposes of discussion herein, each of the 4,000 normal locations on the surface of the display device occupies a 6×10 dot matrix, 6 dots horizontally and 10 dots vertically. The image of a character is constructed by selectively writing dots in th vertical dot columns of 10 dot positions each during tracing of 6 vertical scanlines. In the specific embodiment under discussion, the scanlines are traced vertically downward and odd and even scanlines are interlaced during sweeping of alternating fields. Thus, 6 vertical scanlines, 3 in each field, are required to construct the image of a character in a 6×10 dot matrix location. In order to provide separation between alphanumeric characters in adjacent locations, each alphanumeric character is confined to a 5×7 dot configuration. However, the present invention is concerned not with alphanumeric characters but with special graphic characters which are displayed so as to utilize up to the full 6×10 dot matrix as will be explained hereinbelow. As will be made apparent in further discussion of the system in accordance with the present invention, the characters may be shifted vertically from their normal locations and positioned in one of 400 possible locations for each vertical column, or 40,000 possible locations on the face of the display. The characters are shifted in incremental divisions of 1 dot, or 1/10 of a character location in the vertical dimension.

Codes designating the characters to be displayed are transferred from the computer **10** to appropriate storage positions in the refresh memory **16**. If a character is to be positioned on the display in a location shifted from a normal location, a delay code is stored in the storage position designating the previous row of the same column. The delay code designates the amount the associated character is to be delayed or shifted vertically downward from what would be its normal location. The storage positions in the memory are read out vertically from top to bottom within a single column in

timed relationship with the tracing of each scanline by the display controller **14.** Thus, during each field, each column of storage positions is addressed in sequence for three successive scanlines. The total number of active scanlines for a complete frame of two fields is 600.

In the specific embodiment as illustrated, three different types of code words may be entered in the refresh memory **16** from the computer **10.** The code words, which contain eight binary bits, designate either an alphanumeric character, a special graphic character, or an amount of delay. The following table explains the nature of the three types of code words.

	Bit No. 8 7 6 5 4 3 2 1	
Alphanumeric Character Code Word	O A *x x x x x x x*	O for eighth bit indicates code for alphanumeric character. Seventh bit (A) is **0** for low amplitude or **1** for high amplitude. x x x x x x is binary number designating one of **64** possible alphanumeric characters.
Graphic Character Code Word	1 A 1 *y y y y y*	1 for eighth bit and **1** for sixth bit indicates code for graphic character. Seventh bit (A) is **0** for low amplitude or **1** for high amplitude. y y y y y is binary number designating one of **32** possible graphic characters.
Delay Code Word	1 – **0** z z z z z	**1** for eighth bit and **0** for sixth bit indicates code for delay. z z z z z is binary number designating an amount of delay in number of vertical dots.

In the system under discussion, the display device **18** may include the capability of displaying a character with relatively high or relatively low brightness levels. The seventh bit for the character code word is either a 1 or a 0 to designate the brightness amplitude.

The various code words are loaded into the storage positions of the refresh memories **16** from the computer **10** through the input/output buffer **15** during appropriate times in the operating cycles of the apparatus under control of the controller **12** and display controller **14.** The code words are read out of the refresh memory **16** to the video generator **17** under the control of the display controller **14** in proper timed relationship with the sweeping of the raster scan line pattern of the display device **18.** The display controller **14** supplies the timing and control signals to the refresh memory **16** and to the video generator **17.** These signals include the horizontal and vertical synchronizing signals for the display device as well as various coordinated clock pulse signals occuring at the scanline rate, the character location rate, and the individual character bit or dot position rate. These signals are repetitive over each operating cycle of the apparatus during the sweeping of a complete raster scanline frame over the face of the display device **18.** The display controller **14** is, therefore, an element of straightforward design for providing a multitude of synchronized pulses at different frequencies which are appropriately gated to the refresh memory **16** and video generator **17** so as to properly coordinate operations throughout the system.

As a code word is read out of its storage position in the refresh memory **16** by the display controller **14,** the code bits designating the character or the amount of delay are loaded into the character or delay code register **27** of the video generator **17** as shown in FIG. **2.** At the same time, the portion of the code word designating whether the code is for a delay, an alphanumeric character, or a graphic character, as well as the bit indicating the amplitude, is decoded by a decoder **25** and loaded in the delay, alphanumeric or graphic, and amplitude indication register **28.** Also while the code word is being read out of the storage position in the memory, the decoder **25** produces a "delay next" signal to a graphic fill-in control **60** if the decoder detects that the code word is for a delay. The information on the particular dot column or scanline is received from the display controller **14** and loaded into the dot column address register **26.**

The code in the character or delay code register **27** is then applied to the alphanumeric character generator **29,** the graphic character generator **30,** or the delay register **31** as determined by the appropriate alphanumeric, graphic, or delay signal from the delay, alphanumeric or graphic, and amplitude indication register **28.** The character generators **29** and **30** are read-only memories of the well-known type which are widely employed to convert digital code designations to the appropriate signals for producing the dot images for the particular scanline of the character. The particular scanline is identified by the data from the dot column address register **26.** If the code from the character or delay code register **27** is a delay code which is transferred to the delay register **31,** the delay arrangement **40** operates to control handling of the associated character code which is read out from the next storage position to be addressed in the refresh memory.

The graphic fill-in control **60** responds to a graphic signal from the delay, alphanumeric or graphic, and amplitude indication register **28** indicating that the code in the character or delay code register **27** is a graphic character in combination with a delay next signal from the decoder **25** indicating that the next storage position in sequence is being read out and contains a delay code. If this set of conditions occurs, such information remains in the graphic fill-in control **60** to be employed at a later step in the processing of the graphic character data, as will be explained hereinbelow.

The video buffer control **48** causes the character data from either character generator **29** or **30** to be entered in the no delay video buffer **45** if there was no previous delay code for it to be associated with. If the character data is associated with a delay, it is loaded into the delay 1 video buffer **46** or the delay 2 video buffer **47.** The system utilizes the delay 1 video buffer **46** and the delay 2 video buffer **47** in alternation.

Character data is read out of the video buffers **45, 46,** and **47** by the multiplexers **50** and **51** together or by multiplexer **51** alone under control of the respective multiplexer controls **41, 42,** and **43.** The appropriate multiplexers **50** and **51** or **51** are selected by the multiplexer controls depending on the amplitude signal. The appropriate multiplexer controls **41, 42,** and **43** operate at the proper time with respect to the scanline being traced to cause data to be transferred from the video buffers **45, 46,** and **47** to the appropriate shift registers **52** and **53** or **53** and from there to a summing network **54** where it is combined with the synchronizing signals to produce the composite video signal. Amplitude information is available by virtue of there being an output

either from both of the shift registers **52** and **53** or from only the shift register **53**, and this information may be utilized by employing any of various techniques to produce displays of two different intensities.

The no delay multiplexer control **41** enables the proper multiplexers **50** and **51** or **51** to read out the no delay video buffer **45** at the proper time to cause the resulting image of the data to appear in the normal location on the surface of the display device. The delay arrangement **40** processes the delay information in the delay register **31** so as to cause the delay 1 multiplexer control **42** or the delay 2 multiplexer control **43** to read out the associated character data in the delay 1 video buffer **46** or the delay 2 video buffer **47** at the proper time to cause the resulting image of the data to appear in a location on the display surface shifted vertically downward by an amount determined by the delay code.

If the graphic fill-in control **60** has stored therein information indicating a fill-in situation as applied to the graphic character data stored in the video buffer **45, 46,** or **47,** then upon read out of the graphic character data from the buffer the graphic fill-in control **60** produces an enabling signal. This signal activates the fill-in video buffer **61** and the character data being supplied by the buffer **45, 46,** or **47** to the shift register **53** through the low and high amplitude multiplexer **51** is caused to be loaded in the fill-in video buffer **61.** An amplitude detector **62** which is connected to the two shift registers **52** and **53** detects the amplitude signal and this data is also loaded into the fill-in video buffer **61.**

A fill-in multiplexer control **63** enables the proper multiplexers **50** and **51** or **51** to read out the fill-in video buffer **61** repeatedly at the proper times to cause the resulting images of the data to appear in normal locations on the surface of the display device. Operation of the fill-in multiplexer control **63** is terminated by a signal from the graphic fill-in control **60** indicating that the delay arrangement **40** has completed measuring the delay which generated the delay next signal to activate the graphic fill-in control **60** and the character associated with that delay is now to be read out of either the delay 1 video buffer **46** or the delay 2 video buffer **47** and applied to the appropriate shift registers **52** and **53** or **53.**

Detailed Operation — No Fill-In

A detailed explanation of the manner in which the apparatus of the invention operates to produce displays of text in which the characters appear in their normal locations by rows and columns is included in the aforementioned application filed concurrently herewith. The aforementioned application also explains the details of operation of the system in order to cause a character to be displaced vertically downward a precise distance from its normal location by a delay arrangement which is the same as that described herein. Systems in accordance with the present invention may also be employed to display alphanumeric text and curves, but the discussion herein will be limited to its use in producing vertical bargraphs.

FIG. **5** illustrates examples of graphic characters which may be employed to construct bargraphs on the surface of a display device in accordance with the present invention. Specific characters are designated in the 8-bit code for graphic characters as explained hereinabove. Each graphic character in FIG. **5** is positioned in the 6×10 dot matrix of a character location. Graphic characters (a), (b), (c), and (j) are solid characters (every dot). Graphic characters (d), (e), and (f) are half-tone characters (every other dot), and characters (g), (h), and (i) are quarter-tone characters (every fourth dot).

These characters may be employed to produce bargraph displays of various types, such as illustrated in FIG. **6B.** By employing the apparatus in the manner described in the aforementioned application, the height of each bar can be positioned within an accuracy of one dot (1/10 of the vertical height of a character location), thus permitting precise positioning of the upper edge of the bar. Operation of the apparatus of FIGS. **1** and **2** to produce such a display may be understood by reference to the map of a portion of the memory as shown in FIG. **6A.** The resulting portion of the display is illustrated in FIG. **6B.** For purposes of illustration, the solid graphic character (a) of FIG. **5** is employed in this example.

The following is a description of the manner in which the apparatus operates in accordance with the explanation in the aforementioned application in order to produce a single bargraph as illustrated in FIG. **6B** without the need for the fill-in sections of the apparatus. As the storage positions in the memory for the column as arranged in FIG. **6A** are addressed in timed relationship with an appropriate scanline, the delay code word for 6 dots delay is read out first and applied to the video generator **17.** The first five bits which designate the amount of delay are loaded in the character or delay code register **27.** The decoder **25** decodes the eighth and sixth bits as indicating a delay and enters this information in the delay, alphanumeric and amplitude indication register **28.**

When the data is read out of the input registers **26, 27,** and **28,** the presence of a "delay" signal from the register **28** activates a delay control **32.** The delay control **32** enables the delay register **31** on a subsequent clock pulse so that the delay code from the character or delay code register **27** is placed in the delay register **31.** The delay control **32** holds the delay code in the delay register **31** for a period of time equivalent to the tracing of the scanline through 10 dots, the vertical dimension of a character location. This period of time is determined by the period of the clock pulses applied to the delay control **32.** On the clock pulse upon termination of this period (when the data for the solid character read out from the third row of the column is being loaded into the delay 1 video buffer **46** or the delay 2 video buffer **47** as will be explained), the delay control **32** produces a "delay 1" or "delay 2" signal. The delay control **32** includes a flip-flop arrangement which is caused to be triggered by each delay signal and in effect divides by two so that every other delay code is processed as a delay 1 and intervening delay codes are processed as a delay 2. Assuming a delay 1 signal is produced by the delay control **32,** the delay 1 signal activates a delay 1 counter **34** causing a count represented by the delay code in the delay register **31** to be loaded into the delay 1 counter **34.** At the same time a delay 1 clock generator **33** is also activated. The delay 1 clock generator **33** produces periodic clock pulses at the dot position rate. When the delay 1 clock generator **33** has provided the proper number of clock pulses (six in this example) to the delay 1 counter **34** causing the delay 1 counter to count down from the delay of six received from the delay register **31** to a count of zero, a "delay 1 complete" signal is produced by the delay 1

counter. This signal deactivates the delay 1 clock generator **33** and is also applied to the delay 1 multiplexer control **42.**

When the delay code from the character or delay code register **27** is applied to the delay register **31,** the next storage position in the refresh memory **16** is read out. Thus, the code word for the solid character is read out of the third row and placed in the character or delay code register **27,** and the indication that it is a graphic character as determined by the decoder **25** and the amplitude information is stored in the delay, alphanumeric or graphic, and amplitude indication register **28.** The graphic signal, character code, and dot column information are applied to the graphic character generator **30** from the input registers **28, 27,** and **26,** respectively. The graphic character generator **30** thus produces the appropriate data bits for writing the image of the character in the appropriate dot column of the character location.

The data bits pertinent to the solid character are applied to the video buffers **45, 46,** and **47** by the graphic character generator **30.** The video buffer control **48** receives the delay 1 signal from the delay control **32.** In response to the delay 1 signal the video buffer control **48** inhibits the enabling signal to the no delay video buffer **45** on the next clock pulse, and instead produces an enabling signal to the delay 1 video buffer **46** on the clock pulse. Thus the data bits pertinent to the solid character from the graphic character generator **30** and the amplitude information from the delay, alphanumeric or graphic, and amplitude indication register **28** are loaded into the delay 1 video buffer **46.**

The character data information remains stored in the delay 1 video buffer **46** until the delay 1 counter **34** completes its countdown as explained and the delay 1 complete signal is transmitted to the delay 1 multiplexer control **42.** In response to the delay 1 complete signal, the delay 1 multiplexer control **42** produces an enabling signal to the appropriate gates of either both the low amplitude multiplexer **50** and the low and high amplitude multiplexer **51** or only to the low and high amplitude multiplexer **51** depending upon the amplitude information from the delay 1 video buffer **46.** In the present example, the enabling signal occurs six dot positions of movement of the scanline later than if there were no delay and the data were being transferred from the no delay video buffer **45.** The data bits pertinent to the character are thus transferred through the appropriate multiplexers **50** and **51** or **51** to the associated parallel-to-serial shift registers **52** and **53** or **53.** The bits are clocked out of the shift registers at the rate of one bit for the tracing of a scanline through one dot position, and pass through the summation network **54** to become part of the composite video signal to the display device. As illustrated by the solid character labeled first character in FIG. **6B,** by delaying the data bits for each scanline by six dot positions, the image is constructed in a location which is 6 dots lower in the display than its normal location.

The storage position for the fourth row of the column is read out of the memory in proper timed relationship with the tracing of each scanline. The code bits designating the solid character are loaded into the character or delay code register **27.** The decoder **25** decodes the information in the eighth, seventh, and sixth bits and loads information identifying the code as designating a graphic character and also the data on the amplitude in the delay, alphanumeric or graphic, and amplitude indication register **28.**

The data in the input registers **26, 27,** and **28** is applied to the character generators **29** and **30.** Since the delay, alphanumeric or graphic, and amplitude indication register **28** produces a graphic signal, only the graphic character generator **30** is enabled.

The video buffer control **48** receives clock pulses at the character location scanning rate. In response to each clock pulse, the video buffer control **48** enables the no delay video buffer **45** unless a delay 1 or delay 2 signal is present as explained previously. Since there is no delay 1 or delay 2 signal present, the no delay video buffer **45** is enabled and the character data from the graphic generator **30** together with the amplitude indication from the delay, alphanumeric or graphic, and amplitude indication register **28** are loaded into the no delay video buffer **45.**

The character data stored in the no delay video buffer **45** is read out under control of the no delay multiplexer control **41.** The no delay multiplexer control **41** operates on periodic clock pulses which occur at the character location scanning rate. Since there is no delay information being applied to the no delay multiplexer control **41** to indicate that the no delay video buffer **45** contains anything except character data which is not to be delayed, the no delay multiplexer control **41** is not inhibited. A clock pulse causes the no delay multiplexer control **41** to operate in timed relationship to the tracing of the scanline to enable either both the low amplitude multiplexer **50** and the low and high amplitude multiplexer **51** or only the low and high amplitude multiplexer **51** depending upon the amplitude signal from the no delay video buffer **45.** The data bits relating to the character are transferred in parallel from the no delay video buffer **45** to the appropriate parallel-to-serial shift registers **52** and **53** or **53.**

Ten bits of character data are entered into the shift registers **52** and **53** or **53** and are clocked out in series at the dot position rate to enter the video stream by way of the summing network **54.** Each bit enters the video stream in timed coordination with the tracing of the scanline through the corresponding dot column position at the normal location on the display surface. The series of data bits from the shift registers **52** and **53** or **53** are combined with the horizontal and vertical synchronizing signals from the display controller **14** to produce the composite video signal which is transmitted to the display device **18** to construct the image of the appropriate dot column of the character in its normal location. Upon completion of sweeping through a complete frame of the raster scanline pattern, the image of the character is completely constructed in dot matrix form in its normal location as illustrated in the fourth row in FIG. **6B** and labeled second character. As shown in FIG. **6B,** portions of the two characters overlap, but the images of the characters are such that the entire bar is uniform in appearance.

The code words for the solid graphic character from the fifth and sixth rows are read out and processed with no delay as explained previously to produce a continuous bar extending to the desired baseline of the graph.

Similarly, code words for the graphic characters (b) through (j) of FIG. **5** may be utilized to produce various graphical displays. Each bar may be several character columns wide. For the graphic characters (a), (b), and (c) the upper levels may be positioned within one

dot. In order for the bars produced with the characters (e) through (i) to appear uniform, the delay must be in even numbers of dots.

Detailed Operation — Fill-In

The display system in accordance with the present invention may also be employed to display information in overlapping bargraph form as illustrated in FIGS. **8** and **9.** In each group of bars illustrated, the upper bar is constructed of quarter-tone characters, the intermediate bar is constructed of half-tone characters, and the lower bar is constructed of solid characters. The upper edge of each bar is positioned precisely by delaying the first character of that type for the desired number of dots.

However, since the delay information required to properly position the first character of each type with respect to its normal location requires a storage position in the memory, that storage position cannot be used to contain a graphic character code word for the preceding character. The problem caused by this situation is illustrated by the memory map of FIG. 7A and the resulting display shown in FIG. 7B. As illustrated in FIG. 7B, the upper edge of the solid character stored in the third row of the memory is shifted six dots downward from the normal location for the third row. Since the last previous half-tone character occupies the normal location for the first row, there is a gap in the normal location for the second row and the first six dot positions of the third row. The system of the present invention provides for filling in this gap by repeating the half-tone character of the first row in the second and third rows to produce the resulting display as illustrated in FIG. 7C.

The system operates to read out the code word for the half-tone character from the storage position for the first row of the memory and process the code word in the manner explained previously to cause the half-tone character to be displayed as shown in the normal location for the first row of FIG. 7C. In addition, when the code for the half-tone character is being applied to the graphic character generator **30** from the character or delay code register **27** and a graphic signal is being produced by the delay, alphanumeric or graphic, and amplitude indication register **28,** the code word for six dots delay in the second column is being read out of the storage position for the second column causing the decoder **25** to produce a delay next signal to the graphic fill-in control **60.**

The graphic fill-in control **60** is illustrated in greater detail in FIG. **3.** The portion of the control for processing data in the present situation includes an AND gate **71** to which is applied the graphic and delay next signals. The output of the AND gate **71** is applied to a gate **75.** The gate **75** has an inhibiting input which is the output of an OR gate **74** having input connections from the delay control **32.** These connections cause the gate **75** to be inhibited if there is a previous delay situation as will be explained later in this application. The output of the gate **75** is applied to the D input of a D-type flip-flop **78** which is clocked at a rate equal to the character location scanning rate.

The output of the D-type flip-flop **78** is applied to an AND gate **81** having another input from the no delay multiplexer control **41.** The output of the AND gate **81** causes the flip-flop **78** to be cleared and is applied through an OR gate **82** directly to the fill-in video buffer **61** as a loading or enabling signal and to the J input of a J-K flip-flop **85.** The J-K flip-flop **85** is clocked at a rate equal to the dot position scanning rate. The output of the J-K flip-flop **85** is applied to an AND gate **86.** Periodic clock pulses at the character location scanning rate are applied at the second input of the AND gate **86.** The output of the AND gate **86** is applied to the fill-in multiplexer control **63.**

Delay 1 complete and delay 2 complete signals from the respective delay 1 and delay 2 counters **34** and **36** are applied through an OR gate **83** to a gate **84.** An inhibiting input to the gate **84** is provided from the output of the OR gate **82,** the loading signal to the fill-in buffer **61.** The output of the gate **84** is applied to the K input of the J-K flip-flop **85.**

In the example under discussion, as illustrated by FIGS. 7A and 7C, while the half-tone character code for the first row is being applied to the graphic character generator **30,** the graphic signal from the delay, alphanumeric or graphic, and amplitude indication register **28** and the delay next signal from the decoder **25** are applied to the AND gate **71.** An output signal from the AND gate **71** passes through the gate **75** since, in the present example, it is not inhibited by a delay in process in the delay register. The signal is applied to the D input of the D-type flip-flop **78.**

When the code for the half-tone character of the first row is loaded into the no delay video buffer **45,** the clock pulse to the flip-flop **78** sets the flip-flop since there is a signal at its D input. On the next clock pulse at the no delay multiplexer control **41,** which occurs a character location time later, the half-tone character data is read out from the no delay video buffer **45** and the AND gate **81** passes the same clock pulse. This pulse passes through the OR gate **82** and is applied to the fill-in video buffer **61** as a loading signal. It also causes the D-type flip-flop **78** to be cleared to its reset condition. Thus, the data bits being read out of the no delay video buffer **45** through either the low and high amplitude multiplexer **51** and the low amplitude multiplexer **50** to the appropriate shift registers **52** and **53** or **53** are also applied to the fill-in video buffer **61** to be stored therein. At the same time the amplitude detector **62** by virtue of its being connected to both the multiplexers **50** and **51** detects the associated amplitude signal to be stored in the fill-in video buffer **61.** Thus, while the code for the half-tone character for the first row is read out and the image for the character is caused to be displayed in its normal location, labeled normal character in the first row of FIG. 7C,in addition the data bits relating to the character are placed in the fill-in video buffer **61.**

The code word for six dots delay in the second row of the memory and the code word for the associated solid character in the third row are processed as explained previously. While this information is being processed, the periodic clock pulses at the character location rate applied to the AND gate **86** of the graphic fill-in multiplexer control **63.** The pulses occur in proper timed relationship with the tracing of the scanline so as to cause the fill-in multiplexer control **63** to read out the character data from the fill-in video buffer **61** through the appropriate multiplexers **50** and **51** or **51** to produce images in succeeding normal locations. The first occurrence of reading out the fill-in video buffer **61** causes the character image for the scanline to be written in the second row as illustrated in FIG. 7C. A character location time later, the next pulse from the

fill-in multiplexer control **63** causes the character image to be repeated in the third row as illustrated in FIG. 7C. These two character images are labeled fill-in characters in FIG. 7C.

During the first six bits of tracing a scanline for the third row location, the half-tone character image is produced. Since the six dot delay countdown is now complete, a delay 1 complete or delay 2 complete signal from the appropriate delay counter **34** or **36** causes the appropriate multiplexer control **42** or **43** to read out the solid character data from the appropriate video buffer **46** or **47.** The solid character is thus produced six dots delayed from its normal location as shown in FIG. 7C and labeled delayed character.

The delay complete signal is also applied to the OR gate **83** of the graphic fill-in control **60.** This pulse is passed by the OR gate **83** and the AND gate **84** since there is no inhibiting signal from the OR gate **82.** This signal is applied to the K input of the J-K flip-flop **85** so that the clock pulse to the flip-flop resets the flip-flop. Thus, the graphic fill-in control **60** is returned to its quiescent state with the AND gate **86** inactive so that subsequent clock pulses thereto will not cause the fill-in multiplexer control **63** to be activated. Thus, the fill-in video buffer **61** is not read out subsequent to the writing of images in the normal location for the third row as illustrated in FIG. 7C.

The delayed solid character from the third row of the memory is displayed as illustrated and labeled delayed character in FIG. 7C overlapping the last four dot positions of the half-tone character in the normal loation location the third row. The code words in the fourth, fifth, and sixth rows are read out and the images produced in the fourth, fifth, and sixth rows of the display as illustrated in FIG. 7C in the usual manner as explained previously when there is no delay situation.

Thus, the system in accordance with the invention as described detects the need for a fill-in when writing graphic characters for constructing bargraphs and fills in the gap which would otherwise exist as in the second and third row locations as shown in FIGS. 7B and 7C. Thus, the system may be employed to display overlapping and composite bargraphs of the type illustrated in FIGS. **8** and **9.**

A detailed block diagram of a multiplexer and its associated shift register which operate to permit the superimposing of characters as in the third and fourth rows of the display of FIG. 7C is shown in FIG. **4.** The low and high amplitude multiplexer **51** and its associated shift register **53** are illustrated. The other multiplexer **50** and shift register **52** are similar. The shift register **53** includes 10 flip-flop stages FF1–FF**10,** one for each data bit in a character dot column. The occurrence of a clock pulse at the C input sets each flip-flop to produce an output signal at its output if there is a signal present at its D input. If no signal is present at the D input, a clock pulse resets the flip-flop and no output signal is produced.

The multiplexer **51** includes 10 groups of four AND gates **91–100,** a group associated with each flip-flop. Each AND gate has two inputs. A first input of one AND gate of one group **91** is connected to the no delay video buffer **45** to receive the first character data bit therefrom and the second input is connected to the no delay multiplexer control **41** to receive a no delay readout pulse therefrom. A second AND gate of the group **91** is connected to the delay 1 video buffer **46** to receive the first character data bit therefrom, and to the delay 1 multiplexer control **42** to receive a delay 1 readout pulse therefrom. The third gate of the group **91** is connected in similar fashion to receive the first character data bit from the delay 2 video buffer **47** and a delay 2 readout pulse from the delay 2 multiplexer control **43.** In the same manner, the fourth gate of the group **91** is connected to receive the first character data bit from the fill-in video buffer **61** and a fill-in readout pulse from the fill-in multiplexer control **63.**

The AND gates **92** of the second group are appropriately connected to receive the second character data bits from the video buffers **45, 46, 47,** and **61** and the readout pulses from the multiplexer controls **41, 42, 43,** and **63.** The other groups of AND gates are also appropriately connected in similar fashion.

The outputs of each group of AND gates **91–100** are connected to an associated OR gate **101–110.** The outputs of each OR gate except for the first OR gate **110** in sequence are connected to an associated second OR gate **111, 112,** . . . . A second input of each second OR gate **111, 112,** . . . is connected to the output of the previous flip-flop in sequence, and its output is connected to the D input of its associated flip-flop. The output of the first OR gate **110** is connected directly to the D input of its associated flip-flip FF**10.**

The multiplexer **51** operates in response to a readout pulse from a multiplexer control **41, 42, 43,** or **63** to apply the ten data bits from the respective video buffer **45, 46, 47,** or **61** to the D input of the corresponding ten flip-flops FF1–FF**10.** The data bits are loaded into the flip-flops on the next clock pulse and on subsequent clock pulses are moved along the sequence of flip-flops to be transferred out serially from the output of the last flip-flop in the sequence FF1 to the summing network **54** to become part of the video stream. The clock pulse rate is equal to the dot position scanning rate.

It can be seen that the reading out of the video buffers **45, 46, 47,** and **61** is independently controlled by the respective multiplexer controls **41, 42, 43,** and **63.** Thus, the data bits from one of the buffers can be read out while those from another are in the shift register, causing the two characters to be superimposed on the display surface. This situation is illustrated in FIG. 7C wherein the delayed solid character is superimposed with the fill-in half-tone character appearing in the third row location and also with the solid character appearing in the fourth row location.

Data bits for a scanline of the half-tone character are in the fill-in video buffer **61** and data bits for the scanline of the solid character are in the delay 1 video buffer **46.** During the scanline, a fill-in readout pulse is produced by the fill-in multiplexer control **63** applying the data bits for the half-tone character from the fill-in video buffer **61** to the appropriate flip-flops FF1–FF**10** of the shift register. The next clock pulse loads the data bits into the flip-flops thereby clocking the first data bit into the video stream. On the next clock pulse, the data bits each shift one flip-flop to the right and the second data bit for the half-tone character enters the video stream.

After six data bits or dot positions have been clocked out from the shift register a delay 1 readout pulse is produced by the delay 1 multiplexer control **42** applying the data bits for the solid character from the delay 1 video buffer **46** to the appropriate flip-flops FF1–FF**10** of the shift register. The next clock pulse

shifts the data bits for the half-tone character one stage to the right placing the seventh bit in the video stream. At the same time, the data bits for the solid character are loaded into the flip-flops FF1–FF10 and the first data bit for the solid character enters the video stream.

That is, if either the data bit for the half-tone character applied to a particular flip-flop through a previous flip-flop in the sequence or the data bit for the solid character applied to the particular flip-flop from the delay 1 video buffer **46** is a 1, then the flip-flop will be set to produce an output signal. In this manner, data bits from one video buffer are combined with or caused to overlap those from another video buffer, and the resulting image displayed is the two characters superimposed as illustrated in the third row of FIG. 7C. For this particular example, since the solid character is all 1's, it overlies and obscures the half-tone character providing the proper representation of the bargraph as shown in FIG. 7C.

The system also provides for handling the particular situation when the character to be the fill-in character is itself being delayed and is not being displayed in its That location. Thiat is, a first delay code word is in a storage position of the memory followed by an associated first graphic character code word in the next storage position, a second delay code word in the next storage position, and an associated second graphic character code word in the following storage position.

As illustrated in the graphic fill-in control **60** in FIG. **3**, different portions are used depending upon whether the first delay is to be processed by the delay arrangement **40** as a delay 1 or as a delay 2. For a delay 1, the graphic fill-in control **60** includes an AND gate **72** having one input connected to the AND gate **71** previously described and another input connected to the delay control **32**. The output of AND gate **72** is connected to the D input of a D-type flip-flop **76**. The D-type flip-flop is clocked at the character location scanning rate. The output of the flip-flop **76** is connected to an AND gate **79**. The other input of the AND gate **79** receives the delay 1 complete signal from the delay 1 counter **34**. The output of the AND gate **79** is connected to cause the D-type flip-flop **76** to be cleared to its reset condition and also is one of the inputs to the previously mentioned OR gate **82**.

A similar arrangement for the delay 2 situation includes an AND gate **73** having its inputs connected to the output of AND gate **71** and to the delay control **32**. Its output is connected to the D input of a D-type flip-flop **77** which is also clocked at the character location scanning rate. The output of the D-type flip-flop **77** is connected to the input of an AND gate **80** having its other input connected to the delay 2 counter **36** to receive the delay 2 complete signal therefrom. The output of the AND gate **80** is applied to the D-type flip-flop **77** to cause the flip-flop to be reset and also to one of the inputs of the OR gate **82**.

The appatatus operates in the following manner assuming that the first delay code word and its associated graphic character code word are to be processed as a delay 1. The delay 1 code word and the associated graphic character code word are processed in a straightforward manner without employing the fill-in sections since they do not produce the combination of the graphic and delay next signals required to activate the graphic fill-in control **60**. When the first character code is being applied to the graphic generator **30**, the graphic signal from the delay, alphanumeric or graphic, and amplitude indication register **28** occurs at the same time as the delay next signal from the decoder **25** for the second delay code word.

At this time, the representation of the amount of delay for the first delay has been placed in the delay register **31** and is holding prior to being transferred to the delay 1 counter **34**. The delay control **32** provides an indication that there is a delay representation in the delay register **31** and that it will be transferred to the delay 1 counter **34**. This information is applied to the AND gate **72** and is labeled as a delay 1 in delay register signal. This signal passes through the OR gate **74** to inhibit the gate **75** so that the output of the AND gate **71** does not produce a signal at the D input of the D-type flip-flop **78**.

Instead, the signal from the AND gate **71** passes through the AND gate **72** to the D input of the D-type flip-flop **76**. On the subsequent clock pulse, which occurs at the character location rate, when the first graphic character data is placed in the delay 1 video buffer **46** and the associated first delay is transferred from the delay register **31** to the delay 1 counter **34**, the D-type flip-flop **76** is set to produce an output signal to the AND gate **79**.

The D-type flip-flop **76** remains stable in this condition until such time as the delay 1 counter **34** has counted down the amount of delay of the first delay and produces a delay 1 complete signal. This signal causes the delay 1 multiplexer control **42** to read out the character data from the delay 1 video buffer **46** through the appropriate multiplexers **50** and **51** or **51** to the appropriate shift registers **52** and **53** in the manner explained previously. This same delay 1 complete signal is applied to the AND gate **79** in the graphic fill-in control **60** causing a signal to be produced which clears the D-type flip-flop **76** to its reset condition and passes through the OR gate **82**. The output of the OR gate **82** is a loading signal to the fill-in video buffer **61** causing the data being read out of the delay 1 video buffer **46** for display also to be loaded into the fill-in video buffer **61**. The output of the OR gate **82** is also applied to the J input of the J-K flip-flop **85** causing it to be set on the next clock pulse thereto. The inhibiting connection of the OR gate **82** to the gate **84** prevents the delay 1 complete signal from reaching the K input of the J-K flip-flop **85**.

The output of the J-K flip-flop **85** to the AND gate **86** permits the next character location clock pulse applied thereto to cause the fill-in multiplexer control **63** to read out the character data in the fill-in video buffer **61** by way of the multiplexers **50** and **51** or **51** as explained previously. Also as explained previously, the fill-in video buffer **61** is repeatedly read out by the fill-in multiplexer control **63** causing the images of the first character to be displayed in succeeding normal locations until the J-K flip-flop **85** is reset by a delay complete signal. This resetting action occurs when the delay 2 counter **36** completes the countdown for the second delay and produces a delay 2 complete signal.

Thus, as shown herein, the system in accordance with the invention may be employed to display information in the form of overlapping or composite bargraphs which are esthetically pleasing and exhibit a high degree of accuracy. The capability of the system to superimpose displayed characters permits the construction of bargraphs which may have their upper edges posi-

tioned accurately to within a fraction of the dimension of a character. The apparatus permits the display of overlapping bargraphs by providing for filling-in at certain locations to provide continuity thus presenting readable arrangements of a multiplicity of bargraphs such as those illustrated in FIGS. **8** and **9.**

While there has been shown and described what is considered a preferred embodiment of the present invention, it will be obvious to those skilled in the art that various changes and modifications may be made therein without departing from the invention as defined by the appended claims.

What is claimed is:

1. A system for displaying characters on a video display means of the type producing images on a display surface by selectively writing on the display surface while repeatedly sweeping a raster scanline pattern over the display surface, said system including in combination

memory means for storing sata in a plurality of storage positions, each storage position corresponding to a normal location on the display surface, said data being character data representing a character to be displayed or being delay data representing an amount of delay associated with the character data stored in a particular storage position;

addressing means for reading out data from said memory means by addressing said storage positions in a predetermined sequence;

video signal generating means coupled to said memory means and operable in resonse to character data read out of said memory means to generate video signal patterns for producing images related to the character data on the display surface;

control means operable in response to character data being read out of a storage position in the memory means and in the absence of delay data associated therewith to cause the video signal generator to generate video signal patterns for producing an image of the character on the display surface in its normal location corresponding to the storage position in which the respective character data is stored;

delay means operable in response to character data being read out of a storage position in the memory means and having delay data associated therewith to cause the video signal generator to generate video signal patterns for producing an image of the character on the display surface in a location displaced from its normal location by an amount determined by the associated delay data; and

fill-in means including first means operable to detect the reading out of delay data associated with a change in the character data being read out of the memory means, and second means coupled to the first means and to the video signal generating means and operable in response to the detection of delay data associated with a change in the character data by the first means to cause the video signal generating means to repeat generating the video signal patterns for producing images related to the character data.

2. A system for displaying characters in accordance with claim **1** including

fill-in input detection means for causing said fill-in means to be activated in response to a predetermined input condition including the absence of character data in the storage position addressed next in sequence after addressing a storage position containing character data; and

fill-in deactivating means for causing said fill-in means to be deactivated in response to the subsequent reading out of character data from said memory means and the generating of video signal patterns in response thereto by the video signal generating means.

3. A system for displaying characters in accordance with claim **2** wherein

said fill-in means includes means for re-applying character data to said video signal generating means immediately subsequent to the generation of video signal patterns for producing images related to the character data by the video signal generating means during the tracing of a scanline whereby images related to the character data are repeated on the display surface contiguous the location of the images previously produced and displaced therefrom in the direction of tracing of individual scanlines.

4. A system for displaying characters in accordance with claim **3** wherein

said fill-in means includes

fill-in storage means coupled to said video signal generating means for receiving and storing character data therefrom;

fill-in storage control means for causing character data from said video signal generating means to be stored in said fill-in storage means; and

fill-in readout control means for causing character data stored in said fill-in storage means to be reapplied to said video signal generating means whereby said video signal generating means again generates video signal patterns for producing images related to the character data.

5. A system for displaying characters on a video display means of the type producing images on a display surface by selectively writing on the display surface while repeatedly sweeping a raster scanline pattern over the display surface, said system including in combination

memory means for storing coded data in a plurality of storage positions, each storage position corresponding to a normal location on the display surface, the storage positions being arranged in an array designating rows and columns of corresponding normal locations on the display surface, said coded data being a digital character code word representing a character to be displayed or being a digital delay code word representing an amount of delay;

memory addressing means for reading out digital code words from the storage positions designating a column in sequence for each tracing of a scanline;

a digital delay code word stored in a storage position being associated with the digital character code word stored in the adjacent storage position next in the sequence;

video signal generating means coupled to said memory means and operable in response to a digital character code word being read out of a storage position in the memory means to generate video signal patterns for producing an image of the character on the display surface;

control means operable in response to a digital character code word being read out of a storage position in the memory means and in the absence of an associated digital delay word being read out of the previous storage position in the sequence to cause the video signal generating means to generate video signal patterns for producing an image of the character on the display surface in timed relationship with signals for controlling the raster scanline pattern so that the image of the character is produced on the display surface in its normal location corresponding to the storage position in which the respective digital character code word is stored;

delay means operable in response to a digital delay code word being read out of a storage position in the memory means and an associated digital character code word being read out of the following storage position in the sequence to cause the video signal generating means to generate video signal patterns for producing an image of the character on the display surface in time relationship with signals for controlling the raster scanline pattern so that the image of the character is produced on the display surface in a location displaced from its normal location in the direction of tracing of the individual scanlines by an amount determined by the amount of delay represented by the digital code word; and

fill-in means including first means operable to detect a digital character code word being read out of a storage position in the memory means and a digital delay code word being read out of the following storage position in the sequence, and second means coupled to the first means and to the video signal generating means and operable in response to the detection of a digital character code word being read out of a storage position and a digital delay code word being read out of the following storage position to cause the video signal generating means to repeat generating the video signal patterns for producing an image of the character so that images of the character are repeatedly produced on the display surface in locations between the normal location for the image of the character and the displaced location for the image of the subsequent character associated with the digital delay code word.

6. A system for displaying characters in accordance with claim **5** including

first character data storage means for storing data related to a character read out of a storage position of said memory means;

and wherein

said delay means includes

delay data storage means for storing data representing an amount of delay read out of a storage position in said memory means;

delayed character data storage means for storing data relating to the associated character read out of the following storage position in sequence;

said fill-in means includes

fill-in character data storage means coupled to said first character data storage means and operable in response to a loading signal being applied thereto to receive and store data relating to the character being read out of the first character data storage means;

said control means includes

readout control means coupled to said first character data storage means and operable to read out the data relating to the character stored in the first character data storage means and to cause the video signal generating means to generate video signal patterns for producing an image as determined by the data relating to the character;

said delay means also includes

delay readout control means coupled to said delay data storage means and to said delayed character data storage means and operable to read out the data relating to the character stored in the delayed character data storage means upon completion of the amount of delay represented by the data stored in the delay data storage means and cause the video signal generating means to generate video signal patterns for producing an image as determined by the data relating to the character; and

said fill-in means also includes

fill-in detection means coupled to said fill-in character data storage means and operable in response to a digital character code word being read out of a storage position in the memory means and data relating to the character being stored in the first character data storage means and a digital delay code word being read out of the following storage position in the sequence and data representing the amount of delay being stored in said delay data storage means to produce a loading signal when said readout control means reads out the data relating to the character stored in the first character data storage means thereby storing data relating to said character in the fill-in character data storage means; and

fill-in readout control means coupled to the fill-in character data storage means and operable to repeatedly read out the data relating to the character stored in the fill-in character data storage means and cause the video signal generating means repeatedly to generate video signal patterns for producing an image as determined by the data relating to the character, the repeated reading out of data being terminated in response to completion of the amount of delay represented by the data stored in the delay data storage means.

7. A system for displaying characters in accordance with claim **6** including

input decoding means coupled to said memory means and operable to produce a delay signal in response to a digital delay code word being read out of said memory means;

and wherein

said delay means includes

delay input control means coupled to said input decoding means and operable in response to said delay signal to cause data representing the amount of delay to be stored in said delay data storage means and also operable in response to said delay signal to cause subsequent data relating to the associated character to be stored in said delayed character data storage means; and

said delay readout control means includes

counting means coupled to said delay data storage means for receiving a count representative of the amount of delay stored in the delay data storage means, the count representing a number of incremental divisions of the dimension of a location on the display surface along the direction in which the scanlines are traced;

said counting means being operable to receive periodic clock pulses and to produce an indication when the number of clock pulses received equals the count received from said delay data storage means;

clock pulse generating means for applying periodic clock pulses to said counting means when activated, the clock pulses occurring at the rate of one clock pulse for the tracing of a scanline through one incremental division;

counting control means for applying the count representative of the amount of delay stored in the delay data storage means to the counting means and for activating said clock pulse generating means when data relating to the associated character is loaded into said delayed character data storage means; and

delay readout means operable in response to said indication to cause the data relating to the character stored in the delayed character data storage means to be read out of the delayed character data storage means and the video signal generating means to generate video signal patterns for producing an image as determined by the data relating to the character.

8. A system for displaying characters in accordance with claim **7** wherein

said fill-in readout control means includes means coupled to said fill-in detection means and operable in response to said loading signal to read out the data relating to the character stored in said fill-in character data storage means in timed relationship with the tracing of a scanline so that the images relating to the character data are produced in successive normal locations along the scanline, said means being coupled to said counting means and being operable in response to an indication therefrom to terminate further reading out of character data from the fill-in character data storage means.

9. A system for displaying characters in accordance with claim **8** wherein

said fill-in detection means includes

fill-in delay detection means coupled to said delay data storage means and to said counting means and operable in response to a first digital delay code word being read out of a storage position in the memory means, an associated first digital character code word being read out of the next storage position, a second digital delay code word being read out of the next storage position, and an associated second digital character code word being read out of the next storage position, to produce a loading signal in response to the indication from said counting means when the counting means has counted the number of clock pulses equal to the count representative of the amount of delay of the first digital delay code word.

10. A system for displaying characters in accordance with claim **8** wherein

said video signal generating means includes

video output means coupled to said first character data storage means, said delayed character data storage means, and said fill-in character data storage means and operable to convert character data applied thereto to a stream of video signals in timed relationship with the tracing of a scanline;

said control means includes

output control means coupled to said video output means and operable to apply the data stored in the first character data storage means thereto in timed relationship with the tracing of a scanline;

said fill-in readout control means includes

fill-in control means coupled to said video output means and operable to apply the data stored in the fill-in character data storage means thereto in timed relationship with the tracing of a scanline to cause the images to be produced in successive normal locations on the display surface; and

the delay readout means of the delay readout control means is coupled to said video output means and is operable to apply the data stored in the delayed character data storage means thereto in response to said indication from said counting means;

whereby upon time coincidence of data being applied to the video output means from more than one of said data storage means, the stream of video signals generated by the video output means consists of signals for causing images related to the characters to be superimposed.

11. A system for displaying characters in accordance with claim **10** wherein said video output means includes

a shift register having a plurality of stages arranged in succession, the number of stages being equal to the number of incremental divisions of the dimension of a location on the display surface along the direction in which the scanlines are traced, each stage of said shift register having an output terminal, a signal input terminal, and a clock input terminal;

a like plurality of triads of AND gates, each triad being associated with a different stage of said shift register, a first input connection of the first AND gate of each triad being connected together and coupled to said output control means of said control means, a second input connection of the first AND gate of each triad being coupled to the first character data storage means, a first input connection of the second AND gate of each triad being connected together and coupled to said fill-in control means of the fill-in readout control means, a second input connection of the second AND gate of each triad being coupled to the fill-in character data storage means, a first input connection of the third AND gate of each traid being connected together and coupled to said delay readout means of the delay readout control means, and a second input connection of the second AND gate of each triad being coupled to the delayed character data storage means;

a like plurality of first OR arrangements each associated with a different triad of AND gates, each first OR arrangement having a first input connection connected to the output connection of the first AND gate of its associated triad, a second input

connection connected to the output connection of the second AND gate of its associated triad, and a third input connection connected to the output connection of the third AND gate of its associated triad;

a like plurality minus one of second OR arrangements each associated with a different stage of the shift register except for the first stage in the succession, each second OR arrangement having a first input connection connected to the output connection of the associated first OR arrangement, a second input connection connected to the output terminal of the previous stage in the succession, and an output connection connected to the signal input terminal of its associated stage, the output connection of the first OR arrangement associated with the first stage in the succession being connected to the signal input terminal of its associated stage;

means connected to the clock input terminals for applying clock pulses thereto, the clock pulses occurring at the rate of one clock pulse for the tracing of a scanline through one incremental division;

a video signal output terminal connected to the output terminal of the final stage of the succession; and

fill-in connection means for coupling the output connection of each first OR arrangement to said fill-in character data storage means.

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