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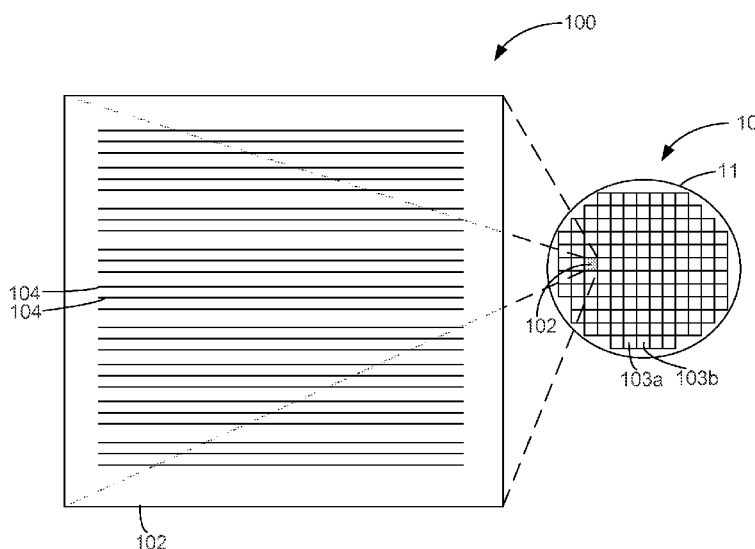


FIG. 1

(57) **Abstract:** Embodiments of the present disclosure describe materials and processes for filling feature gaps of semiconductor devices using an organosilane material in a chemical vapor deposition (CVD) chamber. The process may include placing a semiconductor device in a CVD chamber. The device may have a surface with a number of narrow and high aspect ratio feature gaps on the surface. An organosilane material may be introduced into the CVD chamber. The organosilane material may be deposited on the surface, wherein the feature gaps are filled with the organosilane material. The organosilane material may be cross-linked using oxygen radicals to provide a crosslinked organosilane material. The cross-linked organosilane material may be cured using a radiation source. Other embodiments may be described and/or claimed.

GAP FILLING MATERIAL AND PROCESS FOR SEMICONDUCTOR DEVICES

Field

Embodiments of the present disclosure generally relate to the field of integrated
5 circuits, and more particularly, to a feature gap fill material and process for semiconductor devices.

Background

As the size of semiconductor devices becomes smaller and with the delay in
development of extreme ultraviolet (EUV) lithography, patterning schemes using conventional
10 lithography and multiple patterning cycles per layer may be required. Some of these patterning schemes rely on the ability to fill features with dielectric materials. Challenges may arise related to defects in filled feature gaps as a result of the dielectric materials and methods used to fill the gaps. In particular, as the gap size shrinks and/or aspect ratios increase, current materials and methods, such as high volume manufacturing (HVM) EUV lithography may result in voids
15 within the materials deposited within the gaps. In HVM EUV lithography, multiple lithographic printing steps per layer may be used for improved resolution and registration for scaled dimensions. However, this multi-layer method still may result in voids, which are a problem for backend processes. In addition to the potential void problems in multi-layer lithography, the materials used, such as silicon carbide (SiC) and silicon nitride (SiN), may be incompatible with
20 backend requirements because of the need of these materials for high temperature processing (annealing) and oxidation concerns associated with flowable oxides.

Brief Description of the Drawings

Embodiments will be readily understood by the following detailed description in
conjunction with the accompanying drawings. To facilitate this description, like reference
25 numerals designate like structural elements. Embodiments are illustrated by way of example and not by way of limitation in the figures of the accompanying drawings.

FIG. 1 schematically illustrates a top view of an example die in wafer form and in singulated form, in accordance with some embodiments.

FIG. 2 schematically illustrates a cross-section side view of an integrated circuit
30 (IC) assembly, in accordance with some embodiments.

FIG. 3 illustrates schematics of cross-sections of semiconductor devices, showing defect types in gaps filled by step-wise atomic layer deposition of multiple layers.

FIG. 4 illustrates a gap fill material having resistance to oxide etch and subsequent metal deposition, in accordance with some embodiments.

FIG. 5 illustrates a process to fill gaps of a semiconductor device with an organosilane material using a chemical vapor deposition chamber, in accordance with some
5 embodiments.

FIG. 6 illustrates a semiconductor manufacturing process using an organosilane material as a feature gap fill material, in accordance with some embodiments.

FIG. 7 illustrates a semiconductor device with an organosilane material deposited in gaps of the semiconductor device, in accordance with some embodiments.

FIG. 8 illustrates a system with a semiconductor device with an organosilane
10 material deposited in gaps of the semiconductor device, in accordance with some embodiments.

Detailed Description

Embodiments of the present disclosure describe processes and materials that may be used to fill gaps in semiconductor devices with an organosilane type material that is cross-
15 linked (e.g., annealed) via oxygen and radiation-cured to provide void-free fills in such gaps. In the following detailed description, reference is made to the accompanying drawings which form a part hereof, wherein like numerals designate like parts throughout, and in which is shown by way of illustration embodiments in which the subject matter of the present disclosure may be practiced. It is to be understood that other embodiments may be utilized and structural or logical
20 changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense, and the scope of embodiments is defined by the appended claims and their equivalents.

For the purposes of the present disclosure, the phrase “A and/or B” means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase “A, B, and/or C” means
25 (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C).

The description may use perspective-based descriptions such as top/bottom, side, over/under, and the like. Such descriptions are merely used to facilitate the discussion and are not intended to restrict the application of embodiments described herein to any particular orientation.

The description may use the phrases “in an embodiment,” or “in embodiments,”
30 which may each refer to one or more of the same or different embodiments. Furthermore, the

terms “comprising,” “including,” “having,” and the like, as used with respect to embodiments of the present disclosure, are synonymous. The term “coupled” may refer to a direct connection, an indirect connection, or an indirect communication.

The term “coupled with,” along with its derivatives, may be used herein.

5 “Coupled” may mean one or more of the following. “Coupled” may mean that two or more elements are in direct physical or electrical contact. However, “coupled” may also mean that two or more elements indirectly contact each other, but yet still cooperate or interact with each other, and may mean that one or more other elements are coupled or connected between the elements that are said to be coupled with each other. The term “directly coupled” may mean that two or
10 more elements are in direct contact. By way of example and not limitation, “coupled” may mean two or more elements or devices are coupled by electrical connections on a printed circuit board such as a motherboard for example. By way of example and not limitation, “coupled” may mean two or more elements/devices cooperate and/or interact through one or more network linkages such as wired and/or wireless networks. By way of example and not limitation, a computing
15 apparatus may include two or more computing devices “coupled” by one or more network linkages.

In various embodiments, the phrase “a first feature formed, deposited, or otherwise disposed on a second feature” may mean that the first feature is formed, deposited, or disposed over the second feature, and at least a part of the first feature may be in direct contact
20 (e.g., direct physical and/or electrical contact) or indirect contact (e.g., having one or more other features between the first feature and the second feature) with at least a part of the second feature.

As used herein, the term “module” may refer to, be part of, or include an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared,
25 dedicated, or group) and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational logic circuit, state machine, and/or other suitable components that provide the described functionality.

The terms “gap” or “feature gap,” and the plurals thereof, may refer to any number of feature gaps on a semiconductor device such as trenches, lines, and/or holes of
30 various lengths, depths, shapes, sizes, and aspect ratios.

With continued device scaling, the need for a compositional variety of dielectric

materials that provide permanent or sacrificial fills in high aspect ratios (e.g., with a depth significantly greater than a width of the fill and on the order of 3:1 or greater) for interconnect layers may have increased. This increase in need may be driven by delays in engineering a high volume manufacturing (HVM) extreme ultraviolet (EUV) lithography solution for improved

5 resolution at the smaller pitches of a scaled device. In HVM EUV lithography, multiple lithographic printing steps may be used for the layers, using existing lithographic capability, and may be used for improved resolution and registration for scaled dimensions. In some methods, permanent and sacrificial dielectric fill materials may allow for patterning in one area of the layer while another area remains protected. Historically, flowable oxide fill materials, such as
10 silicon carbide (SiC) and silicon nitride (SiN) have been for similar frontend patterning processes and are deposited using chemical vapor deposition (CVD) or atomic layer deposition. However, incompatibilities with backend requirements in these materials, such as the presence of voids/seams, their need for high temperature processing or annealing, as well as oxidation concerns associated with flowable oxides, may drive the need for so-called "bottom-up" fill
15 materials.

Bottom-up fill materials may include α -SiC:H, α -SiOC:H, α -SiCN:H, and α -SiN:H materials. For α -SiOC:H films, etch selectivity may be influenced not only by the carbon content but also by the type of Si-C bonding. Maximizing the amount of bridging -Si-C-Si-C-Si-
20 bonding may provide better etch selectivity than a film based on Si-O-Si networks with terminal alkyl groups. Likewise, materials with lengthy alkyl chains separating the silicon (Si) atoms may behave similar to carbon hard masks and may suffer greatly during patterning. In some embodiments, a flowable α -SiOC:H film may be used as a gap fill material in which the building blocks are saturated carbo-silane rings of alternating Si and carbon (C) atoms that are linked by oxygen (O) bridges. If the repeat unit is kept low, the material may fill aggressive features, and
25 then the material may be cross-linked and annealed with ultraviolet (UV) irradiation to achieve desirable film properties.

In some embodiments, a method of filling gaps in semiconductor devices may include depositing a gap fill α -SiCO:H material in high aspect ratio patterning features, where the deposited material is void-free and provides etch selectivity to other dielectric and hard mask
30 patterning materials. In some embodiments, a CVD chamber may be used. In some embodiments, a cyclic carbo-silane precursor consisting of alternating Si-C bonds in a 1:1 atomic

ratio (e.g., -Si-C-Si-C-Si-) may be used. In some embodiments, the precursor may be used in the presence of oxygen radicals. There are numerous types of CVD chambers that may be used. In some embodiments, a plasma-enhanced chemical vapor deposition (PECVD) chamber may be used. In some embodiments, a cyclic carbo-silane starting material (precursor) may be used, where the precursor consists of alternating Si-C bonds in a 1:1 atomic ratio (-Si-C-Si-C-Si-). In some embodiments, the precursor may not contain any terminal alkyl hydrocarbon or -SiH₃ groups. In some embodiments, the precursor is used in the presence of oxygen radicals, which may be generated by a remote system and fed into a chamber. The film may be formed by exposing the starting material to oxygen radicals generated by a remote plasma system (RPS) such that Si-H bonds of the silicon precursor are replaced by oxygen radicals that act as bridges between rings without damaging the ring structure itself.

In some embodiments, the precursor consists of a cyclic carbo-silane with alternating Si-C bonds in a 1:1 atomic ratio (-Si-C-Si-C-Si-), where the precursor may not contain any terminal alkyl hydrocarbon or -SiH₃ groups and may contain one or two alkoxy groups (-OR) bonded to the silicon atoms of the ring structure. A film may be formed by stoichiometrically reacting an alkoxy derivative with a cyclic carbo-silane in the presence of a catalyst. In this embodiment, a RPS may not be needed to generate oxygen radicals since oxygen is present in the alkoxy starting material. The reaction may be in a PECVD chamber.

If the process is done at temperature of less than about 100 °C, oligomers of the starting material may condense on the substrate surface. The film may be annealed in an oxygen laden environment at a temperature of about 300 °C or less to crosslink the film. The film may be cured with UV radiation of a wavelength between 200 nm - 400 nm to remove any physio-absorbed water and remaining Si-H bonds, and to make the film hydrophobic by the formation of Si-CH₃ groups.

In some embodiments, a method of filling gaps in semiconductor devices may include filling device designs with patterning of 30 nanometers (nm) or less pitch structures with permanent or sacrificial dielectric materials that are free of voids or seams and can be tailored for patterning selectivity, namely for etch and chemical-mechanical planarization/polishing (CMP). In some embodiments, the designs may have patterning with gaps of less than 20 nm. The device design requirements for the filling material may be more stringent than what is possible with current materials and processes. In some embodiments, a method of filling gaps in

semiconductor devices may include filling device features of some designs with an aspect ratio (e.g., of depth:width) that is greater than about 8:1 and with feature openings of less than about 20 nm, wherein the designs may exhibit re-entrant profiles. Device designs of such parameters may make the use of techniques such as high density plasma (HDP) difficult or impractical. For pattering schemes in which the gap fill material remains in the final product, (laser diode) LD or CVD stepwise processes may not be used due to the formation of voids or seams that will create shorts between metal contacts.

FIG. 1 schematically illustrates a top view of an example die 102 in wafer form 10 and in singulated form 100, in accordance with some embodiments. In some embodiments, the die 102 may be one of a plurality of dies (e.g., dies 102, 103a, 103b) of a wafer 11 composed of semiconductor material such as, for example, silicon or other suitable material. The plurality of dies may be formed on a surface of the wafer 11. Each of the dies may be a repeating unit of a semiconductor product that includes one or more transistor assemblies and/or other device assemblies that include feature gaps filled with the materials and using the processes described herein and as illustrated in FIGS. 4-7. For example, the die 102 may include circuitry having transistor structures 104 and/or other device structures where the feature gaps may be filled with the organosilane materials using the processes described herein for deposition, crosslinking, and curing of the organosilane material. The organosilane materials may be permanent fills remaining in the final product or sacrificial fills used during manufacturing of the semiconductor product.

Although the transistor structures 104 are depicted in rows that traverse a substantial portion of the die 102 in FIG. 1 for the sake of simplicity, it is to be understood that the transistor structures 104 may be configured in any of a wide variety of other suitable arrangements on the die 102 in other embodiments, including, for example, vertical and horizontal features having much smaller dimensions than depicted. After a fabrication process of the semiconductor product embodied in the dies is complete, the wafer 11 may undergo a singulation process in which each of the dies (e.g., die 102) is separated from one another to provide discrete “chips” of the semiconductor product. The wafer 11 may be any of a variety of sizes. In some embodiments, the wafer 11 has a diameter ranging from about 25.4 mm to about 450 mm. The wafer 11 may include other sizes and/or other shapes in other embodiments. According to various embodiments, the transistor structures 104 may be disposed on a

semiconductor substrate in wafer form 10 or singulated form 100. The transistor structures 104 described herein may be incorporated in a die 102 for logic or memory, or combinations thereof. In some embodiments, the transistor structures 104 may be part of a system-on-chip (SoC) assembly.

5 **FIG. 2** schematically illustrates a cross-section side view of an integrated circuit (IC) assembly 200, in accordance with some embodiments. In some embodiments, the IC assembly 200 may include one or more dies (hereinafter “die 102”) electrically and/or physically coupled with a package substrate 121. In some embodiments, the package substrate 121 may be electrically coupled with a circuit board 122, as can be seen. In some embodiments, an integrated
10 circuit (IC) assembly 200 may include one or more of the die 102, package substrate 121 and/or circuit board 122, according to various embodiments. Embodiments described herein for an organosilane feature gap fill material and process for filling may be incorporated in the one or more die 102, according to various embodiments.

The die 102 may represent a discrete product made from a semiconductor material
15 (e.g., silicon) using semiconductor fabrication techniques such as thin film deposition, lithography, etching and the like used in connection with forming CMOS devices. In some embodiments, the die 102 may be, include, or be a part of a processor, memory, SoC or ASIC. In some embodiments, an electrically insulative material such as, for example, molding compound or underfill material (not shown) may encapsulate at least a portion of the die 102 and/or die-
20 level interconnect structures 106.

The die 102 can be attached to the package substrate 121 according to a wide variety of suitable configurations including, for example, being directly coupled with the package substrate 121 in a flip-chip configuration, as depicted. In the flip-chip configuration, an active side, S1, of the die 102 including circuitry is attached to a surface of the package substrate
25 121 using die-level interconnect structures 106 such as bumps, pillars, or other suitable structures that may also electrically couple the die 102 with the package substrate 121. The active side S1 of the die 102 may include active devices such as, for example, transistor devices. An inactive side, S2, may be disposed opposite to the active side S1, as can be seen.

The die 102 may generally include a semiconductor substrate 102a, one or more
30 device layers (hereinafter “device layer 102b”) and one or more interconnect layers (hereinafter “interconnect layer 102c”). The semiconductor substrate 102a may be substantially composed of

a bulk semiconductor material such as, for example silicon, in some embodiments. The device layer 102b may represent a region where active devices such as transistor devices are formed on the semiconductor substrate. The device layer 102b may include, for example, transistor structures such as channel bodies and/or source/drain regions of transistor devices. The interconnect layer 102c may include interconnect structures (e.g., electrode terminals) that are configured to route electrical signals to or from the active devices in the device layer 102b. For example, the interconnect layer 102c may include horizontal lines (e.g., trenches) and/or vertical plugs (e.g., vias) or other suitable features to provide electrical routing and/or contacts.

In some embodiments, the die-level interconnect structures 106 may be electrically coupled with the interconnect layer 102c and configured to route electrical signals between the die 102 and other electrical devices. The electrical signals may include, for example, input/output (I/O) signals and/or power/ground signals that are used in connection with operation of the die 102.

In some embodiments, the package substrate 121 is an epoxy-based laminate substrate having a core and/or build-up layers such as, for example, an Ajinomoto Build-up Film (ABF) substrate. The package substrate 121 may include other suitable types of substrates in other embodiments including, for example, substrates formed from glass, ceramic, or semiconductor materials.

The package substrate 121 may include electrical routing features configured to route electrical signals to or from the die 102. The electrical routing features may include, for example, pads or traces (not shown) disposed on one or more surfaces of the package substrate 121 and/or internal routing features (not shown) such as, for example, trenches, vias or other interconnect structures to route electrical signals through the package substrate 121. For example, in some embodiments, the package substrate 121 may include electrical routing features such as pads (not shown) configured to receive the respective die-level interconnect structures 106 of the die 102.

The circuit board 122 may be a printed circuit board (PCB) composed of an electrically insulative material such as an epoxy laminate. For example, the circuit board 122 may include electrically insulating layers composed of materials such as, for example, polytetrafluoroethylene, phenolic cotton paper materials such as Flame Retardant 4 (FR-4), FR-1, cotton paper and epoxy materials such as CEM-1 or CEM-3, or woven glass materials that are

laminated together using an epoxy resin prepreg material. Interconnect structures (not shown) such as traces, trenches, or vias may be formed through the electrically insulating layers to route the electrical signals of the die 102 through the circuit board 122. The circuit board 122 may be composed of other suitable materials in other embodiments. In some embodiments, the circuit board 122 is a motherboard.

Package-level interconnects such as, for example, solder balls 112 may be coupled to one or more pads (hereinafter “pads 110”) on the package substrate 121 and/or on the circuit board 122 to form corresponding solder joints that are configured to further route the electrical signals between the package substrate 121 and the circuit board 122. The pads 110 may be composed of any suitable electrically conductive material such as metal including, for example, nickel (Ni), palladium (Pd), gold (Au), silver (Ag), copper (Cu), and combinations thereof. Other suitable techniques to physically and/or electrically couple the package substrate 121 with the circuit board 122 may be used in other embodiments.

The IC assembly 200 may include a wide variety of other suitable configurations in other embodiments including, for example, suitable combinations of flip-chip and/or wire-bonding configurations, interposers, multi-chip package configurations including system-in-package (SiP) and/or package-on-package (PoP) configurations. Other suitable techniques to route electrical signals between the die 102 and other components of the IC assembly 200 may be used in some embodiments.

FIG. 3 illustrates schematics of cross-sections 300, 310, 320, 330 of semiconductor devices 300, 310, 320, 330, showing defect types 306 in gaps 305 filled by step-wise atomic layer deposition of multiple layers 304. The ALD layers 304 are deposited in a gap 305 of a semiconductor substrate 302 (e.g., silicon or another suitable substrate). One or more types of defects may be formed in the ALD layers. For example, the first cross section 300 illustrates a through defect 306.1 in the middle of the ALD deposition layers 304 that extends into the gap 305 in the semiconductor substrate 302. The second cross section 310 illustrates a middle gap 306.2 in the middle of the ALD layers 304. The third cross section 320 illustrates an intermittent gap 306.3 in the middle of the ALD deposition layers 304. The fourth cross section 330 illustrates the middle gap 306.2 of cross section 310 turned 90 degrees as illustrated by the dotted line in semiconductor device 320 and with metal layers 308 coupled to the substrate 302 and/or one or more of the ALD layers 304. When metal layers 308 are added, metal may fill a

portion of the middle gap 306.2 to form fill 309, thereby causing a short circuit through the fill 309.

Currently available methods may attempt to remove the various gaps 306.1, 306.2, and/or 306.3 by using etch back and re-deposition. However, this approach may be costly and still may not remove the gaps in the middle of the ALD layers 304. Furnace CVD deposited SiC and SiN films generally require an excess of 600 °C for extended times (greater than one hour), which is not desirable for the backend thermal budget and is not compatible with the back end of line applications. Moreover, thermal anneal temperatures of greater than about 450 °C may cause significant shrinkage in the gap fill material causing the material to pull away from the feature sidewall or form a tear within the fill.

In some embodiments, the gap fill material may be thermally stable at 450 °C. Generally, at this temperature, some organic-based fill materials may be unsuitable as a gap fill material. In some embodiments, the gap fill material may be compatible with dry plasma etches for carbon hard mask (CHM) patterning, which may preclude the use of some organic-based fill materials. In some embodiments, the gap fill material may have etch-selectivity of greater than about 7:1 relative to adjacent materials. For example, if an adjacent line is filled with an oxide, the other material must survive the oxide etch and subsequent patterning for that line to be filled with other materials.

FIG. 4 illustrates cross-sectional views of an example semiconductor device 401 at various stages 400, 410, 420, and 430 of a gap fill process, in accordance with some embodiments. The gap fill process may use a gap fill material 406 having resistance to oxide etch and subsequent metal deposition, in accordance with some embodiments. In FIG. 4, the semiconductor device 401 may include a semiconductor substrate 402 having feature gaps 407.1, 407.2, 407.3 with various materials deposited therein. In some embodiments, as illustrated by semiconductor device 401, one or more feature gaps 407.1, 407.3 in the semiconductor substrate 402 may have an oxide 404.1 deposited therein. Additionally, a gap fill material 406 may be deposited in an adjacent gap 407.2. In some embodiments, a material 405 may be deposited in a feature gap 407.2 below the gap fill material 406. The material 405 may be tungsten in some embodiments. The material 405 may be another dielectric material or metal alloy in some embodiments. The material 405 may include any interconnect or work function metal. Non-limiting examples of interconnect or work function metals include tungsten, titanium, aluminum,

copper, or cobalt, or alloy thereof. After an oxide etch to remove oxide 404.1 from the gaps 407.1, 407.3, there may be open gaps 404.2 without any oxide material as shown at 410, and the gap fill material 406 may remain after the oxide etch. As shown at 420, a metal 404.3 may be deposited in the open gaps 404.2 where the oxide was removed, while the gap fill material 406 remains in one or more gaps. As shown at 430, the metal 404.3 may be partially removed and another material 404.5 may be deposited over the metal 404.3 in the gaps. The material 404.5 may be another dielectric material or metal alloy. The material 404.5 may be a dielectric or a conductor material, depending on desired electrical routing.

In some embodiments, the gap fill material described herein (e.g., gap fill material 406) may be an organosilane deposited in gaps using a spin-on process and/or a vapor phase flowable process. In some embodiments, vapor phase processing may be used for “leave behind” films. In spin-on processes, an organosilane solution spin cast film may be susceptible to contamination through residual catalyst used during oligomerization, contamination from ambient oxidation and hydrolysis at multiple steps in the manufacturing process of the oligomer, and/or costly equipment and chemical handling costs. For example, an organosilane oligomer solution used as a spin cast film requires inert synthesis and manufacturing infrastructure not only for fundamental contamination concerns to maintain product quality, but specifically to address the safety hazards with silicon hydride based molecules, which may spontaneously and violently react with air/moisture.

Generally, an organosilane oligomer is built from organosilane small molecule, which is termed a precursor or monomer. The manufacture of an organosilane precursor is performed in an inert environment with care to eliminate air/moisture due to the pyrophoric/highly reactive nature of the starting materials. There are several synthetic strategies that may be employed to produce an organosilane precursor, where the specific concerns held by the electronics industry are associated with the impurities that are present. For example, chlorine/halogen contamination, from a silicon halogen reagent, can occur through several divergent synthesis techniques, such as from a Grignard or Wurtz type reaction. Additionally, the catalyst utilized can lead to trace metal contamination (e.g., magnesium (Mg), sodium (Na), lithium (Li)). An organosilane may be produced through a variety of polymerization methods involving an organosilane precursor, where there are also contamination and safety concerns that need to be obviated to maximize the quality. Additional polymerization process steps may be

needed to transform the stock oligomer solution into a factory ready solution, which involves formulating the stock to the correct viscosity, filtration to remove particles and insoluble trace metals, and performing quality control (QC) validation of the film on a track.

Because organosilane films may require high temperature or specific
5 environments and tracks are typically limited in their baking options or control (the preferred operational model baking < 200 °C in ambient air on a hotplate), additional tooling may be used. With vapor phase flowable films, in contrast, the gap fill material may be formed directly from the raw chemicals, or solutions containing low molecular weight oligomers of the raw materials, in a controlled environment. In a multiple-chamber tool, gap fill deposition and anneal may be
10 performed on a single tool. Spin cast capability may require additional infrastructure and special tooling for facilities and track equipment, namely the introduction of dedicated drains for the water/air reactive oligomeric organosilane and copious use of solvents for to wash track cups and rinse drains in order to minimize risk of fire or clogging.

In some embodiments, the use of a vapor phase flowable process to form a gap fill
15 directly from the starting raw materials provides manufacturing flexibility because parameters such as molecular weight, polydispersity, atomic composition, and formulation/thickness may be changed relatively quickly. With spin-cast, any changes to the molecular weight, polydispersity, atomic composition, and formulation/thickness may require lengthy lead times and significant development from the precursor supplier.

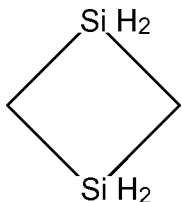
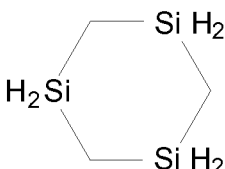
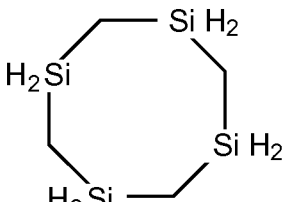
20 In some embodiments, the formation of an α -SiOC:H film may be based, at least in part, on a spin-on dielectric (SOD) process. A SOD process may include, at least in part, reacting a trisilacyclohexane (TSCH) with an alkoxide derivative of TSCH in the presence of a boron catalyst in toluene. The resulting film may be annealed in an oxygen containing atmosphere and UV cured (e.g., with a wavelength of about 200 nm - 400 nm), resulting in a film
25 with a modulus of elasticity of equal to or less than about 30 gigapascals (GPa) and etch selective to oxide.

The spin-on process described herein may require modifications to current manufacturing processes. For example, the use of a boron catalyst may preclude the use of the resulting films in electrically sensitive areas due to concerns over boron activation as an
30 electrical dopant. The casting solvent, toluene, possesses low vapor pressure and requires dedicated drains, solvent rinse steps, and the manufacture of custom plastic parts in the track

module that are toluene compatible. Additionally, a fundamental synthesis route uses precursors, which are structurally viable for use in CVD applications, to build solution borne oligomers. In some embodiments, small molecules may be used and a process may not require a polymerization step to create oligomers, thus saving cost and simplifying a supply chain.

5 In some embodiments, gap fill materials may be based on saturated carbosilane rings with alternating Si and C atoms. A carbosilane may be referred to as an organosilane. Such materials may include 1,3-disilacyclobutane (DSCB) and 1,3,5-trisilacyclohexane (TSCH), both of which may be used as a CVD precursor for SiC films. Another such material may include 1,3,5,7-tetrasilacyclooctane (TSCO). Table 1 provides structures and properties of DSCB,
10 TSCH, and TSCO.

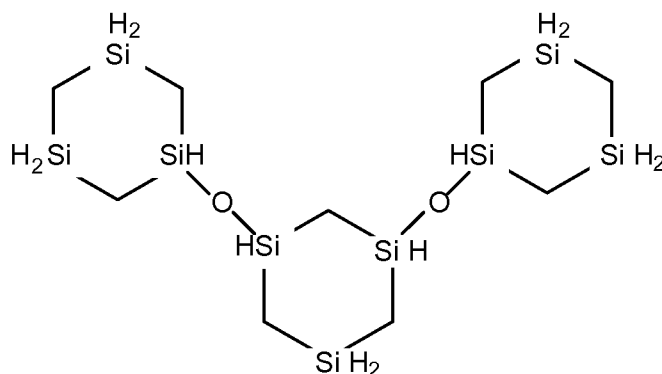
Table 1

1,3-disilacyclobutane (DSCB) Formula: $C_2H_8Si_2$ CAS No.: 287-55-8 Boiling point: 64.4 °C Vapor pressure: 176.8 mmHg at 25 °C  Structure I	1,3,5-trisilacyclohexane (TSCH) Formula: $C_3H_{12}Si_3$ CAS No.: 291-27-0 Boiling point: 135 °C Melting point: -10 °C Vapor pressure: 10.7 mmHg at 25 °C  Structure II	1,3,5,7-tetrasilacyclooctane (TSCO) Formula: $C_4H_{16}Si_4$  Structure III
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In an embodiment, a precursor may be comprised of a monomer (neat or dissolved in an appropriate solvent), such as the monomers of Table 1. Because oxygen radicals
15 will react with the most facile Si-H bonds, the resultant molecular structure may be linear or hyper-branched.

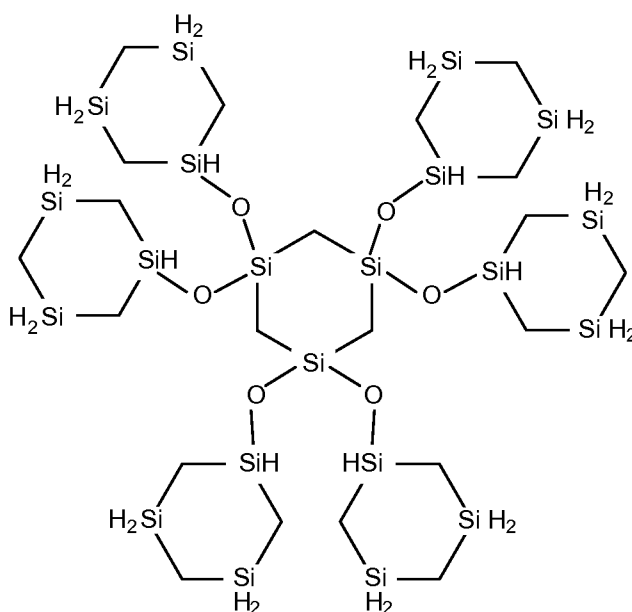
In an embodiment, the monomers of Table 1 may be pre-polymerized from a starting material to produce a controlled molecular structure using a suitable catalyst. This approach may result in a lower amount of additional polymerization required in a chamber. In an
20 example, a short chained molecule may be formed from the monomers of Table 1 as illustrated

by **Structure IV** for TSCH monomer.



Structure IV

In an example, a dendritic molecule (oligomer) may be pre-formed from TSCH
5 prior to being introduced into a PECVD chamber as illustrated by Structure V.



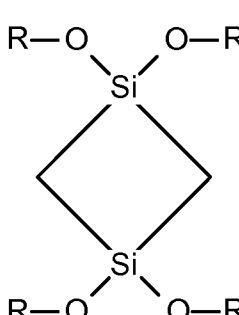
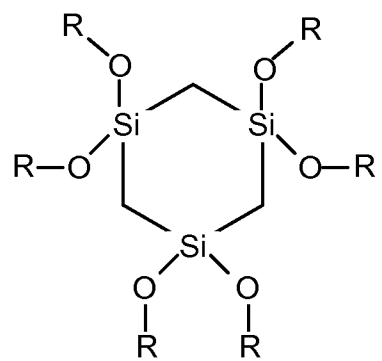
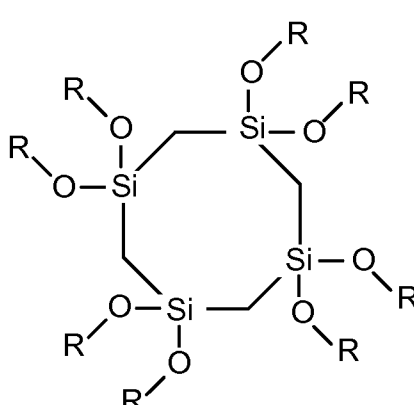
Structure V

The oligomeric Structures IV and V may be formed in a CVD chamber or may be formed in another reaction chamber and pushed into a CVD chamber using an inert gas.

10 In some embodiments, an alkoxy derivative of the compounds of Table 1 may be used to fill gaps. Table 2 illustrates examples of alkoxy derivatives of the compounds from Table 1. Generally, the R group may be an alkyl group such as methyl, ethyl, propyl, butyl, pentyl, hexyl, heptyl, octyl, nonyl, decyl, undecyl, dodecyl, and the like, for example. In some embodiments, an alkoxy compound of Table 2 may be stoichiometrically reacted with a

compound of Table 1 to form a film to fill feature gaps of a semiconductor device. In some embodiments, a mixture of two or more compounds from Tables 1 and 2 may be reacted to form a film. In some embodiments, coreactants may be stoichiometrically reacted where the primary reactant is from Table 1, and the secondary reactant is an alkoxy version from Table 2 of the primary reactant. For example, a stoichiometric reaction may be $6A + B = C$, where A is from Table 1 and B is from Table 2. A RPS may not be needed to generate oxygen radicals since oxygen is present in the alkoxy starting material. The reaction may be in a CVD chamber.

Table 2

1,1,3,3 -Tetraalkoxy-1,3-disilacyclobutane Formula: $C_xH_yO_4Si_2$  Structure VI	1,1,3,3,5,5-Hexaalkoxy-1,3,5-trisilacyclohexane Formula: $C_xH_yO_6Si_3$  Structure VII	1,1,3,3,5,5,7,7-Octaalkoxy-1,3,5,7-tetrasilacyclooctane Formula: $C_xH_yO_8Si_4$  Structure VIII
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In some embodiments, a carbosilane precursor may be delivered to a PECVD chamber by using a push gas, such as helium (He) or argon (Ar), and managed with a liquid flow controller (LFC). After a precursor is pushed into a chamber, Si-H bonds on a carbosilane ring may react with oxygen radicals that are generated using a remote plasma system (RPS). The processing conditions may allow for the reaction to occur while keeping the precursor rings intact. During a successful chemical reaction, the rings may be bridged via $-Si-O-Si-$ linkages, as illustrated by Structures III and IV, by way of example and not limitation. The reaction may produce a distribution of low molecular weight oligomers that will condense on a substrate that is kept at a temperature that is equal to or less than about 100 °C. These oligomers may fill gaps in a substrate without voids due to liquid/flowable properties of the deposited oligomeric

material. In some embodiments, a carbosilane precursor may be a mixture of different monomers.

After a film is deposited on a substrate, the film may be annealed in the presence of oxygen at a temperature of between 200 °C and 350 °C and then undergo a UV cure (200 nm to 400 nm) to set the final film properties.

FIG. 5 illustrates a process 500 to fill gaps of a semiconductor device with an organosilane material using a chemical vapor deposition chamber, in accordance with some embodiments.

At **502** of the process 500, a semiconductor device is placed into a chemical vapor deposition (CVD) chamber. The semiconductor device has a surface with feature gaps on the surface. The gaps are to be filled with sacrificial or permanent fill material. In some embodiments, the CVD chamber is a plasma enhanced chemical vapor deposition (PECVD) chamber. In some embodiments, the PECVD chamber is a multi-chamber tool capable of having the entire process 500 performed inside the chamber. In some embodiments, the semiconductor device may be a processor or any number of different types of semiconductor devices. The semiconductor device may have feature gaps that are less than 20 nanometers in width. The semiconductor device may have feature gaps with an aspect ratio of depth to width of greater than 8 to 1. Alternatively, the semiconductor device may have feature gaps less than 20 nanometers in width and have an aspect ratio less than 8 to 1.

At **504** of the process 500, an organosilane material may be introduced into the CVD chamber. The organosilane material may be introduced into the CVD chamber using a push gas. The push gas may be any type of inert gas or mixture of inert gases. The push gas may be He or Ar. The organosilane material may be a ring structure of alternating silicon and carbon atoms in a one to one atomic ratio, wherein the organosilane material does not have terminal alkyl hydrocarbon groups or $-\text{SiH}_3$ groups. The organosilane material may be 1,3-disilacyclobutane. The organosilane material may be 1,3,5-trisilacyclohexane. The organosilane material may be 1,3,5,7-tetrasilacyclooctane. The organosilane material may be an oligomer of 1,3-disilacyclobutane. The organosilane material may be an oligomer of 1,3,5-trisilacyclohexane. The organosilane material may be an oligomer of 1,3,5,7-tetrasilacyclooctane. The organosilane material may be selected from the group consisting of 1,3-disilacyclobutane, 1,3,5-trisilacyclohexane, an oligomer of 1,3-disilacyclobutane, and an

oligomer of 1,3,5-trisilacyclohexane, and combinations thereof. The organosilane material may be selected from the group consisting of 1,3-disilacyclobutane, 1,3,5-trisilacyclohexane, 1,3,5,7-tetrasilacyclooctane, an oligomer of 1,3-disilacyclobutane, an oligomer of 1,3,5-trisilacyclohexane, and an oligomer of 1,3,5,7-tetrasilacyclooctane, and combinations thereof.

5 At **506** of the process 500, the organosilane material may be deposited on the surface, wherein the feature gaps are filled with the organosilane material. The depositing may be performed by chemical vapor deposition inside the CVD chamber.

 At **508** of the process 500, the organosilane material may be crosslinked/annealed using oxygen radicals to provide a crosslinked organosilane material. The oxygen may be
10 generated by a remote plasma system.

 At **510** of the process 500, the crosslinked organosilane material may be cured using a radiation source. The radiation source may be an ultraviolet (UV) radiation source. The wave length of the radiation generated by the UV radiation source may be 200 nm to 400 nm.

 Various operations are described as multiple discrete operations in turn, in a
15 manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent.

FIG. 6 illustrates a semiconductor manufacturing process 600 using an organosilane material as a feature gap fill material, in accordance with some embodiments.

20 At **602** of the process 600, a semiconductor device may be placed in a plasma enhanced chemical vapor deposition (PECVD) chamber. The device may include a surface with feature gaps. The feature gaps may have an opening or width of less than 20 nanometers across and may have an aspect ratio of depth to width that is greater than 8 to 1. The semiconductor device may be comprised of any type of semiconductor substrate material, as disclosed herein.

25 At **604** of the process 600, the feature gaps may be filled with an organosilane material by deposition in the PECVD chamber in the presence of oxygen radicals to provide a crosslinked organosilane material. The organosilane material may be a ring structure of alternating silicon and carbon atoms in a one to one atomic ratio, wherein the organosilane material does not have a terminal alkyl hydrocarbon group or silyl ($-\text{SiH}_3$) group. The
30 organosilane material may be selected from the group consisting of 1,3-disilacyclobutane, 1,3,5-trisilacyclohexane, 1,3,5,7-tetrasilacyclooctane, an oligomer of 1,3-disilacyclobutane, an

oligomer of 1,3,5-trisilacyclohexane, and an oligomer of 1,3,5,7-tetrasilacyclooctane, and combinations thereof.

At **606** of the process 600, the crosslinked organosilane material may be cured using a UV radiation source to provide a cured organosilane material. A wave length of radiation
5 generated by the UV radiation source may be 200 nanometers (nm) to 400 nm.

At **608** of the process 600, planarizing the surface of the semiconductor device may be planarized to remove the cured organosilane material from the surface while the feature gaps remain filled with the crosslinked and cured organosilane material.

At **610** of the process 600, a silicon dioxide material may be etched from one or
10 more of the feature gaps on the surface of the semiconductor device to provide one or more open feature gaps. The silicon dioxide material may have been deposited in another process during the manufacturing process. The silicon dioxide material may be partially or completely removed from the feature gap.

At **612** of the process 600, a metal may be deposited in the one or more open
15 feature gaps. The metal may be any type of commonly used metals in semiconductor manufacturing such as copper, silver, or gold.

At **614** of the process 600, planarizing the surface is planarized to remove the metal from the surface while leaving the metal in the feature gap in which it was deposited.

At **616** of the process 600, a portion of the metal may be removed by etching the
20 metal from the one or more open feature gaps in which the metal was deposited.

At **618** of the process 600, a dielectric material may be deposited in the etched feature gaps to cover the partially etched metal. This dielectric material may include one of the organosilane materials disclosed herein or some other dielectric material.

FIG. 7 illustrates a semiconductor device 700 with a substrate 710 with feature
25 gaps 702, 704, 706, 708, 710, 712 having deposited therein an organosilane material 720 on top of a conductor 730 in the feature gaps 702, 704, 706, 708, 710, 712 of the semiconductor device 720, in accordance with some embodiments. In some embodiments, the semiconductor device may include different types of transistors and/or other devices/components manufactured using the organosilane materials and processes described herein, where the organosilane materials may
30 be permanent or sacrificial fills. In some embodiments, the device 700 may be a memory chip, a processor chip, a standard chip, or a complex system on chip. In some embodiments, the device

700 may be a digital chip, an analog chip, or a mixed signal chip. In some embodiments, the device 700 may be a comparator chip, a chip with audio processor circuits, UV eraser chip, frequency control circuit chip, data converter chip, discrete semiconductor chip, display driver chip, interface integrated circuit chip, memory chip, power management integrated circuit chip, microcontroller chip, logic circuit chip, radio frequency circuit chip, sensor integrated circuit chip, standard logic chip, or video processor circuit chip. The device 700 may be any type of semiconductor chip in which dielectric materials are used to sacrificially or permanently fill feature gaps in a substrate. The substrate 710 may be any type of semiconductor substrate including, for example: silicon, silicon on insulator, gallium arsenide, gallium nitride, cadmium selenide, cadmium telluride, cadmium mercury telluride, zinc sulfide, silicon carbide, gallium indium nitride, fused quartz, fused silica, epitaxial silicon, or organic semiconductor. The conductor 730 may be any type of conductor used in semiconductor manufacturing including, for example: copper, silver, gold, various alloys, conductive carbon nanomaterials, and various conductive semiconductor materials doped to various levels. The organosilane material 720 may be any one of the organosilane materials disclosed herein, including structures III and IV that have been further polymerized by crosslinking with oxygen and then UV cured to remove water and remaining Si-H bonds on the surface of the material and replace them with Si-CH₃ groups as terminal groups on the polymer surface. The structure I may be similarly polymerized by crosslinking with oxygen and then UV cured.

Embodiments of the present disclosure may be implemented into a system using any suitable hardware and/or software to configure as desired. **FIG. 8** illustrates a system with a semiconductor device with an organosilane material deposited in gaps of the semiconductor device, in accordance with some embodiments. The computing device 800 may house a board such as motherboard 802 (e.g., in housing 808). The motherboard 802 may include a number of components, including but not limited to a processor 804 and at least one communication chip 806. The processor 804 may be physically and electrically coupled to the motherboard 802. In some implementations, the at least one communication chip 806 may also be physically and electrically coupled to the motherboard 802. In further implementations, the communication chip 806 may be part of the processor 804.

Depending on its applications, computing device 800 may include other components that may or may not be physically and electrically coupled to the motherboard 802.

These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, MEMS sensors, a Geiger counter, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 806 may enable wireless communications for the transfer of data to and from the computing device 800. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 806 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including WiGig, Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultra mobile broadband (UMB) project (also referred to as “3GPP2”), etc.). IEEE 802.16 compatible broadband wireless access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 806 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 806 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 806 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond.

The communication chip 806 may operate in accordance with other wireless protocols in other embodiments.

The computing device 800 may include a plurality of communication chips 806. For instance, a first communication chip 806 may be dedicated to shorter range wireless communications such as WiGig, Wi-Fi and Bluetooth and a second communication chip 806 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, and others.

The processor 804, communications chip 806, chipset 812, memory chips 814, 816, 818, and other devices with chips shown in computing device 800 may contain feature gaps filled with an organosilane material as described herein. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

In various implementations, the computing device 800 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. The computing device 800 may be a mobile computing device in some embodiments. In further implementations, the computing device 800 may be any other electronic device that processes data.

EXAMPLES

According to various embodiments, the present disclosure describes organosilane materials and processes for filling gaps in semiconductor devices.

Example 1 of a process of filling gaps of a semiconductor device may comprise: placing a semiconductor device in a chemical vapor deposition (CVD) chamber, the semiconductor device including a surface with feature gaps on the surface; depositing the organosilane material on the surface, wherein the feature gaps are filled with the organosilane material; crosslinking the organosilane material to provide a crosslinked organosilane material; and curing the crosslinked organosilane material using a radiation source to provide a cured organosilane material.

Example 2 may include the process of Example 1 and other examples herein,

wherein the process may further comprise: planarizing the surface of the semiconductor device to remove the cured organosilane material from the surface and leave the cured organosilane material in the feature gaps; etching a silicon dioxide material from one or more of the feature gaps on the surface of the semiconductor device to provide one or more open feature gaps, wherein the cured organosilane material remains in the feature gaps; depositing a metal in the one or more open feature gaps; planarizing the surface of the semiconductor device to remove the metal from the surface and leave the metal in the one or more open feature gaps; partially etching to remove a portion of the metal in the one or more open feature gaps to provide one or more partially etched feature gaps, wherein the cured organosilane material remains in the one or more partially etched feature gaps; and depositing a dielectric material in the partially etched feature gaps.

Example 3 may include the process of Example 1 and other examples herein, wherein the CVD chamber is a plasma enhanced chemical vapor deposition (PECVD) chamber.

Example 4 may include the process of Example 3 and other examples herein,, wherein the PECVD chamber is a multi-chamber design, and wherein the process is performed in the PECVD chamber.

Example 5 may include the process of Example 1 and other examples herein, wherein the semiconductor device is a processor.

Example 6 may include the process of Example 1 and other examples herein, wherein the feature gaps are less than 20 nanometers in width.

Example 7 may include the process of Example 1 and other examples herein, wherein the feature gaps have an aspect ratio of depth to width greater than 8 to 1.

Example 8 may include the process of Example 1 and other examples herein, wherein the organosilane material is introduced into the CVD chamber using a push gas.

Example 9 may include the process of Example 8 and other examples herein, wherein the push gas is an inert gas.

Example 10 may include the process of Example 9 and other examples herein, wherein the push gas includes helium (He) or argon (Ar).

Example 11 may include the process of any one of Examples 1-10 and other examples herein, wherein the organosilane material is a ring structure of alternating silicon and carbon atoms in a one to one atomic ratio, wherein the organosilane material does not have a

terminal alkyl hydrocarbon group or silyl ($-\text{SiH}_3$) group.

Example 12 may include the process of any one of Examples 1-10 and other examples herein, wherein the organosilane material is 1,3-disilacyclobutane.

5 Example 13 may include the process of any one of Examples 1-10 and other examples herein, wherein the organosilane material is 1,3,5-trisilacyclohexane.

Example 14 may include the process of any one of Examples 1-10 and other examples herein, wherein the organosilane material is 1,3,5,7-tetrasilacyclooctane.

10 Example 15 may include the process of any one of Examples 1-10 and other examples herein, wherein wherein the organosilane material is an oligomer of 1,3-disilacyclobutane.

Example 16 may include the process of any one of Examples 1-10 and other examples herein, wherein the organosilane material is an oligomer of 1,3,5-trisilacyclohexane.

15 Example 17 may include the process of any one of Examples 1-10 and other examples herein, wherein the organosilane material is an oligomer of 1,3,5,7-tetrasilacyclooctane.

Example 18 may include the process of any one of Examples 1-10 and other examples herein, wherein the organosilane material is selected from the group consisting of 1,3-disilacyclobutane, 1,3,5-trisilacyclohexane, an oligomer of 1,3-disilacyclobutane, an oligomer of 1,3,5-trisilacyclohexane, 1,1,3,3 -Tetraalkoxy-1,3-disilacyclobutane, and 1,1,3,3,5,5-Hexaalkoxy-1,3,5-trisilacyclohexane, and combinations thereof, wherein the alkyl group of the alkoxy group is selected from the group consisting of methyl, ethyl, propyl, butyl, pentyl, hexyl, heptyl, octyl, nonyl, decyl, undecyl, and dodecyl, and combinations thereof.

20

Example 19 may include the process of any one of Examples 1-10 and other examples herein, wherein the organosilane material is selected from the group consisting of 1,3-disilacyclobutane, 1,3,5-trisilacyclohexane, 1,3,5,7-tetrasilacyclooctane, an oligomer of 1,3-disilacyclobutane, an oligomer of 1,3,5-trisilacyclohexane, an oligomer of 1,3,5,7-tetrasilacyclooctane, , 1,1,3,3 -tetraalkoxy-1,3-disilacyclobutane, 1,1,3,3,5,5-hexaalkoxy-1,3,5-trisilacyclohexane, and 1,1,3,3,5,5,7,7-octaalkoxy-1,3,5,7-tetrasilacyclooctane, and combinations thereof, wherein the alkyl group of the alkoxy group is selected from the group consisting of

25

30 methyl, ethyl, propyl, butyl, pentyl, hexyl, heptyl, octyl, nonyl, decyl, undecyl, and dodecyl, and combinations thereof.

Example 20 may include the process of any one of Examples 1-10 and other examples herein, wherein the oxygen radicals are generated by a remote plasma system.

Example 21 may include the process of any one of Examples 1-10 and other examples herein, wherein the radiation source is an ultraviolet (UV) radiation source,

5 Example 22 may include the process of any one of Examples 1-10 and other examples herein, wherein a wave length of radiation generated by the UV radiation source is 200 nanometers (nm) to 400 nm.

 Example 23 of a semiconductor device manufacturing process may comprise: placing a semiconductor device including a surface with feature gaps in a plasma enhanced
10 chemical vapor deposition (PECVD) chamber; filling the feature gaps with an organosilane material by deposition in the PECVD chamber to provide a crosslinked organosilane material; curing the crosslinked organosilane material using a UV radiation source to provide a cured organosilane material; planarizing the surface of the semiconductor device to remove the cured organosilane material from the surface; etching a silicon dioxide material from one or more of
15 the feature gaps on the surface of the semiconductor device to provide one or more open feature gaps; depositing a metal in the one or more open feature gaps; planarizing the surface to remove the metal from the surface; etching to remove a portion of the metal in the one or more open feature gaps; depositing a dielectric material in the etched feature gaps.

 Example 24 may include the process of Example 23 and other examples herein,
20 wherein the feature gaps are less than 20 nanometers in width and have an aspect ratio of depth to width greater than 8 to 1.

 Example 25 may include the process of any one of Examples 23-24 and other examples herein, wherein the organosilane material is a ring structure of alternating silicon and carbon atoms in a one to one atomic ratio, wherein the organosilane material does not have a
25 terminal alkyl hydrocarbon group or silyl ($-\text{SiH}_3$) group.

 Example 26 may include the process of any one of Examples 23-24 and other examples herein, wherein the organosilane material is selected from the group consisting of 1,3-disilacyclobutane, 1,3,5-trisilacyclohexane, an oligomer of 1,3-disilacyclobutane, an oligomer of 1,3,5-trisilacyclohexane, 1,1,3,3 -tetraalkoxy-1,3-disilacyclobutane, and 1,1,3,3,5,5-hexaalkoxy-
30 1,3,5-trisilacyclohexane, and combinations thereof, wherein the alkyl group of the alkoxy group is selected from the group consisting of methyl, ethyl, propyl, butyl, pentyl, hexyl, heptyl, octyl,

nonyl, decyl, undecyl, and dodecyl, and combinations thereof.

Example 27 may include the process of any one of Examples 23-24 and other examples herein, wherein a wave length of radiation generated by the UV radiation source is 200 nanometers (nm) to 400 nm.

5 Example 28 of a semiconductor device with an organosilane material in feature gaps may comprise: a semiconductor substrate including a plurality of feature gaps; and a polymerized organosilane material deposited in the feature gaps, wherein the organosilane material includes a ring structure of alternating silicon and carbon atoms in a one to one atomic ratio and does not have a terminal alkyl hydrocarbon group or silyl ($-\text{SiH}_3$) group, and wherein
10 the polymerized organosilane material includes a plurality of bonds of silicon to oxygen to silicon between different rings of the ring structure of the organosilane material and has Si-CH_3 groups on a finish surface.

Example 29 may include the device of Example 28 and other examples herein, wherein the organosilane material is 1,3-disilacyclobutane.

15 Example 30 may include the device of Example 28 and other examples herein, wherein the organosilane material is 1,3,5-trisilacyclohexane.

Example 31 may include the device of Example 28 and other examples herein, wherein the organosilane material is 1,3,5,7-tetrasilacyclooctane.

20 Example 32 may include the device of Example 28 and other examples herein, wherein the organosilane material is an oligomer of 1,3-disilacyclobutane.

Example 33 may include the device of Example 28 and other examples herein, wherein the organosilane material is an oligomer of 1,3,5-trisilacyclohexane.

Example 34 may include the device of Example 28 and other examples herein, wherein the organosilane material is an oligomer of 1,3,5,7-tetrasilacyclooctane.

25 Example 35 may include the device of Example 28 and other examples herein, wherein the organosilane material is selected from the group consisting of 1,3-disilacyclobutane, 1,3,5-trisilacyclohexane, an oligomer of 1,3-disilacyclobutane, an oligomer of 1,3,5-trisilacyclohexane, 1,1,3,3 -tetraalkoxy-1,3-disilacyclobutane, and 1,1,3,3,5,5-hexaalkoxy-1,3,5-trisilacyclohexane, and combinations thereof, wherein the alkyl group of the alkoxy group is
30 selected from the group consisting of methyl, ethyl, propyl, butyl, pentyl, hexyl, heptyl, octyl, nonyl, decyl, undecyl, and dodecyl, and combinations thereof.

Example 36 may include the device of Example 28 and other examples herein, wherein the organosilane material is selected from the group consisting of 1,3-disilacyclobutane, 1,3,5-trisilacyclohexane, 1,3,5,7-tetrasilacyclooctane, an oligomer of 1,3-disilacyclobutane, an oligomer of 1,3,5-trisilacyclohexane, an oligomer of 1,3,5,7-tetrasilacyclooctane, 1,1,3,3 -

5 tetraalkoxy-1,3-disilacyclobutane, 1,1,3,3,5,5-hexaalkoxy-1,3,5-trisilacyclohexane, and 1,1,3,3,5,5,7,7-octaalkoxy-1,3,5,7-tetrasilacyclooctane, and combinations thereof, wherein the alkyl group of the alkoxy group is selected from the group consisting of methyl, ethyl, propyl, butyl, pentyl, hexyl, heptyl, octyl, nonyl, decyl, undecyl, and dodecyl, and combinations thereof

Example 37 of a computing device may comprise: a circuit board; and a

10 semiconductor device with an organosilane material in feature gaps, the semiconductor device coupled with the circuit board and including: a semiconductor substrate including a plurality of feature gaps; and a polymerized organosilane material deposited in the feature gaps, wherein the organosilane material includes a ring structure of alternating silicon and carbon atoms in a one to one atomic ratio and does not have a terminal alkyl hydrocarbon group or silyl ($-\text{SiH}_3$) group,

15 wherein the polymerized organosilane material includes a plurality of bonds of silicon to oxygen to silicon between different rings of the ring structure of the organosilane material and has $\text{Si}-\text{CH}_3$ groups on a finish surface.

Example 38 may include the computing device of Example 37 and other examples herein, wherein the organosilane material is selected from the group consisting of 1,3-

20 disilacyclobutane, 1,3,5-trisilacyclohexane, 1,3,5,7-tetrasilacyclooctane, an oligomer of 1,3-disilacyclobutane, an oligomer of 1,3,5-trisilacyclohexane, an oligomer of 1,3,5,7-tetrasilacyclooctane, , 1,1,3,3 -tetraalkoxy-1,3-disilacyclobutane, 1,1,3,3,5,5-hexaalkoxy-1,3,5-trisilacyclohexane, and 1,1,3,3,5,5,7,7-octaalkoxy-1,3,5,7-tetrasilacyclooctane, and combinations thereof, wherein the alkyl group of the alkoxy group is selected from the group consisting of

25 methyl, ethyl, propyl, butyl, pentyl, hexyl, heptyl, octyl, nonyl, decyl, undecyl, and dodecyl, and combinations thereof.

Example 39 may include the computing device of Example 37 and other examples herein, wherein the computing device is a wearable device or a mobile computing device, the wearable device or the mobile computing device including one or more of an antenna, a display,

30 a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, a Geiger counter, an

accelerometer, a gyroscope, a speaker, or a camera coupled with the circuit board.

Various embodiments may include any suitable combination of the above-described embodiments including alternative (or) embodiments of embodiments that are described in conjunctive form (and) above (e.g., the “and” may be “and/or”). Furthermore, some
5 embodiments may include one or more articles of manufacture (e.g., non-transitory computer-readable media) having instructions, stored thereon, that when executed result in actions of any of the above-described embodiments. Moreover, some embodiments may include apparatuses or systems having any suitable means for carrying out the various operations of the above-described
10 embodiments. The above description of illustrated implementations, including what is described in the Abstract, is not intended to be exhaustive or to limit the embodiments of the present disclosure to the precise forms disclosed. While specific implementations and examples are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the present disclosure, as those skilled in the relevant art will recognize. These
15 modifications may be made to embodiments of the present disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit various embodiments of the present disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim
20 interpretation.

Claims

What is claimed is:

1. A process of filling gaps of a semiconductor device, comprising:
placing a semiconductor device in a chemical vapor deposition (CVD) chamber, the
5 semiconductor device including a surface with feature gaps on the surface;
depositing the organosilane material on the surface, wherein the feature gaps are filled
with the organosilane material;
crosslinking the organosilane material to provide a crosslinked organosilane material; and
curing the crosslinked organosilane material using a radiation source to provide a cured
10 organosilane material.
2. The process of claim 1, further comprising:
planarizing the surface of the semiconductor device to remove the cured organosilane
material from the surface and leave the cured organosilane material in the feature gaps;
etching a silicon dioxide material from one or more of the feature gaps on the surface of
15 the semiconductor device to provide one or more open feature gaps, wherein the cured
organosilane material remains in the feature gaps;
depositing a metal in the one or more open feature gaps;
planarizing the surface of the semiconductor device to remove the metal from the surface
and leave the metal in the one or more open feature gaps;
20 partially etching to remove a portion of the metal in the one or more open feature gaps to
provide one or more partially etched feature gaps, wherein the cured organosilane material
remains in the one or more partially etched feature gaps; and
depositing a dielectric material in the partially etched feature gaps.
3. The process of claim 1, wherein the CVD chamber is a plasma enhanced chemical vapor
25 deposition (PECVD) chamber.
4. The process of claim 3, wherein the PECVD chamber is a multi-chamber design, and
wherein the process is performed in the PECVD chamber.
5. The process of claim 1, wherein the semiconductor device is a processor.
6. The process of claim 1, wherein the feature gaps are less than 20 nanometers in width.
- 30 7. The process of claim 1, wherein the feature gaps have an aspect ratio of depth to width
greater than 8 to 1.

8. The process of claim 1, wherein the organosilane material is introduced into the CVD chamber using a push gas.

9. The process of any one of claims 1-8, wherein the organosilane material is a ring structure of alternating silicon and carbon atoms in a one to one atomic ratio, wherein the organosilane material does not have a terminal alkyl hydrocarbon group or silyl ($-\text{SiH}_3$) group.

10. The process of any one of claims 1-8, wherein the organosilane material is selected from the group consisting of 1,3-disilacyclobutane, 1,3,5-trisilacyclohexane, an oligomer of 1,3-disilacyclobutane, an oligomer of 1,3,5-trisilacyclohexane, 1,1,3,3 -tetraalkoxy-1,3-disilacyclobutane, and 1,1,3,3,5,5-hexaalkoxy-1,3,5-trisilacyclohexane, and combinations thereof, wherein the alkyl group of the alkoxy group is selected from the group consisting of methyl, ethyl, propyl, butyl, pentyl, hexyl, heptyl, octyl, nonyl, decyl, undecyl, and dodecyl, and combinations thereof.

11. The process of any one of claims 1-8, wherein the organosilane material is selected from the group consisting of 1,3-disilacyclobutane, 1,3,5-trisilacyclohexane, 1,3,5,7-tetrasilacyclooctane, an oligomer of 1,3-disilacyclobutane, an oligomer of 1,3,5-trisilacyclohexane, an oligomer of 1,3,5,7-tetrasilacyclooctane, , 1,1,3,3 -tetraalkoxy-1,3-disilacyclobutane, 1,1,3,3,5,5-hexaalkoxy-1,3,5-trisilacyclohexane, and 1,1,3,3,5,5,7,7-octaalkoxy-1,3,5,7-tetrasilacyclooctane, and combinations thereof, wherein the alkyl group of the alkoxy group is selected from the group consisting of methyl, ethyl, propyl, butyl, pentyl, hexyl, heptyl, octyl, nonyl, decyl, undecyl, and dodecyl, and combinations thereof.

12. The process of any one of claims 1-8, wherein oxygen radicals are generated by a remote plasma system during crosslinking.

13. The process of any one of claims 1-8, wherein the radiation source is an ultraviolet (UV) radiation source, wherein a wave length of radiation generated by the UV radiation source is 200 nanometers (nm) to 400 nm

14. A semiconductor device manufacturing process, comprising:

placing a semiconductor device including a surface with feature gaps in a plasma enhanced chemical vapor deposition (PECVD) chamber;

filling the feature gaps with an organosilane material by deposition in the PECVD chamber to provide a crosslinked organosilane material;

curing the crosslinked organosilane material using a UV radiation source to provide a

cured organosilane material;

planarizing the surface of the semiconductor device to remove the cured organosilane material from the surface;

etching a silicon dioxide material from one or more of the feature gaps on the surface of the semiconductor device to provide one or more open feature gaps;

depositing a metal in the one or more open feature gaps;

planarizing the surface to remove the metal from the surface;

etching to remove a portion of the metal in the one or more open feature gaps;

depositing a dielectric material in the etched feature gaps.

15. The process of claim 14, wherein the feature gaps are less than 20 nanometers in width and have an aspect ratio of depth to width greater than 8 to 1.

16. The process of any one of claims 14-15, wherein the organosilane material is a ring structure of alternating silicon and carbon atoms in a one to one atomic ratio, wherein the organosilane material does not have a terminal alkyl hydrocarbon group or silyl ($-\text{SiH}_3$) group.

17. The process of any one of claims 14-15, wherein the organosilane material is selected from the group consisting of 1,3-disilacyclobutane, 1,3,5-trisilacyclohexane, an oligomer of 1,3-disilacyclobutane, an oligomer of 1,3,5-trisilacyclohexane, 1,1,3,3-tetraalkoxy-1,3-disilacyclobutane, and 1,1,3,3,5,5-hexaalkoxy-1,3,5-trisilacyclohexane, and combinations thereof, wherein the alkyl group of the alkoxy group is selected from the group consisting of methyl, ethyl, propyl, butyl, pentyl, hexyl, heptyl, octyl, nonyl, decyl, undecyl, and dodecyl, and combinations thereof.

18. The process of any one of claims 14-15, wherein a wave length of radiation generated by the UV radiation source is 200 nanometers (nm) to 400 nm.

19. A semiconductor device with an organosilane material in feature gaps, comprising:

a semiconductor substrate including a plurality of feature gaps; and

a polymerized organosilane material deposited in the feature gaps,

wherein the polymerized organosilane material comprises an organosilane material that includes a ring structure of alternating silicon and carbon atoms in a one to one atomic ratio and does not have a terminal alkyl hydrocarbon group or silyl ($-\text{SiH}_3$) group, and

wherein the polymerized organosilane material includes a plurality of bonds of silicon to oxygen to silicon between different rings of the ring structure of the organosilane material and

has Si-CH₃ groups on a finish surface.

20. The device of claim 19, wherein the organosilane material is 1,3-disilacyclobutane.

21. The device of claim 19, wherein the organosilane material is 1,3,5-trisilacyclohexane.

22. The device of claim 19, wherein the organosilane material is selected from the group
5 consisting of 1,3-disilacyclobutane, 1,3,5-trisilacyclohexane, an oligomer of 1,3-disilacyclobutane, an oligomer of 1,3,5-trisilacyclohexane, 1,1,3,3 -tetraalkoxy-1,3-disilacyclobutane, and 1,1,3,3,5,5-hexaalkoxy-1,3,5-trisilacyclohexane, and combinations thereof, wherein the alkyl group of the alkoxy group is selected from the group consisting of methyl, ethyl, propyl, butyl, pentyl, hexyl, heptyl, octyl, nonyl, decyl, undecyl, and dodecyl, and
10 combinations thereof.

23. A computing device, comprising:

a circuit board; and

a semiconductor device with an organosilane material in feature gaps, the semiconductor device coupled with the circuit board and including:

15 a semiconductor substrate including a plurality of feature gaps; and
a polymerized organosilane material deposited in the feature gaps,
wherein the polymerized organosilane material comprises an organosilane material that includes a ring structure of alternating silicon and carbon atoms in a one to one atomic ratio and does not have a terminal alkyl hydrocarbon group or silyl (–SiH₃) group,
20 wherein the polymerized organosilane material includes a plurality of bonds of silicon to oxygen to silicon between different rings of the ring structure of the organosilane material and has Si-CH₃ groups on a finish surface.

24. The computing device of claim 23, wherein the organosilane material is selected from the group consisting of 1,3-disilacyclobutane, 1,3,5-trisilacyclohexane, 1,3,5,7-tetrasilacyclooctane,
25 an oligomer of 1,3-disilacyclobutane, an oligomer of 1,3,5-trisilacyclohexane, an oligomer of 1,3,5,7-tetrasilacyclooctane, , 1,1,3,3 -tetraalkoxy-1,3-disilacyclobutane, 1,1,3,3,5,5-hexaalkoxy-1,3,5-trisilacyclohexane, and 1,1,3,3,5,5,7,7-octaalkoxy-1,3,5,7-tetrasilacyclooctane, and combinations thereof, wherein the alkyl group of the alkoxy group is selected from the group consisting of methyl, ethyl, propyl, butyl, pentyl, hexyl, heptyl, octyl, nonyl, decyl, undecyl, and
30 dodecyl, and combinations thereof.

25. The computing device of claim 23, wherein the computing device is a wearable device or

a mobile computing device, the wearable device or the mobile computing device including one or more of an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, a Geiger counter, an accelerometer, a gyroscope, a speaker, or a camera coupled with
5 the circuit board.

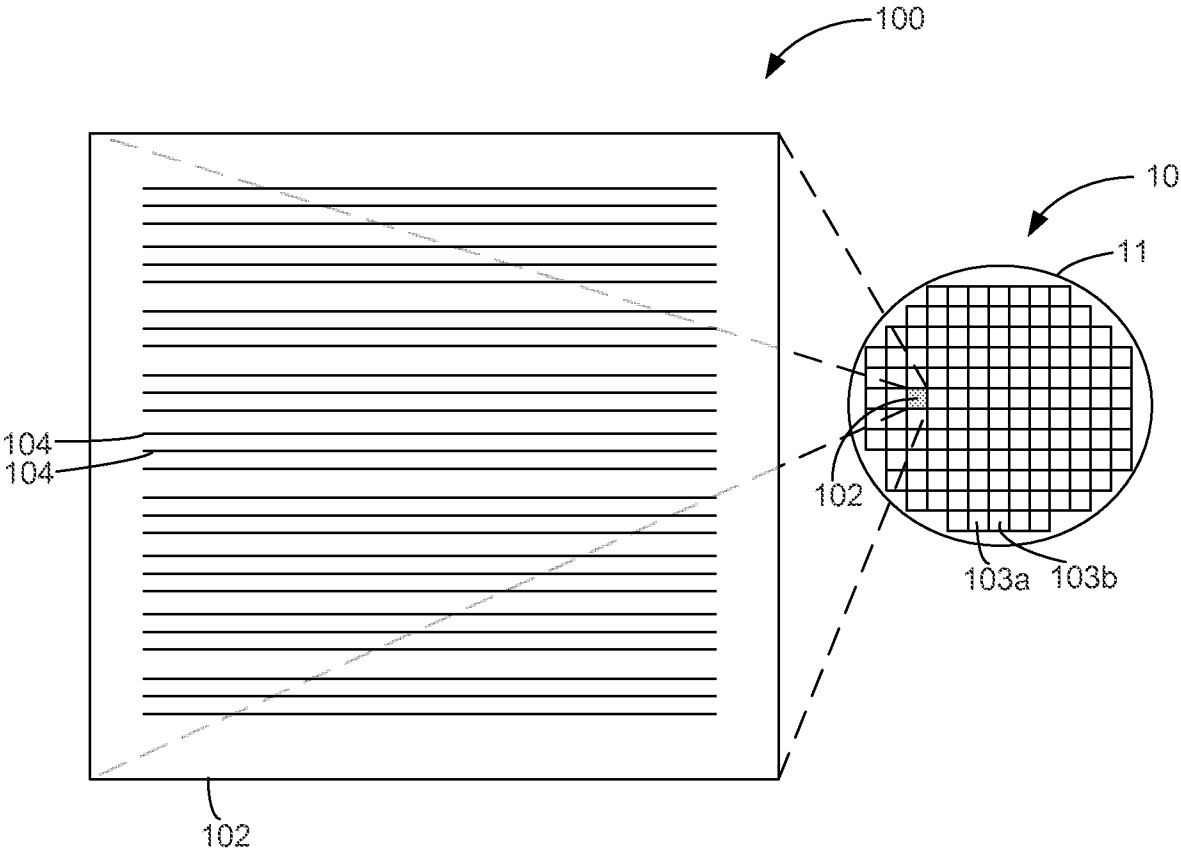


FIG. 1

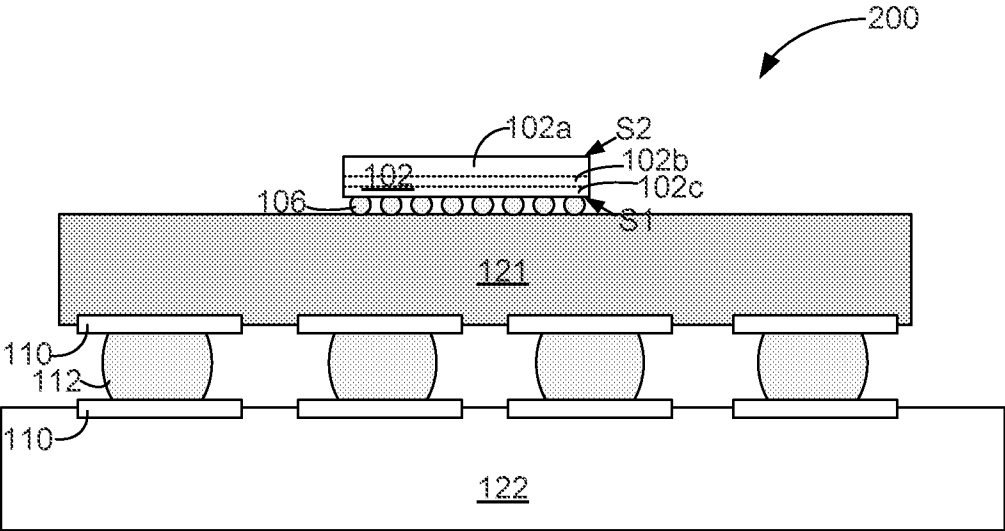


FIG. 2

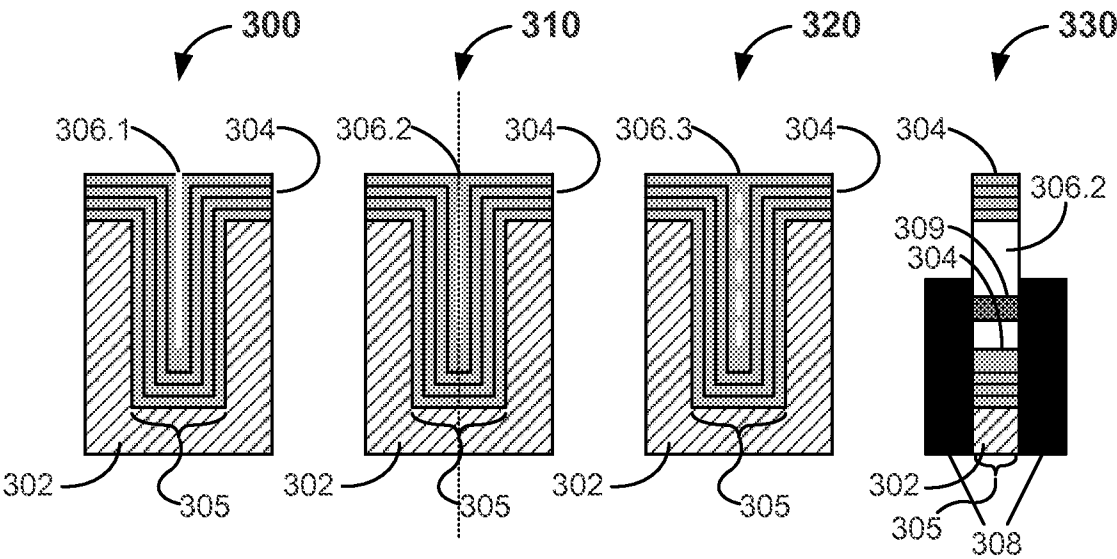
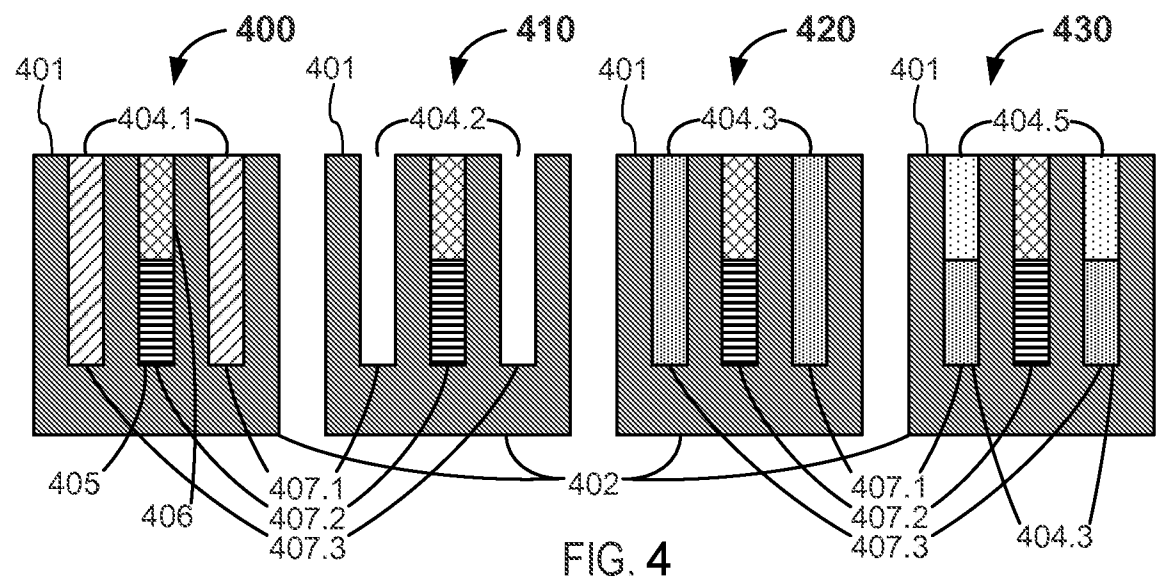


FIG. 3



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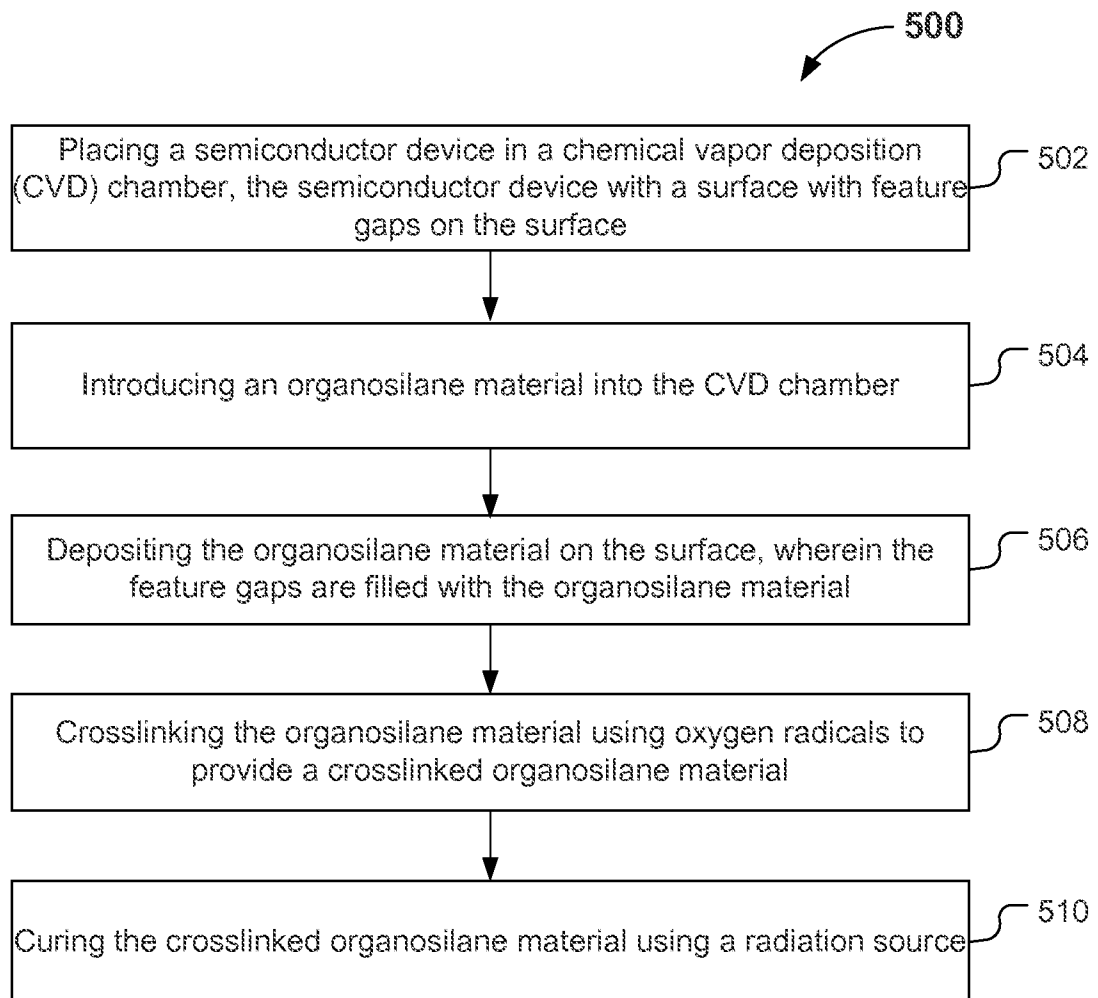


FIG. 5

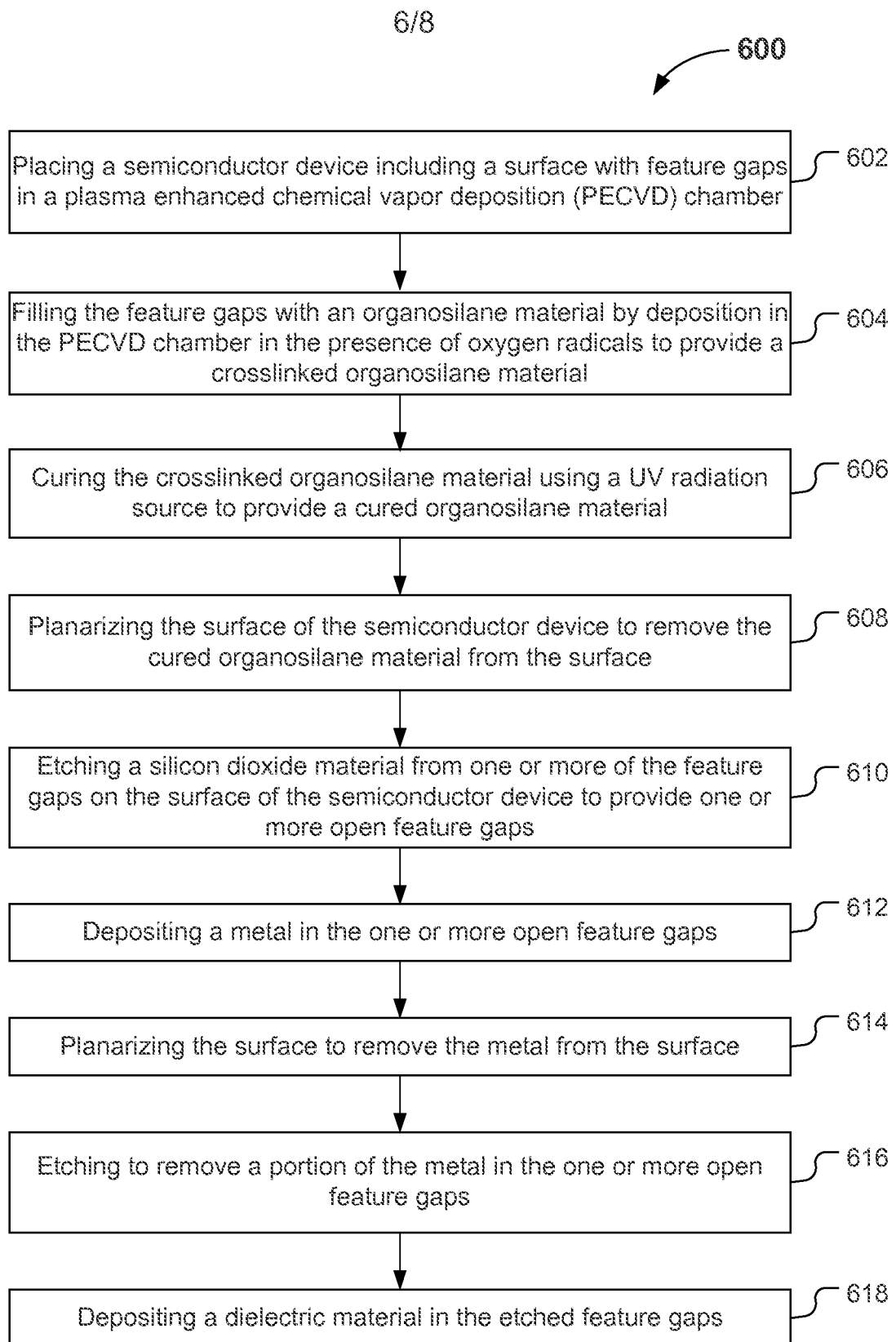


FIG. 6

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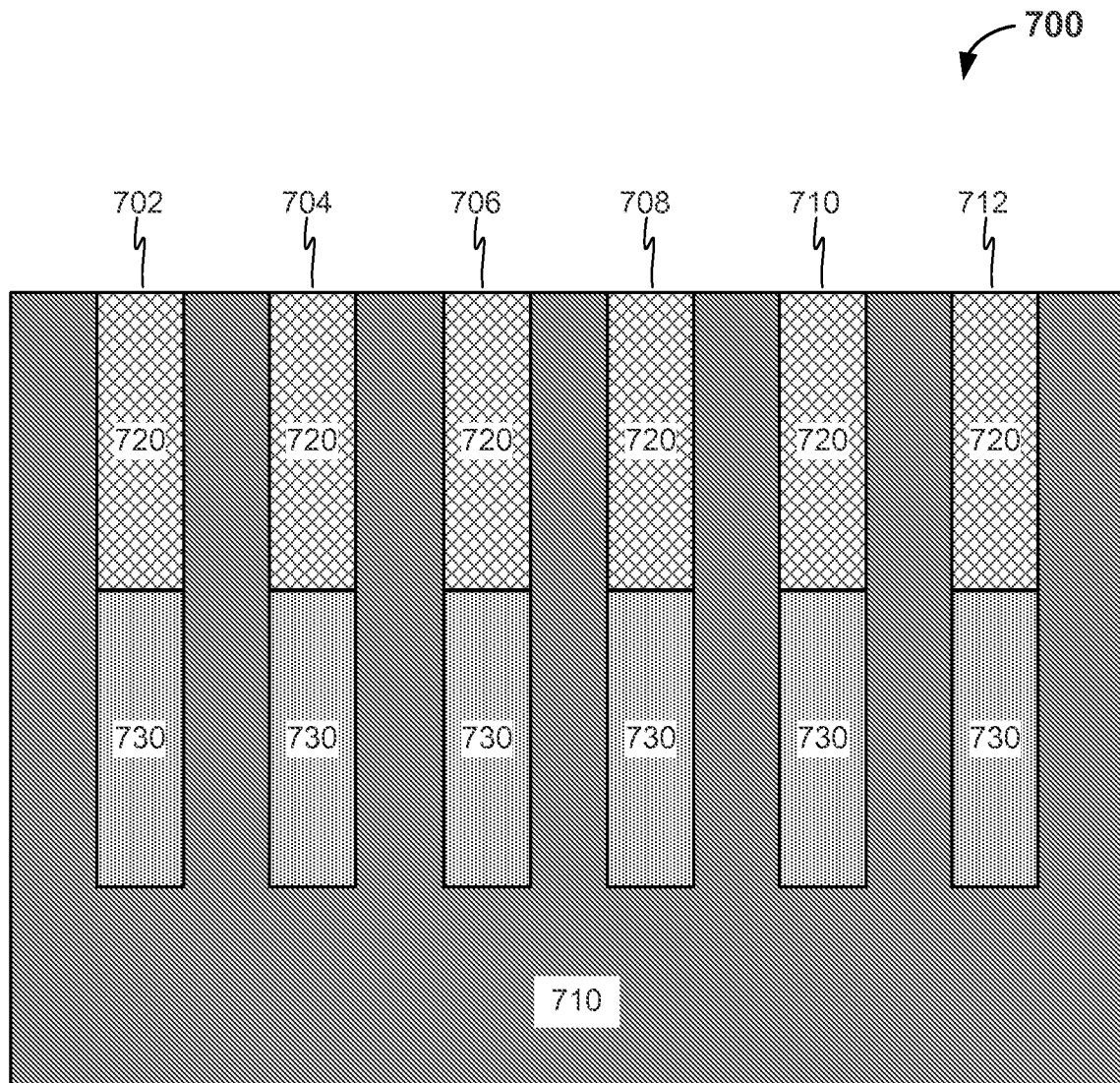


FIG. 7

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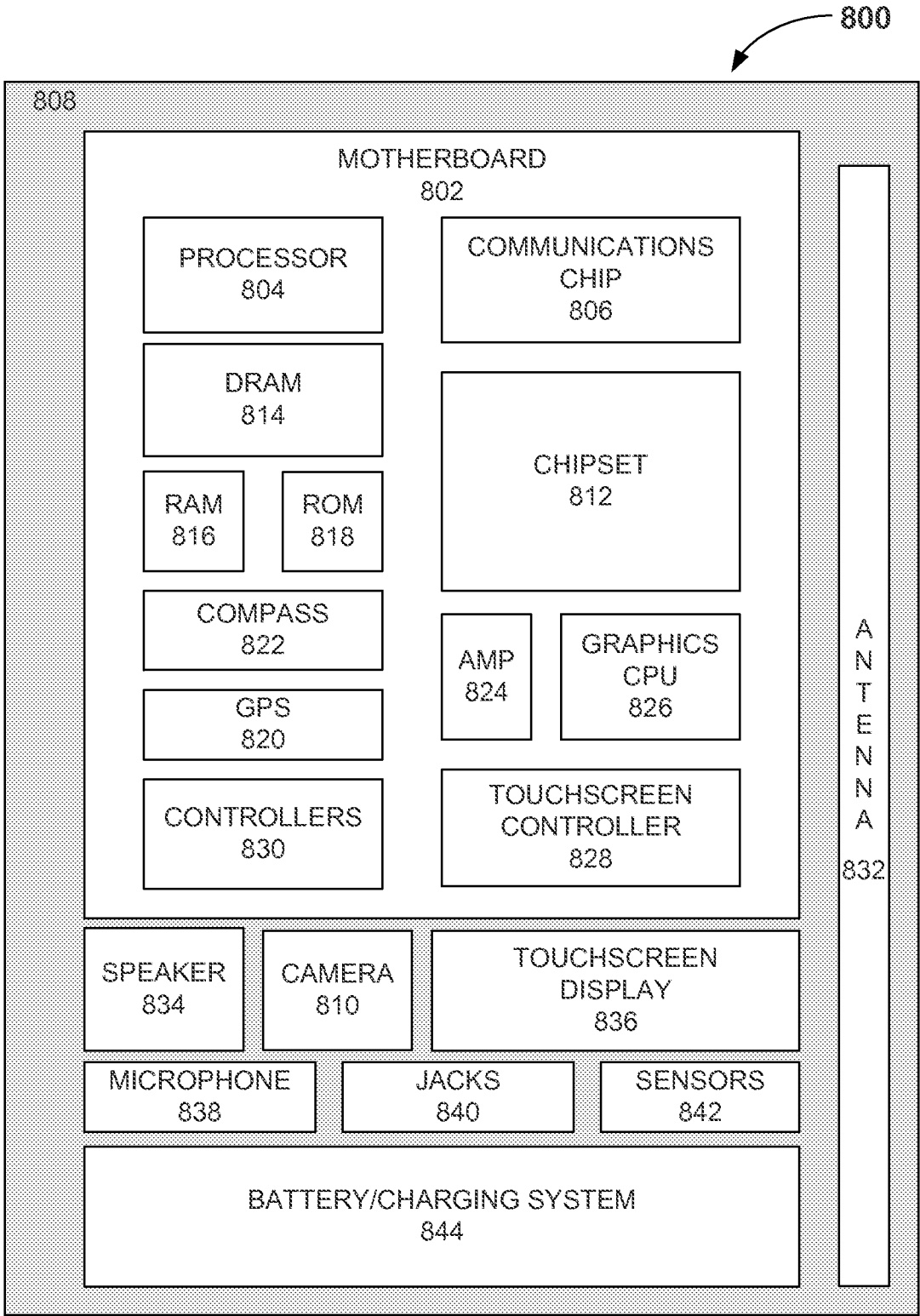


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/050806**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/027(2006.01)i, H01L 21/205(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/027; C08G 77/12; H01L 21/302; H01L 21/312; H01L 21/469; H01L 21/316; H01L 21/31; H01L 21/461; H01L 21/76; H01L 21/205

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:gap, fill, organsilane, curing, crosslinking

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010-0167553 A1 (CHANG SOO WOO et al.) 01 July 2010 See abstract; paragraphs [0003], [0065]; and claim 9.	1-25
A	US 2003-0124859 A1 (DAVID CHEUNG et al.) 03 July 2003 See abstract; paragraphs [0098]-[0101]; claim 1; and figures 6A-6E.	1-25
A	KR 10-2012-0099243 A (NOVELLUS SYSTEMS, INC.) 07 September 2012 See abstract; paragraphs [0059]-[0061]; claim 1; and figures 1a-1c.	1-25
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Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

30 May 2016 (30.05.2016)

Date of mailing of the international search report

30 May 2016 (30.05.2016)

Name and mailing address of the ISA/KR

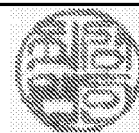
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