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(54) **Title**: ATOMIC LAYER ETCHING OF TRANSITION METALS BY HALOGEN SURFACE OXIDATION

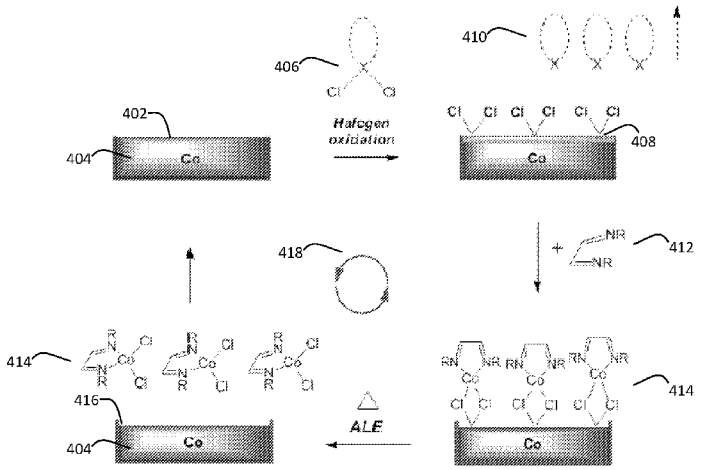

FIG. 4

(57) **Abstract**: Atomic layer etch methods for etching surfaces containing transition metals and their alloys are disclosed. Methods are based on halogenation of surfaces to be etched followed by complexation, with the aid of appropriate chelating organic ligands, in order to produce etch fragments as volatile species containing transition metals of the surfaces. Resulting etch fragments are not only volatile at relatively low temperatures, but also thermally stable, which makes clean vaporization of these fragments, at relatively low temperatures, possible. Furthermore, proposed etch methods are, advantageously, highly selective to the transition metal(s) to be etched. As a result, transition metals and their alloys can be etched in a controlled, atomically precise manner, and the etch fragments can be cleanly driven off in their gas phase.

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ATOMIC LAYER ETCHING OF TRANSITION METALS BY HALOGEN SURFACE OXIDATION

Technical Field

[0001] This disclosure relates generally to the field of integrated circuits and semiconductor manufacturing, and more specifically, to atomic layer etching of transition metals and metal alloys.

Background

[0002] For the past several decades, the scaling of features in integrated circuits (ICs) has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor IC chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity.

[0003] IC chips are used in a variety of devices including automobiles, computers, appliances, mobile phones and consumer electronics. A plurality of IC chips can typically be formed on a single silicon wafer, i.e. a silicon disk having a diameter of, for example, 300 millimeters (mm), which is then diced apart to create individual chips. IC chips can include features sizes on the nanometer and sub-nanometer scale and can comprise hundreds of millions of components.

[0004] The drive for the ever-increasing capacity, however, is not without issue. The desire to make smaller IC chips continuously places demands on the methods and materials used to manufacture these devices. In particular, as traditional scaling continues reduction of critical dimensions to below 14 nanometers (nm) and as individual layers in film stacks used in many applications are now routinely approaching dimensions (e.g. thickness) of less than 2-3 nm, the need to control manufacturing of features at the sub-nanometer level becomes essential. Some examples include stacks of magnetoresistive materials in non-volatile magnetic memory devices based on tunneling magnetoresistance used in Magnetic Random Access Memory (MRAM) applications and stacks of dielectric materials used in backend interconnects.

[0005] Implementation of features in film layers of such small dimensions necessitates adoption of atomically precise etching techniques to pattern these layers. Traditional plasma etch processes cannot meet the extreme selectivity requirements for patterning nanometer- and sub-nanometer scale features, making softer, molecular chemistry-based techniques an attractive alternative. One example of such a technique is atomic layer etching, which is an emerging technique in semiconductor manufacturing based on chemically modifying target areas of top atomic layers of a surface to be etched, followed by removal of individual atomic layers in the modified areas.

[0006] In particular, efficient etch of transition metals in semiconductor processing is becoming increasingly important as more of these elements are incorporated with every passing technology node. For example, in metallization of interconnects features at narrow critical dimensions, copper (Cu) lines connected with cobalt (Co) vias are used, Co being a transition metal. In another example, in MRAM devices, data storage relies on Co, iron (Fe), and nickel (Ni) (all being transition metals) and their corresponding alloys as the basic magnetic building blocks of magnetoresistive stacks.

[0007] As the foregoing illustrates, improvements with respect to atomic layer etching of transition metals and their alloys would be desirable.

Brief Description of the Drawings

[0008] FIG. 1 illustrates division of elements in the periodic table.

[0009] FIG. 2 provides a schematic flow chart illustrating a process of etching a material comprising one or more transition metals, according to some embodiments of the present disclosure.

[0010] FIG. 3 provides a schematic illustration of a cross-section of an exemplary structure comprising a material patterned using atomic layer etching by halogen surface oxidation, according to some embodiments of the present disclosure.

[0011] FIG. 4 illustrates an example of etching cobalt surface, according to some embodiments of the present disclosure.

[0012] FIGs. 5a-5c provide examples of chlorinating agents, according to some embodiments of the present disclosure.

[0013] FIG. 6 illustrates an example of etching CoFeB surface, according to some embodiments of the present disclosure.

[0014] FIG. 7 provides a schematic illustration of an interposer, according to some embodiments of the present disclosure.

[0015] FIG. 8 provides a schematic illustration of a computing device built in accordance with some embodiments of the present disclosure.

Detailed Description

[0016] In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present disclosure may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0017] Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0018] The terms "over," "under," "between," and "on" as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed

between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer "on" a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0019] Implementations of the disclosure may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

[0020] In various embodiments, the interconnects as described herein may be used to connect various components associated with an integrated circuit. Components include, for example, transistors, diodes, power sources, resistors, capacitors, inductors, sensors, transceivers, receivers, antennas, etc. Components associated with an integrated circuit may include those that are mounted on an integrated circuit or those connected to an integrated circuit. The integrated circuit may be either analog or digital and may be used in a number of applications, such as microprocessors, optoelectronics, logic blocks, audio amplifiers, etc., depending on the components associated with the integrated circuit. The integrated circuit may be employed as part of a chipset for executing one or more related functions in a computer.

[0021] In the embodiments where at least some of the components associated with an integrated circuit are transistors, a plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be

fabricated on the substrate. In various implementations of the disclosure, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein may illustrate only planar transistors, it should be noted that the disclosure may also be carried out using nonplanar transistors.

[0022] Each MOS transistor includes a gate stack formed of at least two layers, a gate interconnect support layer and a gate electrode layer. The gate interconnect support layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO_2) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate interconnect support layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate interconnect support layer to improve its quality when a high-k material is used.

[0023] The gate electrode layer is formed on the gate interconnect support layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer.

[0024] For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal

oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

[0025] In some implementations, when viewed as a cross-section of the transistor along the source-channel-drain direction, the gate electrode may consist of a "U"-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0026] In some implementations of the disclosure, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0027] As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition

process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[0028] One or more interlayer dielectrics may be deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO_2), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

[0029] In general, an interlayer dielectric (ILD) or inter metal dielectric (IMD) film is the insulating material used between metal conductors and devices (such as transistors) in integrated circuit devices.

[0030] To provide context, as mentioned in the Background section above, atomically precise patterning of semiconductor and metal surfaces has recently been carried out using atomic layer etch methods in which reaction of elements of these surfaces with reactive halogen-containing molecules results in creation of volatile species containing elements of

the surfaces. Because these species are volatile (i.e. rapidly evaporating), they may subsequently be removed, thereby forming a patterned surface where parts of the surface have been removed.

[0031] This type of etching is an example of plasma etching because, oftentimes, reactive halogen-containing molecules are provided in a plasma form. For example, metallic aluminum (Al) surface can be readily and anisotropically etched with chlorine (Cl) plasma by forming volatile Al_2Cl_6. Volatile Al_2Cl_6 is removed, resulting in patterned Al surface.

[0032] However, patterning by plasma etching using an approach similar to that described above cannot currently be applied to most transition metals of interest, such as Co, Fe, Ni, platinum (Pt), ruthenium (Ru), etc., because these metals form polymeric compounds in the form $\{MX_n\}_x$, which are essentially non-volatile. In the notation $\{MX_n\}_x$, M denotes a transition metal, X denotes a halogen used in dry etching, n is an integer equal to 2 or 3, and x denotes a finite polymer chain. Because such compounds are non-volatile, they cannot be easily removed from the etched structures. Due to the absence of a mechanism to cleanly volatilize and eliminate the etched fragments, patterning by dry etching, e.g. plasma etching, of semiconductor architectures containing transition metals, in particular late transition metal elements, such as e.g. Co, Ru, Pt, and Fe, and their alloys, is currently an unsolved problem.

[0033] Alternative etching methods that could, in principle, be applied to etching of transition metals and their alloys have their own drawbacks. For example, wet etch schemes are for the most part isotropic and, hence, suffer from significant undercuts in patterned features. On the other hand, current methods such as high energy sputtering result in significant re-deposition of species containing etched elements on the side walls of the structures being etched, leading to high levels of contamination with little net elimination of the etched material.

[0034] To improve on one or more of these issues, some embodiments of the present disclosure provide improved, alternative atomic layer etch methods for etching surfaces containing transition metals and their alloys. Methods provided herein are based on halogenation of surfaces to be etched (i.e. generation of metal halides on the surfaces)

followed by complexation (i.e. generation of a metal complex), with the aid of appropriate chelating organic ligands, in order to produce etch fragments in a form of volatile species containing transition metals of the surfaces. Resulting etch fragments are not only volatile at relatively low temperatures, but also thermally stable (i.e. they do not decompose at temperatures typically used in their processing), which makes clean vaporization of these fragments, at relatively low temperatures, possible. Furthermore, proposed etch methods are, advantageously, highly selective to the transition metal (i.e. there is sufficient contrast between etch characteristics of the transition metals and their alloys and etch characteristics of possible surrounding materials, such as e.g. surrounding dielectric materials). As a result, transition metals and their alloys can be etched in a controlled, atomically precise manner, and the etch fragments can be cleanly driven off in their gas phase.

[0035] FIG. 1 illustrates division of elements in the periodic table. As is well-known, the elements in the periodic table are often divided into four categories illustrated in FIG. 1: (1) main group elements, (2) transition metals, (3) lanthanides, and (4) actinides. The main group elements include the active metals in the two columns on the extreme left of the periodic table and the metals, semimetals, and nonmetals in the six columns on the far right. The transition metals are the metallic elements that serve as a bridge, or transition, between the left and the right sides of the table containing the main group elements. Embodiments of the present disclosure relate to etching of materials comprising one or more of such transition elements and their alloys.

[0036] FIG. 2 provides a schematic flow chart 200 illustrating a process of etching a material that includes one or more transition metals, according to some embodiments of the present disclosure. First, the process is described in general terms, with reference to boxes 202-206 shown in FIG. 2, followed by descriptions of various examples illustrating various exemplary etching scenarios.

[0037] The process may begin with oxidizing a surface of the material to be etched using chemical halogenation to form halides of the one or more transition metals on the surface (box 202). In some embodiments, oxidation may be carried out by delivering one or more

halogenating agents (i.e. compounds containing one or more halogen atoms and configured to transfer some or all of their halogen atoms to a compound with which they are reacting, in this case - to the surface of the material to be etched). For example, halogenating agents such as halosuccinimides, dihalo-triorganophosphines, and/or iodobenzenedichlorides may be delivered in their gas phase.

[0038] As is well-known, in general, "oxidation" is any chemical reaction that involves moving of electrons. In context of the present disclosure, "oxidizing the surface of the material" to be etched refers to a self-limiting and controlled oxidation of the metal surface with a molecular halogenating agent to ensure layer by layer removal.

[0039] As is also well-known, in general, "halogenation" refers to replacement of one or more hydrogen atoms in an organic compound by a halogen (fluorine, chlorine, bromine or iodine). In context of the present disclosure, a transition metal is oxidized by a higher valent halogenating agent or a source of radical halogen, which are volatile, forming a metal halide.

[0040] In general, "halide" refers to a binary compound of which one part is a halogen atom, e.g. Cl, and the other part is an element or radical that is less electronegative. In context of the present disclosure, the other part is a transition metal atom, e.g. Co, and the halide is a metal halide. For example, if the material to be etched included Co and the surface is oxidized with a chlorinating agent (i.e. an agent comprising chlorine (Cl)), then $CoCl_2$ halides are formed on the surface.

[0041] Next, the oxidized surface of the material to be etched is complexed with one or more complexing agents to form adducts that include atoms of the one or more transition metals of the material being etched (box 204).

[0042] In general, "complexing" refers to forming a metal complex (also referred to as a "coordination complex") where a central atom or ion, which is usually metallic, is surrounded by an array of bound molecules or ions, which are, in turn, known as ligands or complexing agents. Related term "complexing agent" (also referred to as "ligand") refers to

a non-metal compound in which independently existing molecules or ions form coordinate bonds with a metal atom or ion.

[0043] In some embodiments, the complexing agents may include chelating ligands, preferably neutral chelating ligands. In general, "chelating" refers to an enhanced affinity of a ligand for a metal ion, in this case – transition metal ion, where a single ligand can form two or more bonds to the metal (i.e. a multidentate ligand). In context of the present disclosure, "neutral" refers to bidentate or tridentate ligands that form dative bonds between the donor atoms in the ligand and the transition metal being etched.

[0044] One example of a complexing agent includes N,N'-tert-butyl-1,4-diazabutadiene (DABD). However, in other embodiments, suitable complexing agents may include e.g. any bidentate or tridentate ligand, preferentially neutral and containing donor atoms such as carbon, nitrogen, phosphorus, oxygen, sulphur or arsenic.

[0045] In some embodiments, the halogenating as well as the complexing agents are delivered in their gas phase. However, in various other embodiments, the halogenating and/or complexing agents may be delivered in other phases, e.g. as liquids or/and plasma.

[0046] In general, the term "adduct" refers to a product of a direct addition of two or more distinct molecules, resulting in a single reaction product containing all atoms of all components, such product typically being considered to be a distinct molecular species. In context of the present disclosure, adducts formed in box 204 are products of addition of, on one hand, complexing agents and, on the other hand, halides of the transition metals of the material to be etched. For example, when DABD is used as a complexing agent and when the material to be etched includes Co, either as an alloy or as a single element (i.e. not a part of an alloy) and halogenation is performed using chlorinating agents resulting in formation of a metal halide $CoCl_2$, the resulting adduct is (DABD)$CoCl_2$.

[0047] Adducts formed as a combination of transition metal halides and chelating ligands are volatile and, therefore, may be subsequently thermally driven off, as etch fragments, from the surface of the material to be etched (box 206).

[0048] In some embodiments, thermal removal of the adducts may include evaporating the adducts from the surface by heating the material to a temperature between 50 and 400 degrees Celsius. In various embodiments, such evaporation may be carried out over a time period between 0.1 and 4 hours. In other embodiments, evaporation of the adducts may be carried out at a room temperature.

[0049] In some embodiments, the process described above may be applied to etching of a material that includes a transition metal as a single element (i.e., not in an alloy), e.g. Co, Fe, or any other single element of the transition metals shown in FIG. 1. In other embodiments, the process described above may be applied to etching of a material that may include one or more transition metals in an alloy with other elements. For example, the material may be a ferromagnetic alloy of iron (Fe), cobalt (Co), or nickel (Ni) mixed with one or more of main group elements, such as e.g. CoFeB, or a permalloy (Ni/Fe).

[0050] Materials comprising one of more transition metals etched in the manner described herein, i.e. patterned materials, may be included in devices such as MRAM devices (e.g. in planar magnetic stacks) or interconnects (e.g. in vias). Depending on the halogenating agents being used to oxidize the surface during the etch process described herein, surface of such a patterned material may include characteristic trace amounts of e.g. phosphorous (P), nitrogen (N), or carbon (C), typically in concentration between 0.5 and 5 atomic percent, including all ranges and values therein. This residual P, N, or/and C present e.g. in vias or planar magnetic stacks, can be detectable by e.g. transmission electron microscopy (TEM) or X-ray photoelectron spectroscopy (XPS).

[0051] FIG. 3 provides a schematic illustration of a cross-section of an exemplary structure 300 comprising a material 302 patterned using atomic layer etching by halogen surface oxidation, according to some embodiments of the present disclosure. As can be seen, FIG. 3 is drawn to reflect example real world process limitations, in that the features are not drawn with precise right angles and straight lines.

[0052] The material 302 may include one or more transition metals, either in their single element form, or in alloys with other elements. As a result of the etch process, the material 302 may be recessed, as shown with a recess 304, with respect to the surrounding material

306. In some embodiments, the depth of the recess 304 may be in the range of 2 to 500 Angstrom, including all values and ranges therein, such as 2 to 50 Angstrom, 2 to 20 Angstrom, etc.

[0053] The surrounding material 306 may be disposed on or be a substrate, and may be e.g. comprised of one or more of silicon, silicon dioxide, germanium, indium, antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide and gallium antimonide. In some embodiments, the surrounding material 306 may be an interlayer dielectric (ILD). In some embodiments, the material 302 may include different materials 306 surrounding it on different sides. The etching approach described herein is, advantageously, highly selective to the material 302 comprising one or more transition metals opposed to the surrounding material 306 in that there is sufficient contrast between etch characteristics of the material 302 and etch characteristics of possible surrounding material 306, such as e.g. surrounding dielectric material.

[0054] FIG. 4 illustrates an example of etching cobalt surface, according to some embodiments of the present disclosure. FIG. 4 illustrates that a surface 402 of a cobalt layer 404 is oxidized by delivering a chlorinating agent 406 in the gas phase to convert metallic elements (in this case – cobalt elements) to its most stable chloride form (in this particular case - $CoCl_2$), as shown with a surface 408. Remaining part 410 of the chrolinating agent may be thermally removed. Gas phase addition of a ligand such as DABD 412 then forms a discreet adduct 414 that could be thermally driven off leading to clean removal of the metallic element from the surface 402, shown with a recess 416. The process may then be repeated, as illustrated in FIG. 4 with arrows 418, removing further atomic layers and providing a deeper recess in the material comprising transition metal(s).

[0055] It should be noted that, for DABD, the volatility of the expected (DABD)$CoCl_2$ adduct has been experimentally verified. Independent synthesis of this molecule by reaction of $CoCl_2$ and DABD yielded the expected 1:1 adduct, characterized by single crystal X-ray diffraction. Furthermore, thermal analysis of this material confirmed the long term stability and volatility of this adduct. An isothermal trace for the evaporation of (DABD) $CoCl_2$ at 150

degrees C and 0.2 Torr, showed more than 60 percent of clean mass loss over a period of about 6 hours.

[0056] FIGs. 5a-5c provide examples of chlorinating agents, according to some embodiments of the present disclosure. In particular, FIG. 5a illustrates an iodobenzenedichloride, FIG. 5b illustrates a dihalo-triorganophosphine, and FIG. 5c illustrates an N-chlorosuccinimide (NCS).

[0057] For non-volatile magnetic memory devices featuring either permalloy (Ni/Fe) or CoFeB thin films the same approach as illuatrated for cobalt in FIG. 4 may be applied, which is illustrated in FIG. 6. FIG. 6 illustrates an example of etching CoFeB surface, according to some embodiments of the present disclosure.

[0058] FIG. 6 illustrates that a surface 602 of a CoFeB layer 604 is oxidized by delivering a chlorinating agent ("Cl treatment") 606 in the gas phase to convert metallic elements (in this case – cobalt and iron elements) to their most thermodynamically stable chloride forms (in this particular case - $CoCl_2$ and $FeCl_2$), as shown with a surface 608. In this case, chloride exposure would lead to formation of not only volatile metal chlorides $CoCl_2$ and $FeCl_2$ but also volatile BCl_3, which could be driven off under relatively mild conditions, with the boiling point being around 12 degrees Celsius. As in the example shown in FIG. 4, gas phase complexation with a ligand such as DABD, shown as a complexing agent 610, would lead to formation of monomeric (DABD)$CoCl_2$ 612, but also (DABD)$FeCl_2$ 614, both of which can be thermally removed from a substrate 616. While FIG. 6 illustrates that, after removal of the adducts 612 and 614, substrate 616 is exposed with no CoFeB material left on it, of course in other embodiments, only one or more atomic layers of CoFeB layer may be removed, leaving other layers of this material on the substrate.

[0059] (DABD)$FeCl_2$ was independently synthesized and characterized by single-crystal X-ray diffraction and thermal analysis confirmed the long term stability and volatility of this adduct. An isothermal trace for the evaporation of (DABD)$FeCl_2$ at 110 degrees Celsius and 0.2 Torr showed more than 25 percent of clean mass loss over a period of approximately 12 hours. Comparison to a thermal trace of (DABD)$CoCl_2$ under identical conditions reveals that this type of the iron adduct is significantly more volatile than the cobalt adduct.

Evaporation time may be adjusted based on the evaporation rates of the different adducts, which could differ by as much as about one order of magnitude.

Implementation in an interposer

[0060] In accordance with embodiments of the disclosure, materials comprising one of more transition metals and patterned by the atomic layer etching as disclosed herein may be used in the fabrication of an interposer, such as e.g. the one shown in FIG. 7. In particular, such patterned materials may be used in the fabrication of various interconnects of the interposer shown in FIG. 7. For example, the patterned materials described herein may be used in forming at least some of the trenches 708 and vias 710, which could be done instead of or in addition to a conventional dual damascene process.

[0061] FIG. 7 illustrates an interposer 700 that includes one or more embodiments of the disclosure. The interposer 700 is an intervening substrate used to bridge a first substrate 702 to a second substrate 704. The first substrate 702 may be, for instance, an integrated circuit die. The second substrate 704 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 700 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 700 may couple an integrated circuit die to a ball grid array (BGA) 706 that can subsequently be coupled to the second substrate 704. In some embodiments, the first and second substrates 702/804 may be attached to opposing sides of the interposer 700. In other embodiments, the first and second substrates 702/804 may be attached to the same side of the interposer 700. In further embodiments, three or more substrates may be interconnected by way of the interposer 700.

[0062] The interposer 700 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[0063] The interposer may include metal interconnect trenches 708 and vias 710, including but not limited to through-silicon vias (TSVs) 712. The vias 710 may be enclosed by first and second diffusion barrier layers as described herein. The interposer 700 may further include embedded devices 714, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 700.

Implementation in a computing device

[0064] In accordance with embodiments of the disclosure, materials comprising one of more transition metals and patterned by the atomic layer etching as disclosed herein may be used in the fabrication of a computing device, such as e.g. the one shown in FIG. 8. In particular, such patterned materials may be used in the fabrication of various interconnects of the computing device shown in FIG. 8 or/and in the fabrication of various memory elements shown in FIG. 8, such as e.g. on-die memory 806.

[0065] Figure 8 illustrates a computing device 800 in accordance with one embodiment of the disclosure. The computing device 800 may include a number of components. In one embodiment, these components may be attached to one or more motherboards. In an alternate embodiment, some or all of these components may be fabricated onto a single system-on-a-chip (SoC) die. The components in the computing device 800 include, but are not limited to, an integrated circuit die 802 and at least one communications logic unit 808. In some implementations the communications logic unit 808 may be fabricated within the integrated circuit die 802 while in other implementations the communications logic unit 808 may be fabricated in a separate integrated circuit chip that may be bonded to a substrate or motherboard that may be shared with or electronically coupled to the integrated circuit die 802. The integrated circuit die 802 may include a CPU 804 as well as on-die memory 806, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STT-MRAM).

[0066] Computing device 800 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 810 (e.g., DRAM), non-volatile memory 812 (e.g., ROM or flash memory), a graphics processing unit 814 (GPU), a digital signal processor 816, a crypto processor 842 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 820, an antenna 822, a display or a touchscreen display 824, a touchscreen controller 826, a battery 828 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 828, a compass 830, a motion coprocessor or sensors 832 (that may include an accelerometer, a gyroscope, and a compass), a speaker 834, a camera 836, user input devices 838 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 840 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0067] The communications logic unit 808 enables wireless communications for the transfer of data to and from the computing device 800. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communications logic unit 808 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 800 may include a plurality of communications logic units 808. For instance, a first communications logic unit 808 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communications logic unit 808 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0068] The processor 804 of the computing device 800 may include one or more interconnects or other lithographically patterned features that are formed in accordance

with embodiments of the present disclosure. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0069] The communications logic unit 808 may also include one or more interconnects or other lithographically patterned features that are formed in accordance with embodiments of the present disclosure.

[0070] In further embodiments, another component housed within the computing device 800 may contain one or more interconnects or other lithographically patterned features that are formed in accordance with embodiments of the present disclosure.

[0071] In various embodiments, the computing device 800 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 800 may be any other electronic device that processes data.

[0072] Some Examples in accordance with various embodiments of the present disclosure are now described.

[0073] Example 1 provides a method of etching a material including one or more transition metals, the method including oxidizing a surface of the material using halogenation; complexing the oxidized surface of the material with one or more complexing agents to form adducts including atoms of the one or more transition metals; and thermally removing the adducts from the surface.

[0074] Example 2 provides the method according to Example 1, where said oxidizing includes delivering one or more halogenating agents.

[0075] Example 3 provides the method according to Example 2, where the one or more halogenating agents are delivered in a gas phase.

[0076] Example 4 provides the method according to Examples 2 or 3, where the one or more halogenating agents include halosuccinimides, dihalo-triorganophosphines, and iodobenzenedichlorides.

[0077] Example 5 provides the method according to any one of the preceding Examples, where the one or more complexing agents include neutral chelating ligands.

[0078] Example 6 provides the method according to Example 5, where the one or more complexing agents include N,N'-tert-butyl-1,4-diazabutadiene (DABD).

[0079] Example 7 provides the method according to any one of the preceding Examples, where said complexing includes delivering the one or more complexing agents in a gas phase.

[0080] Example 8 provides the method according to any one of the preceding Examples, where each adduct includes a product of addition of a halide of one of the one or more transition metals and one of the one or more complexing agents.

[0081] Example 9 provides the method according to any one of the preceding Examples, where said thermal removing includes evaporating the adducts from the surface by heating the material to a temperature between 50 and 400 degrees Celsius.

[0082] Example 10 provides the method according to any one of the preceding Examples, where said thermal removing includes evaporating the adducts from the surface during a time period between 0.1 and 4 hours.

[0083] Example 11 provides the method according to any one of Examples 1-8, where said thermal removing includes evaporating the adducts from the surface at a room temperature during a time period between 0.1 and 4 hours.

[0084] Example 12 provides the method according to any one of Examples 1-11, where the one or more transition metals include cobalt (Co).

[0085] Example 13 provides the method according to any one of Examples 1-11, where the one or more transition metals include iron (Fe).

[0086] Example 14 provides the method according to any one of Examples 1-11, where the material includes a ferromagnetic alloy of iron (Fe), cobalt (Co), or nickel (Ni) mixed with one or more of main group elements.

[0087] Example 15 provides the method according to Example 14, where the ferromagnetic alloy includes CoFeB.

[0088] Example 16 provides the method according to any one of Examples 1-11, where the material includes permalloy (Ni/Fe).

[0089] Example 17 provides a device including a patterned material including one or more transition metals, where a surface of the material includes phosphorous (P) in concentration between 0.5 and 5 atomic percent.

[0090] Example 18 provides the device according to Example 17, where the device is a MRAM device.

[0091] Example 19 provides the device according to Example 17, where the device is an interconnect.

[0092] Example 20 provides a device including a patterned material including one or more transition metals, where a surface of the material includes nitrogen (N) in concentration between 0.5 and 5 atomic percent.

[0093] Example 21 provides the device according to Example 20, where the device is a MRAM device.

[0094] Example 22 provides the device according to Example 20, where the device is an interconnect.

[0095] Example 23 provides a device including a patterned material including one or more transition metals, where a surface of the material includes carbon (C) in concentration between 0.5 and 5 atomic percent.

[0096] Example 24 provides the device according to Example 23, where the device is a MRAM device.

[0097] Example 25 provides the device according to Example 23, where the device is an interconnect.

[0098] Example 26 provides an integrated circuit package that includes a component, and an interconnect region for providing electrical connectivity to the component, the interconnect region including: a patterned material including one or more transition metals, where a surface of the material includes phosphorous (P), nitrogen (N), or/and carbon (C) in concentration between 0.5 and 5 atomic percent.

[0099] Example 27 provides the integrated circuit package according to Example 26, where the component includes a transistor, a die, a sensor, a processing device, or a memory device.

[00100] Example 28 provides a computing device that includes the integrated circuit package according to Example 26.

[00101] Example 29 provides a computing device that includes a memory device comprising a patterned material including one or more transition metals, where a surface of the material includes phosphorous (P), nitrogen (N), or/and carbon (C) in concentration between 0.5 and 5 atomic percent.

[00102] The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

[00103] These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Claims

1. A method of etching a material comprising one or more transition metals, the method comprising:

oxidizing a surface of the material using halogenation;

complexing the oxidized surface of the material with one or more complexing agents to form adducts comprising atoms of the one or more transition metals; and

thermally removing the adducts from the surface.

2. The method according to claim 1, wherein said oxidizing comprises delivering one or more halogenating agents.

3. The method according to claim 2, wherein the one or more halogenating agents are delivered in a gas phase.

4. The method according to claims 2 or 3, wherein the one or more halogenating agents comprise halosuccinimides, dihalo-triorganophosphines, and iodobenzenedichlorides.

5. The method according to any one of claims 1-3, wherein the one or more complexing agents comprise neutral chelating ligands.

6. The method according to claim 5, wherein the one or more complexing agents comprise N,N'-tert-butyl-1,4-diazabutadiene (DABD).

7. The method according to any one of claims 1-3, wherein said complexing comprises delivering the one or more complexing agents in a gas phase.

8. The method according to any one of claims 1-3, wherein each adduct comprises a product of addition of a halide of one of the one or more transition metals and one of the one or more complexing agents.

9. The method according to any one of claims 1-3, wherein said thermal removing comprises evaporating the adducts from the surface by heating the material to a temperature between 50 and 400 degrees Celsius.

10. The method according to any one of claims 1-3, wherein said thermal removing comprises evaporating the adducts from the surface during a time period between 0.1 and 4 hours.

11. The method according to any one of claims 1-3, wherein said thermal removing comprises evaporating the adducts from the surface at a room temperature during a time period between 0.1 and 4 hours.

12. The method according to any one of claims 1-3, wherein the one or more transition metals comprise cobalt (Co).

13. The method according to any one of claims 1-3, wherein the one or more transition metals comprise iron (Fe).

14. The method according to any one of claims 1-3, wherein the material comprises a ferromagnetic alloy of iron (Fe), cobalt (Co), or nickel (Ni) mixed with one or more of main group elements.

15. The method according to claim 14, wherein the ferromagnetic alloy comprises CoFeB.

16. The method according to any one of claims 1-3, wherein the material comprises permalloy (Ni/Fe).

17. A device comprising:

a patterned material comprising one or more transition metals,

wherein a surface of the material comprises phosphorous (P) in concentration between 0.5 and 5 atomic percent.

18. The device according to claim 17, wherein the device is a Magnetic Random Access Memory (MRAM) device.

19. The device according to claim 17, wherein the device is an interconnect.

20. A device comprising:

a patterned material comprising one or more transition metals,

wherein a surface of the material comprises nitrogen (N) in concentration between 0.5 and 5 atomic percent.

21. The device according to claim 20, wherein the device is a Magnetic Random Access Memory (MRAM) device.

22. The device according to claim 20, wherein the device is an interconnect.

23. A device comprising:

a patterned material comprising one or more transition metals,

wherein a surface of the material comprises carbon (C) in concentration between 0.5 and 5 atomic percent.

24. The device according to claim 23, wherein the device is a Magnetic Random Access Memory (MRAM) device.

25. The device according to claim 23, wherein the device is an interconnect.

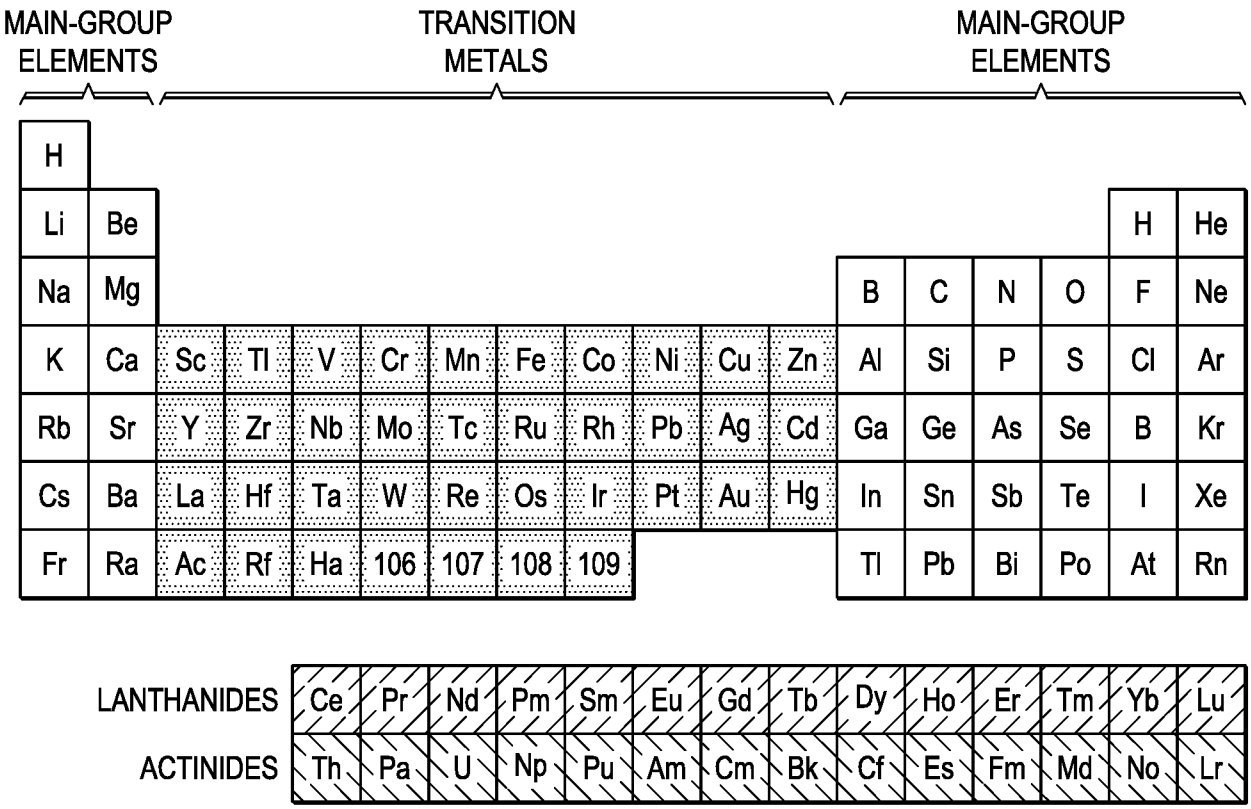
MAIN-GROUP ELEMENTS
TRANSITION METALS
MAIN-GROUP ELEMENTS
H
Li Be
Na Mg
K Ca Sc Tl V Cr Mn Fe Co Ni Cu Zn
Rb Sr Y Zr Nb Mo Tc Ru Rh Pb Ag Cd
Cs Ba La Hf Ta W Re Os Ir Pt Au Hg
Fr Ra Ac Rf Ha 106 107 108 109
B C N O F Ne
Al Si P S Cl Ar
Ga Ge As Se B Kr
In Sn Sb Te I Xe
Tl Pb Bi Po At Rn
H He
LANTHANIDES Ce Pr Nd Pm Sm Eu Gd Tb Dy Ho Er Tm Yb Lu
ACTINIDES Th Pa U Np Pu Am Cm Bk Cf Es Fm Md No Lr

FIG. 1

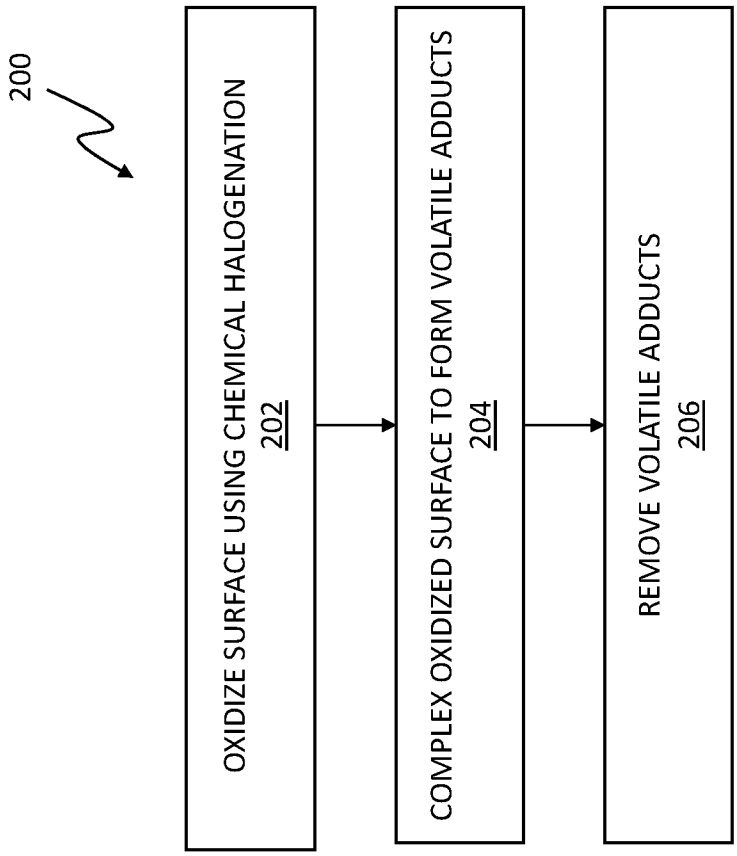
200
OXIDIZE SURFACE USING CHEMICAL HALOGENATION
202
COMPLEX OXIDIZED SURFACE TO FORM VOLATILE ADDUCTS
204
REMOVE VOLATILE ADDUCTS
206

FIG. 2

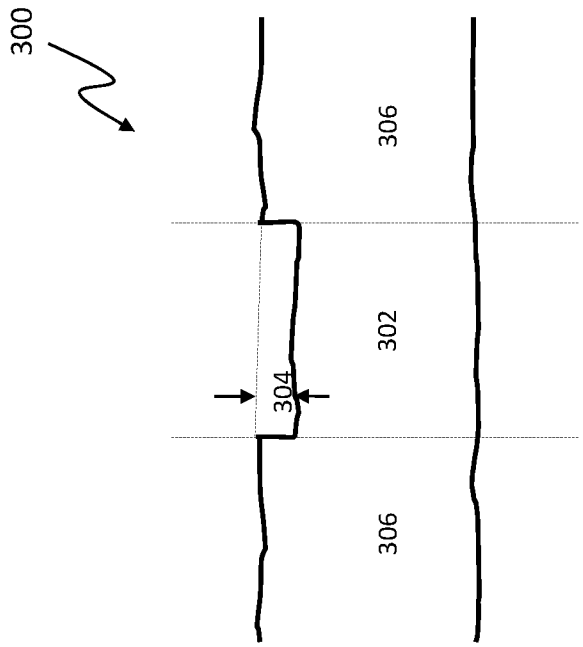

FIG. 3

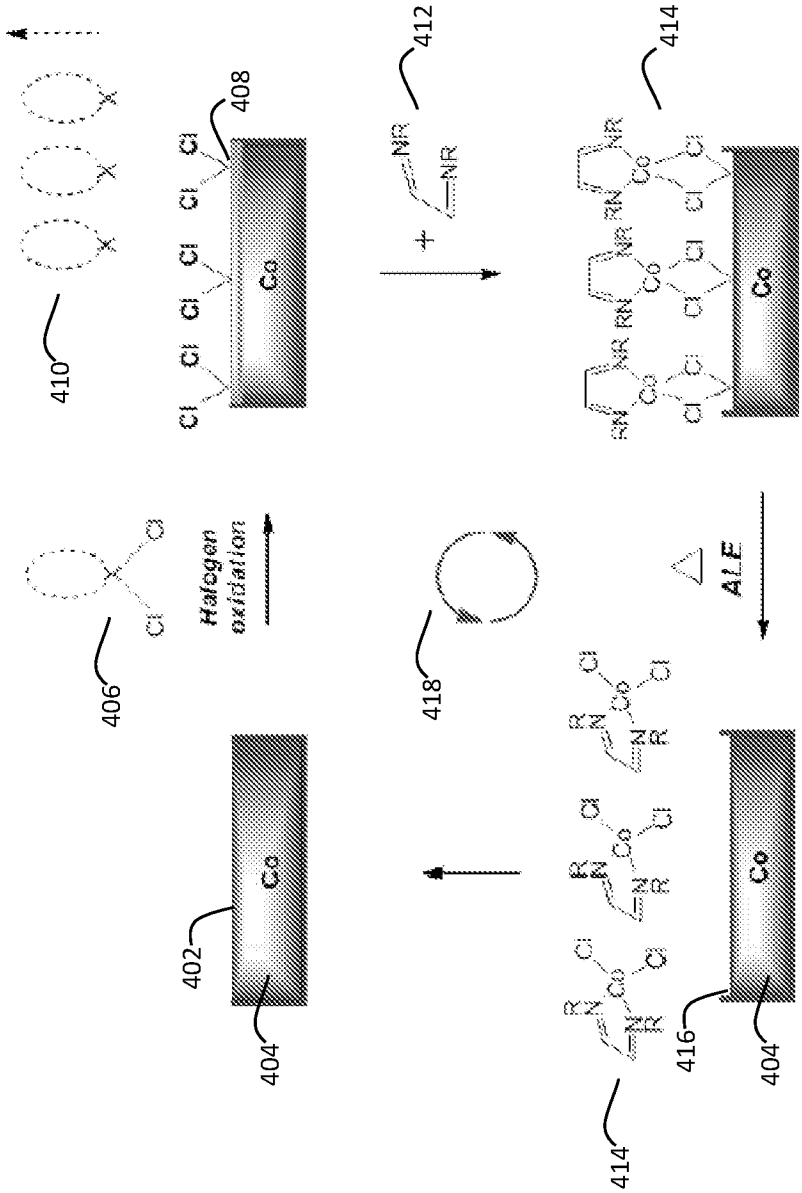
Halogen oxidation
ALE
Co
Cl
NR
RN
R
N
402
404
406
408
410
412
414
416
418

FIG. 4

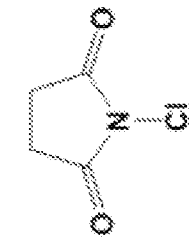

FIG. 5c

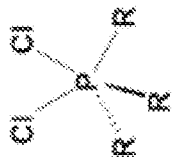

FIG. 5b

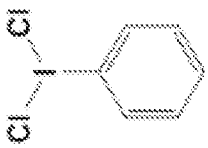

FIG. 5a

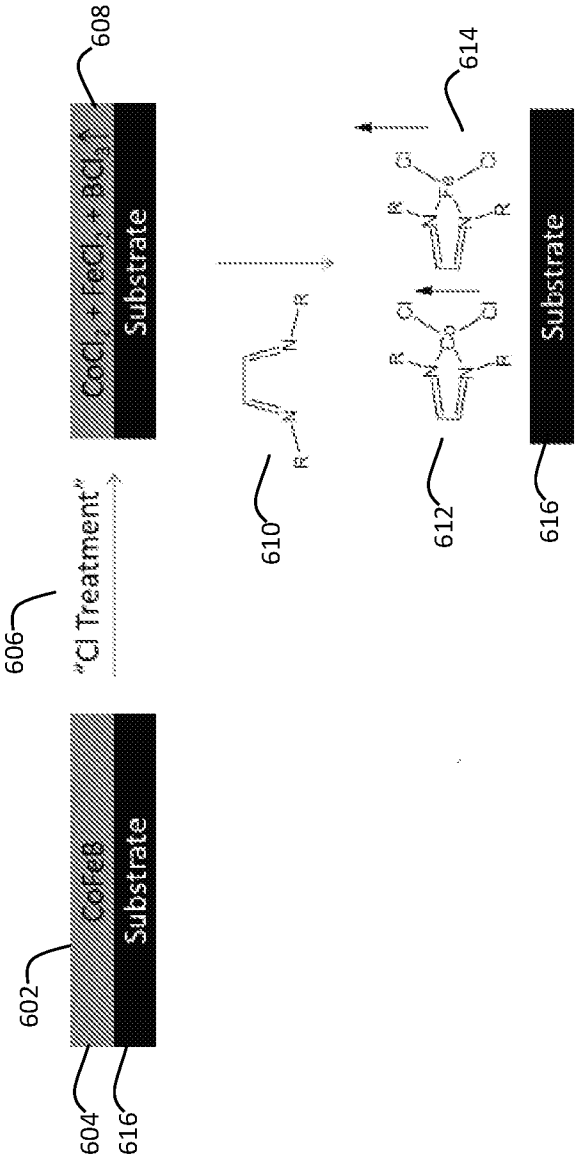
CoFeB
Substrate
602
604
616
606
"Cl Treatment"
CoCl + FeCl + BCl
Substrate
608
610
612
614
Substrate
616

FIG. 6

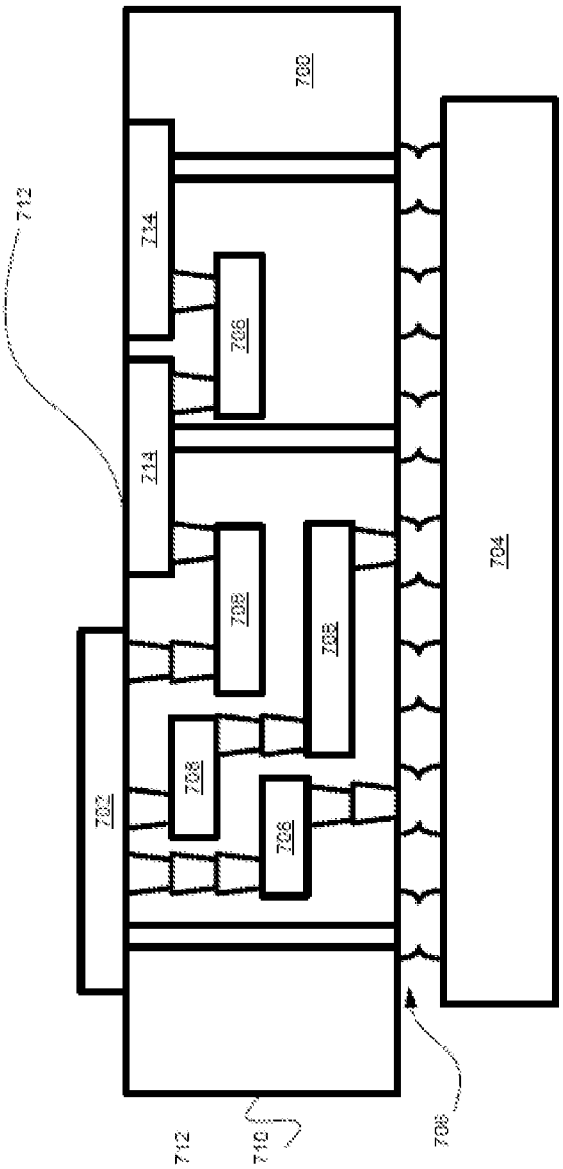

FIG. 7

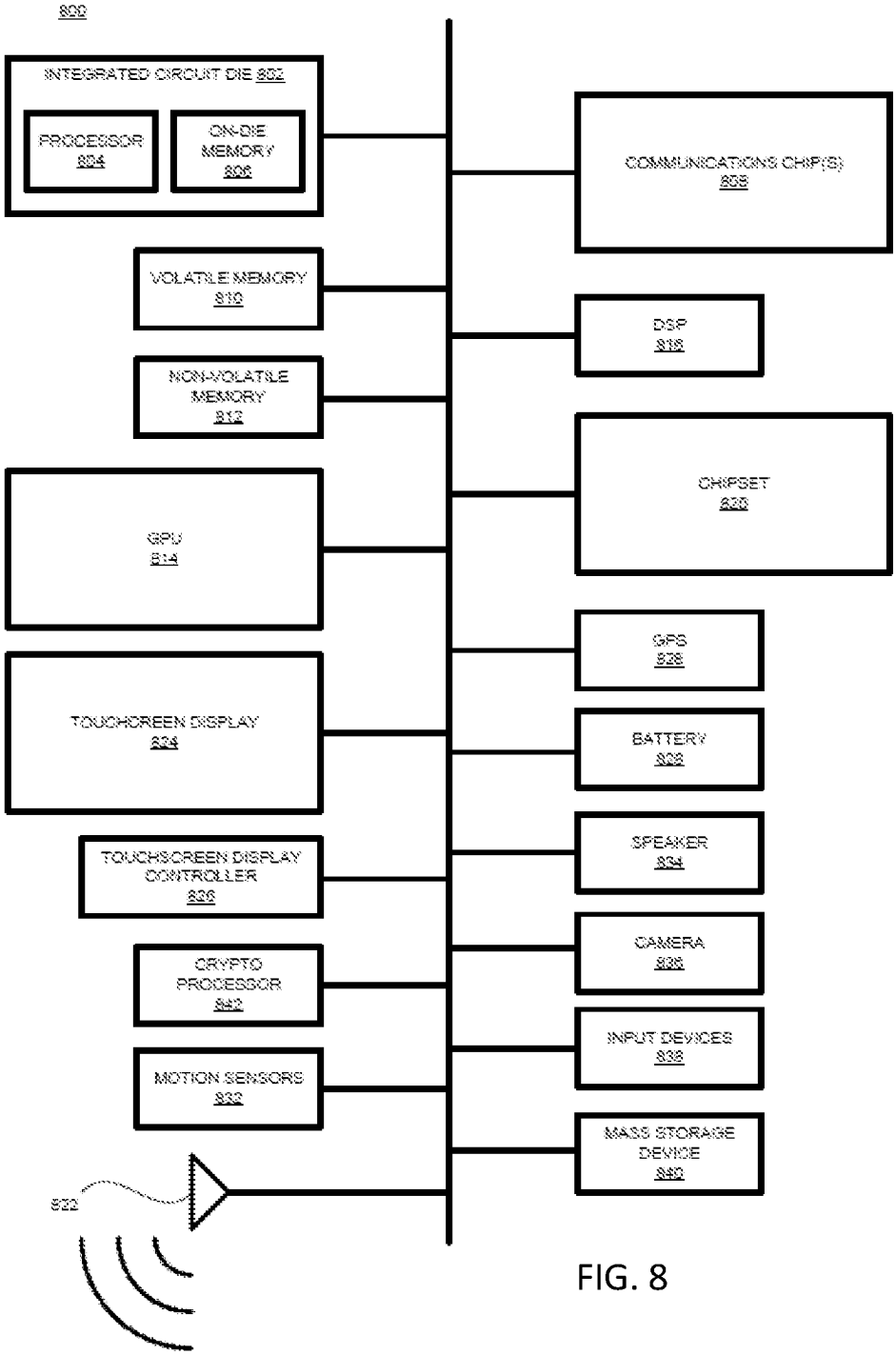
800
INTEGRATED CIRCUIT DIE 802
PROCESSOR 804
ON-DIE MEMORY 806
VOLATILE MEMORY 810
NON-VOLATILE MEMORY 812
GPU 814
TOUCHSCREEN DISPLAY 824
TOUCHSCREEN DISPLAY CONTROLLER 826
CRYPTO PROCESSOR 842
MOTION SENSORS 832
822
COMMUNICATIONS CHIP(S) 808
DSP 818
CHIPSET 820
GPS 828
BATTERY 830
SPEAKER 834
CAMERA 836
INPUT DEVICES 838
MASS STORAGE DEVICE 840

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/064357

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/3065(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/3065; H01L 21/3213; C23F 1/00; C23F 1/02; C23F 1/30; C23F 1/12; C03C 15/00; H01J 37/32; B44C 1/22; H01L 21/461

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: etching, patterning, transition metal, halogenation, chelating ligand, gas phase

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015-0345029 A1 (APPLIED MATERIALS, INC.) 03 December 2015 See abstract, paragraphs [0019]-[0029], claims 1-4 and figure 2.	1-25
A	US 2015-0129545 A1 (APPLIED MATERIALS, INC.) 14 May 2015 See abstract, paragraphs [0019]-[0035], claims 1-5 and figures 1, 2.	1-25
A	US 8124541 B2 (EUGENE P. MARSH) 28 February 2012 See abstract, columns 4, 5, claims 1-9 and figures 1A-1C.	1-25
A	US 2015-0162213 A1 (ADVANCED TECHNOLOGY MATERIALS, INC.) 11 June 2015 See abstract, paragraphs [0022]-[0034] and claim 1.	1-25
A	US 5814238 A (CAROL I. H. ASHBY et al.) 29 September 1998 See abstract and columns 3-7.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 August 2016 (24.08.2016)	**24 August 2016 (24.08.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
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CHOI, Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/064357

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2015-0345029 A1	03/12/2015	None	
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		US 2015-0129546 A1	14/05/2015
US 8124541 B2	28/02/2012	US 2008-0248653 A1	09/10/2008
		US 2012-0138850 A1	07/06/2012
		US 8475677 B2	02/07/2013
US 2015-0162213 A1	11/06/2015	EP 2847364 A1	18/03/2015
		EP 2847364 A4	28/10/2015
		KR 10-2015-0013268 A	04/02/2015
		TW 201406931 A	16/02/2014
		WO 2013-170130 A1	14/11/2013
US 5814238 A	29/09/1998	None	