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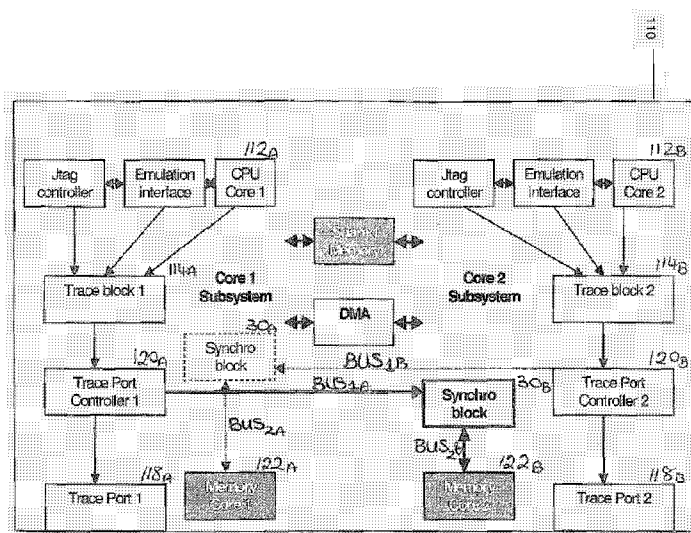
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(54) Title: METHOD AND SYSTEM FOR STORING DATA FROM A PLURALITY OF PROCESSORS



(57) Abstract: A method of storing data from a plurality of processors comprising the steps of : (a) transferring data along a first bus connectable between a first processor and a synchronising means and operable with a first protocol; (b) synchronising the synchronising means with a second processor; and (c) transferring the data along a second bus to a memory of the second processor wherein the second bus is connectable between the synchronising means and the memory of a second processor and operable with a second protocol.

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Title : Method and System for Storing Data from a Plurality of Processors**Description**Field of the invention

- 5 The present invention relates to a method and system for storing data from a plurality of processors. In particular, the present invention relates to a method and system for storing trace data from a plurality of sensors provided in a same integrated circuit.

Background of the invention

- 10 System-on-a-chip (SoC) technology is the packaging of all the electronic circuits and parts of a system, such as a cell phone or digital camera, on a single integrated circuit (IC). At present, a typical wireless baseband SoC comprises one or more microcontrollers, microprocessors or DSP core(s). The growing complexity of these systems has rendered the process of debugging increasingly
15 difficult.

There are a number of well-known embedded systems debugging tools including:

- (a) the Joint Test Action Group (JTAG) (IEEE
1149.1 specification);
- (b) background debug mode (BDM);
- 20 (c) on-chip emulation (OnCE);
- (d) break points and watch points.

However, these traditional debugging tools are proving inadequate to cope with the growing complexity of multi-core SoC systems. More recently, hardware tracing has been considered as a means of overcoming this problem.

- 25 Klaus McDonald-Maier & Andrew Hopkins, University of Kent, (<http://esemagazine.co.uk/common/viewer/archive/2004/Sep/28/feature6.phtm>) highlights the need for multi-core debuggers, but concentrates on the debugging tools aspect rather than the architecture of
30 such systems.

Abramson, T., C/C++ Users Journal 22 (6), June 2004 and Lemon, D, C/C++ Users Journal 20(4), April 2002 describe techniques for trace buffer manipulation. However, these techniques are mainly software based and targeted at single core architectures. Similarly, Balakrishanan S. et al.; Integrated Circuits and Systems Design, 2002. Proceedings, 15th Symposium 9-14 Sept. 2002 relates to single core tracing for a hyper-threaded processor.

Debug Support, Calibration and Emulation for Multiple Processor and Powertrain Control SoCs. Mayer, H. Siebert, K.D. McDonald-Maier. Infineon Technologies AG, Automotive & Industrial, Munich, Germany. University of Kent, Department of Electronics, Canterbury, CT2 7NT, UK, describes the inclusion of an additional package connected on an SoC. However, since additional hardware is required to implement this approach, it is likely to increase the die size of an SoC.

Summary of the invention

The present invention provides a method and system for storing data from a plurality of processors as described in the accompanying claims.

Brief description of the drawings

An embodiment of the invention will now be described by way of example only with reference to the accompanying Figures in which:

Figure 1 is a block diagram of a conventional SoC trace system; and

Figure 2 is a block diagram of a SoC trace system in accordance with the invention.

Detailed description of the preferred embodiments

A hardware trace comprises a history of the instructions executed by a microprocessor. It may also include context-switches between various tasks and addresses and values written to, or read from, memory.

In a conventional SoC trace system, each core on the SoC is provided with a dedicated hardware trace module that generates trace information from the core. For instance, the SoC trace system depicted in Figure 1 comprises two cores 12a and 12b, wherein cores 12a and 12b are respectively provided with hardware trace modules 14a and 14b. Each of the cores 12a and 12b is further provided

with an internal trace buffer 16a and 16b respectively (i.e. an embedded dedicated memory that may be accessed by software as scratch RAM) and/or a trace port 18a and 18b respectively. The trace ports 18a and 18b of the cores 12a and 12b respectively are connected to an external trace buffer (not shown). The trace
5 ports 18a and 18b may be alternatively connected to external analysis hardware (e.g. a logic analyser) to enable trace data to be analysed by the analysis hardware without first passing through the external trace buffer.

If any given core 12a or 12b on the SoC is provided with both an internal trace
10 buffer 16a or 16b and a trace port 18a or 18b, the core 12a or 12b is further provided with a trace port controller 20a or 20b respectively. The trace port controllers 20a and 20b act as data routers redirecting trace information to the internal trace buffers 16a and 16b respectively (via a dedicated bus BUS_{1a} or BUS_{1b} respectively) or the trace ports 18a and 18b as appropriate.

15 In use, trace data from the cores 12a and 12b is transmitted through their associated trace ports 18a and 18b respectively to the external trace buffer (not shown) wherein the trace data is stored for later processing. Although it should be noted that trace data may also be transmitted from trace ports 18a and 18b to
20 external hardware (such as a logic analyser) without passing through an external trace buffer.

However, trace data may also be stored in each core's internal trace buffer 16a or 16b respectively. This is mainly used if a number of events need to be tracked
25 over a short period of time. In particular, the rate at which data may be sampled and stored in the external trace buffer is limited by the response rate of the core's trace port 18a or 18b. However, if data is stored directly in the core's internal trace buffer 16a or 16b, the delay associated with core's trace port 18a or 18b can be avoided. A core's internal trace buffer 16a or 16b is also used if the core's trace
30 port 18a or 18b cannot be accessed because it has been multiplexed with another functional interface (e.g. a USB).

Each core may be further provided with a virtual trace buffer, which is essentially a part of the core's own memory 22a or 22b that is reserved for the storage of trace data.

5 However, internal trace buffers 16a and 16b are dedicated memory components, which are not used by the software of an SoC during normal operation. Since the internal trace buffers 16a and 16b cannot be used both as memory for tracing and as a scratch memory, the inclusion of internal trace buffers 16a and 16b on an SoC effectively reduces the amount of memory that could otherwise be
10 incorporated in the SoC for the applications running on the SoC. Furthermore, the inclusion of internal trace buffers 16a and 16b in an SoC increases the die size of the chip and hence the cost of the chip.

A virtual trace buffer 22a or 22b does not require the inclusion of an additional
15 memory element on an SoC, since the virtual trace buffer 22a or 22b is effectively a portion of the core's own memory. However, it limits the amount of the core's memory available for programs running thereon. This is likely to be particularly problematic when tracing part of a full production software stack, which uses all the memory available.

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The present invention modifies the traditional SoC trace system by removing the on-chip internal trace buffer(s) of the cores.

For the sake of simplicity, the SoC trace system in accordance with the invention
25 will be known henceforth as a modified SoC trace system. Similarly, the following discussion of the operation of the modified SoC trace system will focus on an exemplary dual core SoC. However, it will be understood that the modified SoC trace system is not limited to SoCs comprising only two cores, but could instead be extended to SoCs comprising more than two cores.

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Referring to Figure 2, in common with a conventional SoC trace system, each core 112a and 112b in a modified SoC trace system 110 is provided with a dedicated

hardware trace module 114a and 114b respectively that generates trace information from the core 112a or 112b. In further similarity with a conventional SoC trace system, each core 112a and 112b in a modified SoC trace system 110 is provided with a trace port 118a and 118b respectively and a trace port controller 120a and 120b respectively.

However, in contrast with a conventional SoC trace system, the cores 112a and 112b in a modified SoC trace system are not provided with an internal trace buffer. This significantly reduces the cost of the modified SoC trace system. Accordingly, the trace port controller in a modified SoC trace system redirects trace data (from a core) to either the trace port of the core or the memory of any other cores in the SoC (by means of a dedicated bus).

For simplicity, let the core whose trace data is being acquired be known as a donor core and the core in whose memory the trace data is being stored, be known as the recipient core. Then, using the modified SoC trace system depicted in Figure 2, trace data from donor core 12a may be stored inside a memory 122b of recipient core 12b. Alternatively, trace data from donor core 12b may be stored inside a memory 122a of recipient core 12a.

20

Thus, in contrast with the process of storing trace data in the virtual memory of a core in some prior art SoC trace systems, the modified SoC trace system is non-intrusive on the memory of a donor core. On another note, it should be recognised that since the size of the trace buffers in the modified SoC trace system is largely dependent on the memory available to a recipient core, the trace buffers in the modified SoC trace system can be significantly larger than that of the dedicated internal trace buffers of conventional SoC systems.

Since the cores in an SoC typically operate at different speeds, the transfer of trace data from a donor core into the memory of a recipient core must be carefully synchronised with the operation of the recipient core. Nonetheless, trace blocks

typically have an internal first-in first out (FIFO) register, which partially buffers the flow of trace data.

- In particular, information is transmitted from a donor core's trace port controller 120a or 120b to a synchronisation block 30a or 30b respectively through a dedicated bus $BUS_{1,a}$ or $BUS_{1,b}$ respectively. The dedicated bus $BUS_{1,a}$ or $BUS_{1,b}$ is the same as the bus between the trace port controller (20a and 20b respectively) and the internal trace buffer (16a and 16b respectively) in Figure 1.
- 10 The synchronisation block 30a or 30b is in turn connected to the memory 120a or 120b of the recipient core by another dedicated bus BUS_{2a} or BUS_{2b} respectively. This may be a shared bus if the synchronisation block 30a or 30b is connected to an arbiter (such as a cross-bar switch) to access the memory 120a or 120b.
- 15 The synchronisation block 30a or 30b synchronises the clock rates of BUS_{1a} or BUS_{1b} respectively; and BUS_{2a} or BUS_{2b} respectively. The synchronisation block 30a or 30b also acts as a bus protocol converter insofar as it converts the protocol of BUS_{1a} or BUS_{1b} respectively, into that of BUS_{2a} or BUS_{2b} respectively; for instance if BUS_{1a} or BUS_{1b} employs the Freescale IP bus protocol and BUS_{2a} or
- 20 BUS_{2b} employs the advanced high-performance bus (AHB) protocol.

- The tracing mechanism in the modified SoC trace system remains non-intrusive insofar as once programmed the hardware trace module 114a or 114b in each core generates trace data as normal. In particular, since the differences between
- 25 the modified SoC trace system and the conventional SoC trace system are mainly confined to the relationship between the trace port controller of a donor core and the memory of a recipient core, the modified SoC trace system has substantially no impact on the trace blocks and trace ports of the donor and recipient cores.

Accordingly, the modified SoC trace system has no impact on multicore tracing to external trace buffers through the trace ports or external hardware (e.g. a logic analyzer) that bypasses the external trace buffers. Furthermore, the modified SoC trace system has limited impact on the trace port controllers of the ports. Similarly, the modified SoC trace system does not impact on static debugging and multicore debugging if trace data is not being acquired.

The down side of the modified SoC trace system is that it is adapted for single core tracing. In particular, since it is necessary to reserve some space in a recipient core's memory for receipt of data from a donor core, the architecture of the modified SoC trace system impacts on the recipient core's software. However, if the software stacks running on the cores in an SoC are highly independent, there is no need to trace all the cores simultaneously. Consequently, it is sufficient to trace each core individually. This is more and more the tendency in wireless applications, wherein a single core modem stack runs on a DSP and applications run on the MCU.

Similarly, whilst, it is possible for the trace buffers on the different cores on the modified SoC system to be used simultaneously, it is not possible to simultaneously use the trace buffer of a recipient core and the trace port of a donor core.

Furthermore, accessing the content of the trace buffer at the end of a test is more complex than with a conventional SoC trace system. In particular, trace data analysis software cannot access the memory buffer directly but must setup a direct memory access (DMA) transfer therewith.

Modifications and alterations may be made to the above without departing from the scope of the invention.

Claims

A method of storing data from a plurality of processors comprising the steps of:

- (a) transferring data along a first bus (BUS_{1a}, BUS_{1b}) connectable between a first processor (12a, 12b) and a synchronising means (30a, 30b) and operable with a first protocol;
 - (b) synchronising the synchronising means (30a, 30b) with a second processor (12b, 12a); and
 - (c) transferring the data along a second bus (BUS_{2b}, BUS_{2a}) to a memory (122b, 122a) of the second processor (12b, 12a) wherein the second bus (BUS_{2a}, BUS_{2b}) is connectable between the synchronising means (30a, 30b) and the memory (122b, 122a) of a second processor (12b, 12a) and operable with a second protocol.
2. The method of Claim 1 wherein the step of synchronising the synchronising means (30a, 30b) with the second processor (12b, 12a) comprises the step of synchronising the synchronising means (30a, 30b) to a frequency of the second processor (12b, 12a).
3. The method of claim 1 or claim 2 wherein the step of synchronising the synchronising means (30a, 30b) with the second processor (12b, 12a) comprises the step of converting between the first protocol and the second protocol.
4. A system (110) for storing data from a plurality of processors comprising
 - a means of transferring data from a first processor (12a, 12b) to a synchronising means (30a, 30b);
 - a means of synchronising the synchronising means (30a, 30b) with a second processor (12b, 12a); and
 - a means of transferring the data from the synchronising means (30a, 30b) to a memory (122b, 122a) of the second processor (12b, 12a).

5. The system (110) according to Claim 4 wherein the data is hardware trace data.

6. The system (110) according to Claim 4 or Claim 5 wherein all the processors are provided on the same integrated circuit.

7. The system (110) according to any one of Claims 4 to 6 wherein the means of transferring data from the first processor (12a, 12b) to the synchronising means (30a, 30b) is a first bus (BUS_{1a}, BUS_{1b}) connectable therebetween; and

10 the means of transferring data from the synchronising means (30a, 30b) to the memory (122b, 122a) of the second processor (12b, 12a) is a second bus (BUS_{2b}, BUS_{2a}) connectable therebetween;

wherein the second bus (BUS_{2b}, BUS_{2a}) is a dedicated bus.

15 8. The system (110) according to any one of Claims 4 to 6 wherein the means of transferring data from the first processor (12a, 12b) to the synchronising means (30a, 30b) is a first bus (BUS_{1a}, BUS_{1b}) connectable therebetween; and

the means of transferring data from the synchronising means (30a, 30b) to the memory (122b, 122a) of the second processor (12b, 12a) is a second bus
20 (BUS_{2b}, BUS_{2a}) connectable therebetween;

wherein the second bus (BUS_{2b}, BUS_{2a}) is a shared bus and the system is further provided with an arbiter connected between the synchronising means (30a, 30b) and the second bus (BUS_{2b}, BUS_{2a}).

25 9. The system (110) according to Claim 8 wherein the arbiter is a crossbar switch.

10. The system (110) according to Claims 7 or Claim 8 wherein the first bus (BUS_{1a}, BUS_{1b}) is operable with a first protocol and the second bus (BUS_{2b},
30 BUS_{2a}) is operable with a second protocol and the synchronising means (30a, 30b) is adaptable to convert between the first and second protocols.

11. The system (110) according to any one of Claims 7 to 10 wherein the synchronising means (30a, 30b) is operable to synchronise with a frequency of the second processor (12b, 12a).

AMENDED CLAIMS

[Received by the International Bureau on 07 August 2007

(07.08.2007). Original claims 1-11 replaced by amended claims 1-10]

1. A method of storing hardware trace data from a plurality of processors comprising the steps of:

5 (a) transferring data along a first internal bus (BUS_{1a}, BUS_{1b}) connectable between a first processor (12a, 12b) and a synchronising block (30a, 30b) and operable with a first protocol;

(b) synchronising the synchronising block (30a, 30b) with a second processor (12b, 12a); and

10 (c) transferring the data along a second internal bus (BUS_{2b}, BUS_{2a}) to a memory (122b, 122a) of the second processor (12b, 12a) wherein the second internal bus (BUS_{2a}, BUS_{2b}) is connectable between the synchronising block (30a, 30b) and the memory (122b, 122a) of the second processor (12b, 12a) and operable with a second protocol, such that trace data from the first processor (12a, 15 12b) is stored in the memory (122b, 122a) of the second processor (12b, 12a).

2. The method of Claim 1 wherein the step of synchronising the synchronising block (30a, 30b) with the second processor (12b, 12a) comprises the step of synchronising the synchronising block (30a, 30b) to a frequency of the second 20 processor (12b, 12a).

3. The method of claim 1 or claim 2 wherein the step of synchronising the synchronising block (30a, 30b) with the second processor (12b, 12a) comprises the step of converting between the first protocol and the second protocol.

25

4. A system (110) for storing hardware trace data from a plurality of processors comprising

a means of transferring data from a first processor (12a, 12b) to a synchronising block (30a, 30b);

30 a means of synchronising the synchronising block (30a, 30b) with a second processor (12b, 12a); and

a means of transferring the data from the synchronising block (30a, 30b) to a memory (122b, 122a) of the second processor (12b, 12a), such that trace data from the first processor (12a, 12b) is stored in the memory (122b, 122a) of the second processor (12b, 12a).

5

5. The system (110) according to claim 4 wherein all the processors are provided on the same integrated circuit.

6. The system (110) according to any one of claims 4 to 5 wherein the means of transferring data from the first processor (12a, 12b) to the synchronising block (30a, 30b) is a first internal bus (BUS_{1a}, BUS_{1b}) connectable therebetween; and

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the means of transferring data from the synchronising block (30a, 30b) to the memory (122b, 122a) of the second processor (12b, 12a) is a second internal bus (BUS_{2b}, BUS_{2a}) connectable therebetween;

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wherein the second internal bus (BUS_{2b}, BUS_{2a}) is a dedicated internal bus.

7. The system (110) according to any one of claims 4 to 5 wherein the means of transferring data from the first processor (12a, 12b) to the synchronising block (30a, 30b) is a first internal bus (BUS_{1a}, BUS_{1b}) connectable therebetween; and

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the means of transferring data from the synchronising block (30a, 30b) to the memory (122b, 122a) of the second processor (12b, 12a) is a second internal bus (BUS_{2b}, BUS_{2a}) connectable therebetween;

wherein the second internal bus (BUS_{2b}, BUS_{2a}) is a shared internal bus and the system is further provided with an arbiter connected between the synchronising block (30a, 30b) and the second internal bus (BUS_{2b}, BUS_{2a}).

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8. The system (110) according to claim 7 wherein the arbiter is a crossbar switch.

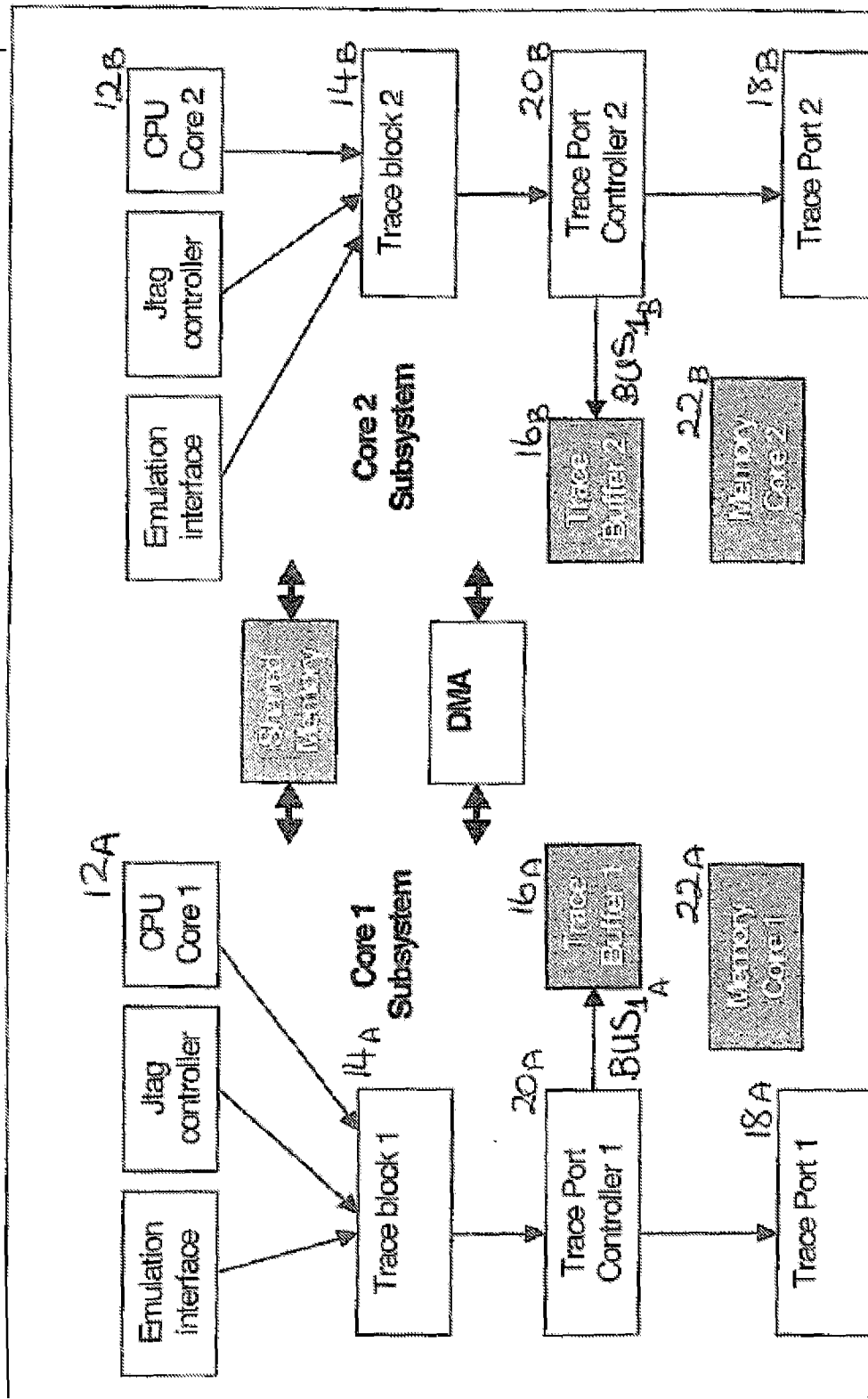
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9. The system (110) according to claims 6 or 7 wherein the first internal bus (BUS_{1a}, BUS_{1b}) is operable with a first protocol and the second internal bus

(BUS_{2b}, BUS_{2a}) is operable with a second protocol and the synchronising block (30a, 30b) is adaptable to convert between the first and second protocols.

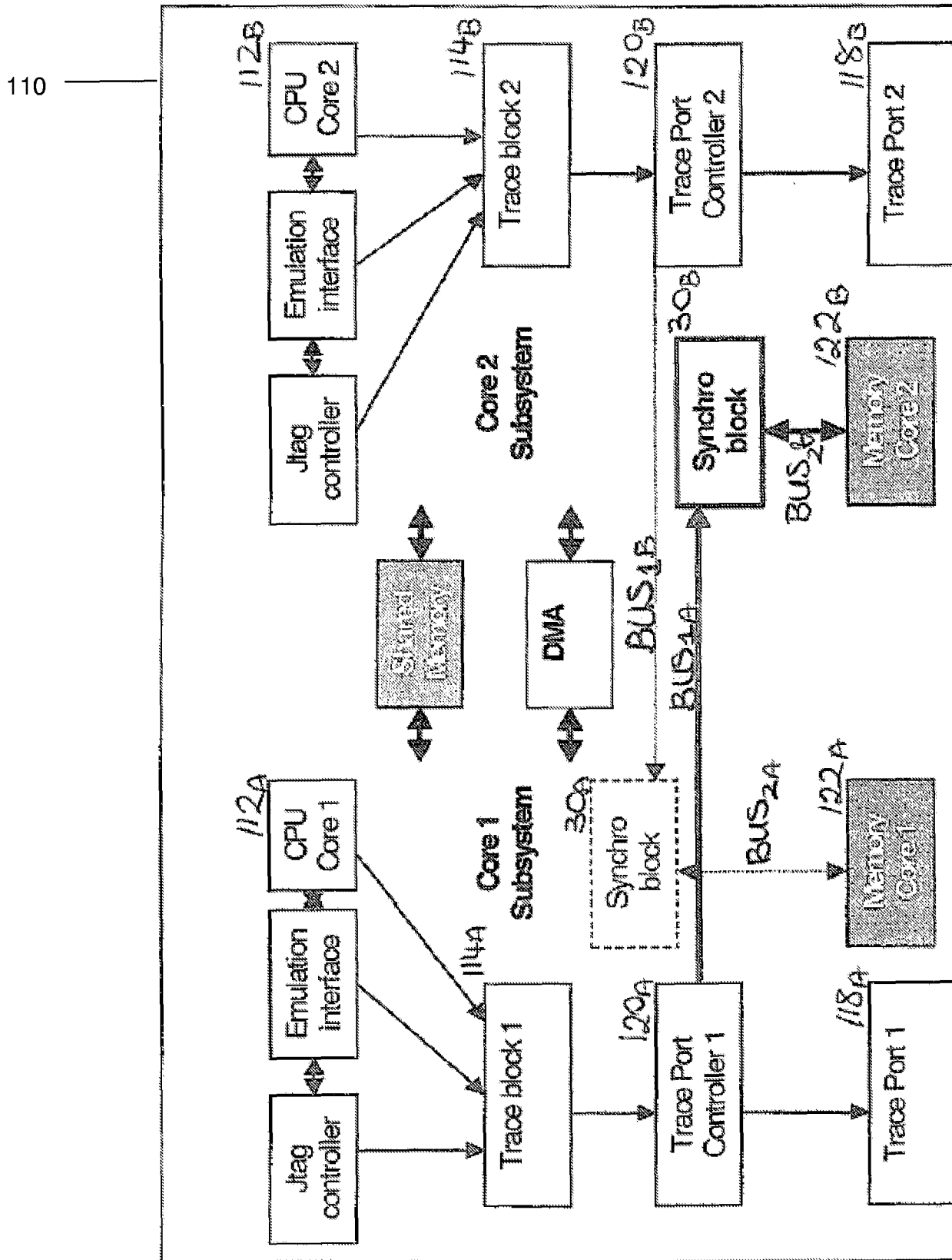
10. The system (110) according to any one of claims 7 to 9 wherein the
5 synchronising block (30a, 30b) is operable to synchronise with a frequency of the second processor (12b, 12a).

Figure 1



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Figure 2



INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER

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ADD. G06F13/40

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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 191 653 A (BANKS JOHN D J [US] ET AL) 2 March 1993 (1993-03-02) column 1, line 6 - column 2, line 61 claim 1	1-11
X	WO 99/66402 A (SUN MICROSYSTEMS INC [US]) 23 December 1999 (1999-12-23) abstract page 1, line 6 - page 2, line 3 page 6, line 16 - line 28	1-11
A	US 6 021 261 A (BARRETT JR ARCHIE DON [US] ET AL) 1 February 2000 (2000-02-01) column 1, line 9 - column 2, line 57 claims 1-5	1-11
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See patent family annex.

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INTERNATIONAL SEARCH REPORT

International application No

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

Information on patent family members

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