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Online:WPI,EPODOC,JAPIO

(54) Abstract Title
Signal receiver corrects baseline wander

(57) A signal receiver particularly for the reception of multi-level signals from a wire-based communication link has an isolating transformer 4 having a high-pass characteristic. A band-pass filter 5 of which the lower cut-off frequency is substantially above the cut-off frequency of the isolating transformer is disposed in line between the transformer and a signal slicer 2. A decision feedback equalizer 8 is responsive to a succession of values provided at an output of the slicer to provide a correction signal for the input of the slicer. The band-pass filter facilitates the correction of baseline wander by the decision feedback equalizer.

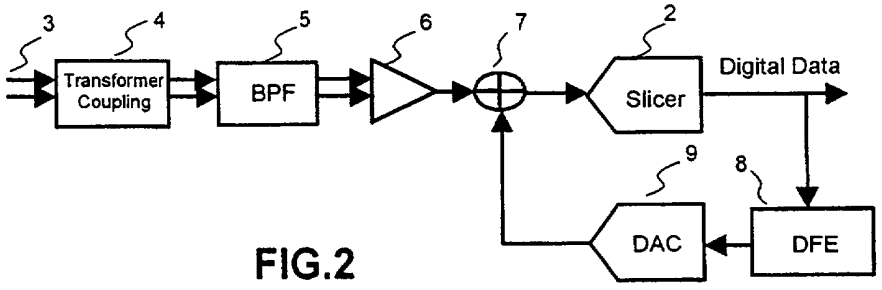

FIG.2

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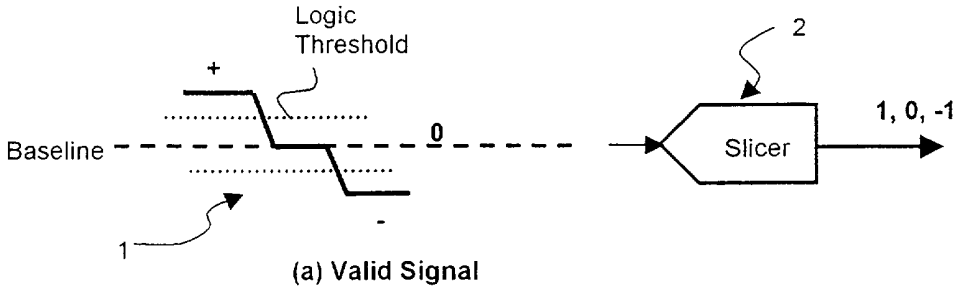

(a) **Valid Signal**

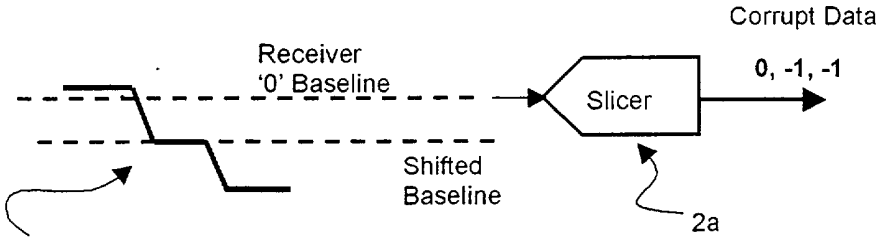

FIG.1

(b) **Invalid Signal with Baseline Wander**

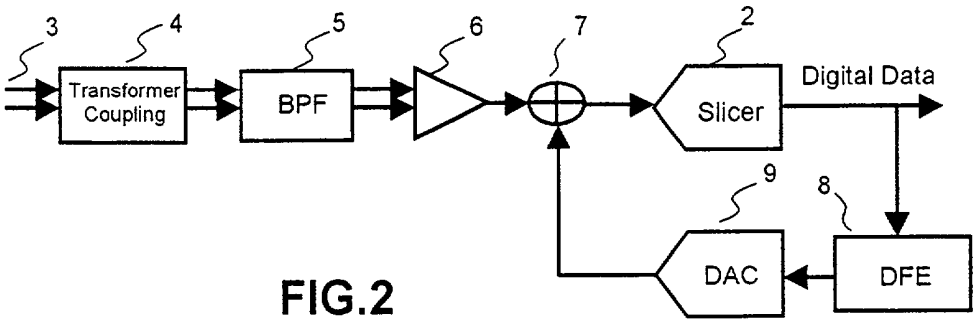

FIG.2

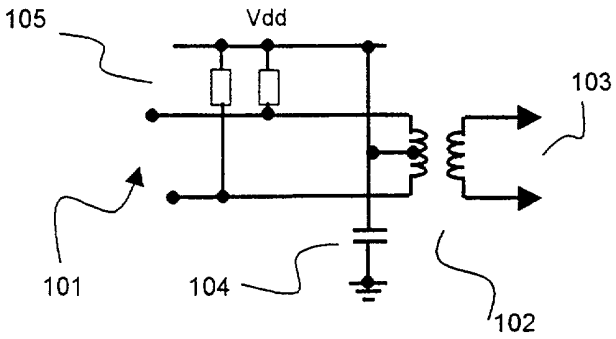

FIG.3

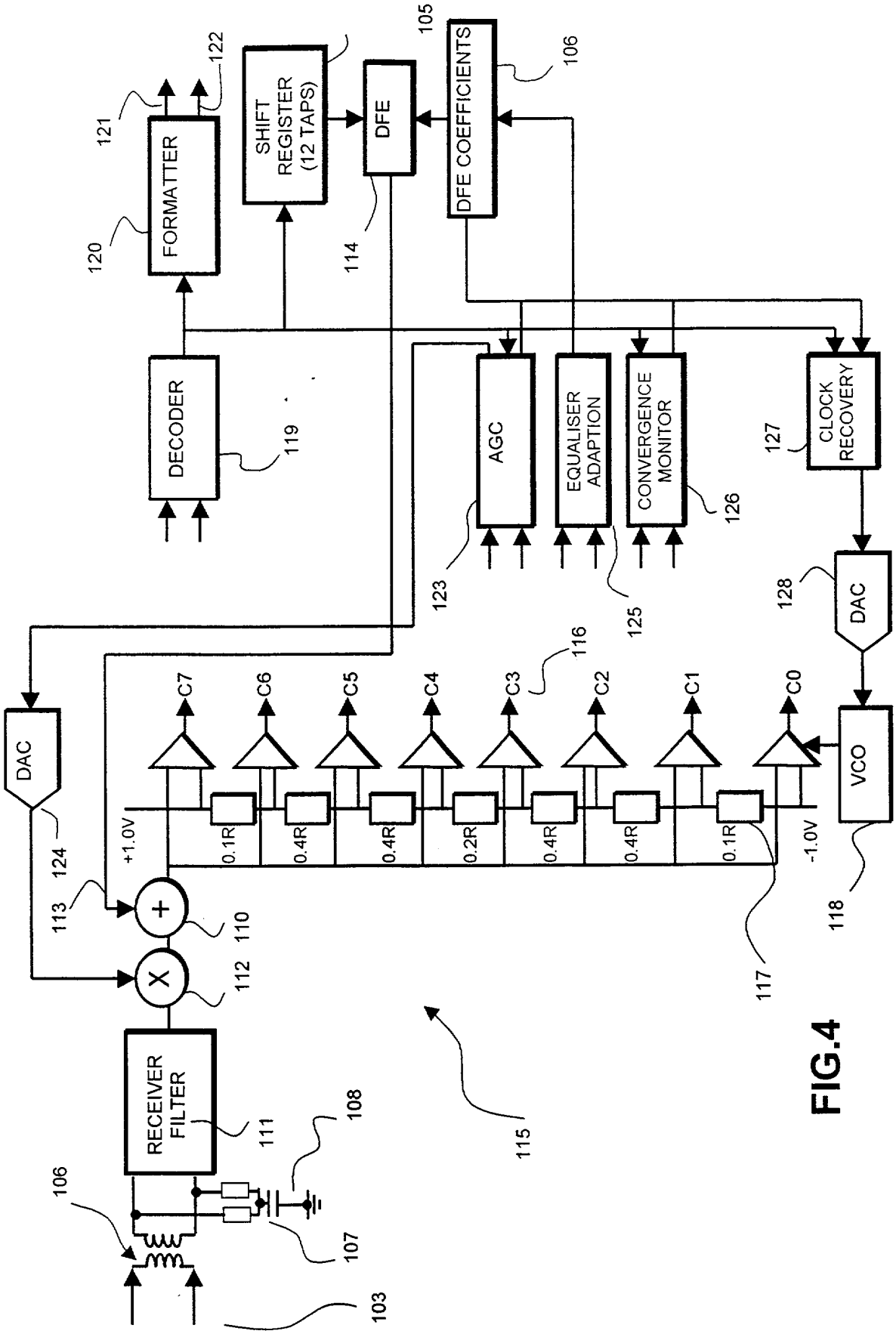
RECEIVER FILTER
111
108
106
107
103
115
112
110
113
124
DAC
+1.0V
-1.0V
0.1R
0.4R
0.4R
0.2R
0.4R
0.4R
0.1R
C7
C6
C5
C4
C3
C2
C1
C0
116
117
VCO
118
DAC
128
CLOCK RECOVERY
127
AGC
EQUALISER ADAPTION
CONVERGENCE MONITOR
126
123
125
DECODER
119
FORMATTER
120
121
122
SHIFT REGISTER (12 TAPS)
DFE
114
DFE COEFFICIENTS
105
106

FIG.4

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SIGNAL RECEIVER INCLUDING BAND-PASS FILTERING AND COMPENSATION FOR BASELINE WANDER

Field of the Invention

This invention relates to the reception of multi-level signals from a wire-based communication link. It is more particularly concerned with providing compensation for a wandering baseline caused by the attenuation of low frequencies by isolation transformers.

The invention is particularly though not exclusively intended for use in transmission systems in which an analog carrier signal of constant frequency has its amplitude modulated usually in accordance with a binary digital bit stream, by a multi-level signal. For example the amplitude variation applied to the analog carrier signal may provide three nominal amplitude levels, known as -1, 0 and +1 respectively, represented by a negative voltage relative to a datum or baseline level, the datum or baseline level and a positive voltage relative to the datum or baseline level. Typically, a binary zero is represented by the occurrence of two consecutive similar symbols, namely the occurrence of the same carrier amplitude in one symbol period as in the previous symbol period and a binary 1 is represented by a change from one symbol to another. Since the signal needs to be decoded by means of a signal slicer which has logic thresholds positioned between the baseline and the aforementioned positive and negative levels, it follows that variation or wandering of the baseline is liable to corrupt the output data.

Known methods for the correction of baseline wander include estimating the baseline droop based on an knowledge of the history of decoded symbols and the characteristics of the transformer and then adding back a correction factor to the input signal. This is the same principle as is used by a decision feedback equalizer. However, the time constant of the baseline wander is very long and for its full correction would require a very long decision feedback equalizer. Decision feedback equalizers are commonly employed to assist the correct decoding of received signals in the presence of frequency and phase distortion, particularly in systems employing partial response signalling. Typically, if a

decision feedback equalizer is to have, for example, twelve taps of the received data stream in order to provide correct decoding, it might require up to thirty taps if it were to be used for providing compensation for baseline wander. It is possible to provide modelling of a transformer's impulse response by means of an IIR (infinite impulse response) filter but the provision of an additional filter of this nature adds unwanted complexity to a receiver.

In a preferred form of the present invention, a transformer-coupled receiver which includes a decision feedback equalizer includes an in-line band-pass filter. This may be realized such that the long time constant high pass effect of the transformer is replaced with a much shorter time constant high pass effect due to the band-pass filter and accordingly the decision feedback equalizer may be much shorter than it would otherwise be. More particularly a single decision feedback equalizer may be employed not only for equalizing the frequency response of the transmission cable but also for effective compensation for baseline wander.

Further features of the invention will become apparent from the following description and the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a diagram illustrating baseline wander.

Figure 2 is a schematic drawing illustrating an embodiment of the invention in a basic simplified form.

Figure 3 illustrates a transmitting end of a transmission line.

Figure 4 illustrates a specific embodiment of the invention.

Figure 1 of the drawings illustrates at (a) valid signal levels in a multi-level signal format, particularly the format known as Fast Ethernet, which employs a three level coding scheme usually called MLT-3. There are three levels of coding, a positive level denoted +1, a datum or baseline level, denoted 0, and a negative level, denoted -1. Although the invention is not limited to any specific form of coding, one form of coding of binary digital signals in a Fast Ethernet format provides for a binary 0 to be represented by two consecutive levels of the same value and a binary 1 by a change from one of the three signal levels to another.

In the absence of any alteration of the baseline by virtue of, typically, attenuation of low frequency signals, a signal received in the format shown in Figure 1(a) is received by a signal slicer 2, which in any convenient manner provides logical switching thresholds between the nominal signal levels. In the present case there would be a logic threshold between the +1 level and the 0 level and between the 0 level and the -1 level respectively.

Figure 1(b) also shows a data signal 1a which suffers from baseline wander, so that its baseline or '0' data level is offset from the receiver's '0' level. Although the separation of the nominal signal levels in these types of signal format are selected in order to allow for signal distortion and some baseline wander, the baseline wander for even short lengths of cable, such as a few metres thereof, can be severe enough to cause an offset or wander which substantially completely corrupts the receive data. In the specific example shown in Figure 1(b) the three shifted signal levels are interpreted by the slicer 2a as 0, -1 and 1 respectively instead of 1, 0 and -1.

Figure 2 illustrates in simplified form one embodiment of the invention. It shows part of a receiver which may be employed in, for example, a Fast Ethernet data communication network. It is not concerned with the processing or onward transmission of signals which are decoded from a transmission link.

In Figure 2, a transmission line 3, which may be a 'twisted-pair', is isolated from the receiver by means of an isolation transformer coupling 4. The received signal may, as

previously indicated, be in the form of a constant frequency carrier signal which has multi-level amplitude modulation such as is shown in Figure 1. It is customary to employ a decision feedback equalizer of which the main purpose is to compensate for high frequency attenuation and phase distortion caused by the transmission line. However, an isolation transformer disposed at each end of a transmission cable such as line 3 necessarily alternates low frequencies and typically has a high pass characteristic with a cut off (i.e. the 3dB point) between, for example, 30 Khz and about 500 Khz. The attenuation of these lower frequencies causes droop of the received signal when the transmitted signal contains significant low frequency components. In order that the receiver may achieve error free decoding, the baseline of the signal needs to be restored to its nominal centre level.

In the present embodiment, the receiver includes a band-pass filter 5 disposed in line between the transformer (as will be more particularly described with reference to Figure 3) and the input of a preamplifier 6. The output of this amplifier 6 is coupled to a summing junction 7 of which the output is coupled to a slicer 2 that provides a decoded output as explained with reference to Figure 1(a). A succession of values obtained from the output of the slicer is employed by a decision feedback equalizer 8 to generate a correction signal. This may be in digital form and therefore would be converted back into an analog signal by a digital to analog converter 9 before it is applied to the summing junction 7.

It should be understood that the purpose of the decision feedback equalizer is in any event to restore signal integrity by compensating for high frequency attenuation and phase distortion caused by the transmission cable 3. For this purpose the decision feedback equalizer may typically comprise a multi-tap digital FIR (finite impulse response) structure generating the feedback correction signal. Typically the decision feedback equalizer multiplies each of a succession of symbol values obtained at the output of the slicer with a respective coefficient, the sum of the products of the symbol values and the coefficients constituting the correction signal. It is known to adjust the coefficients employing some appropriate LMS (least mean squares) algorithm.

The band-pass filter 5 may be realised in any convenient manner, typically as a passive RC filter, to provide a transmission zero at zero frequency and real axis poles at frequencies below and above the carrier frequency of the signals to be received. The poles may be selected to provide, for a 125 Mhz carrier frequency (actually the clock frequency for the MLT-3 symbols), lower and higher 'cut off' frequencies (i.e. the 3dB points) between 12 and 24 Mhz and between 140 and160 Mhz respectively. The lower cut-off frequency of the filter 5 is substantially higher (e.g. at least an order of magnitude higher) than the cut-off frequency of the isolating transformers.

Thus, the incoming signal is filtered by the band-pass filter 5, which removes the low frequency components corrupted by the transformer 4 (and the other transformer at the other end of line 3). In effect, the long time-constant high pass effect of the transformers is replaced with a much shorter time-constant high pass filter owing to the band-pass filter so that the decision feedback equalizer 8 can compensate for the attenuation of the wanted signal at the lower frequencies, such as from zero frequency to 500 Khz.

The same principle is applicable in other wire communication systems, such as FDDI and ATM, which convey signals which may have strong low frequency components.

Figures 3 and 4 illustrate a specific example of the invention, Figure 3 illustrating the far end of a link and Figure 4 a receiver, which may include a decision feedback equalizer as generally described in British patent application number 9820060.3 filed 15 September 1998.

Figure 3 illustrates a transmitter (denoted by terminals 101) which has an output transformer 102, which is connected by way of a 'twisted-pair' transmission line 103 to the receiver shown in Figure 4. The centre tap of the primary winding of transformer 102 is connected to a positive voltage rail V_{dd} and by way of a capacitor 104 to earth. The terminals 101 are connected to V_{dd} by way of respective resistors 105.

At the receiving end the transmission line 103 is coupled to the primary winding of a isolation transformer 106. The ends of the secondary winding are coupled to earth by way of respective appropriate resistors 107 and a common capacitor 108. The secondary is coupled to the input of a receiver filter 111 which comprises a band-pass filter as previously described with reference to Figure 2. The filter 111 feeds a gain control amplifier 112 of which the output is coupled to a summing junction 110 which combines the amplified and filtered input signal with an offset signal which is intended to correct the receive signal prior to its quantization, to cancel both inter-symbol interference and baseline wander. The offset signal is produced by a decision feedback equalizer 114 in a manner to be described.

The compensated input signal is coupled to a slicer 15 which is composed of a plurality of comparators 116 each having a reference level set by a respective node in a chain of resistors 117 and another input coupled to the output from the summing junction 101. Sampling of the input signal by all the comparators 116 is under the control of a voltage controlled oscillator 118. The slicer 115 provides eight levels of quantization and therefore eight binary signals C0 to C7 according as the input signal exceeds the respective level or not. The level for output C0 is defined as a negative datum voltage, such as -1 volts, and the level for output C7 is an upper, positive datum voltage such as 1 volt. The intermediate levels are set by the values of the resistors, which are preferably symmetrically arranged.

In practice the whole of the analog signal path may be differential to improve immunity to noise, rather than 'unbalanced' as shown.

In order to decode a fast Ethernet signal, the outputs C2 and C5, which occur at 25% and 75% of the total range of the comparator between the levels associated with output C0 and C7 may be used. The outputs C2 and C5 are coupled to a decoder 119 which in accordance with slicing levels decodes the three level signal to a binary output which is converted by a formatter 120 into an NRZ output on line 121, accompanied a 'symbol valid' signal on line 122.

The decoded symbol values from the decoder 119 are entered into a shift register 105 which in this embodiment of the invention has twelve taps so as to provide the received symbol values for each of the twelve most recently received symbols. The individual symbol values are multiplied by the decision feedback encoding coefficients, the coefficients being obtained from the coefficient register 106, the sum of the products being converted into analog form before it is applied to the summing junction 124.

The symbol values and, as described in the aforementioned application, the plurality of the residual inter-symbol interference are used to control an automatic gain control circuit 123 which provides a digital gain control signal to a digital to analog converter 24 of which the output controls the gain control amplifier 12.

The symbol values in the plurality of the residual inter-symbol interference are also coupled to an equalizer adaptation circuit 25 which in a manner not relevant to the present invention computes and updates as necessary equalizer coefficients held in coefficient store 106.

The outputs C1, C3, C4 and C6 are used in a clock recovery circuit 127 operable to recover and track the clock signal embedded in the received signal. The output of the clock recovery circuit is a frequency trimming signal which is applied to a digital to analog converter 128 to control the voltage controlled oscillator that determines the sampling times for the slicer 115.

The slicer outputs C1, C3, C4 and C6 preferably control a convergence monitor 126 which is provided to indicate whether the equalizer adaptation, the automatic gain control and a clock recovery all converge satisfactorily.

The operation of a clock recovery circuit 127, the convergence monitor 126, the equalizer adaptation circuit 125, the automatic gain control 123 and the computation of the coefficients for the decision feedback encoder are governed by a high level control unit

which may for example set initial values of the coefficients, set time constants for the equalizer adaptation, check the operation of the convergence monitor and generally handle the transfer of data between the circuits its controls. The organisation and operation of such a high level control circuit is not directly important to the present invention and will not be described in detail.

Claims

1. A signal receiver comprising an isolating transformer having a high-pass characteristic, an in-line band-pass filter of which the lower cut-off frequency is substantially above the cut-off frequency of the isolating transformer, a signal slicer having an input coupled to the band-pass filter, and a decision feedback equalizer responsive to a succession of values provided at an output of the slicer to provide a correction signal for the input of the slicer.

2. A signal receiver according to claim 1 wherein the signal slicer includes comparators defining logic thresholds above and below a baseline datum.

3. A signal receiver according to claim 1 or claim 2 wherein the lower cut-off frequency is at least an order of magnitude higher than the high-pass cut-off frequency of the isolating transformer.

Amendments to the claims have been filed as follows

Claims

1. A signal receiver comprising an isolating transformer having a high-pass characteristic, an in-line band-pass filter of which the input is coupled to the output of the transformer, the lower cut-off frequency of the filter being substantially above the cut-off frequency of the isolating transformer, a signal slicer having an input coupled to the output of the band-pass filter, and a decision feedback equalizer responsive to a succession of values provided at an output of the slicer to provide a correction signal for the input of the slicer.

2. A signal receiver according to claim 1 wherein the signal slicer includes comparators defining logic thresholds above and below a baseline datum.

3. A signal receiver according to claim 1 or claim 2 wherein the lower cut-off frequency is at least an order of magnitude higher than the high-pass cut-off frequency of the isolating transformer.

The Patent Office

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Application No: GB 9926483.0 **Examiner:** B.J.SPEAR
Claims searched: 1-3 **Date of search:** 16 May 2000

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): H4P (PRE,PX)

Int Cl (Ed.7): H04B 3/32

Other: Online :WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	EP0049670A (Pays)	-

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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