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[Continued on next page]

(54) Title: TRACK AND HOLD ARCHITECTURE WITH TUNABLE BANDWIDTH

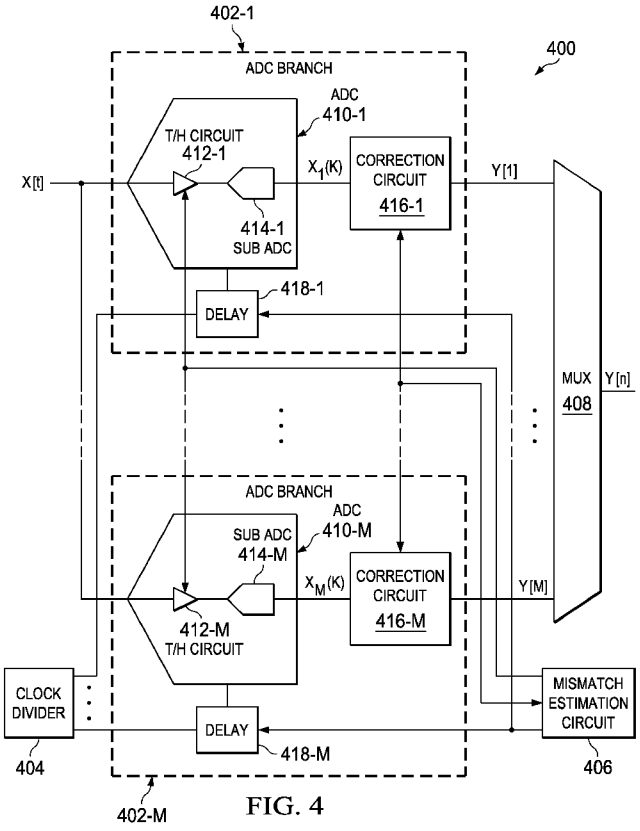

FIG. 4

(57) Abstract: An analog-to-digital converter (ADC) 400 converts analog input signal X(t) to a digital signal Y[n]. To do this, divider 402 divides a clock signal CLK (with a frequency of F_s or period of T_s) into M clock signals (each with a frequency of F_s/M) that are staggered by delay circuits 418- 1 to 418-M and provided to ADCs 410- 1 to 410-M. This allows each of ADCs 410- 1 to 410-M to convert the analog signal X(t) to digital signals $X_1(k)$ to X(k). The gain and DC offset adjustments are applied to digital signals $X_1(k)$ to $X_M(k)$ by correction circuits 416- 1 to 416-M to generate digital signals Y[1] to Y[M], which can then be multiplexed by multiplexer 408 to generate the digital signal Y[N].

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TRACK AND HOLD ARCHITECTURE WITH TUNABLE BANDWIDTH

[0001] This relates generally to analog-to-digital converters (ADCs) and, more particularly, to time-interleaved (TI) ADCs.

BACKGROUND

[0002] FIG. 1 shows a conventional analog-to-digital converter (ADC) 100. ADC 100 generally comprises a track-and-hold (T/H) circuit 102 and a sub-ADC 104 implemented so that, in operation, the ADC 100 can sample an analog input signal X(t) at a plurality of sampling instants and convert the sampled signal into a digital signal Y[n]. As is shown in FIG. 1, the T/H circuit 104 generally comprises switches and capacitors. The switch has a non-zero resistance, which causes the T/H circuit 102 to function as a filter (typically a single pole low pass filter).

[0003] Turning to FIG. 2, a model 200 of the ADC 100 is shown. In model 200, the filter aspects of the ADC 100 are represented by filter 202, while the remainder of the functionality of the ADC 100 is represented by ideal ADC 204. Filter 202 has a transfer function in the time-domain of $h_a(t)$, which can, in turn, be represented in the frequency-domain as:

$$H_a(\omega) = \frac{g_a e^{i\omega\Delta t}}{1 + i\left(\frac{\omega}{\omega_a}\right)}, \quad (1)$$

where g_a is the gain of ADC 100, Δt_a is the time delay relative to a reference, and ω_a is the cutoff frequency (bandwidth). This model 200 can be useful when determining mismatches for ADCs from, for example, Texas Instruments (TI).

[0004] In FIG. 3A, an example of a TI ADC 300 can be seen. TI ADC 300 generally comprises ADCs 100-1 to 100-M (where each of ADCs 100-1 to 100-M generally has the same structure as ADC 100 from FIG. 1) that are clocked by divider 302 so that the outputs from ADCs 100-1 to 100-M can be multiplexed by multiplexer 304 to produce digital signal Y[n]. Yet, when building TI ADC 300, ADCs 100-1 to 100-M are not identical to each other; there are slight structural and operational variations. These slight variations result in direct current (DC)

offset mismatches, timing skew, gain mismatches, and bandwidth mismatches between ADCs 100-1 to 100-M.

[0005] Of the different types of mismatches listed, the performance impact, as the result of bandwidth mismatches, are the weakest, and, to date, have largely been ignored, but, in order to build a high accuracy (generally greater than 6 bits), high speed (generally greater than 1 GS/s) TI ADCs, bandwidth mismatches between interleaved ADC branches need to be corrected. Looking to TI ADC 300, the output spectrum when the input signal is a tone with frequency ω_* can be represented as follows:

$$Y(e^{i\omega}) = \sum_{k=0}^{M-1}\left(\frac{1}{M}\sum_{a=0}^{M-1}H_a(\omega_*)e^{-i\frac{2\pi k}{M}a}\right)\delta\left(\omega-\omega_*-\frac{2\pi k}{M}\right). \quad (2)$$

Assuming a 2-way TI ADC (M=2), which generally represents the upper-bound or worst-case for bandwidth mismatch, equation (2) can be reduced to:

$$Y(e^{i\omega}) = \left(\frac{H_0(\omega_0)+H_1(\omega_0)}{2}\right)X(e^{i\omega}) + \left(\frac{H_0(\omega_0)-H_1(\omega_0)}{2}\right)X(e^{i(\omega-\pi)}) \quad (3)$$

with a Spurious-Free Dynamic Range (SFDR) of

$$SFDR = 20\log_{10}\left(\frac{H_0(\omega_0)+H_1(\omega_0)}{H_0(\omega_0)-H_1(\omega_0)}\right) \quad (4)$$

The SFDR for an M-way interleaved TI ADC, therefore, can then be determined to be:

$$SFDR = \max_k\left(20\log_{10}\left(\frac{A[0]}{A[k]}\right)\right) \quad (5)$$

where

$$A[k] = \sum_{a=0}^{M-1}H_a(\omega_0)e^{-i\frac{2\pi k}{M}a} \quad (6)$$

Now, equation (1) can be applied to TI ADC 300 for the purposes of simulation so

$$H_a(\omega_0) = \frac{1}{1+i\tau_a\omega_0}, \text{ for } T_S > \tau_a = \frac{1}{\omega_a}, \quad (7)$$

where T_S is the period of clock signal CLK. Such a simulation yields that variations in bandwidth mismatches are dependent on gain mismatches and timing skews and that (with high

accuracy, high speed TI ADCs) bandwidth mismatch can significantly affect performance. An example of a simulation of the effect bandwidth mismatch can be seen in FIG. 3B for different gain and skew compensations. Thus, to achieve the desired SFDR (i.e., greater than 70dB) for a TI ADC, the bandwidths of ADCs within the TI ADC should be matched to be within 0.1% to 0.25%.

[0006] To date, however, no estimation algorithm or circuit exists to blindly determine bandwidth mismatches. The two known most relevant conventional circuits are described in the following: Satarzadeh et al., "Bandwidth Mismatch Correction for a Two-Channel Time-Interleaved A/D Converter," Proceedings of 2007 IEEE International Symposium on Circuits and Systems, 2007; and Tsai et al., "Bandwidth Mismatch and Its Correction in Time-Interleaved Analog-to-Digital Converters," IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 53, No. 10, pp. 1133-1137, Oct. 23, 2006. Neither of these circuits adequately addresses blind bandwidth mismatch estimation.

[0007] Assuming, however, that one is able to adequately perform blind bandwidth mismatch estimation, adjustment of bandwidths of the T/H circuits (like T/H circuit 102) in TI ADC 300 can be difficult due at least in part to the precision of the bandwidth matching. A switched capacitor arrangement included within the T/H circuit 102 would be undesirable because it would be difficult to implement, and capacitive tuning (such as with a varactor and a tuning voltage) would also be undesirable because of signal dependencies. Thus, there is a need for a bandwidth adjustment circuit that can be adjusted from a blind bandwidth mismatch estimation.

[0008] Some other conventional circuits are described in U.S. Patent Nos. 5,500,612, 6,232,804 and 6,255,865; U.S. Patent Publ. Nos. 2004/0070439, 2004/0239545 and 2009/0009219; and in the publication Abo et al. "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," IEEE J. of Solid State Circuits, Vol. 34, No. 5, pp. 599-606, May 1999.

SUMMARY

[0009] An example embodiment provides an apparatus that comprises a clock divider that receives a clock signal; a plurality analog-to-digital converter (ADC) branches that each receive an analog input signal, wherein each ADC branch includes: a delay circuit that is coupled to the clock divider; an ADC having: a bootstrap circuit that is coupled to the delay circuit; a

sampling switch that is coupled to the bootstrap circuit; and a controller that is coupled to the bootstrap circuit to provide a control voltage to the bootstrap circuit so as to control a gate voltage of the sampling switch to adjust the impedance of the sampling switch when the sampling switch is actuated; a sampling capacitor that is coupled to the sampling switch; and a correction circuit that is coupled to the ADC; and a mismatch estimation circuit that is coupled to each delay circuit, each correction circuit, and each controller, wherein the mismatch estimation circuit provides a control signal to each controller to adjust for relative bandwidth mismatches between the ADC branches.

[0010] In accordance with an example embodiment, the apparatus further comprises a multiplexer that is coupled to each ADC branch.

[0011] In accordance with an example embodiment, the correction circuit adjusts the output of its ADC to correct for DC offset and gain mismatch.

[0012] In accordance with an example embodiment, the bootstrap circuit further comprises: a boost capacitor that is charged during a hold phase of the ADC; a transistor having first passive electrode, a second passive electrode, and a control electrode, wherein the first passive electrode of the transistor is coupled to the boost capacitor, and wherein the second passive electrode of the transistor is coupled to the sampling switch; a pass gate circuit that is coupled to the delay circuit, that is coupled to the control electrode of the transistor, and that receives the control voltage; and a skew circuit that is coupled to sampling switch and that is controlled by the control voltage.

[0013] In accordance with an example embodiment, the transistor further comprises a first transistor, and wherein the pass gate circuit further comprises: a second transistor having a first passive electrode, a second passive electrode, and a control electrode, wherein the first passive electrode of the second transistor is coupled to the controller so as to receive the control voltage, and wherein the control electrode of the second transistor is coupled to the delay circuit, and wherein the second passive electrode of the second transistor is coupled to the control electrode of the first transistor; a third transistor having a first passive electrode, a second passive electrode, and a control electrode, wherein the first passive electrode of the third transistor is coupled to the second passive electrode of second transistor, and wherein the control electrode of the third transistor is coupled to the delay circuit; and a fourth transistor having a first passive electrode, a second passive electrode, and a control electrode, wherein the first passive electrode

of the fourth transistor is coupled to the control electrode of the first transistor, and wherein the control electrode of the fourth transistor is coupled to the sampling switch, and wherein the second passive electrode of the fourth transistor is coupled to the second passive electrode of the third transistor.

[0014] In accordance with an example embodiment, the skew circuit further comprises a fifth transistor having a first passive electrode, a second passive electrode, and a control electrode, wherein the first passive electrode of the fifth transistor is coupled to the sampling switch, and wherein the control electrode of the fifth transistor is coupled to the controller so as to receive the control voltage.

[0015] In accordance with an example embodiment, the controller is a digital-to-analog converter (DAC).

[0016] In accordance with an example embodiment, the controller is a charge pump.

[0017] In accordance with an example embodiment, an apparatus comprises a clock divider that receives a clock signal; a plurality ADC branches that each receive an analog input signal, wherein each ADC branch includes: a delay circuit that is coupled to the clock divider; an ADC having: a bootstrap circuit that is coupled to the delay circuit; a sampling switch that is coupled to the bootstrap circuit; a controller that is coupled to the bootstrap circuit to provide a control voltage to the bootstrap circuit so as to control a gate voltage of the sampling switch to adjust the impedance of the sampling switch when the sampling switch is actuated; a sampling capacitor that is coupled to the sampling switch; an output circuit that is coupled to the sampling capacitor; and a sub-ADC that is coupled to the output circuit; and an correction circuit that is coupled to the ADC; a mismatch estimation circuit that is coupled to each delay circuit, each correction circuit, and each controller, wherein the mismatch estimation circuit provides a control signal to each controller to adjust for relative bandwidth mismatches between the ADC branches; and a multiplexer that is coupled to each ADC branch.

[0018] In accordance with an example embodiment, an apparatus is provided that comprises a clock divider that receives a clock signal; a plurality ADC branches that each receive an analog input signal, wherein each ADC branch includes: a delay circuit that is coupled to the clock divider; an ADC having: a bootstrap circuit that is coupled to the delay circuit; a PMOS transistor that is coupled to the bootstrap circuit; a controller that is coupled to the bootstrap circuit to provide a control voltage to the bootstrap circuit so as to control a gate

voltage of the sampling switch to adjust the impedance of the sampling switch when the sampling switch is actuated; a sampling capacitor that is coupled to the PMOS transistor at its drain; an output circuit that is coupled to the sampling capacitor; and a sub-ADC that is coupled to the output circuit; and an correction circuit that is coupled to the ADC, wherein the correction circuit adjusts the output of its ADC to correct for DC offset and gain mismatch; a mismatch estimation circuit that is coupled to each delay circuit, each correction circuit, and each controller, wherein the mismatch estimation circuit provides a control signal to each controller to adjust for relative bandwidth mismatches between the ADC branches; and a multiplexer that is coupled to each ADC branch.

[0019] In accordance with an example embodiment, the PMOS transistor further comprises a first PMOS transistor, and wherein the bootstrap circuit further comprises: a boost capacitor that is charged during a hold phase of the ADC; a second PMOS transistor that is coupled to the boost capacitor at its source and the gate of the first PMOS switch at its drain; a pass gate circuit that is coupled to the delay circuit, that is coupled to the gate of the second PMOS transistor, and that receives the control voltage; and a skew circuit that is coupled to sampling switch and that is controlled by the control voltage.

[0020] In accordance with an example embodiment, the pass gate circuit further comprises: a third PMOS transistor that is coupled to the controller at its source, the delay circuit at its gate, and the gate of the second PMOS transistor at its drain; a first NMOS transistor that is coupled to the drain of the third PMOS transistor at its drain and the delay circuit at its gate; and a second NMOS transistor that is coupled to the drain of the third PMOS transistor at its drain, the source of the first NMOS transistor at its source, and the gate of the first PMOS transistor at its gate.

[0021] In accordance with an example embodimen, the skew circuit further comprises a third NMOS transistor that is coupled to the gate of the first PMOS transistor at its drain and the controller at its gate.

[0022] In accordance with an example embodiment, the controller is a DAC or a charge pump.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] Example embodiments are described with reference to accompanying drawings, wherein:

FIG. 1 is a circuit diagram of a conventional ADC;

FIG. 2 is a block diagram of a model of the ADC of FIG. 1;

FIG. 3A is a circuit diagram of a convention TI ADC using the ADC of FIG. 1;

FIG. 3B is an example of a simulation showing the effect of bandwidth mismatch on the Spurious-Free Dynamic Range (SFDR) of a TI ADC;

FIG. 4 is a circuit diagram of a TI ADC in accordance with an example embodiment of the invention;

FIG. 5 is a circuit diagram of the T/H circuit of FIG. 4;

FIG. 6 is a circuit diagram of the bootstrap circuit of 5; and

FIG. 7 is a graph depicting the bandwidth for the T/H circuit of FIG. 5 versus "on" resistance of the sampling switch of the T/H circuit of FIG. 5.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0024] In FIG. 4, the reference numeral 400 generally designates a TI ADC in accordance with an example embodiment of the invention. ADC 400 generally comprises ADC branches 402-1 to 402-M, divider 404, multiplexer or mux 408, and a mismatch estimation circuit 410. Each ADC branch 402-1 to 402-M also generally comprises (respectively) ADC 410-1 to 410-M, correction circuit 416-1 to 416-M, and adjustable delay element or circuit 418-1 to 418-M. Additionally, each ADC 410-1 to 410-M generally comprises (respectively) a T/H circuit 410-1 to 410-M and a sub-ADC 414-1 to 414-M.

[0025] In operation, TI ADC 400 converts analog input signal X(t) to a digital signal Y[n]. To accomplish this, divider 402 divides a clock signal CLK (with a frequency of F_S or period of T_S) into M clock signals (each with a frequency of F_S/M) that are staggered by delay circuits 418-1 to 418-M and provided to ADCs 410-1 to 410-M. This allows each of ADCs 410-1 to 410-M to convert the analog signal X(t) to digital signals $X_1(k)$ to $X_M(k)$. The gain and DC offset adjustments are applied to digital signals $X_1(k)$ to $X_M(k)$ by correction circuits 416-1 to 416-M to generate digital signals Y[1] to Y[M], which can then be multiplexed by mux 408 to generate a digital signal Y[N].

[0026] To generally ensure that signals Y[0] to Y[M-1] are matched, mismatch estimation circuit 410 calculates and compensates for gain mismatches, DC offset mismatches, timing skews, and bandwidth mismatches. The mismatch estimation circuit 410 is generally a digital signals processor (DSP) or dedicated hardware, which determines the gain mismatches,

DC offset mismatches, timing skews, and bandwidth mismatches and which can provide adjustments for gain, DC offset, timing skew, and bandwidth to correction circuits 416-1 to 416-M and T/H circuits 412-1 to 412-M. A more complete explanation of the mismatch estimation circuit 410 can be found in co-pending U.S. Patent Application Serial No. 12/572,717, which is entitled "BANDWIDTH MISMATCH ESTIMATION IN TIME-INTERLEAVED ANALOG-TO-DIGITAL CONVERTERS," and which is incorporated by reference for all purposes.

[0027] Turning now to FIG. 5, T/H circuits 412-1 to 412-M (hereinafter referred to as 412 for the sake of simplicity) can be seen in greater detail. T/H circuit 412 generally comprises a bootstrap circuit 502, a controller 504, a sampling switch S1 (which is typically an NMOS transistor or NMOS switch), a sampling capacitor CSAMPLE, and an output circuit 506. In operation, the bootstrap circuit 502 controls the actuation and de-actuation of the sampling switch S1 based at least in part on a clock signal CLKIN (which is received from a respective delay circuit 418-1 to 418-M) and a control voltage VCNTL from controller 504. Generally, the mismatch estimation circuit 406 provides a control signal to the controller 504 (which may be a digital-to-analog converter (DAC) or charge pump) to generate the control voltage VCNTL. The control voltage VCNTL, through the bootstrap circuit 502, is able to control the gate voltage of the sampling switch S1 to adjust the impedance or "on" resistance of the sampling switch S1 when the sampling switch S1 is actuated.

[0028] Looking to FIG. 6, the bootstrap circuit 502 can be seen in greater detail. When the clock signal CLKIN is logic low (such as during a hold phase), inverter 508 turns transistor Q1 (which is typically an NMOS transistor) "on," while pass gate circuit (which generally comprises transistors Q2, Q3, and Q5) maintains transistor Q4 (which is generally a PMOS transistor) in an "off" state. Assuming that signal CLKZ is logic high so that transistors Q8 and Q9 (which are typically NMOS transistors) are in an "on" state and during this logic low period of clock signal CLKIN, supply voltage VDD charges the boost capacitor CBOOST. When clock signal CLKIN transitions to logic high, pass gate circuit turns transistor Q4 "on," while transistors Q1 is turned "off." At this point, a voltage is applied to the gate of sampling switch S1 to turn it "on." This gate voltage for sampling switch S1 is generated at least in part from the discharge of capacitor CBOOST, the input signal IN (which is applied through transistor Q6), and the control voltage VCNTL (which is applied through the pass gate circuit and the skew circuit (which generally comprises transistors Q7 and Q8)). Generally, this control voltage

VCNTL is applied to the source of transistor Q2 (which is generally a PMOS transistor) and the gate of transistor Q7 (which is generally an NMOS transistor) so as to adjust the gate voltage of sample switch S1. Thus, the gate voltage of the sampling switch S1 can be easily controlled by varying control voltage VCNTL. Additionally, because the sampling switch S1 is generally a NMOS switch operating in a linear region, variation of this gate voltage varies the "on" resistance of the sampling switch S1, which adjusts the filter characteristics (and bandwidth) of the filter created by the sampling switch S1, resistor R1, and sampling capacitor CSAMPLE.

[0029] To illustrate the operation to bootstrap circuit 502 and sampling switch S1, a graph depicting bandwidth of T/H circuit 412 versus "on" resistance for the sampling switch S1 can be seen in FIG. 7. As can be seen, the bandwidth for T/H circuit 502 varies between about 2.956GHz at for a VCNTL DAC code of zero to about 3.051GHz for a VCNTL DAC code of 1023Ω. Thus, the bandwidths for multiple T/H circuits 412 (such as 412-1 to 412-M) with nominal bandwidths of 3GHz can be adjusted to match one another to between about 0.25% and about 0.1%.

[0030] Those skilled in the art to which the invention relates will appreciate that modifications can be made to the described example embodiments and that other embodiments are possible within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a clock divider that receives a clock signal;

a plurality of analog-to-digital converter (ADC) branches that each receives an analog input signal; wherein each ADC branch includes:

a delay circuit that is coupled to the clock divider;

an ADC having:

a bootstrap circuit that is coupled to the delay circuit;

a sampling switch that is coupled to the bootstrap circuit; and

a controller that is coupled to the bootstrap circuit to provide a control voltage to the bootstrap circuit so as to control a gate voltage of the sampling switch to adjust the impedance of the sampling switch when the sampling switch is actuated; and

a sampling capacitor that is coupled to the sampling switch; and

a correction circuit that is coupled to the ADC; and

a mismatch estimation circuit that is coupled to each delay circuit, each correction circuit and each controller; wherein the mismatch estimation circuit provides a control signal to each controller to adjust for relative bandwidth mismatches between the ADC branches.

2. The apparatus of Claim 1, wherein the apparatus further comprises a multiplexer that is coupled to each ADC branch.

3. The apparatus of Claim 2, wherein the correction circuit adjusts the output of its ADC to correct for DC offset and gain mismatch.

4. The apparatus of Claim 2, wherein the bootstrap circuit further comprises:

a boost capacitor that is charged during a hold phase of the ADC;

a transistor having a first passive electrode, a second passive electrode, and a control electrode; wherein the first passive electrode is coupled to the boost capacitor, and the second passive electrode is coupled to the sampling switch;

a pass gate circuit that is coupled to the delay circuit, that is coupled to the control electrode of the transistor, and that receives the control voltage; and

a skew circuit that is coupled to the sampling switch and that is controlled by the control voltage.

5. The apparatus of Claim 4, wherein the transistor further comprises a first transistor, and wherein the pass gate circuit further comprises:

a second transistor having a first passive electrode, a second passive electrode, and a control electrode; wherein the first passive electrode of the second transistor is coupled to the controller so as to receive the control voltage, the control electrode of the second transistor is coupled to the delay circuit, and the second passive electrode of the second transistor is coupled to the control electrode of the first transistor;

a third transistor having a first passive electrode, a second passive electrode, and a control electrode; wherein the first passive electrode of the third transistor is coupled to the second passive electrode of second transistor, and the control electrode of the third transistor is coupled to the delay circuit; and

a fourth transistor having a first passive electrode, a second passive electrode, and a control electrode; wherein the first passive electrode of the fourth transistor is coupled to the control electrode of the first transistor, the control electrode of the fourth transistor is coupled to the sampling switch, and the second passive electrode of the fourth transistor is coupled to the second passive electrode of the third transistor.

6. The apparatus of Claim 5, wherein the skew circuit further comprises a fifth transistor having a first passive electrode, a second passive electrode, and a control electrode; wherein the first passive electrode of the fifth transistor is coupled to the sampling switch, and the control electrode of the fifth transistor is coupled to the controller so as to receive the control voltage.

7. The apparatus of Claim 6, wherein the controller is a digital-to-analog converter (DAC).

8. The apparatus of Claim 6, wherein the controller is a charge pump.

9. An apparatus of Claim 1, wherein the apparatus further includes a multiplexer that is coupled to each ADC branch; and each ADC further includes a sub-ADC that is coupled to the output circuit.

10. The apparatus of claim 1, further comprising a multiplexer that is coupled to each ADC branch; and wherein the sampling switch includes a PMOS transistor coupled to the bootstrap circuit, the sampling capacitor is coupled to the drain of the PMOS transistor, the ADC includes an output circuit coupled to the sampling capacitor and includes a sub-ADC coupled to the output circuit; and the correction circuit adjusts the output of its ADC to correct for DC offset and gain mismatch.

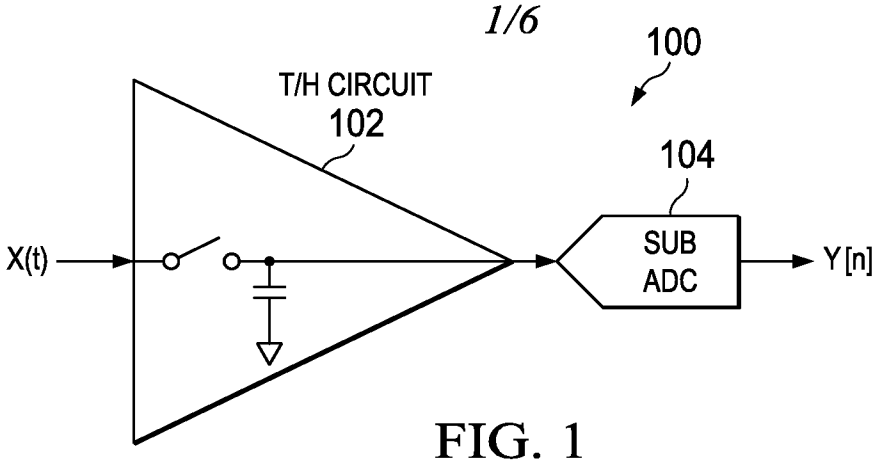


FIG. 1
(PRIOR ART)

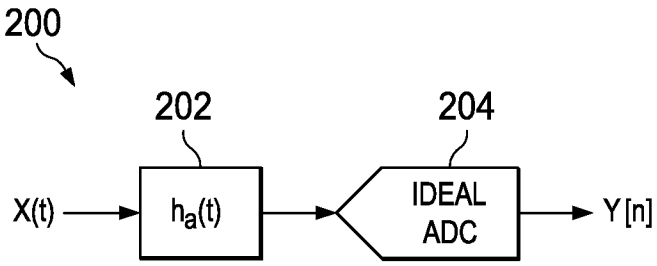


FIG. 2
(PRIOR ART)

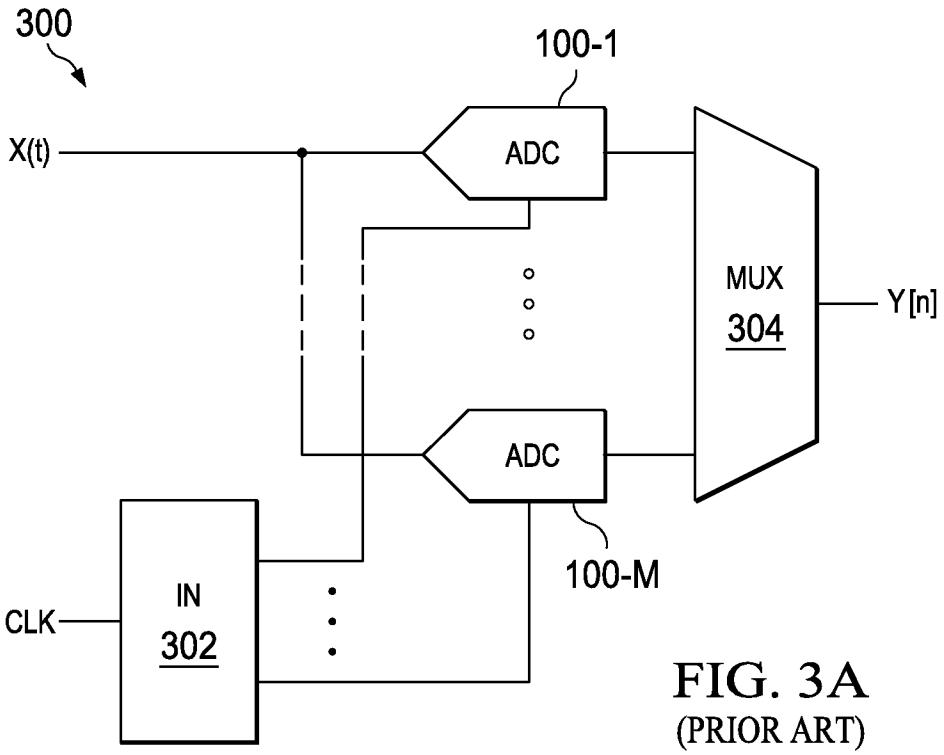
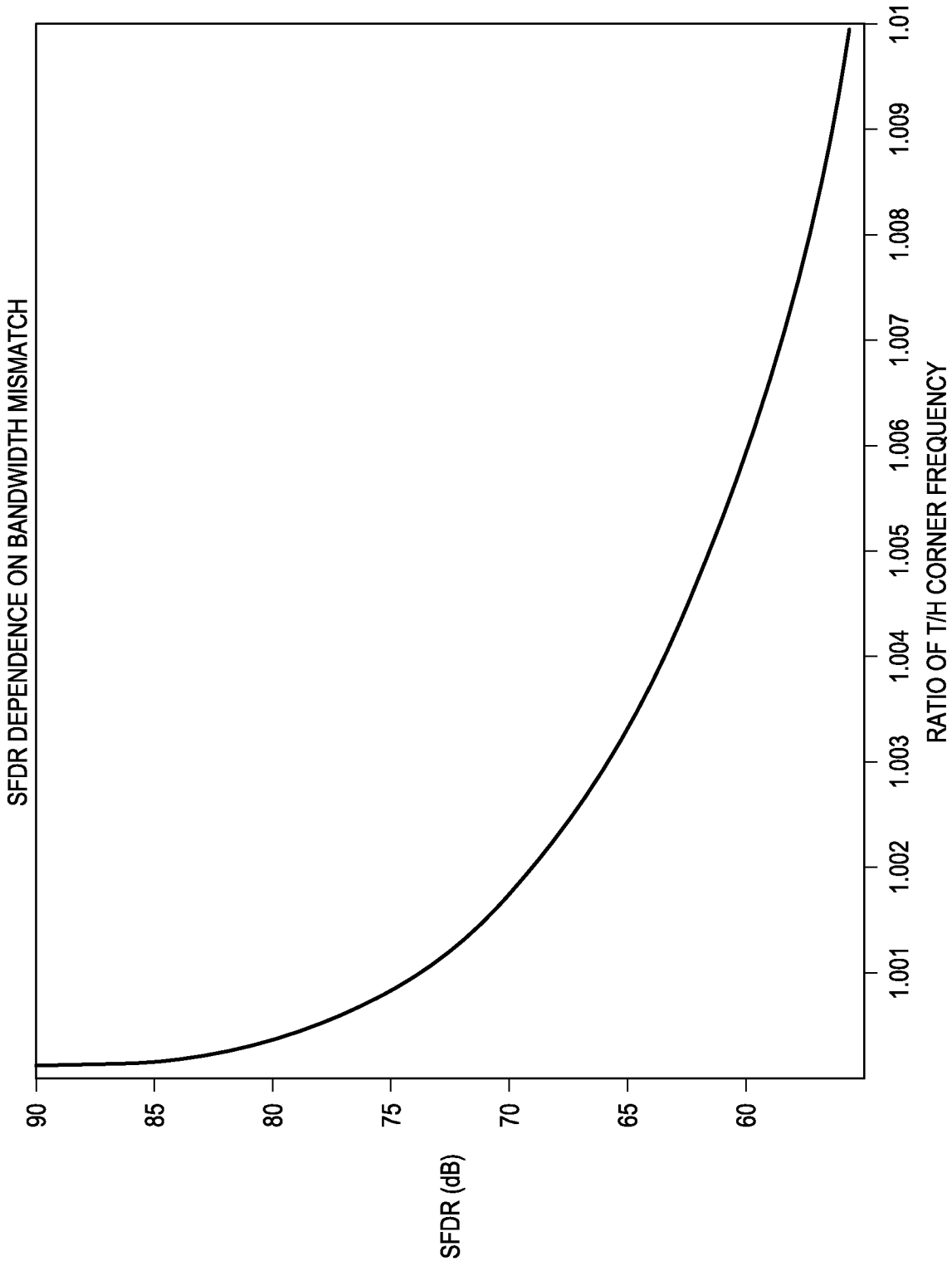


FIG. 3A
(PRIOR ART)

FIG. 3B


SFDR DEPENDENCE ON BANDWIDTH MISMATCH
SFDR (dB)
90
85
80
75
70
65
60
1.001
1.002
1.003
1.004
1.005
1.006
1.007
1.008
1.009
1.01
RATIO OF T/H CORNER FREQUENCY

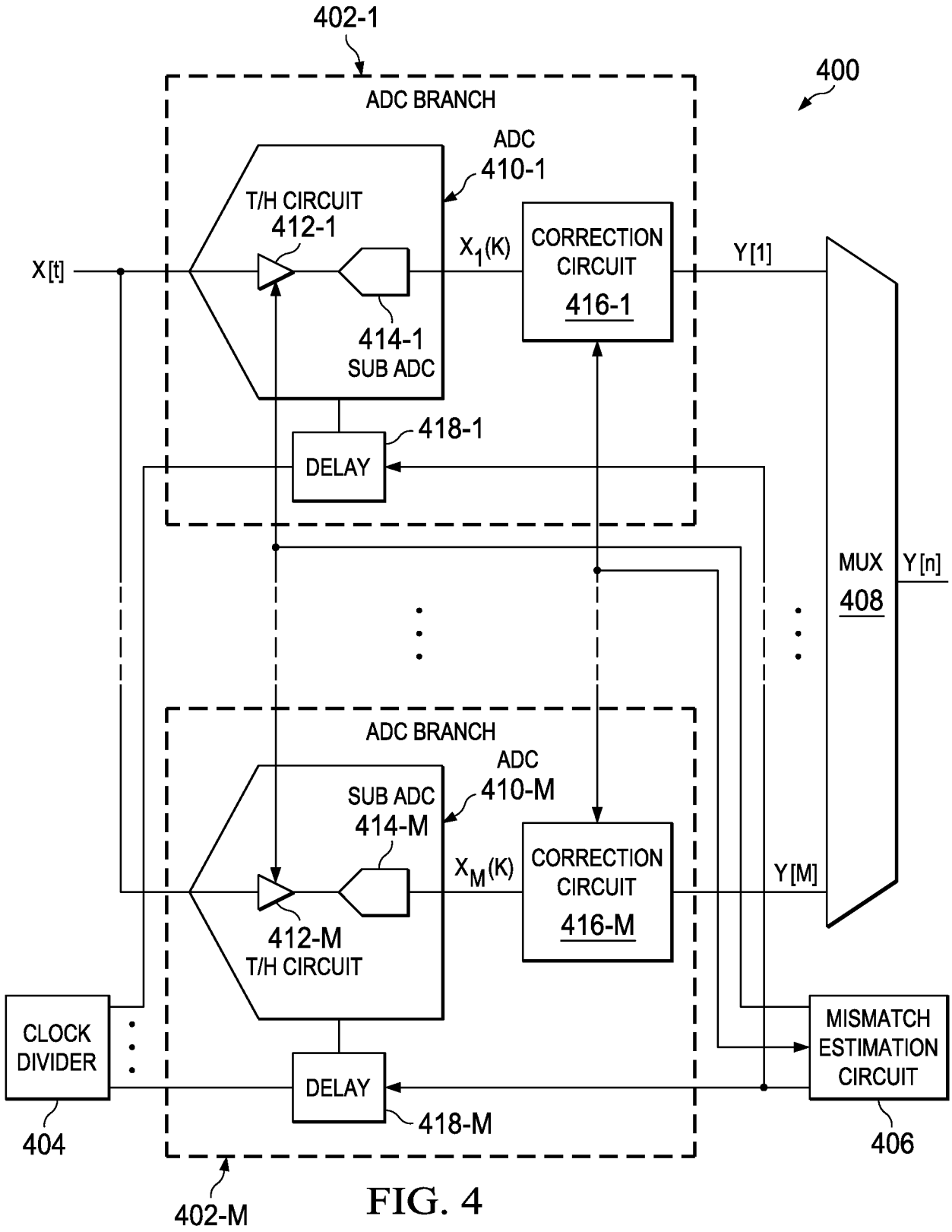
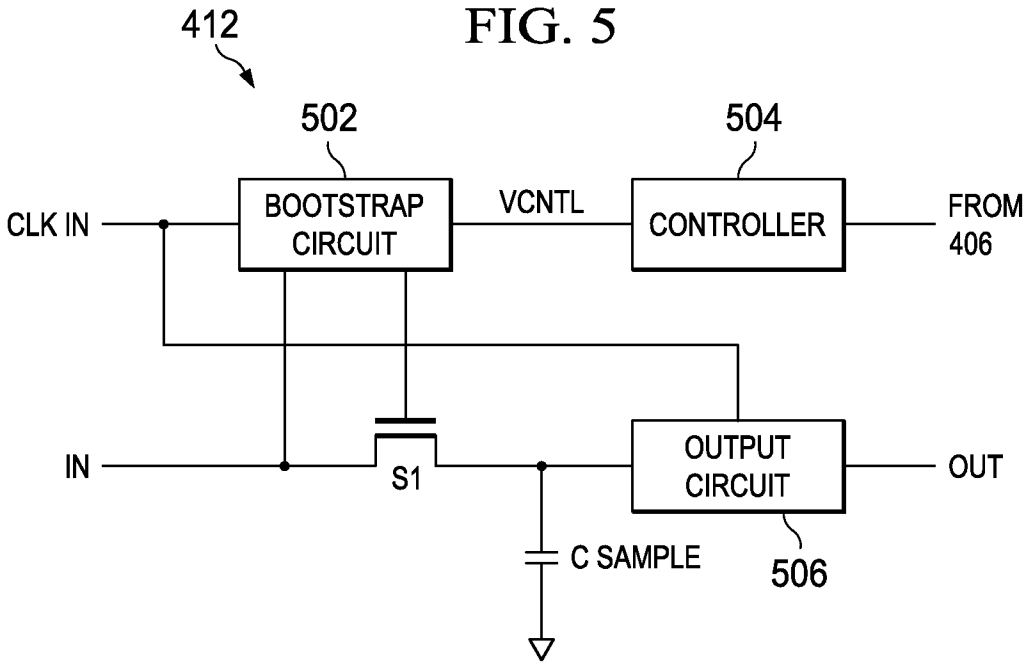

402-1
400
ADC BRANCH
ADC
410-1
T/H CIRCUIT
412-1
X[t]
$X_1(K)$
CORRECTION CIRCUIT
416-1
Y[1]
414-1
SUB ADC
418-1
DELAY
MUX
408
Y[n]
ADC BRANCH
ADC
410-M
SUB ADC
414-M
$X_M(K)$
CORRECTION CIRCUIT
416-M
Y[M]
412-M
T/H CIRCUIT
CLOCK DIVIDER
MISMATCH ESTIMATION CIRCUIT
DELAY
418-M
404
406
402-M

FIG. 4

FIG. 5


412
502
504
CLK IN
BOOTSTRAP CIRCUIT
VCNTL
CONTROLLER
FROM 406
IN
S1
OUTPUT CIRCUIT
OUT
C SAMPLE
506

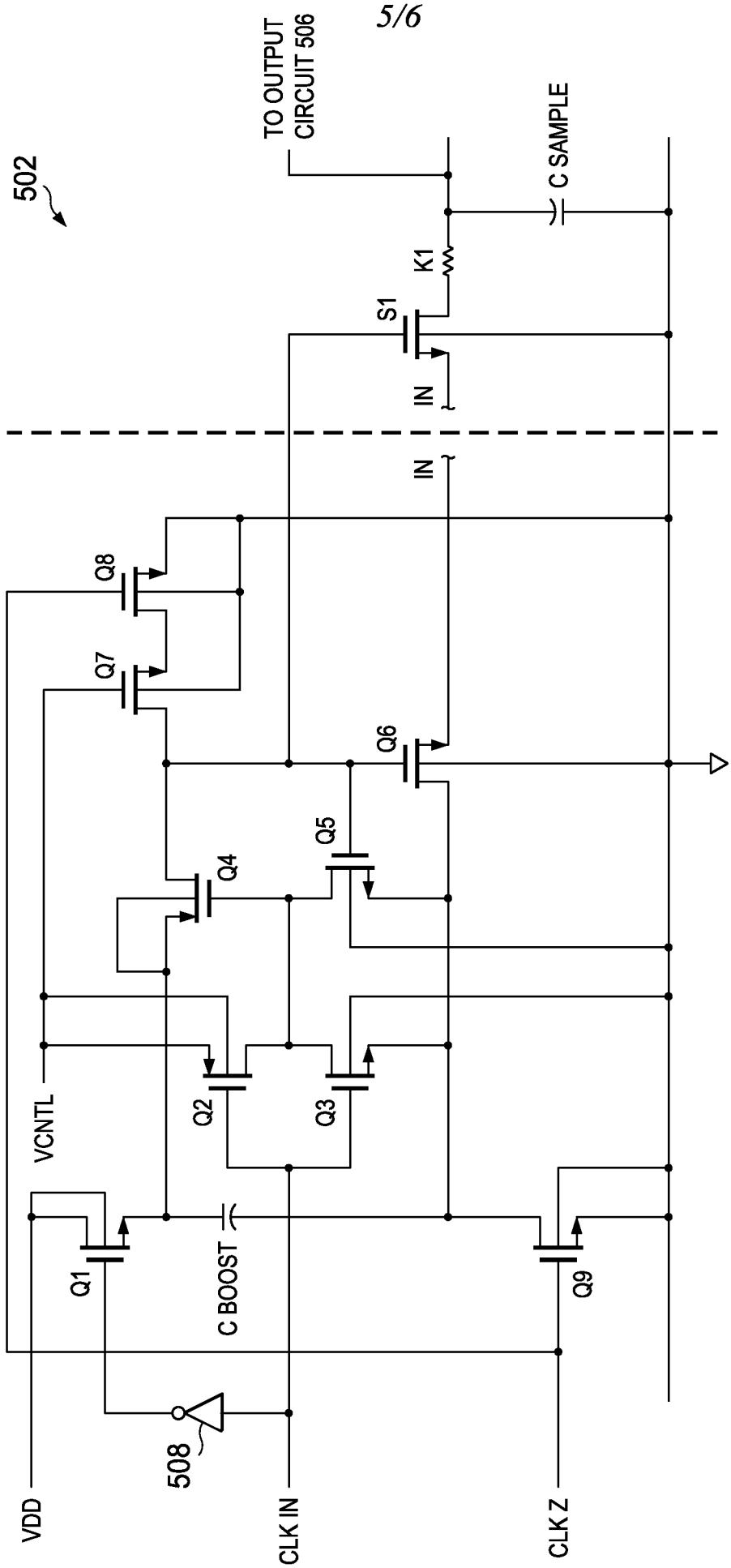
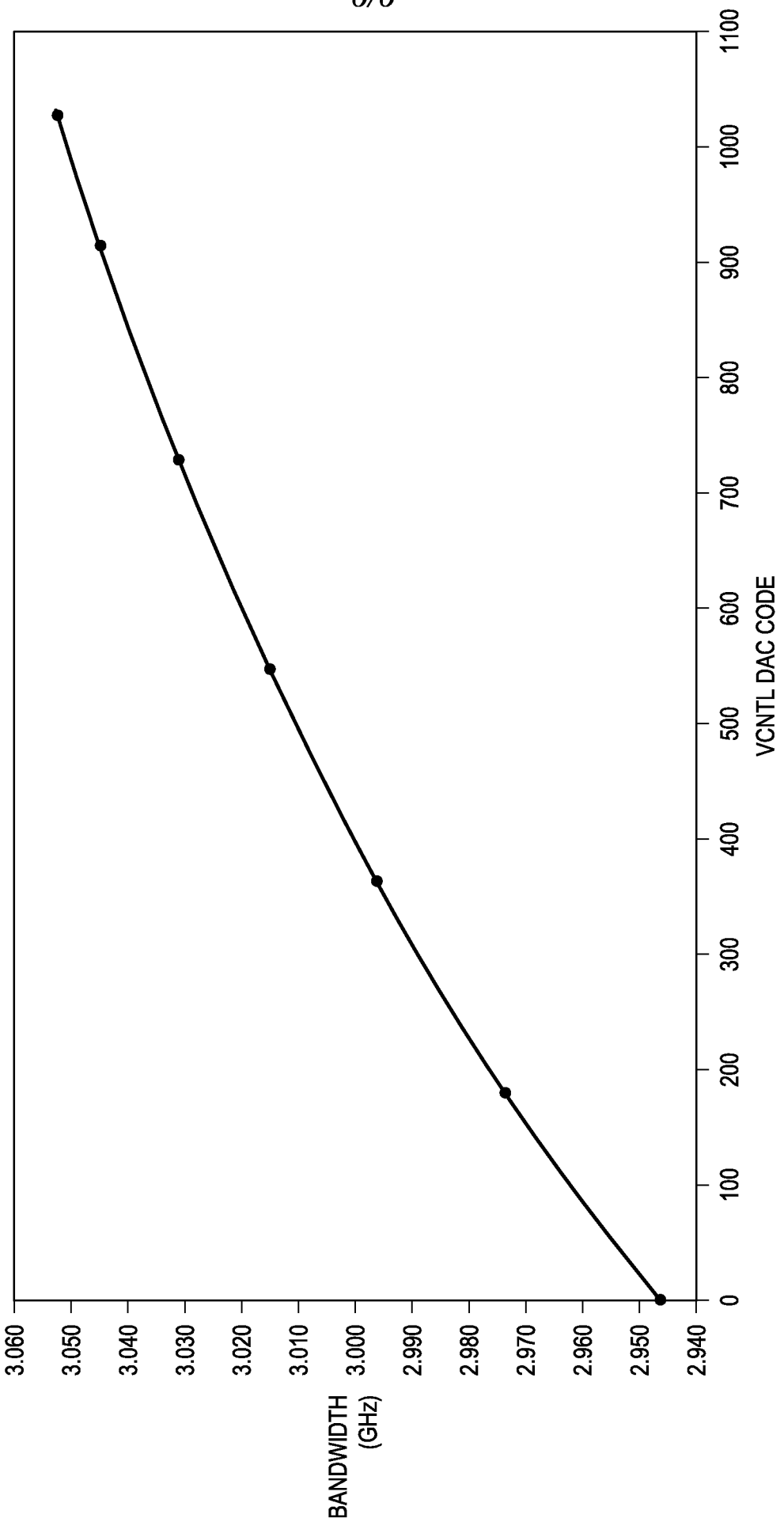

502
TO OUTPUT CIRCUIT 506
C SAMPLE
K1
S1
IN
IN
Q8
Q7
Q6
Q5
Q4
Q2
Q3
VCNTL
Q1
C BOOST
Q9
508
VDD
CLK IN
CLK Z

FIG. 6

FIG. 7


BANDWIDTH (GHz)
3.060
3.050
3.040
3.030
3.020
3.010
3.000
2.990
2.980
2.970
2.960
2.950
2.940
0
100
200
300
400
500
600
700
800
900
1000
1100
VCNTL DAC CODE