

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
2 March 2006 (02.03.2006)

PCT

(10) International Publication Number
WO 2006/023183 A3

(51) International Patent Classification:

H01L 29/06 (2006.01) **H01L 29/76** (2006.01)
H01L 29/12 (2006.01)

(21) International Application Number:

PCT/US2005/025535

(22) International Filing Date: 15 July 2005 (15.07.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

10/924,650 24 August 2004 (24.08.2004) US

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(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN,
CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI,
GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE,
KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA,
MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ,
OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL,
SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC,
VN, YU, ZA, ZM, ZW.

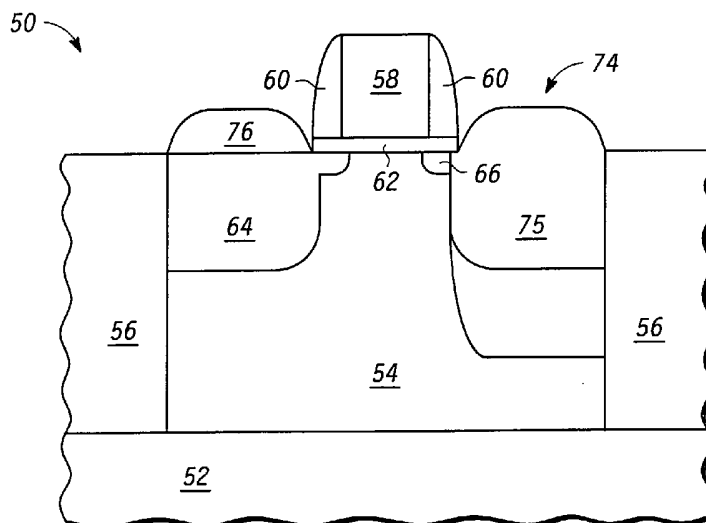
(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,
FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT,
RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA,
GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR PERFORMANCE ENHANCEMENT IN AN ASYMMETRICAL SEMICONDUCTOR DEVICE



(57) Abstract: A method and apparatus is presented that provides performance enhancement in a semiconductor device. In one embodiment, a first current region (64, 76, 23), a channel region and a second current region (75, 33, 66) are adjacent each other. The second current region (75, 33, 66) has a content of a first element of an alloy greater than a content of the first element in the first current region (64, 76, 23), wherein the second current region (75, 33, 66) has a content of the first element greater than a content of the first element in the channel region, the alloy further comprises a second element, the first element has a first valence number, and the second element has a second valence number. Furthermore, the sum of the first valence number and the second valence number is eight.

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— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(88) Date of publication of the international search report:

4 May 2006

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US05/25535

A. CLASSIFICATION OF SUBJECT MATTER

IPC: **H01L 29/06**(2006.01),**29/12**(2006.01),**29/76**(2006.01)

USPC: 257/19,69,412

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/19,69,412

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/0061191 (Paton et al.) 1 April 2004 (01.04.04), figs, 4a - 6; [0032]-[0034]	13-24

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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Date of the actual completion of the international search

09 March 2006 (09.03.2006)

Date of mailing of the international search report

17 MAR 2006

Name and mailing address of the ISA/US

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