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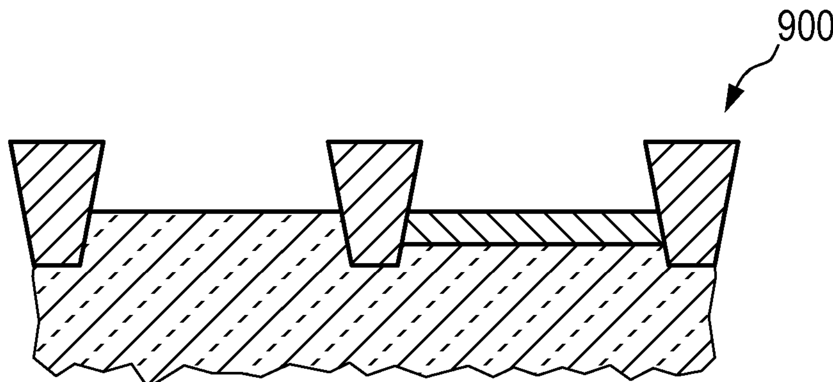
(54) Title: A METHOD FOR FABRICATING A DUAL-ORIENTATION GROUP-IV SEMICONDUCTOR SUBSTRATE



(57) Abstract: The present invention relates to method for fabricating a dual-orientation group-IV semiconductor substrate and comprises in addition to performing a masked amorphization on a DSB-like substrate only in first lateral regions of the surface layer, and a solid-phase epitaxial regrowth of the surface layer in only the first lateral regions so as to establish their (100)-orientation. Subsequently, a cover layer on the surface layer is fabricated, followed by fabricating isolation regions, which laterally separate (1 1θ)-oriented first lateral regions and (100)-oriented second lateral regions from each other. Then the cover layer is removed in a selective manner with respect to the isolation regions so as to uncover the surface layer in the first and second lateral regions and a refilling of the first and second lateral regions between the isolation regions is performed using epitaxy.

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A Method for Fabricating a Dual-Orientation Group-IV Semiconductor Substrate

5 FIELD OF THE INVENTION

The present invention relates to a method for fabricating a dual-orientation group-IV semiconductor substrate.

BACKGROUND OF THE INVENTION

10 Conventional (100)-oriented silicon or silicon-on-insulator (SOI) substrates are commonly used in the field of microelectronics. In comparison with other known surface orientations of silicon substrates, the (100)-orientation provides the highest mobility for electrons. However, the (100)-orientation is not advantageous for the hole mobility. In fact, within the group of surface orientations of commercially available for silicon wafers it 15 provides the poorest mobility. This is detrimental for the performance of pMOS (metal – oxide – p-semiconductor) devices on (100)-silicon.

It has been established that silicon substrates with a (110)-orientation provide the best mobility for holes. However, this orientation is detrimental for the electron mobility, i.e. for nMOS (metal – oxide – n-semiconductor) devices, cf. M.Yang et al., IEEE TED, Vol. 20 53, No. 5, May 2006, pp. 965 – 978.

As is well known, CMOS (complementary metal – oxide – semiconductor) devices incorporate both types, nMOS and pMOS devices, on a single substrate (chip). To achieve optimum mobility for majority charge carriers in both device types on a single chip, proposals have been made to provide dual-orientation substrates with first lateral surface 25 regions having a (100)-orientation for nMOS devices, and with second lateral surface regions having a (110)-orientation for pMOS devices.

US 2006/0276011 A1 describes methods for fabricating such dual-orientation substrates, which are also called hybrid orientation substrates. Methods known from this document are based on direct-silicon-bonded (DSB) substrates, which have a (110)-oriented 30 silicon surface layer bonded to a (100)-oriented silicon wafer. The fabrication of well-defined lateral regions with different crystal orientations is in some known methods performed by fabricating shallow trench isolations (STI) in a masked etching and filling process, followed by chemical mechanical polishing. Subsequently, a resist layer is deposited

and patterned to protect those lateral regions from a subsequent amorphization step, which are to retain their (110)-orientation in the finished substrate. The amorphization is then performed by implanting suitable ions such as silicon or germanium. Subsequently, a solid-phase-epitaxial regrowth is performed, using the (100)-oriented substrate as the template for
5 recrystallization of the amorphized lateral surface layer regions. With removal of the resist layer, the fabrication of a dual-orientation substrate is completed.

However, as is described in US 2006/0276011 A1, defects are created in this process, which are detrimental for device performance. Specifically, crystallographic defects are generated at the STI edge during the solid-phase epitaxy step. STI-edge defects are a
10 major source of junction leakages in a transistors with a wide active area since those defects are placed in junction depletion region. In case of a narrow active area, i.e., reduced STI-to-STI spacing, STI-edge defects are also a mobility degradation factor since the defects are placed in the transistor channel below the gate. Since those defects are a major source of junction leakages, some solutions have been proposed in US 2006/0276011 to reduce the
15 defect density. In particular, a high-temperature annealing step for defect reduction and an integration scheme that uses the solid-phase epitaxy before the STI formation are proposed. The latter concept is explained in the following with reference to Figs. 1 to 4.
Figs. 1 to 4 show schematic cross-sectional views of a dual-orientation silicon substrate during different stages of its fabrication.
20 Initially, a DSB silicon substrate 100 is provided. The DSB substrate has a (100)-oriented silicon substrate 102 and a (110)-oriented silicon surface layer 104 on top of the substrate 102. Note that, in the context of the present invention, numbers in round brackets indicate crystal orientations while numbers which are not bracketed are used as reference labels.
25 In a subsequent processing step, the result of which is shown in Fig. 2, a resist layer 106 is deposited on the surface layer 104 and lithographically patterned to provide openings in first lateral regions of the resist layer 106, which correspond to first lateral regions 108 of the surface layer, in which a (100)-oriented surface is desired. Then, an amorphizing ion implant 110 indicated by arrows pointing towards the substrate 100 is
30 performed. Due to the resist pattern 106 provided in previous processing, the amorphization is performed only in the first lateral region 108, the ion implant 110 thus leads to an amorphized silicon layer 112. The amorphized silicon layer 112 extends slightly deeper into the substrate than the surface layer 104. Therefore, the amorphized layer 112 is arranged on

top of a (100)-oriented substrate region of the substrate 102. The amorphized layer 112 is then recrystallized by a recrystallization anneal in order to establish a (100)-orientation of the substrate 100 in the first lateral region 108. As shown in Fig. 3, the resist layer 106 has also been removed at this processing stage, revealing second lateral regions 114 of the surface layer 106 with (110)-orientation.

As is shown in Fig. 3, a lateral defect region 116 is generated in the course of the amorphization and recrystallization process. The lateral extension l of the lateral defect region 116 roughly corresponds to the thickness d of the originally deposited surface layer 104.

In subsequent processing, STI regions 118 are fabricated in the lateral defect regions 116. In further processing steps, end-of-range defects (not shown) at the former interface between amorphized layer 112 and the substrate 102 are removed by a high-temperature defect-removal anneal.

The processing of US 2006/0276011 A1 has the disadvantage of not being applicable in future CMOS technology nodes with advanced scaling. Moreover, it is not fully compatible with the integration of thin-film devices. Also, the processing scheme is vulnerable to short-channel effects.

Figs. 5 and 6 show schematic cross-sectional views of different CMOS semiconductor devices 500 and 600. The figures are used to illustrate main causes of junction leakages in semiconductor devices integrated on DSB substrates. In both devices, an nMOSFET 502 and 602, respectively, and a pMOSFET 504 and 604, respectively, are shown. The devices are provided on a dual-orientation substrate 506 and 606, respectively. The two devices 500 and 600 differ in the depth extension d of the (110)-oriented surface layer 508 and 608, respectively. The (110)-oriented surface layer 508 has a depth extension d that reaches deeper than source and drain regions 512 and 514 of the pMOS transistor 504. In the case of the semiconductor device 600, the (110)-oriented surface layer 608 has a smaller depth extension than the source and drain regions 612 and 614 of the pMOS transistor 604. The larger depth extension of the surface layer 508 avoids junction leakages in the pMOS transistor 504 of the semiconductor device 500. However, defect regions 516 and 518 are present in the nMOS transistor 502. The defect regions 516 and 518 extend along sidewalls of STI regions 520 and 522, which define the (100)-oriented, recrystallized first lateral surface region of the dual-orientation substrate 506. These defect regions 516 and 518 form a

source of leakages as they extend into source and drain regions 524 and 526 of the nMOS transistor 502.

Therefore, defect problems are present in CMOS semiconductor devices on dual-orientation substrates, with different leakage problems being present in semiconductor devices with surface layers of different thickness.

Thus, one of the main challenges is to provide a dual-orientation substrate which avoids leakage problems in semiconductor devices such as transistors and which can be fabricated also at advanced scaling of the width of the isolation regions and the spacing between isolation regions on opposite lateral sides of an active area.

SUMMARY OF THE INVENTION

According to the present invention, a method for fabricating a dual-orientation group-IV semiconductor substrate is provided. The method comprises the steps:

- providing a substrate with a (100)-oriented group-IV semiconductor substrate and a (110)-oriented group-IV semiconductor surface layer on the substrate;
- performing a masked amorphization only in first lateral regions of the surface layer, in which first lateral regions a (100)-oriented surface is desired;
- performing a solid-phase epitaxial regrowth of the surface layer in only the first lateral regions so as to establish their (100)-orientation;
- fabricating a cover layer on the surface layer;
- fabricating isolation regions, which extend from the surface of the cover layer towards the inner substrate at least to the surface layer and which laterally separate (110)-oriented first lateral regions and (100)-oriented second lateral regions from each other;
- removing the cover layer in a selective manner with respect to the isolation regions so as to uncover the surface layer in the first and second lateral regions,
- refilling the first and second lateral regions between the isolation regions by performing an epitaxy of group-IV semiconductor material.

The method of the present invention provides an innovative way to integrate dual-orientation devices while limiting junction leakages. The method of the present invention has the further advantage that it can be used in embodiments to realize thin-film devices with dual orientation.

The method is suitable for silicon or silicon-germanium semiconductor substrates with or without carbon doping. Of course, other dopants for achieving a desired conductivity type can be present.

The method is based on providing a substrate with a (100)-oriented group-IV
5 semiconductor substrate and a (110)-oriented group-IV semiconductor surface layer on the substrate. The group-IV semiconductor substrate is typically a wafer, such a silicon wafer, used in the industry to fabricate semiconductor devices. The surface layer can be fabricated by any known method including known methods of direct silicon bonding.

The method of the present invention includes the use of a cover layer on a pre-
10 processed substrate with dual orientation. In contrast to the method known from US 2006/0276011 A1, the isolation regions are fabricated starting with a substrate that has the cover layer on top. After fabricating the isolation regions, the remaining cover layer sections are removed. Subsequently, an epitaxy, i.e., an epitaxial deposition of group-IV semiconductor material is performed using the dual-orientation lateral regions fabricated
15 earlier underneath the cover layer as templates for the epitaxial growth.

The method is suitable for silicon and related substrates. Alternative materials such as silicon-germanium semiconductor substrates with or without carbon doping can also be used. Of course, dopants for achieving a desired conductivity type may be present.

Note that the term “lateral region” is used here to identify a localized substrate
20 region that has a well-defined extension in lateral directions. Lateral directions are directions, which are parallel to a reference surface. Note also that even though a lateral region has an extension in lateral directions, it need not necessarily be oriented parallel to the reference surface. Regarding the term “reference surface”, consider as an exemplary and typical embodiment a wafer for use in the semiconductor industry. Here, the reference surface is the
25 main wafer surface, which is used for the fabrication of functional layers of semiconductor devices such as transistors. Of course, a lateral region typically also has a defined extension in a depth direction, which points from the reference surface towards the inner substrate in a direction perpendicular to the reference surface. However, the use of the term “lateral region” as such shall not imply any restriction regarding the depth extension of the lateral region.

30 In the following, embodiments of the method of the invention will be described. The additional features of the various embodiments can be combined with each other to form further embodiments of the method of the invention unless different embodiments are described as forming alternatives to each other.

In one embodiment, the (110)-oriented surface layer has a thickness between 30 and 120 nm. Generally, the lateral extension of a defect zone created during the solid-phase epitaxial regrowth of the surface layer in the first lateral regions is limited by the thickness of the surface layer. Using a thickness of 50 nm in another embodiment will, therefore, generate a defect area with a lateral extension of 50 nm in the worst case, which implies full compatibility with the parameter "N_{active}/P_{active} spacing", indicative of the lateral spacing between the active regions for n- and p-devices, at advanced scaling levels reaching down to the 22 nm CMOS technological node.

The fabrication of the cover layer on the surface layer is preferably performed by depositing a silicon nitride layer. The cover layer is typically deposited on the whole wafer. Using silicon nitride Si_3N_4 has the advantage that well-known removal techniques can be used to free the active areas from the cover layer before the epitaxy. For instance, H_3PO_4 wet chemistry can be used for selective removal of Si_3N_4 without attacking conventional STI-like isolation regions made of SiO_2. However, plasma dry etching techniques can also be used for a selective and isotropical etch.

Regarding the fabrication of isolation regions, different embodiments can be used. Beside the conventional STI concept that implies fabricating trenches in the cover layer and filling the trenches with an isolating material, such as SiO_2, an alternative concept can be used as follows: The fabrication of the cover layer is performed by depositing a suitable isolating material that is in later steps also used for the isolation regions. Again, a suitable material is Si_3N_4. The fabrication of the isolation regions then comprises removing the cover layer in the first and second lateral regions while protecting the cover layer from removal in the desired isolation regions. This can, for instance, be achieved by suitably masking the cover layer and selectively etching the cover layer only in unmasked lateral regions, which correspond to the first and second lateral regions of the surface layer.

In the STI processing alternative, the shallow trenches are preferably fabricated with an extension toward the inner substrate, which reaches beyond an interface between the (100)-oriented substrate and the (110)-oriented surface layer.The refilling of the first and second lateral regions is performed to obtain a flat active area on the substrate surface. There are different processing alternatives to achieve this. One is a selective faceting epitaxy. With this technique, a "rounded" active area is obtained at the end. In this case, an additional planarization step by chemical mechanical polishing (CMP) for instance is therefore needed to re-obtain a flat surface of the active area.

In a preferred alternative processing embodiment, refilling the first and second lateral regions between the isolation regions comprises performing a selective facet-free epitaxy of the group-IV semiconductor material. If the epitaxial growth is performed in a facet free manner, a flat active surface is naturally obtained. Facet-free epitaxy is a technique that is well-known in the art. Selective facet-free epitaxy refers to selective facet-free epitaxial growth only on the group-IV semiconductor material template regions, and not on isolation material, including the isolation region.

Removing the cover layer in a selective manner with respect to the isolation regions and refilling the first and second lateral regions between the isolation regions is in one embodiment performed in the first and second lateral regions at the same time.

However, if desired, these steps can be performed separately for the first and second lateral regions. For instance, these steps are performed at first in the first lateral regions only, and subsequently in the second lateral regions, or vice versa. Suitably, complementary respective masks are used to protect the respective lateral region, which is not being processed.

As mentioned earlier, the method of the present invention is suitable for the fabrication of thin-film devices. To this end, refilling the first and second lateral regions after removal of the cover layer comprises depositing a hetero-stack with a sequence of layers of group-IV-semiconductor material with different material compositions. For instance, a Si/SiGe hetero-stack can be fabricated this way, having a (100)-orientation in the first lateral regions and a (110)-orientation in the second lateral regions.

Embodiments of the method of the invention are also described in the claims.

In the following, further embodiments will be described with reference to the figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other aspects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter. In the following drawings:

Figs. 1 to 4 show schematic cross-sectional views of a dual-orientation substrate during different stages of its fabrication according to a prior-art method;

Fig. 5 and 6 show schematic cross-sectional views of thin prior-art semiconductor devices for illustrating sources of junction leakage in devices with different thicknesses of the surface layer of the dual-orientation substrate;

Figs. 7 to 12 show schematic cross-sectional views of a dual-orientation substrate during different fabrication stages according to an embodiment of the method of the invention;

Figs. 13 and 14 show schematic cross-sectional views of a dual-orientation substrate during two processing stages according to a second embodiment of the invention;

Figs. 15 and 16 show schematic cross-sectional views of a dual-orientation substrate during two processing stages according to a third embodiment of the invention;

DETAILED DESCRIPTION OF EMBODIMENTS

Figs. 7 to 12 show schematic cross-sectional views of a dual-orientation substrate during different fabrication stages according to an embodiment of the method of the invention. The dual-orientation substrate 700 is fabricated starting from a DSB substrate 702 with a (100)-oriented substrate 704 and a (110)-oriented silicon surface layer 706 of approximately 50 nm thickness. As was explained before, the thickness of 50 nm is particularly suitable for advanced CMOS technology nodes. However, different thicknesses may equally be used for other technology nodes.

In a subsequent processing step, the result of which is shown in Fig. 8, the surface layer is covered by a resist layer 708, which is patterned to provide openings in the first lateral regions 710. Subsequently, an ion implant indicated by arrows 712 is performed, using amorphizing ions such as silicon Si, germanium (Ge), argon (Ar) or xenon (Xe) ions, or a suitable combination of these. The ion implant 712 is performed at conditions leading to an amorphization of the surface layer 706 in the first lateral regions 710. The resulting amorphized regions 714 extend slightly deeper into the substrate than the interface between the surface layer 706 and the (100)-oriented underlying substrate 704. End-of-Range defects (not shown here) created in the underlying substrate 704 during the ion implant step 712, can be removed during an STI densification anneal. This way, the high-temperature anneal can be included in the thermal budget of the STI densification anneal.

In a subsequent step of solid phase epitaxy, the amorphized regions 714 are recrystallized. Due to the underlying template of the substrate 704 for recrystallization, the

amorphized regions take on the (100)-orientation. In this step, defects are also formed in the interface regions 716 between the generated first lateral regions 710 with (100)-orientation and the remaining second lateral regions 718 with (110)-orientation of the surface layer 706. Furthermore, as can be seen in Fig. 9, a cover layer 720 of Si_3N_4 is fabricated. It fully covers
5 the substrate after the resist stripping and the recrystallization. The thickness of the cover layer 720 should be selected suitably to accommodate a substantial part of the depth extension of isolation regions 722, which are formed during subsequent processing, cf. Fig. 10. As can be seen, the depth extension of the isolation regions 722 is slightly larger than that of the surface layer 706. That means that the isolation regions 722 extend into the (100)-
10 oriented substrate 704. The thickness of the cover layer 720 furthermore depends on the desired thickness of the (110)-oriented second surface regions 718 in the finalized dual-orientation substrate. The STI regions 722 laterally cover the defect regions 716, thus removing the defect problems at the interface between the (100)-oriented first substrate regions 710 and the (110)-oriented second substrate regions 718.
15 In the present embodiment, the isolation regions 722 are fabricated by known shallow-trench-isolation techniques, leading to a typical trapezoidal shape. The STI isolation regions 722 are fabricated by first etching trenches, using an etching agent that attacks Si_3N_4 and silicon, in a masked etching step. Subsequently, the trenches are filled with a suitable isolating material. An example is silicon dioxide. However, other materials can be used as
20 well, provided that they withstand a subsequent etching step in which the cover layer 720 is completely removed. The result of this etching step is shown in Fig. 11. The etching is performed selectively, i.e. the isolation regions 722 and the underlying silicon in the first and second lateral regions 710 and 718 is not attacked.

After the cover layer has been removed, the first and second lateral regions
25 710 and 718 are filled in a selective facet-free epitaxy step in which silicon is deposited. Known facet-free epitaxial techniques employ chemical vapor deposition (CVD). Due to the different crystalline structures provided as templates in the first and second lateral regions, the epitaxial filling follows the given templates, resulting in a dual-orientation substrate surface after the epitaxy step.
30 Note that the present embodiment allows a fabrication of the (110)-oriented layer to any desired thickness, which is required by a particular device application.

The minimum lateral isolation STI width, as it is observed in a planar top view of the substrate, corresponds to the distance between the N-active and P-active regions and is

given by the respective technology node employed. This spacing between the first and second lateral regions, which in the art is also referred to as the N_{active}/P_{active} spacing, can be scaled to a desired level according to a technology node to be employed by adapting the thickness of the cover layer 720. For instance, the minimum STI width is roughly equal to 100nm in the 45nm node (node n), and will be around 50nm for the 22nm node (node n+2). The STI scaling rule of thumb is for node (n+1), width (node n+1) = 0.7 * width (node n). In order to fulfill those requirements imposed by the technological node, two levers are provided by the present invention: either adapting the thickness of the initial bonded (110)-top layer 706, or adapting the thickness of the sacrificical cover layer 720.

The described technique allows preventing junction leakages at the interface between the (110)-oriented surface layer 706 and the underlying substrate 704 also at high levels of scaling.

A modification of this embodiment can be performed at the procesing stage of Fig.10. In this modification the selective epitaxy is performed separately in the first and second lateral regions 710 and 718, i.e., the nMOS area and pMOS areas of the dual-orientation substrate.

To this end, a masking step is inserted between the processing stages of Fig.10 and Fig.11 in order to realize the following sequence:

a) masking of either pMOS area 718 or nMOS area 710. This step is performed by conventional lithographic techniques;

b) selective removal of the Si_3N_4 cover layer in the non-masked, i.e., just opened area;

c) selective facet-free epitaxy growth in the opened area;

d) mask removal.

e) complementary masking step in order to mask the recently regrown area;

f) Si_3N_4 selective removal in the still non regrown opened area;

g) selective facet-free epitaxy growth in the area just opened; and

h) mask removal.

Figs. 13 and 14 show schematic cross-sectional views of a dual-orientation substrate 800 during two processing stages according to a second embodiment of the invention.

The method of the present embodiment employs an identical processing as the embodiment described with reference to Figs. 7 to 12 up to the deposition of the cover layer 720. Then, instead of fabricating trenches for STI region 722, the cover layer 720 is patterned

to fabricate isolation regions 822 from cover layer material. This can be performed by a masked anisotropical etching step using, for instance, a remote plasma of CF_4 and SF_6, in order to selectively free the first and second lateral regions 810 and 818 from the cover layer material. Subsequently, as shown in Fig. 14, the first and second lateral regions are rebuilt by a facet-free CVD epitaxy step, leading to a flat dual-orientation surface, as described for the previous embodiment with reference to Fig. 12.

Another modification of the embodiment of Figs. 7 to 12 is shown with reference to Figs. 15 and 16. Figs. 15 and 16 show schematic cross-sectional views of a dual-orientation substrate 900 during two processing stages according to a third embodiment of the invention. In this embodiment, the processing stage of Fig. 11, which is shown in Fig. 15, is followed by a facet-free epitaxial deposition of a layer sequence of different materials. In the present embodiment, a first layer 910.1 of silicon is deposited in the first lateral region 910, and at the same time with (110)-orientation in the second lateral region 918 as layer 918.1. Subsequently, SiGe with a desired composition is deposited as (100)-oriented SiGe-layer 910.2 in the first lateral region 910, and as (110)-oriented SiGe-layer 918.2 in the second lateral region 918. Finally, a silicon layer is deposited to finalize the epitaxial step, providing a (100)-oriented silicon layer 910.3 in the first lateral region 910 and a (110)-oriented silicon layer 918.3 in the second lateral region 918.

As explained in the previous sections of the present specification, the invention can be used for device integration with a dual-orientation substrate in order to provide a maximum mobility for both, electrons and holes. In addition, this invention is fully compatible with the so-called silicon-on-nothing (SON) technology for thin-film device integration as shown in the embodiment of Figs. 15 and 16.

In a SON process, a layer sequence as that of Fig. 16 can be used to laterally remove the SiGe-layers 910.2 and 918.2 selectively without attacking the surrounding silicon layers 910.1 and 910.3, and 918.1, 918.3, respectively. An air tunnel is thus formed, which isolates the upper silicon layers 910.3, 918.3 from the substrate. Despite the air tunnel, a gate stack fabricated on top will not collapse because it bridges the active area and is supported at both ends. However, the air tunnel can also be filled with an alternative dielectric material.

While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive; the invention is not limited to the disclosed embodiments.

Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure, and the appended claims.

In the claims, the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measured cannot be used to advantage.

Any reference signs in the claims should not be construed as limiting the scope. In order to clearly differentiate between reference signs and the common type of notation crystal for orientations using parentheses in the claims, reference signs are provided within braces {}.

CLAIMS:

1. A method for fabricating a dual-orientation group-IV semiconductor substrate {700}, comprising the steps:

- providing a (100)-oriented group-IV semiconductor substrate{702} and a (110)-oriented group-IV semiconductor surface layer{704} on the substrate;
5 - performing a masked amorphization{712, 714} only in first lateral regions{710} of the surface layer, in which first lateral regions a (100)-oriented surface is desired;
- performing a solid-phase epitaxial regrowth of the surface layer{706} in only the first lateral regions{712} so as to establish their (100)-orientation;
10 - fabricating a cover layer{720} on the surface layer {706};
- fabricating isolation regions {722; 822}, which extend from the surface of the cover layer{720} towards the inner substrate at least to the surface layer{706} and which laterally separate (100)-oriented first lateral regions {710} and (110)-oriented second lateral regions{718} from each other;
15 - removing the cover layer in a selective manner with respect to the isolation regions{722} so as to uncover the surface layer{706} in the first and second lateral regions,
- refilling the first and second lateral regions{710, 718} between the isolation regions{722} by performing an epitaxy of group-IV semiconductor material.

20 2. The method of claim 1, wherein a direct-silicon-bonded substrate {702, 706} is provided for performing the masked amorphization.

3. The method of claim 1, wherein the (110)-oriented surface layer{706} has thickness of between 30 and 120 nm.

25

4. The method of claim 1, wherein performing the masked amorphization comprises an ion-implantation {712} step.

5. The method of claim 1, wherein fabricating the cover layer{720} comprises depositing a silicon nitride layer on the surface layer.

6. The method of claim 1, wherein fabricating isolation regions{722} comprises
5 fabricating trenches in the cover layer{720} and filling the trenches with an isolating material.

7. The method of claim 6, wherein fabricating isolation regions{722} comprises fabricating the trenches with an extension towards the inner substrate that reaches beyond an
10 interface between the substrate{702} and the surface layer {706}.

8. The method of claim 1, wherein removing the cover layer {720} in a selective manner with respect to the isolation regions and refilling the first and second lateral regions between the isolation regions {722} is performed in the first and second lateral regions at the
15 same time.

9. The method of claim 1, wherein removing the cover layer {720} in a selective manner with respect to the isolation regions and refilling the first and second lateral regions between the isolation regions is performed separately, that is first in the first lateral regions
20 and subsequently in the second lateral regions, and wherein complementary respective masks are used to protect the respective lateral region, which is not being processed.

10. The method of claim 1, wherein fabricating the cover layer comprises depositing an isolating material and the surface layer, and wherein fabricating isolation
25 regions comprises removing the cover layer {720} in the first {810} and second {818} lateral regions, and protecting the cover layer from removal in the desired isolation regions {822}.

11. The method of claim 1, wherein refilling the first and second lateral regions between the isolation regions comprises performing a selective facet-free epitaxy of the
30 group-IV semiconductor material.

12. The method of claim 1, wherein refilling the first {910} and second {918} lateral regions comprises depositing a hetero-stack {910.1 to 3; 918.1 to 3} with a sequence of layers of group-IV-semiconductor material with different material compositions.

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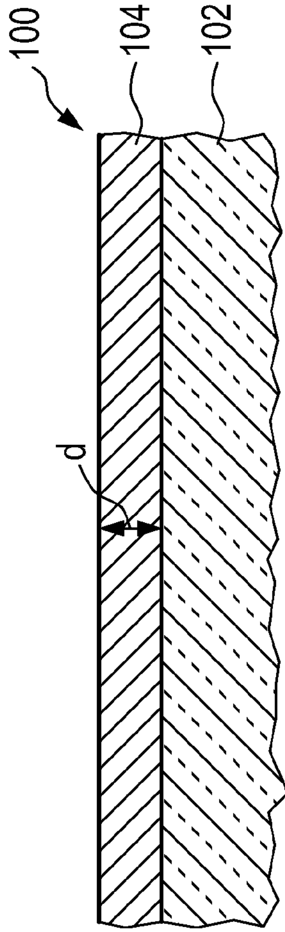

FIG 1
(PRIOR ART)

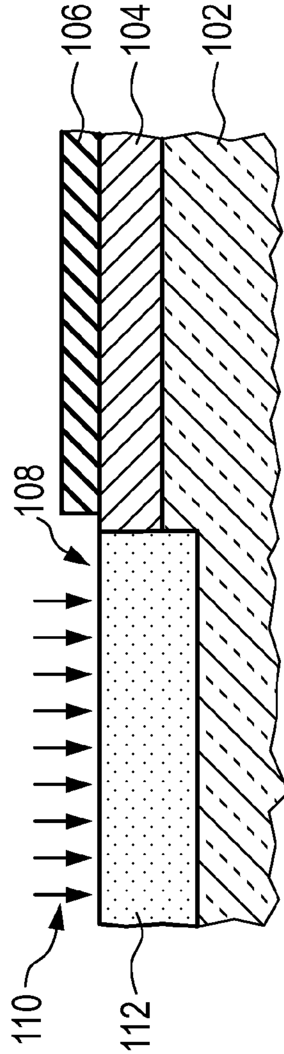

FIG 2
(PRIOR ART)

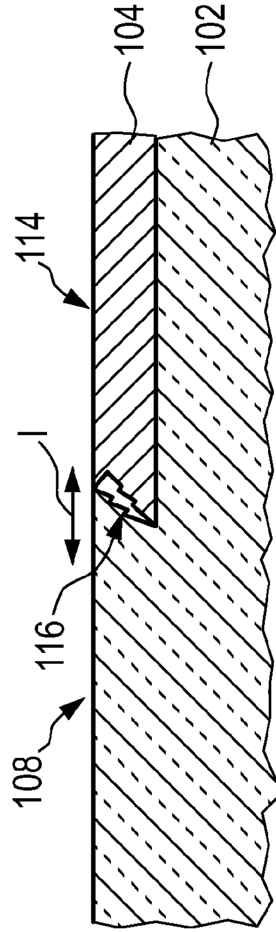

FIG 3
(PRIOR ART)

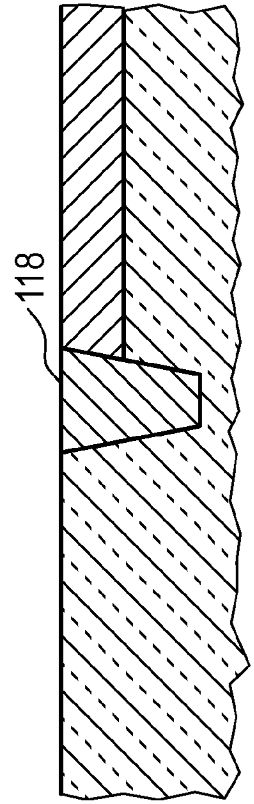

FIG 4
(PRIOR ART)

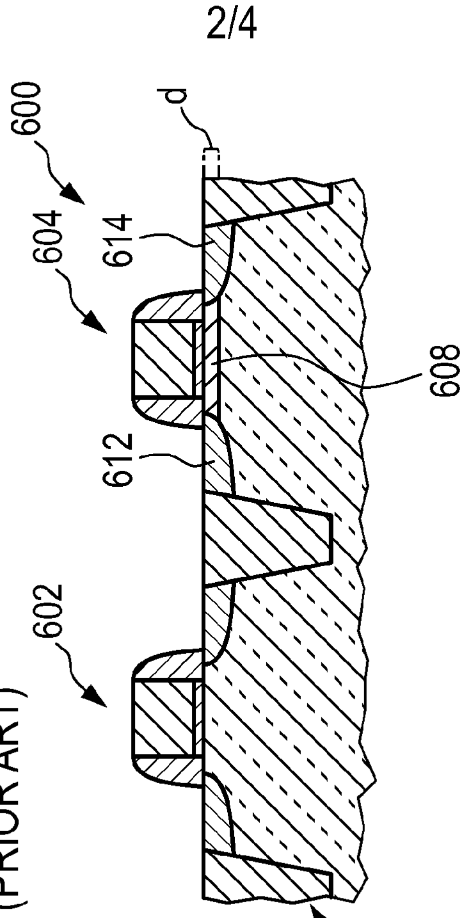

FIG 6
(PRIOR ART)

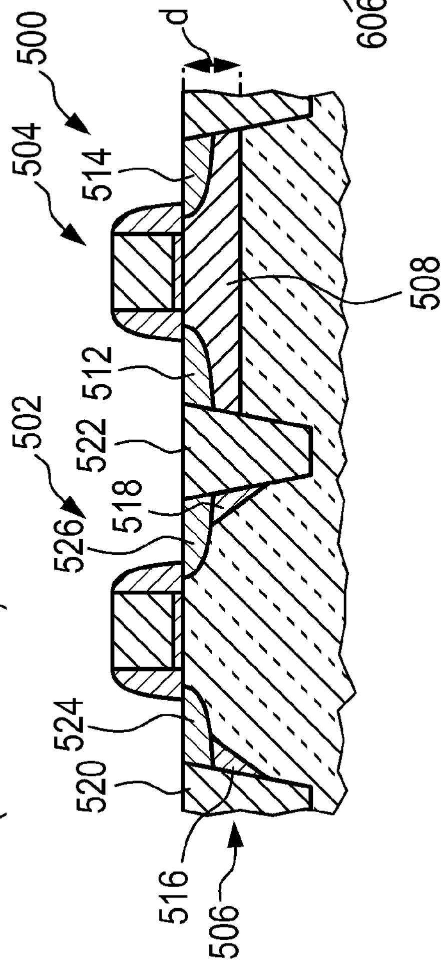

FIG 5
(PRIOR ART)

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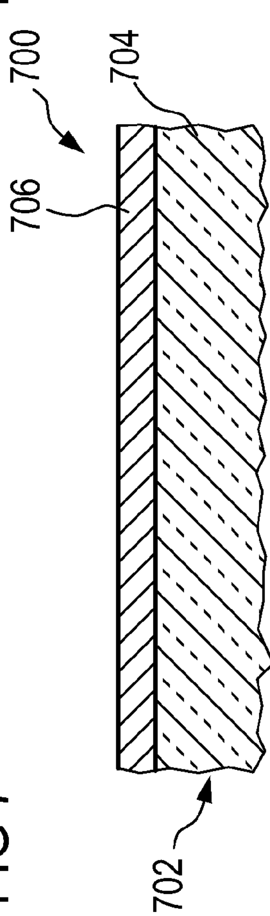

FIG 7

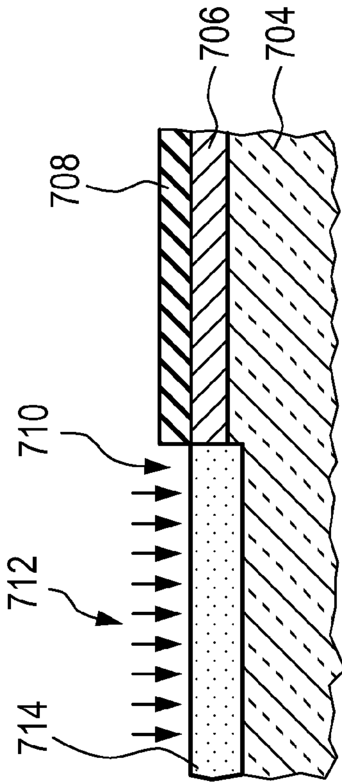

FIG 8

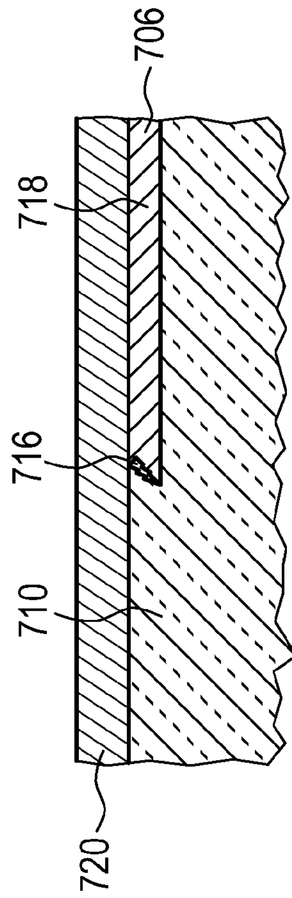

FIG 9

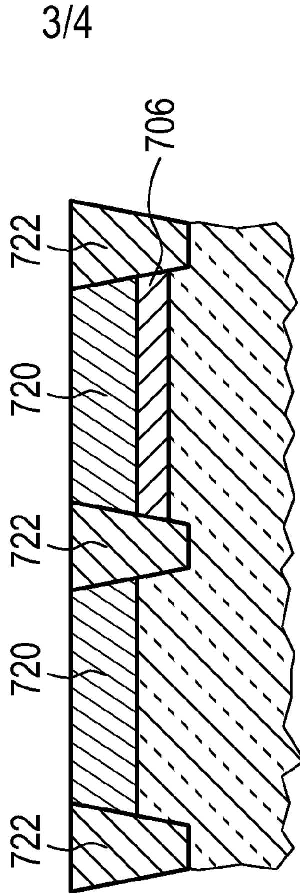

FIG 10

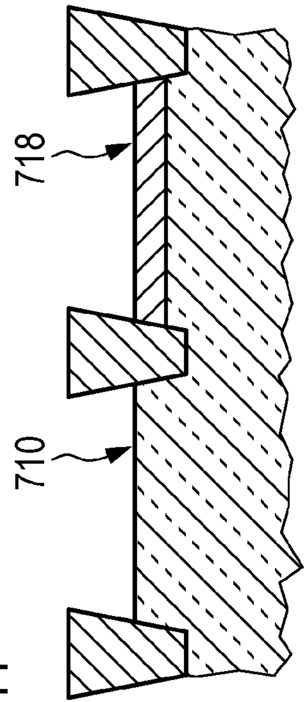

FIG 11

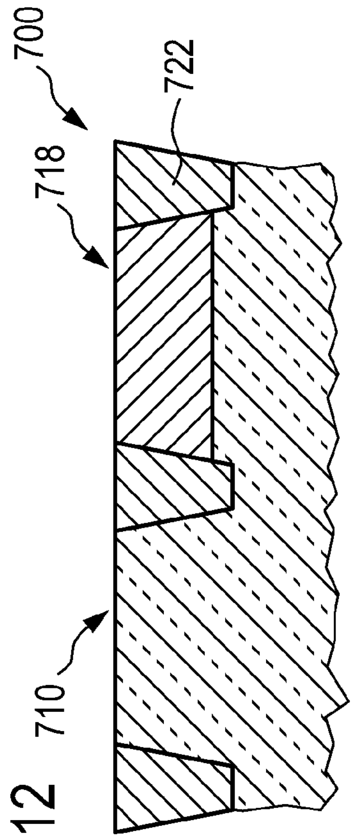

FIG 12

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(NoA ID 81344360)

FIG 13

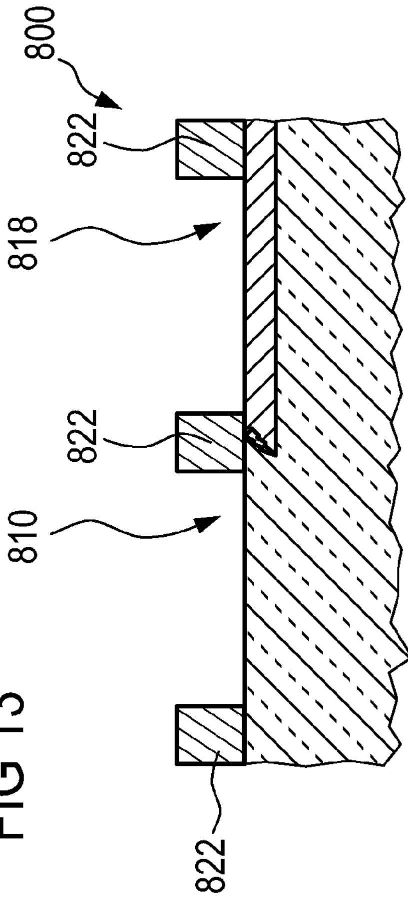


FIG 14

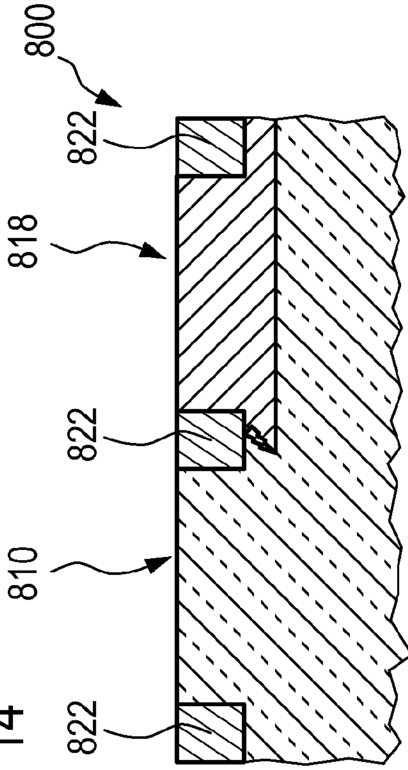


FIG 15

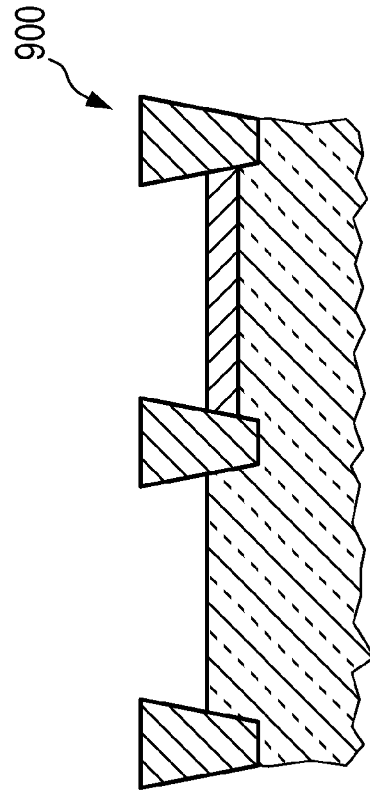
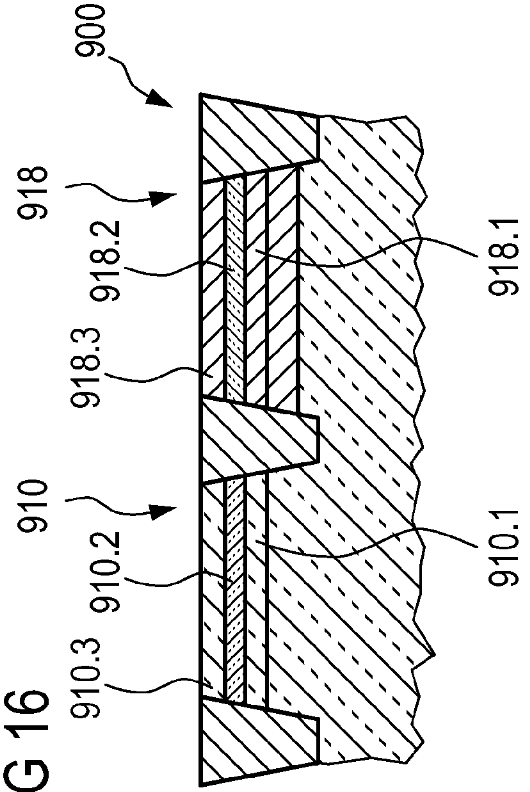


FIG 16



INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/050199

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/8238 H01L21/8234

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	WO 2006/130360 A (IBM [US]; FOGEL KEITH E [US]; SAENGER KATHERINE L [US]; SUNG CHUN-YUNG) 7 December 2006 (2006-12-07) abstract; claims; figures 7J,7K paragraph [0039]	1-12
A	US 7 060 585 B1 (COHEN GUY MOSHE [US] ET AL) 13 June 2006 (2006-06-13) abstract; claims; figures column 9, line 16 - line 45	1-12
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[X] Further documents are listed in the continuation of Box C [X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
7 April 2009	04/05/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Wirner, Christoph

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/050199

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 2007/090467 A1 (ZHU HUILONG [US]) 26 April 2007 (2007-04-26) abstract; figures 8,9 paragraph [0046] -----	1-12
A	US 2006/272574 A1 (WAITE ANDREW M [US] ET AL) 7 December 2006 (2006-12-07) abstract; claims; figures -----	1-12
A	US 2007/241323 A1 (SAENGER KATHERINE L [US] ET AL) 18 October 2007 (2007-10-18) abstract; claims; figures -----	1-12
A	US 2007/063306 A1 (DOYLE BRIAN S [US] ET AL) 22 March 2007 (2007-03-22) abstract; claims; figures -----	1-12
A	SAENGER K ET AL: "Amorphization/templated recrystallization method for changing the orientation of single-crystal silicon: An alternative approach to hybrid orientation substrates" APPLIED PHYSICS LETTERS, AIP, AMERICAN INSTITUTE OF PHYSICS, MELVILLE, NY, vol. 87, no. 22, 23 November 2005 (2005-11-23), pages 221911-221911, XP012076636 ISSN: 0003-6951 abstract; figures -----	1-12
A	DATABASE INSPEC [Online] THE INSTITUTION OF ELECTRICAL ENGINEERS, STEVENAGE, GB; 2007, YAO-TSUNG HUANG ET AL: "Amorphization and templated recrystallization (ATR) study for hybrid orientation technology (HOT) using direct silicon bond (DSB) substrates" XP002522922 Database accession no. 9705888 abstract -& 2007 INTERNATIONAL SYMPOSIUM VLSI TECHNOLOGY, SYSTEMS AND APPLICATIONS (VLSI-TSA) 23-25 APRIL 2007 HSINCHU, TAIWAN, 2007, pages 144-145, XP002522921 2007 International Symposium on VLSI Technology Systems and Applications (VLSI-TSA) IEEE Piscataway, NJ, USA ISBN: 1-4244-0585-8 -----	1-12

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Information on patent family members

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