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(54) Title: INTEGRATION OF SILICON IMPATT DIODE IN ANALOG TECHNOLOGY

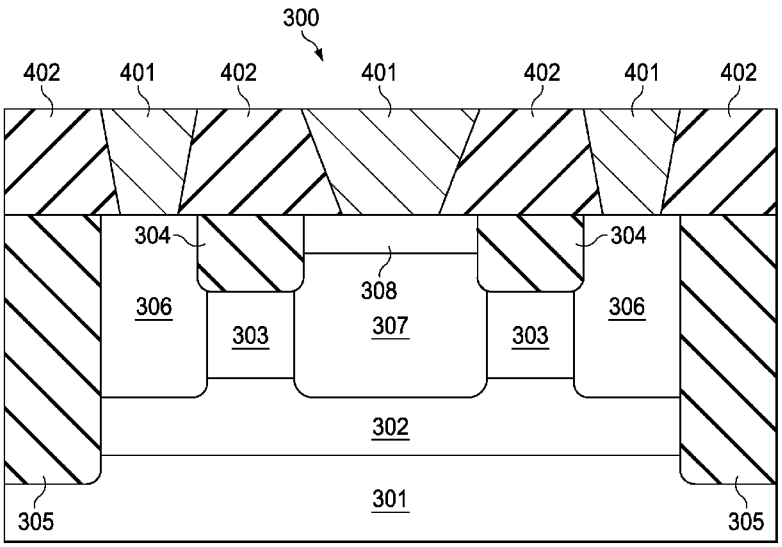

FIG. 3

(57) Abstract: In described examples, a vertical IMPATT diode (300) is fabricated in a standard planar analog process flow.

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INTEGRATION OF SILICON IMPATT DIODE IN ANALOG TECHNOLOGY

[0001] This relates in general to semiconductor devices, and in particular to integration of silicon IMPact Avalanche Transit-Time (IMPATT) diode in analog technology.

BACKGROUND

[0002] The IMPATT diode is a 2-terminal device, such as for applications in radio frequency (RF) power generation and amplification. Compared to a 3-terminal device approach, the IMPATT diode can be fabricated to have relatively small resistive loss and parasitic capacitance. Accordingly, the IMPATT diode can generate high RF power at high frequency, which makes it especially useful for terahertz (such as greater than 300 GHz) applications.

[0003] An n-type IMPATT diode, as shown in FIG. 1, has three distinct regions, a heavily doped P++ region 101 for avalanche breakdown, a lightly doped N region 102 for charge drift, and a heavily doped N++ region 103 for charge collection. When the diode is reverse biased, the free electrons inside the N region are depleted from the device, creating a peak electrical field at the P++ / N junction. When the reverse DC bias increases, the peak electrical field increases, until one of two breakdown processes occurs. In one process, the field may be so high that it exerts sufficient force on a covalently bound electron to free it. This creates two carriers, which are a hole and an electron to contribute to the current. This breakdown is called Zener breakdown or tunneling breakdown. In the second breakdown process, the residual free carriers are able to gain sufficient energy from the electrical field and break covalent bond in the lattice. This process is called avalanche breakdown, and every carrier interacting with the lattice as described above creates two additional carriers. All three carriers can then participate in further avalanching collisions, leading to a sudden multiplication of carriers in the space-charge region when the maximum field becomes sufficiently large to cause avalanche.

[0004] After the carriers are created by breakdown in the high field region, the holes will flow out of the device from the top ohmic contact, resulting in DC current. The electrons will travel across the N region (drift region) 102 and flow out of the device through the bottom ohmic contact. With proper designed doping profile, the electrical field in the N region 102 will be sufficiently high for all of the electrons to move at their saturation velocity v_{sat}. Because the

thickness of N region is nonzero, the electrons take finite time, called transit-time, to flow out of the device. Under alternating current (AC) condition, the diode AC current, coming from the moving electrons within the device, can lag behind the AC voltage applied on the diode, resulting in phase delay between AC current and AC voltage. In the IMPATT diode, the thickness of the N region (drift region) is designed properly to create 180 degree phase delay, so the diode shows negative resistance. After such diode is connected with a resonant circuit, the diode negative resistance can create oscillation and generate RF power.

[0005] Often, a silicon IMPATT diode is fabricated vertically in mesa structure, such as in U.S. Patent No. 3,896,478. Similar structures are also disclosed in U.S. Patent No. 3,649,386 and U.S. Patent Nos. 4,030,943 and 4,064,620. Such mesa structures are still widely used in recent works. In U.S. Patent No. 4,596,070, a slightly different approach is disclosed to fabricate the IMPATT diode, where polyimide is used for isolating different active diodes.

[0006] Two major sources of series parasitic resistance should be minimized. Those sources of resistance are: (a) contact resistance at the substrate contact metal interface; and (b) series resistance of the substrate modified by skin effect. Contact resistance is reduced by maximizing the effective doping level in the substrate at the contact surface, either by maintaining a high level of substrate doping or by contact alloying. Minimizing substrate resistivity also reduces the skin effect contribution to the series resistance. To minimize series resistance, the diode substrate is thinned to micrometer range.

[0007] The discrete mesa shape IMPATT diode in FIG. 1 becomes difficult to adopt at Terahertz range. In that frequency range, an optimized diode should have a diode diameter smaller than 5 um. A challenge exists in fabricating such small diode with thinned substrate, while still being able to assemble the package with desired electrical property, good reproducibility, and long term reliability.

SUMMARY

[0008] In described examples, a vertical IMPATT diode fabricated in a standard planar analog process flow includes: a substrate composed of p-type single crystal silicon; an n-type buried layer touching the top surface of the substrate; an un-doped layer touching the top surface of the n-type buried layer; a deep trench extending down to the substrate and completely surrounding the IMPATT diode and separating the diode from the rest of the elements in an analog circuit; a shallow trench layer covering the top surface of the wafer, where openings are

included to provide for P^{++} and N^{++} areas of the IMPATT diode; an n-well extending through the P^{++} opening in the shallow trench layer into the un-doped layer and touching the top surface of the n-type buried layer; a deep n+ area partially separated from the n-well by a shallow trench structure, where the deep n+ area extends through the N^{++} opening in the shallow trench layer into the un-doped layer touching the top surface of the n-type buried layer; a layer of material touching the top of the n-well selected from the group of highly doped p+ silicon, p+ type SiGe, a composite layer of highly doped p+ silicon on n+ silicon, a composite layer of highly doped p+ silicon on n-type SiGe or a composite layer of p-type SiGe on n-type SiGe; and ohmic contacts separated from each other by a first inter-level dielectric material and separately touching the highly doped n+ layer and the layer of material touching the top of the n-well.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 is a cross-sectional view of an IMPATT diode.

[0010] FIG. 2 is a plan view of an IMPATT diode, detailing the structure below the first metal level and the first inter-level dielectric material according to example embodiments of FIGS. 3-9.

[0011] FIG. 3 is a cross-sectional view through section A-A of FIG. 2 of an IMPATT diode according to an embodiment.

[0012] FIGS. 3A-3D are diagrams of fabrication steps to fabricate the IMPATT diode of FIG. 3 according to an embodiment.

[0013] FIG. 4 is a cross-sectional view through section A-A of FIG. 2 of an IMPATT diode according to another embodiment.

[0014] FIG. 5 is a cross-sectional view through section A-A of FIG. 2 of an IMPATT diode according to another embodiment.

[0015] FIG. 6 is a cross-sectional view through section A-A of FIG. 2 of an IMPATT diode according to another embodiment.

[0016] FIG. 7 is a cross-sectional view through section A-A of FIG. 2 of an IMPATT diode according to another embodiment.

[0017] FIG. 8 is a cross-sectional view through section A-A of FIG. 2 of an IMPATT diode according to another embodiment.

[0018] FIG. 9 is a cross-sectional view through section A-A of FIG. 2 of an IMPATT diode according to another embodiment.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0019] The IMPATT diode FIG. 1 has three distinct regions, which are a heavily doped P^{++} 101 region for breakdown, a lightly doped N region 102 for charge drift, and a heavily doped N^{++} region 103 for charge collection. The diode is reverse biased at breakdown condition, and holes are generated by avalanche in the high field region between P^{++} and N layers. The electrical field in the N region is sufficiently high for the holes to move at saturation velocity, but sufficiently low to prevent the additional charges from being created by impact ionization. The holes finally reach the low field N^{++} region and are absorbed by the bottom ohmic contact.

[0020] Often, a silicon IMPATT diode is fabricated vertically in a mesa structure. This solution works in some cases, but is challenging to integrate with modern analog processing.

[0021] FIG. 2 is a plan view of an IMPATT diode, detailing the structure below the first metal level 401 and the first inter-level dielectric material 402 according to example embodiments of FIGS. 3-9.

[0022] FIG. 3 shows a partial sectional depiction of a semiconductor substrate with an n-type IMPATT diode of example embodiments. FIGS. 3A through 3D show various parts of a process that can be used in fabricating an IMPATT diode, in accordance with an aspect of example embodiments. Many or all portions of the process can be implemented with a bipolar or bi-CMOS process. Also, while the following process steps will be described mainly with respect of forming an n-type IMPATT diode, a p-type IMPATT diode can also could be fabricated in accordance with an aspect of example embodiments. Further, the particular order shown in the figures can be changed and still produce an IMPATT diode in accordance with example embodiments.

[0023] Referring to FIG. 3A, the process begins by providing a substrate composed of p-type single crystal silicon 301, forming an n-type buried (NBL) layer 302 overlaying and touching the top surface of the substrate as shown in FIGS. 3-8, and epitaxially depositing an un-doped layer (EPI) 303 overlaying and touching the top surface of the NBL layer 302. In this embodiment, substrate 301 is p-type silicon wafer. An IMPATT diode may be built on substrate of other group IV elements or compound semiconductor materials, such as gallium arsenide and mercury telluride. The substrate may be mono-crystalline or poly-crystalline. It may be a bonded wafer, where a layer of insulator is bonded to layers of semiconductor material.

[0024] Also, FIG. 3A shows an NBL layer 302. The NBL layer is usually a heavily doped,

mono-crystalline silicon layer, which serves as a low-resistance current path between the drift layer 307 and the sinker layer 306. In a high-performance bipolar or Bi-CMOS integrated-circuit chip, an NBL layer usually exists for other circuit considerations. A second (p-type) buried layer may be incorporated atop the NBL layer for building a p-type IMPATT diode in a p-type substrate. In many circuit applications, a second buried layer is advantageous, because the avalanche noise within the IMPATT diode will not interfere with the components in surrounding environment.

[0025] Also, FIG. 3A shows an epitaxial layer 303, which is an un-doped mono-crystalline silicon layer with high resistivity. In this embodiment, the entire device 300 is mono-crystalline. An IMPATT diode may also be built with poly-crystalline material in the breakdown layer 308, drift layer 307, and sinker layer 306, although mono-crystalline material tends to have some physical properties (such as charge carrier mobility) that are superior to those associated with polycrystalline material.

[0026] Referring to FIG. 3B, the process is followed by forming a field oxide layer 304 covering the top surface of the wafer, where openings are included to provide for drift layers 307 under the breakdown layer 308 and the N^{++} sinker opening 306 of the IMPATT diode. In one example, the field oxide layer 304 is silicon dioxide whose thickness is between 250 and 600 nanometers, which is formed preferably by shallow trench isolation (STI) process, or possibly by local oxidation of silicon (LOCOS) processes. The STI layer 304 electrically isolates the sinker layer 306 from breakdown layer 308.

[0027] As shown in FIG. 3B, the process is followed by forming another field oxide layer 305 extending from the top surface of the un-doped EPI layer 303 down to the substrate and completely surrounding the IMPATT diode, which separates the diode from the rest of the elements in an analog circuit. In one example, the field oxide layer 305 is silicon dioxide whose thickness is between 1 and 10 micrometers, which is formed preferably by deep trench isolation (DT) process. With the DT layer 305, the IMPATT diode 300 is electrically isolated from other electrical components, and is communicable to other circuit elements of an integrated circuit through metallic leads 401.

[0028] Referring to FIG. 3C, the process is followed by forming a deep N^{++} sinker layer 306 through the N^{++} opening surrounded by the STI layer 304, partially separated from the breakdown layer 308 by the STI layer 304 and a portion of the un-doped EPI layer 303, where

the deep N^{++} sinker layer 306 extends through the un-doped EPI layer 303 and touches the top surface of the NBL layer 302. The sinker layer 306 is an n-type layer, which is heavily doped, mono-crystalline silicon layer. It creates a low resistive path between the underneath NBL layer 302 and top metallic leads 401.

[0029] Referring to FIG. 3D, the process is followed by forming a drift layer 307 through the opening in the STI layer 304, where the drift layer 307 extends through the un-doped EPI layer 303 and touches the top surface of the NBL layer 302. The drift layer 307 is an n-type layer, which is lightly doped, mono-crystalline silicon layer. When the IMPATT diode is reverse biased, the free charge is depleted from the drift layer 307, and high electrical field is built up in this drift layer. On a first hand, the electrical field in the drift layer 307 is sufficiently high that charges will move at their saturation velocity from the breakdown layer 308 to the NBL layer 302. On a second hand, the electrical field in the drift region 307 is sufficiently low that no additional avalanche breakdown will occur in this drift layer.

[0030] As shown in FIG. 3D, the process is followed by forming a breakdown layer 308 touching the top of the drift layer 307. The breakdown layer 308 is a p-type layer, which is heavily doped, mono-crystalline silicon layer. Because the drift layer 307 and the sinker layer 306 are doped with n-type dopant, the same doping polarity as that in the NBL layer, a p-n junction exists at the intersection between the breakdown layer 308 and the drift layer 307, while the intersections between the NBL layer 302 and the drift layer 307 and the sinker layer 306 will be ohmic. When the diode is reverse biased, the electrical field at the p-n junction described above is sufficiently high that breakdown will occur. Charges will be generated in this breakdown layer 308, by either avalanche breakdown or tunneling breakdown, or mixed avalanche-tunneling breakdown. Because the electric field in the drift layer 307 is sufficiently high, the electrons created by the avalanche process will drift at their saturation velocity across the drift layer 307. Because the epitaxial layer 303 is un-doped, a potential barrier exists to prevent the current flow directly from the drift layer 307 to the sinker layer 306. Also, the sinker layer 306 is electrically isolated from the breakdown layer 308 by the STI layer 304. Accordingly, the electrons created by the breakdown process will drift through the whole drift layer 307, providing necessary transit-time and creating phase delay between the AC current and the AC voltage. After drifting across the drift layer 307, the electrons will flow through the low resistive paths from the NBL layer 302 and sinker layer 306, and reach the top metallic leads

401.

[0031] The process steps described above are only a portion of the total manufacturing process with which to make an n-type IMPATT diode of example embodiments. Also, FIG. 3 shows a portion of the metallic-lead structure associated with the IMPATT diode, where elements 401 are the first metal level, and where elements 402 are the first inter-level dielectric material. FIG. 3 does not show regions of silicidation, which are commonly employed in the art for reducing the contact resistance between the semiconductor material and the metallic leads 401. Refractory metals (such as nickel, titanium and cobalt) are commonly employed in the silicidation process.

[0032] The doping of the various layers listed above may be implemented by ion-implant techniques, diffusion techniques, or other techniques known in the art of semiconductor processing. In the embodiment of FIG. 3, the NBL layer 302, the sinker layer 306 and the breakdown layer 308 are heavily doped. The drift layer 307 is generally doped more lightly than the breakdown layer 308 and the NBL layer 302, in order to deplete the free charge in the drift layer and create necessary high electric field for the charges to transport at their saturation velocity.

[0033] FIG. 4 shows an alternative approach to implement IMPATT diode, where a heavily doped N^{++} mono-crystalline silicon layer 309 is formed between the breakdown layer 308 and the drift layer 307. With this additional N^{++} layer 309, the electrical field at the p-n junction between the layers 308 and 309 can be independently adjusted to create desired breakdown composition between avalanche and tunneling and, accordingly, create preferred device noise performance. Also, the electrical field in the drift layer 307 can be reduced to minimize the chance of additional breakdown in the drift layer 307.

[0034] FIG. 5 shows another approach to implement IMPATT diode, where both N-type and P-type SiGe heterostructures are available. The heavily doped breakdown layers 308 and 309 in FIG. 4 can be replaced with a heavily doped P^{++} SiGe layer 310 and N^{++} SiGe layer 311, respectively. Because the SiGe material has smaller bandgap, the electrical properties (especially the avalanche breakdown and tunneling breakdown) will be different from that of the bulk mono-crystalline silicon. It requires less electrical field to create either avalanche breakdown or tunneling breakdown within the SiGe layers 310 and 311. Such feature is advantageous, because the breakdown will be confined within the narrow bandgap SiGe layer, and the doping

requirement for the drift layer 307 is relaxed.

[0035] FIG. 6 shows another approach to implement IMPATT diode, where only P-type SiGe material is available. The P^{++} breakdown layer 308 in FIG. 3 is replaced with the P^{++} SiGe breakdown layer 310. With proper design, the breakdown will be confined within the P^{++} SiGe breakdown layer 310, and doping requirement for the drift layer 307 is relaxed.

[0036] FIG. 7 shows another approach to implement IMPATT diode, where only N-type SiGe material is available. The N^{++} breakdown layer 309 in FIG. 4 is replaced with the N^{++} SiGe breakdown layer 311. In this example, the breakdown will be confined within both the P^{++} breakdown layer 308 and the N^{++} SiGe breakdown layer 311. Compared to the example in FIG. 4, the doping requirement for the drift layer 307 is relaxed.

[0037] A modified process can be used for designing a lateral IMPATT diode, as in FIG. 8. In this example, the epitaxial layer 312 is doped with n-type, and current will flow under the STI layer 304 and through the n-type EPI layer 312, instead of through the NBL layer 302 as in FIG. 3. The advantage of such structure is that the diode operation frequency, as defined by the thickness of the drift layer 307 as in FIG. 3, is now controlled by the width of the STI layer 304 through lithography. Because the thickness of the drift layer 307 is usually fixed, the lateral example in FIG. 8 is more flexible to design diode oscillation frequency by designing the width of the STI layer 304 through lithography. Multiple oscillators at various frequencies can be implemented on the same technology. Also, the p-n junction field between the breakdown layer 308 and the drift layer 312 is uniform, which helps to control the avalanche breakdown.

[0038] FIG. 9 shows another approach to implement a lateral IMPATT diode, where the buried NBL layer 302 is replaced with a buried oxide layer 313. Because the current flows under the STI layer 304 and through the n-type EPI layer 312, instead of through the NBL layer 302 as in FIG. 3, the NBL layer 302 has no electrical benefit. The advantage of such structure is that the diode is isolated from rest of component by the buried oxide layer 313 and the DT layer 305, and the avalanche noise within the IMPATT diode will not interfere with the components in a surrounding environment. Also, the p-n junction field between the breakdown layer 308 and the drift layer 312 is uniform, which helps to control the avalanche breakdown.

[0039] Device architectures of the example embodiments allow silicon IMPATT diodes to be integrated into an analog process.

[0040] Accordingly, in described examples, a vertical IMPATT diode fabricated in a

standard planar analog process flow includes: a substrate composed of p-type single crystal silicon; an n-type buried layer touching the top surface of the substrate; an un-doped layer touching the top surface of the n-type buried layer; a deep trench extending down to the substrate and completely surrounding the IMPATT diode and separating the diode from the rest of the elements in an analog circuit; a shallow trench layer covering the top surface of the wafer, where openings are included to provide for P^{++} and N^{++} areas of the IMPATT diode; an n-well extending through the P^{++} opening in the shallow trench layer into the un-doped layer and touching the top surface of the n-type buried layer; a deep n+ area partially separated from the n-well by a shallow trench structure, where the deep n+ area extends through the N^{++} opening in the shallow trench layer into the un-doped layer touching the top surface of the n-type buried layer; a layer of material touching the top of the n-well selected from the group of highly doped p+ silicon, p+ type SiGe, a composite layer of highly doped p+ silicon on n+ silicon, a composite layer of highly doped p+ silicon on n-type SiGe or a composite layer of p-type SiGe on n-type SiGe; and ohmic contacts separated from each other by a first inter-level dielectric material and separately touching the highly doped n+ layer and the layer of material touching the top of the n-well.

[0041] In one embodiment, a method of forming a vertical IMPATT diode in a standard planar analog process flow includes: providing a substrate composed of p-type single crystal silicon; epitaxially depositing an n-type buried layer overlaying and touching the top surface of the substrate; epitaxially depositing an un-doped layer overlaying and touching the top surface of the n-type buried layer; forming a deep trench extending down to the substrate and completely surrounding the IMPATT diode and separating the diode from the rest of the elements in an analog circuit; forming a shallow trench layer covering the top surface of the wafer, where openings are included to provide for P^{++} and N^{++} areas of the IMPATT diode; forming an n-well extending through the P^{++} opening in the shallow trench layer into the un-doped layer and touching the top surface of the n-type buried layer; forming a deep n+ area partially separated from the n-well by a shallow trench structure, where the deep n+ area extends through the un-doped layer and touches the top surface of the n-type buried layer; forming a layer of material touching the top of the n-well selected from the group of highly doped p+ silicon, p-type SiGe, a composite layer of highly doped p+ silicon on n+ silicon, a composite layer of highly doped p+ silicon on n-type SiGe or a composite layer of p-type SiGe on n-type SiGe; and forming ohmic

contacts separated from each other by a first inter-level dielectric material and separately touching the highly doped n+ layer and the layer of material touching the top of the n-well.

[0042] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A vertical IMPATT diode fabricated in a standard planar analog process flow, comprising:

a substrate composed of p-type single crystal silicon;

an n-type buried layer touching the top surface of the substrate;

an un-doped layer touching the top surface of the n-type buried layer;

a deep trench extending down to the substrate and completely surrounding the IMPATT diode and separating the diode from the rest of the elements in an analog circuit;

a shallow trench layer covering the top surface of the wafer, wherein openings are included to provide for P^{++} and N^{++} areas of the IMPATT diode;

an n-well extending through the P^{++} opening in the shallow trench layer into the un-doped layer and touching the top surface of the n-type buried layer;

a deep n+ area partially separated from the n-well by a shallow trench structure, wherein the deep n+ area extends through the N^{++} opening in the shallow trench layer into the un-doped layer touching the top surface of the n-type buried layer;

a layer of material touching the top of the n-well selected from the group of highly doped p+ silicon, p+ type SiGe, a composite layer of highly doped p+ silicon on n+ silicon, a composite layer of highly doped p+ silicon on n-type SiGe or a composite layer of p-type SiGe on n-type SiGe; and

ohmic contacts separated from each other by a first inter-level dielectric material and separately touching the highly doped n+ layer and the layer of material touching the top of the n-well.

2. The vertical IMPATT diode of claim 1, wherein the layer of material touching the top of the n-well is highly doped p+ silicon,

3. The vertical IMPATT diode of claim 1, wherein the layer of material touching the top of the n-well is p-type SiGe.

4. The vertical IMPATT diode of claim 1, wherein the layer of material touching the top of the n-well is a composite layer of highly doped p+ silicon on n+ silicon.

5. The vertical IMPATT diode of claim 1, wherein the layer of material touching the top of the n-well is a composite layer of p+ silicon on n-type SiGe.

6. The vertical IMPATT diode of claim 1, wherein the layer of material touching the top of the n-well is a composite layer of p-type SiGe on n-type SiGe.

7. The vertical IMPATT diode of claim 1, wherein the un-doped layer touching the top surface of the n-type buried layer is doped n-type.

8. The vertical IMPATT diode of claim 7, wherein the n-type buried layer is composed of buried oxide.

9. A method of forming a vertical IMPATT diode in a standard planar analog process flow, the method comprising:

providing a substrate composed of p-type single crystal silicon;

epitaxially depositing an n-type buried layer overlaying and touching the top surface of the substrate;

epitaxially depositing an un-doped layer overlaying and touching the top surface of the n-type buried layer;

forming a deep trench extending down to the substrate and completely surrounding the IMPATT diode and separating the diode from the rest of the elements in an analog circuit;

forming a shallow trench layer covering the top surface of the wafer, wherein openings are included to provide for P^{++} and N^{++} areas of the IMPATT diode;

forming an n-well extending through the P^{++} opening in the shallow trench layer into the un-doped layer and touching the top surface of the n-type buried layer;

forming a deep n+ area partially separated from the n-well by a shallow trench structure, wherein the deep n+ area extends through the un-doped layer and touches the top surface of the n-type buried layer;

forming a layer of material touching the top of the n-well selected from the group of highly doped p+ silicon, p-type SiGe, a composite layer of highly doped p+ silicon on n+ silicon, a composite layer of highly doped p+ silicon on n-type SiGe or a composite layer of p-type SiGe on n-type SiGe; and

forming ohmic contacts separated from each other by a first inter-level dielectric material and separately touching the highly doped n+ layer and the layer of material touching the top of the n-well.

10. The method of claim 9, wherein the layer of material touching the top of the n-well is highly doped p+ silicon.

11. The method of claim 9, wherein the layer of material touching the top of the n-well is p-type SiGe.

12. The method of claim 9, wherein the layer of material touching the top of the n-well is a composite layer of highly doped p+ silicon on n+ silicon.

13. The method of claim 9, wherein the layer of material touching the top of the n-well is a composite layer of p+ silicon on n-type SiGe.

14. The method of claim 9, wherein the layer of material touching the top of the n-well is a composite layer of p-type SiGe on n-type SiGe.

15. The method of claim 9, wherein the un-doped layer touching the top surface of the n-type buried layer is doped n-type.

16. The method of claim 15, wherein the n-type buried layer is composed of buried oxide.

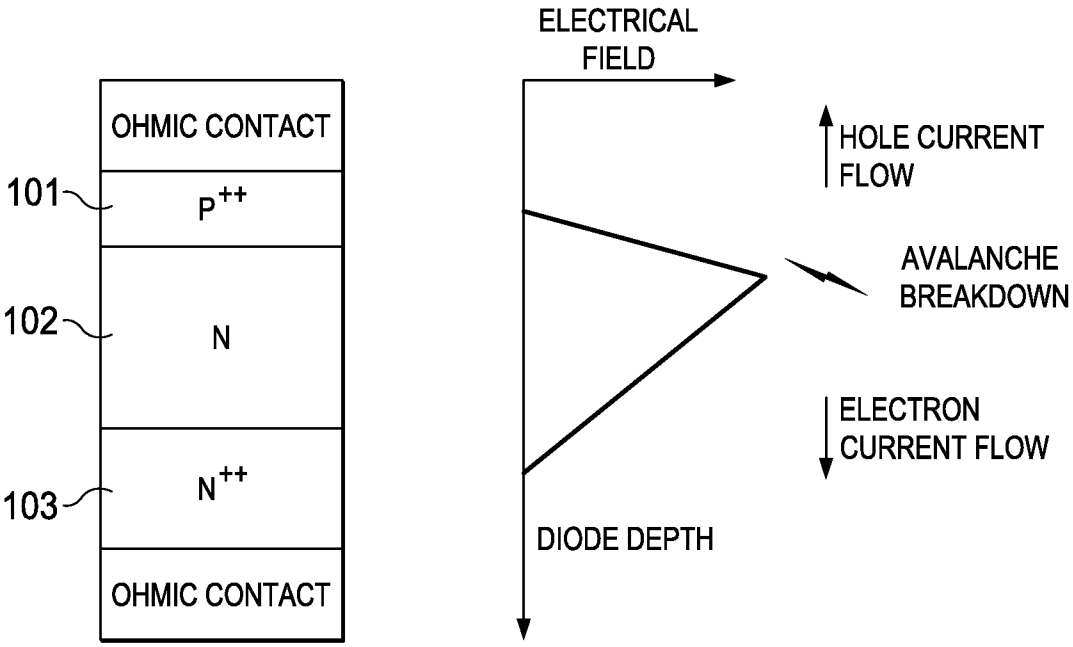
OHMIC CONTACT
101
P++
102
N
103
N++
OHMIC CONTACT
ELECTRICAL FIELD
HOLE CURRENT FLOW
AVALANCHE BREAKDOWN
ELECTRON CURRENT FLOW
DIODE DEPTH

FIG. 1

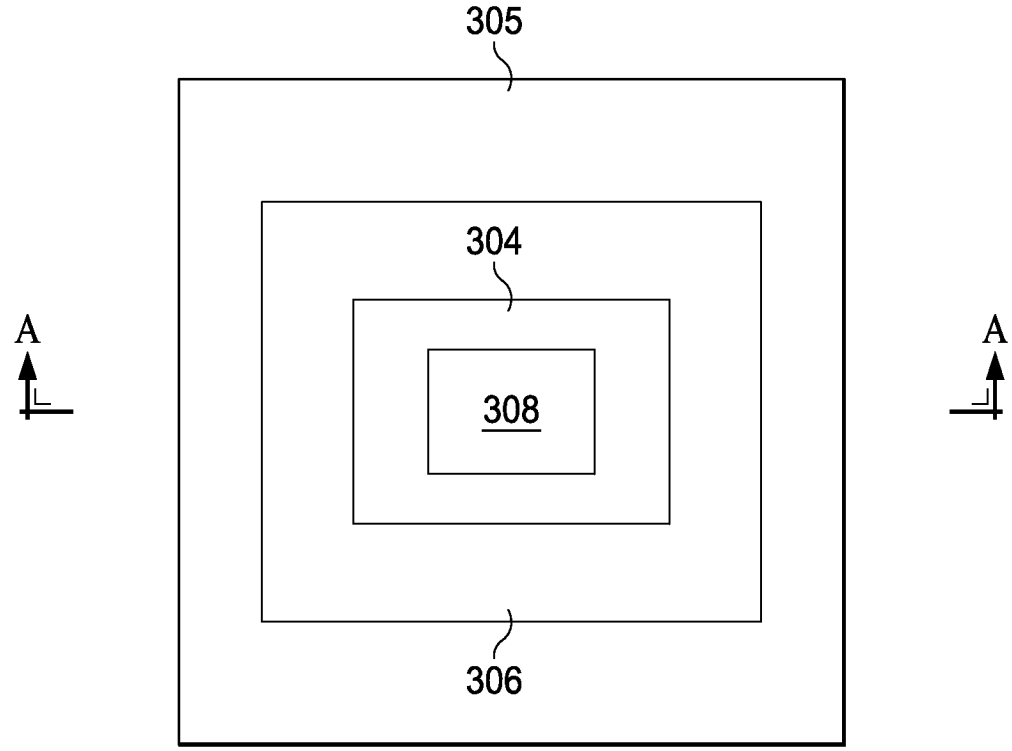
305
304
308
306
A
A

FIG. 2

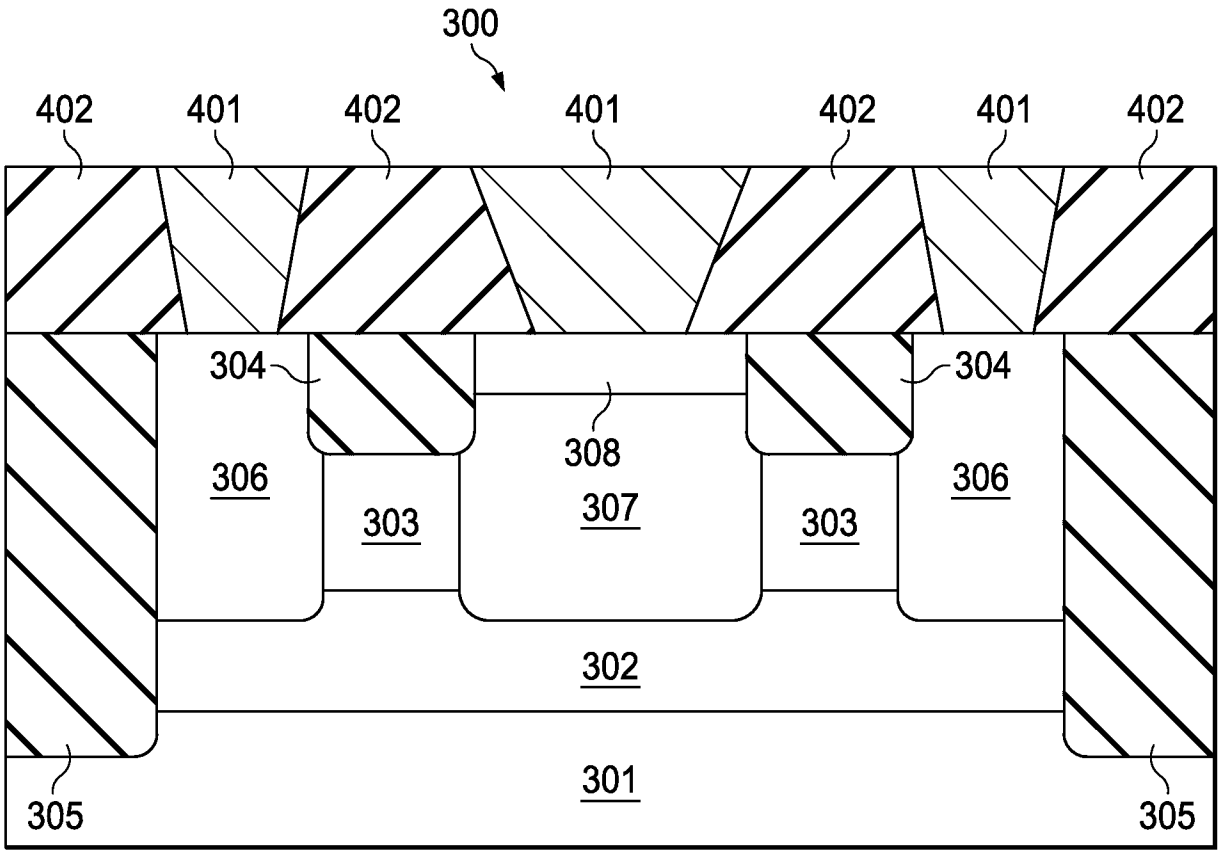
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FIG. 3

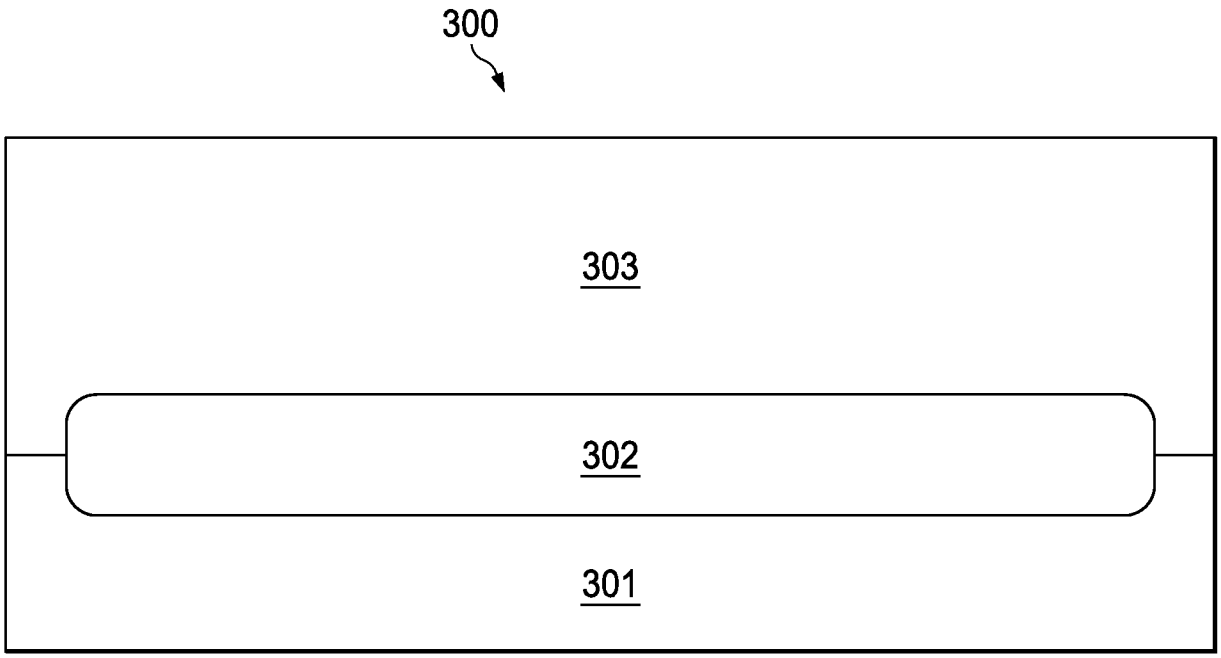

FIG. 3A

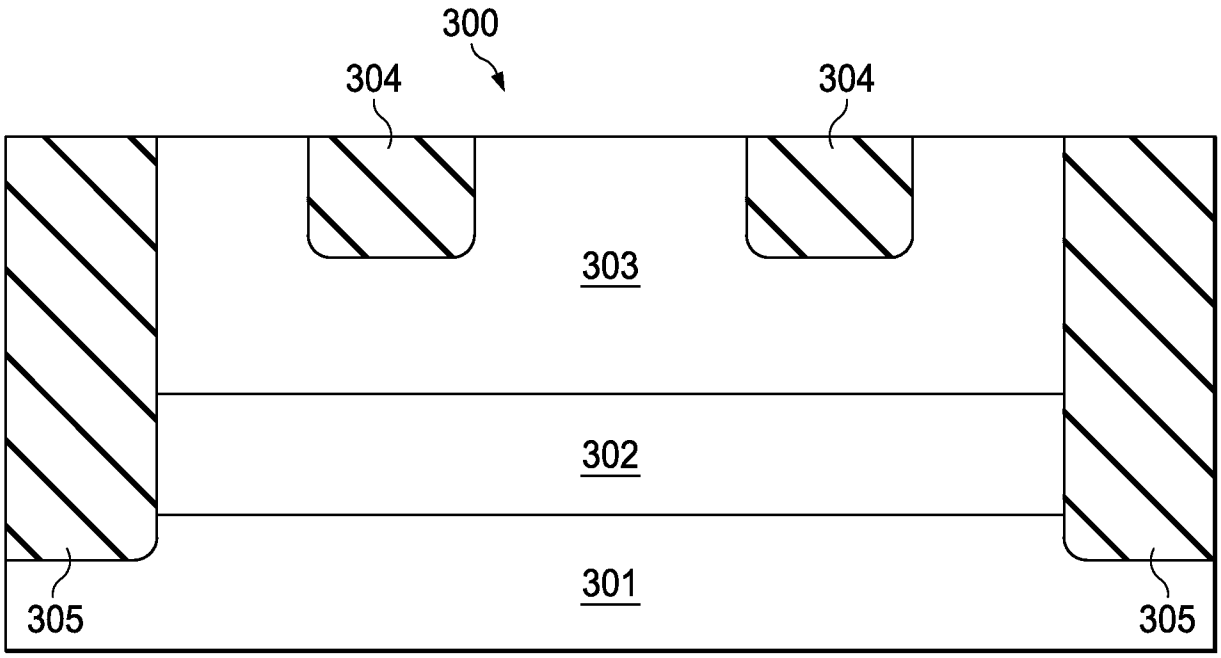

FIG. 3B

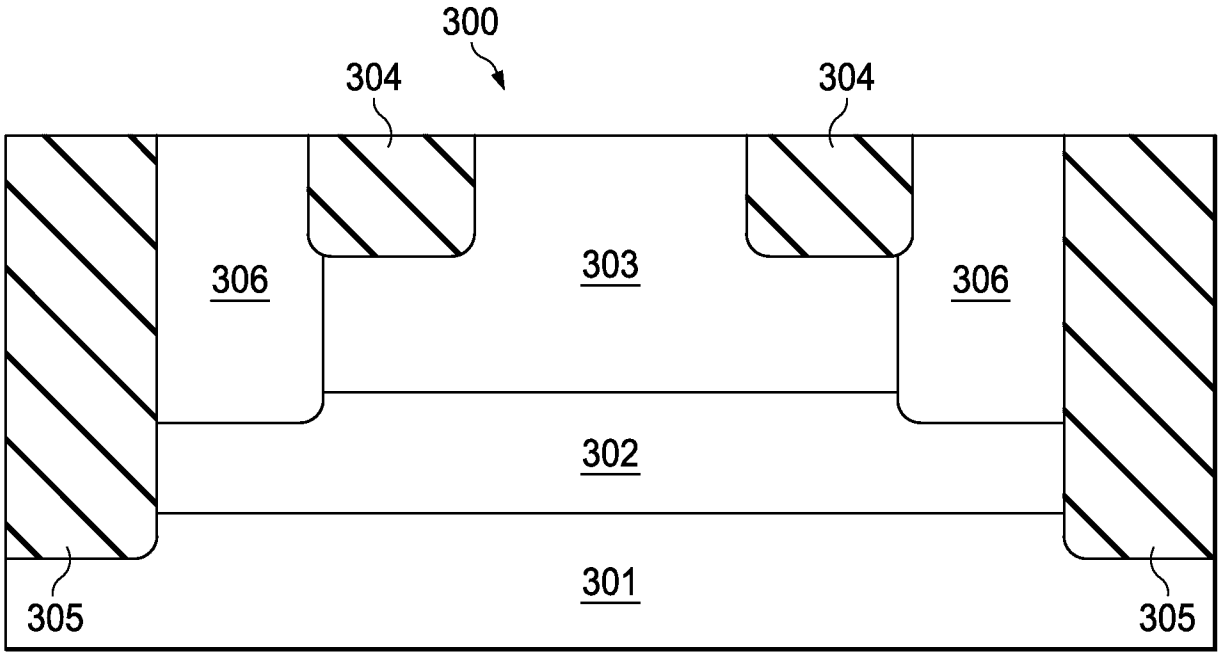
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FIG. 3C

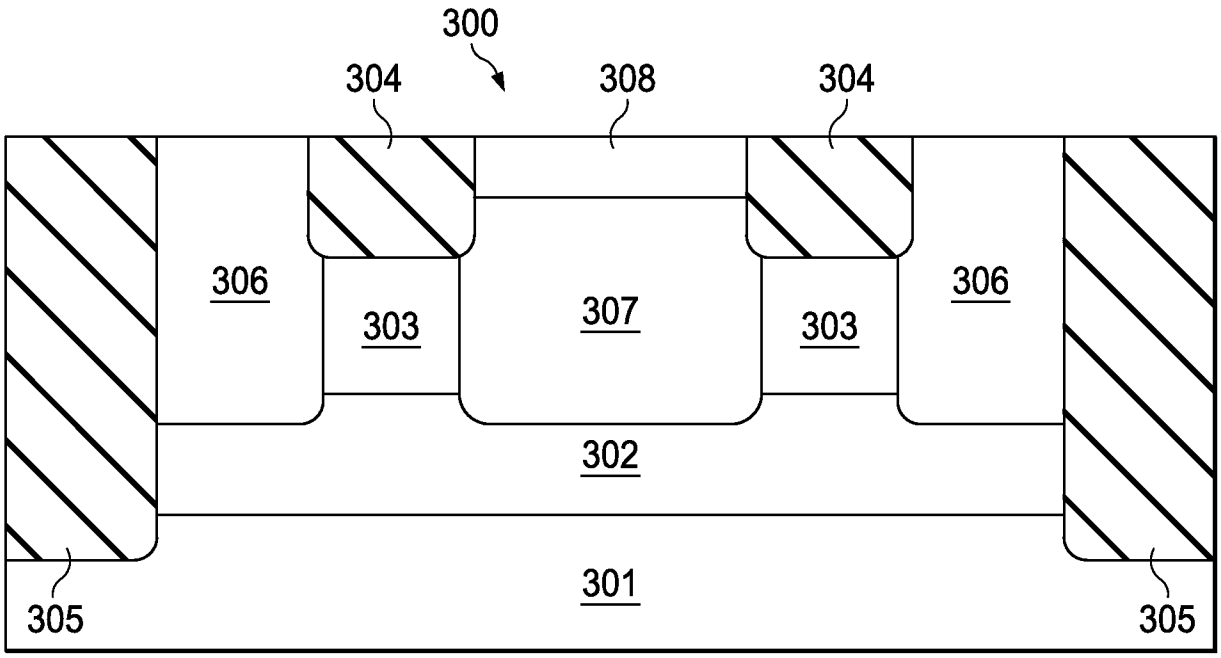
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FIG. 3D

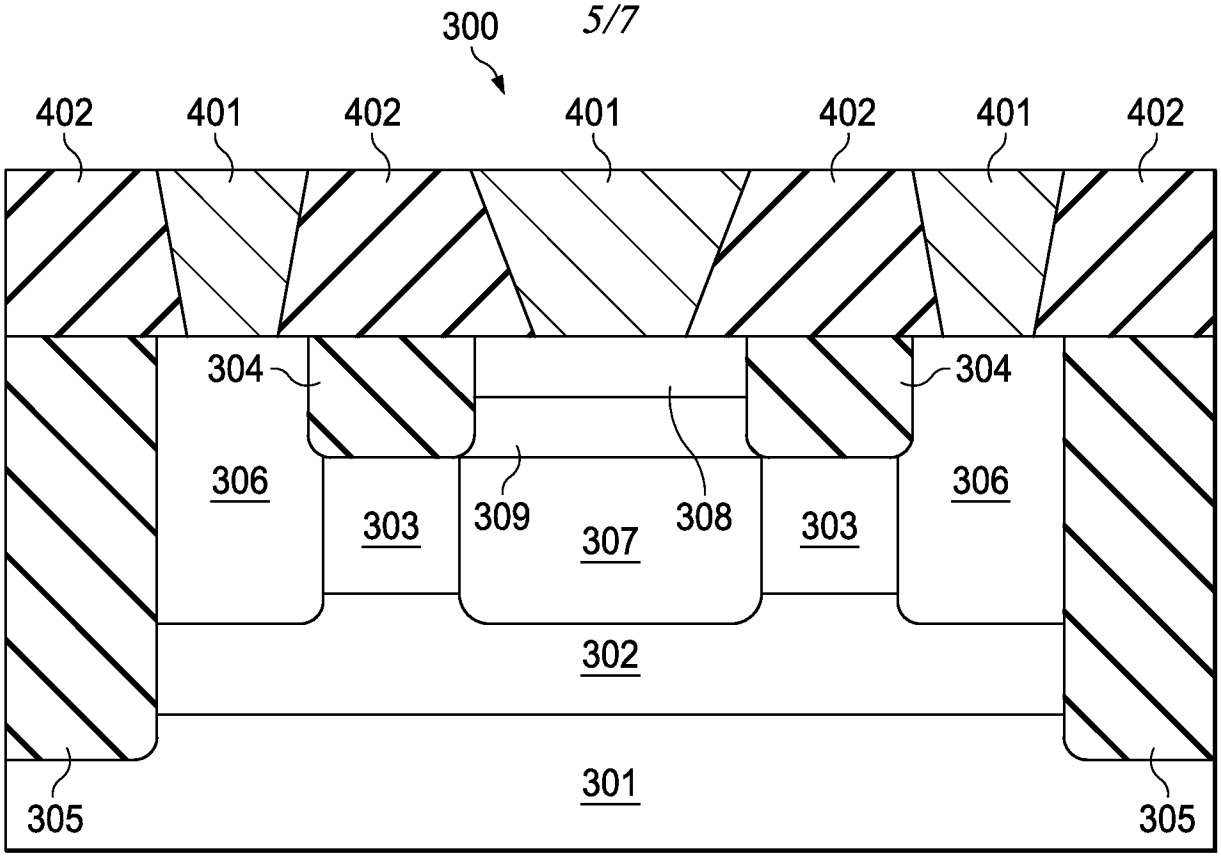
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FIG. 4

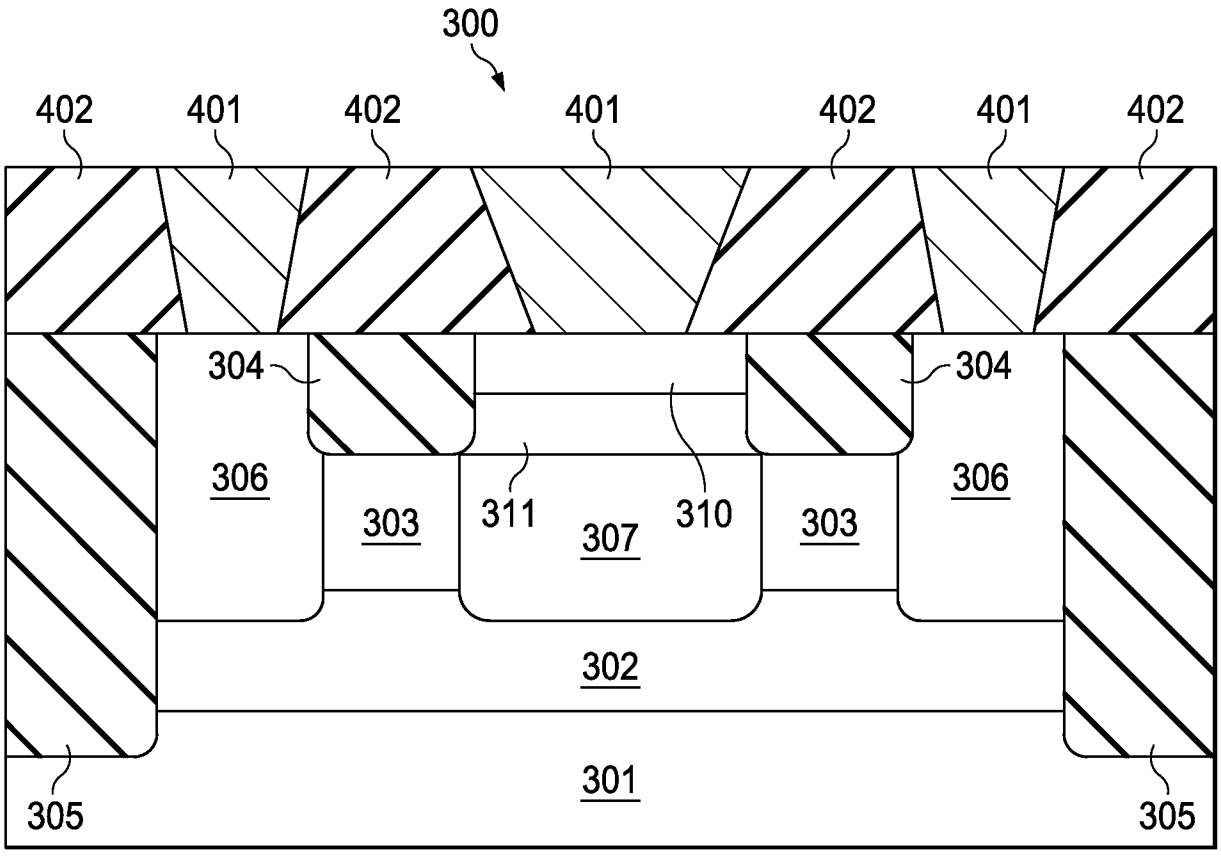
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FIG. 5

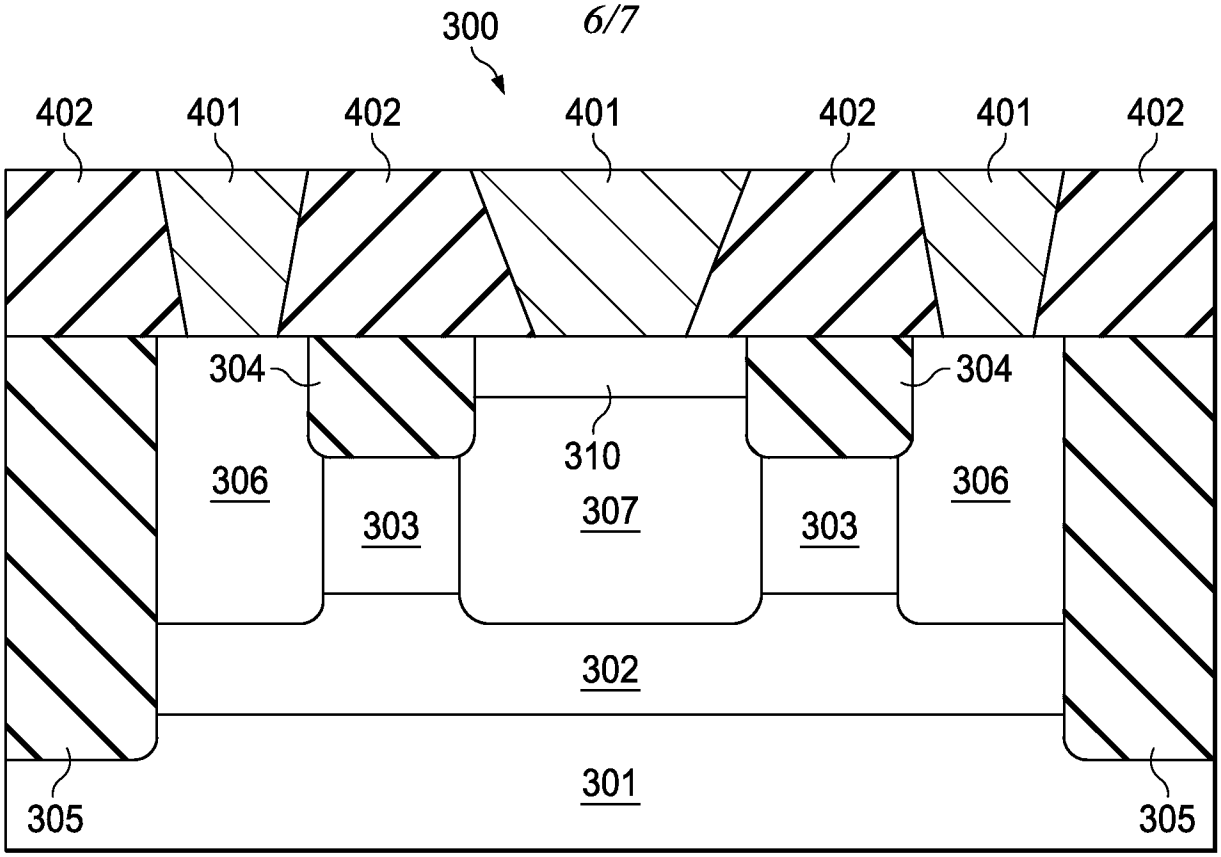
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FIG. 6

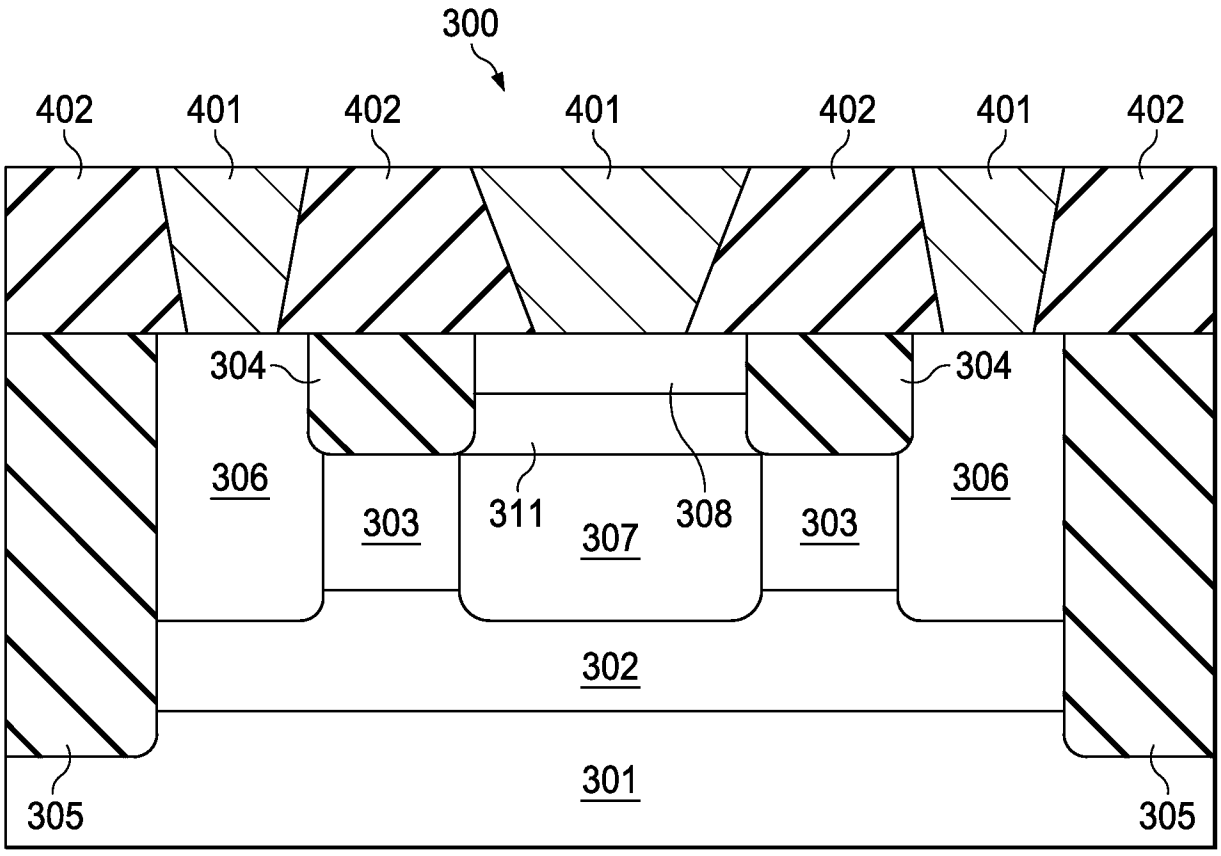
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FIG. 7

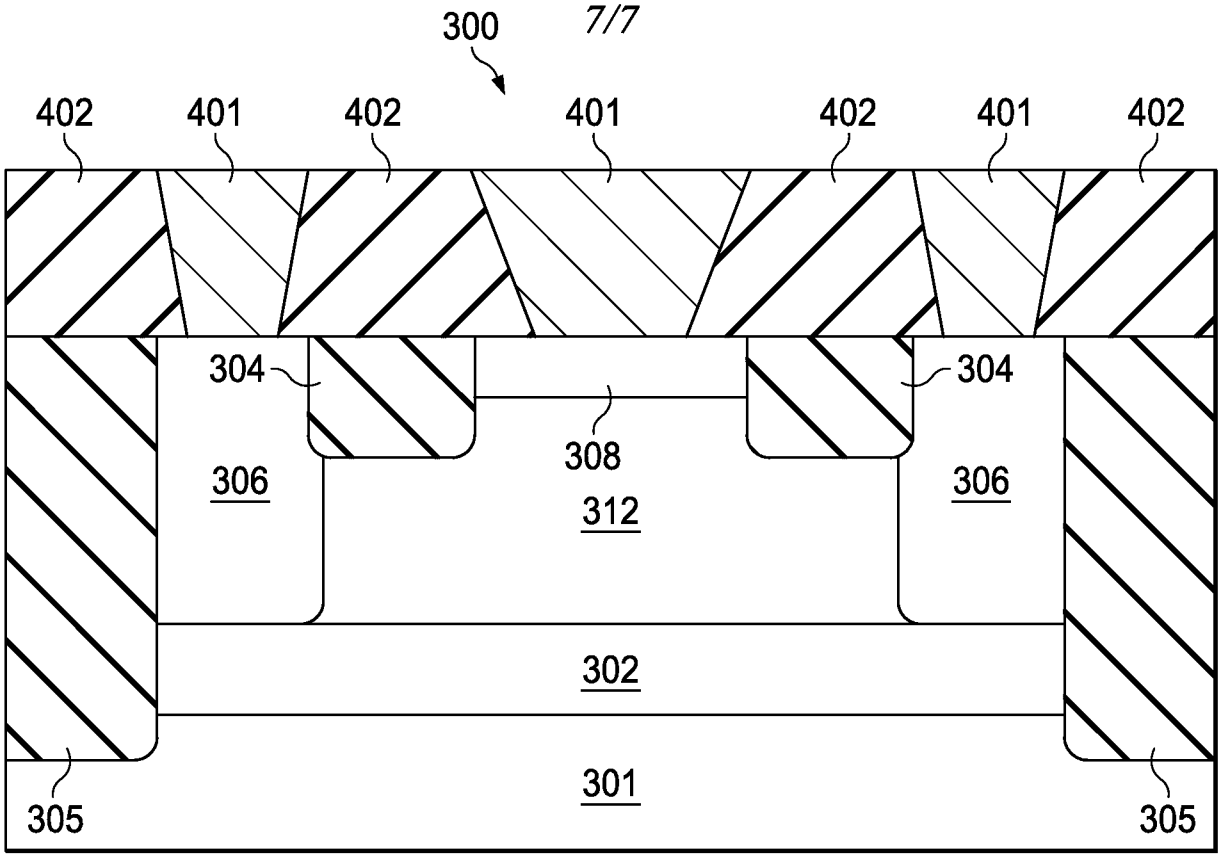
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FIG. 8

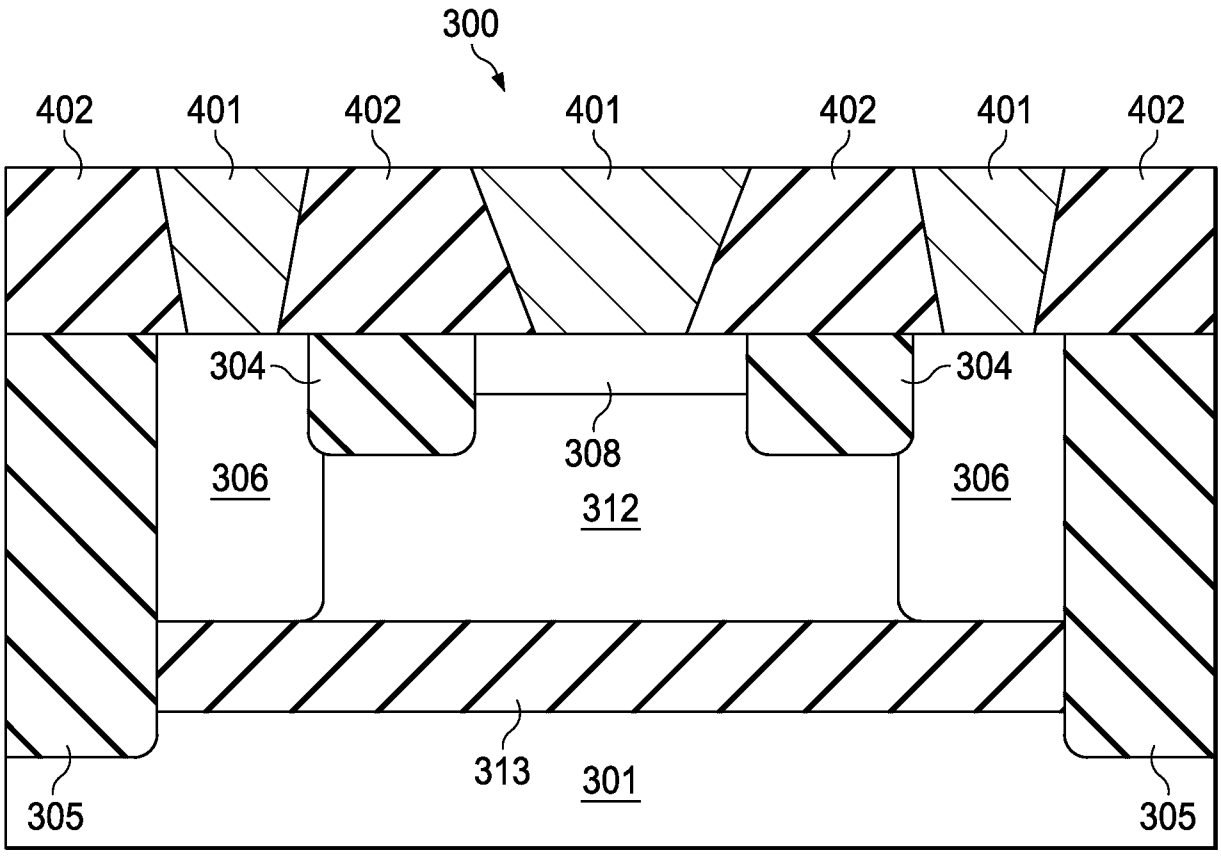
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FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2014/047298

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/329 *(2006.01)*
H01L 29/864 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/328-21/329, 29/861-29/864

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4596070 A (TEXAS INSTRUMENTS INCORPORATED) 24.06.1986	1-16
A	US 6774460 B1 (QINETIQ LIMITED) 10.08.2004	1-16
A	US 4859633 A (TEXAS INSTRUMENTS INCORPORATED) 22.08.1989	1-16
A	US 4857972 A (LICENTIA PATENT-VERWALTUNGS-GMBH) 15.08.1989	1-16

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 October 2014 (24.10.2014)	20 November 2014 (20.11.2014)

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