

[54] **SIGNALING AND INDICATING SYSTEM**

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[51] Int. Cl. .... **H04q 9/00**  
[58] Field of Search .... **340/167, 167 A, 167 B, 169,**  
**340/147 PC, 172; 325/28, 38; 328/109, 115, 116;**  
**329/107, 109; 324/188, 189**

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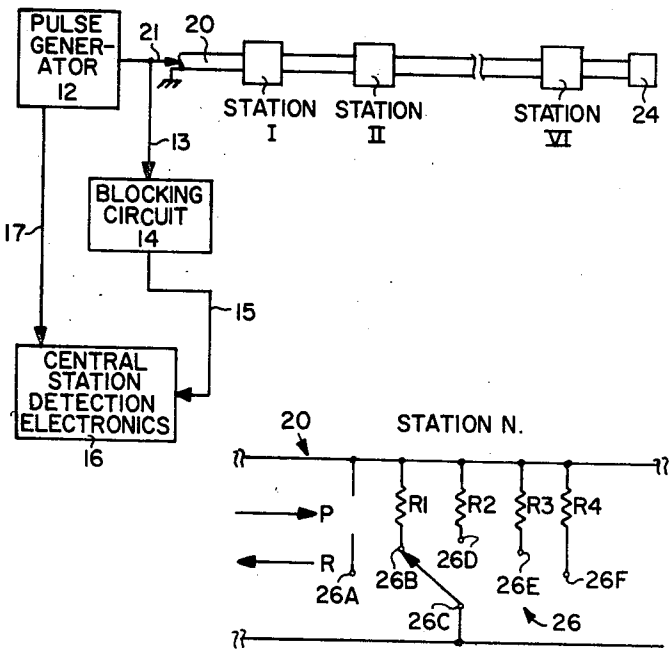
[57] **ABSTRACT**

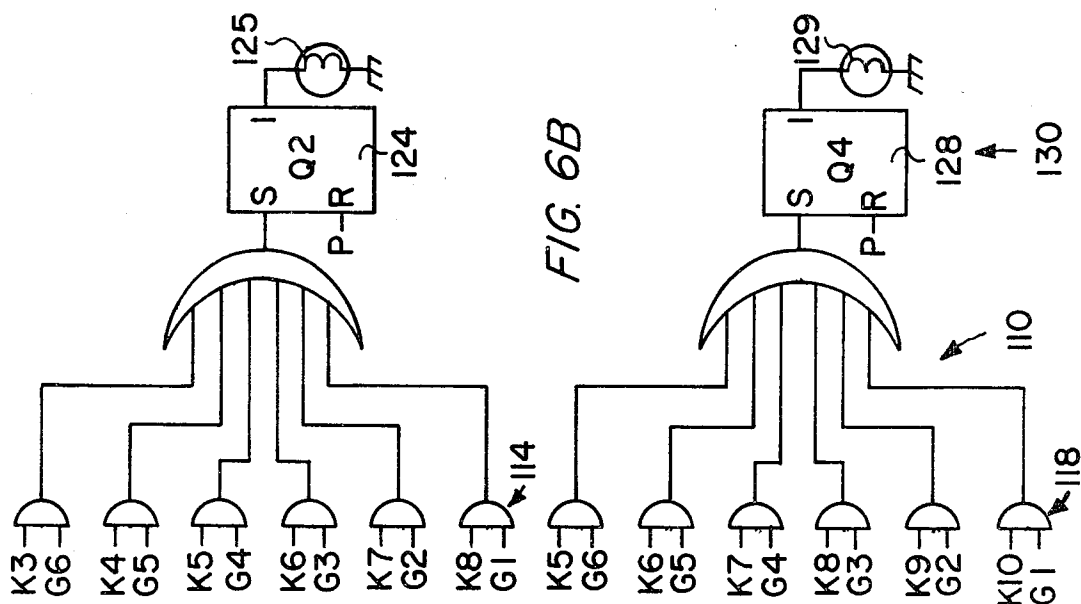
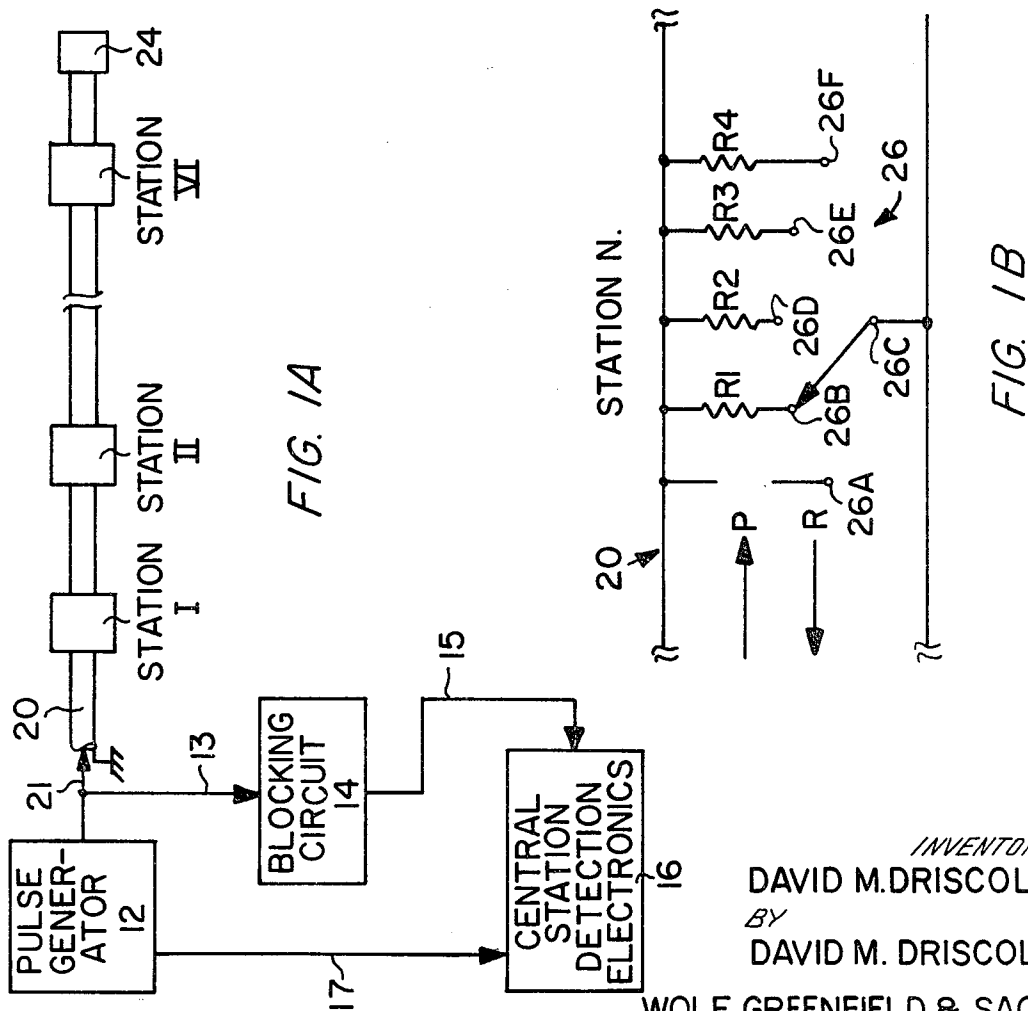
A signaling system is preferably used along a limited access

highway for registering an indication of the location of a motorist in distress. A plurality of remote stations may be positioned at fixed intervals along the highway and are connected to a central control station by a coaxial cable. Each such station comprises a switching means including means which when actuated change the impedance of the cable to one of a selected number of different impedances, each such impedance providing for different degrees of reflection of a pulse transmitted from the central station. Means are provided, coupled to the cable and forming part of the central control station, for transmitting electrical pulses at a predetermined repetition rate along the coaxial cable. The central control station also includes detection electronics for storing an indication of both the occurrence of the transmitted pulse and a pulse reflected from one of the remote stations, and means for indicating which of said stations has been actuated by a distressed motorist.

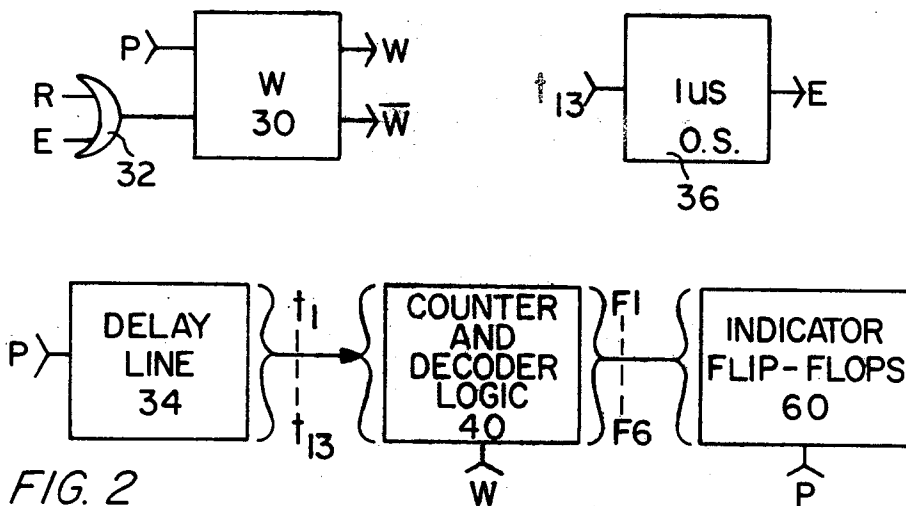
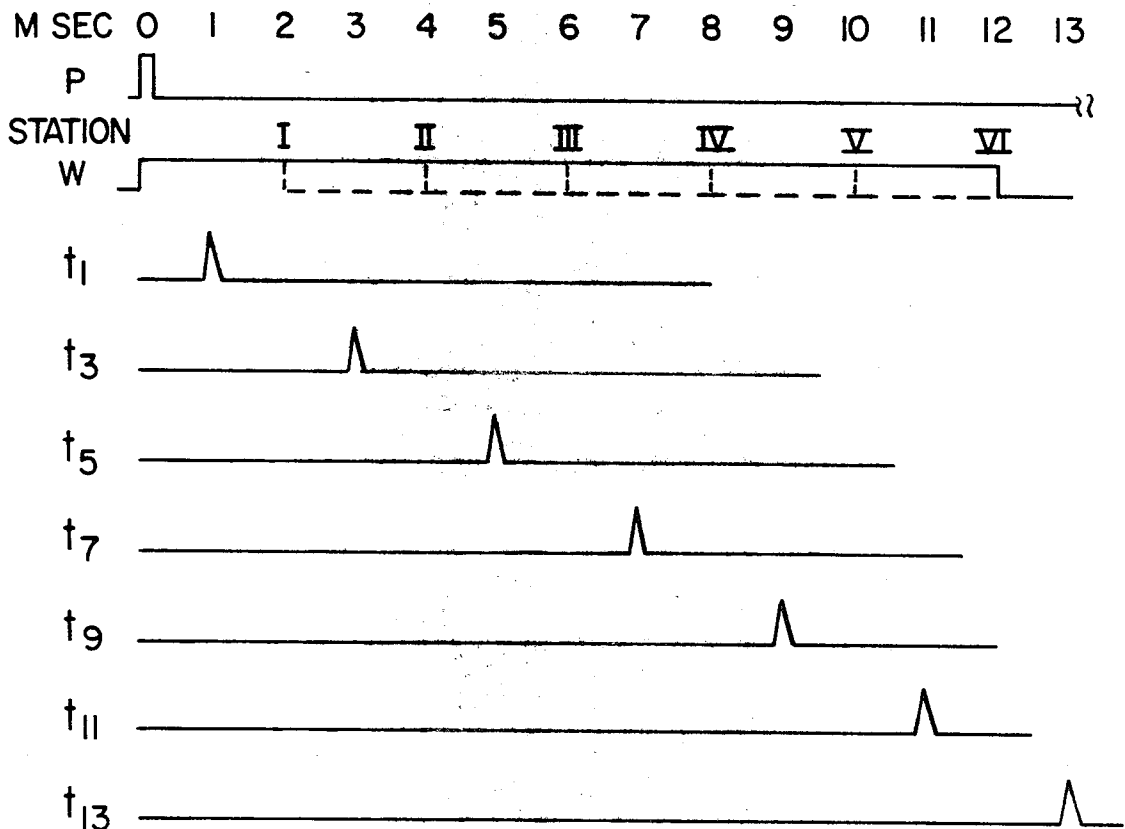
In another embodiment of the invention the detection electronics comprises means for monitoring the plurality of stations and for registering a call (actuation of a switching means at a station) from more than one remote station. In this embodiment, in addition to providing means for indicating which station has called, amplitude detection means in association with logic means may also be provided to determine which of said different impedances have been selected at any one remote station.

10 Claims, 8 Drawing Figures





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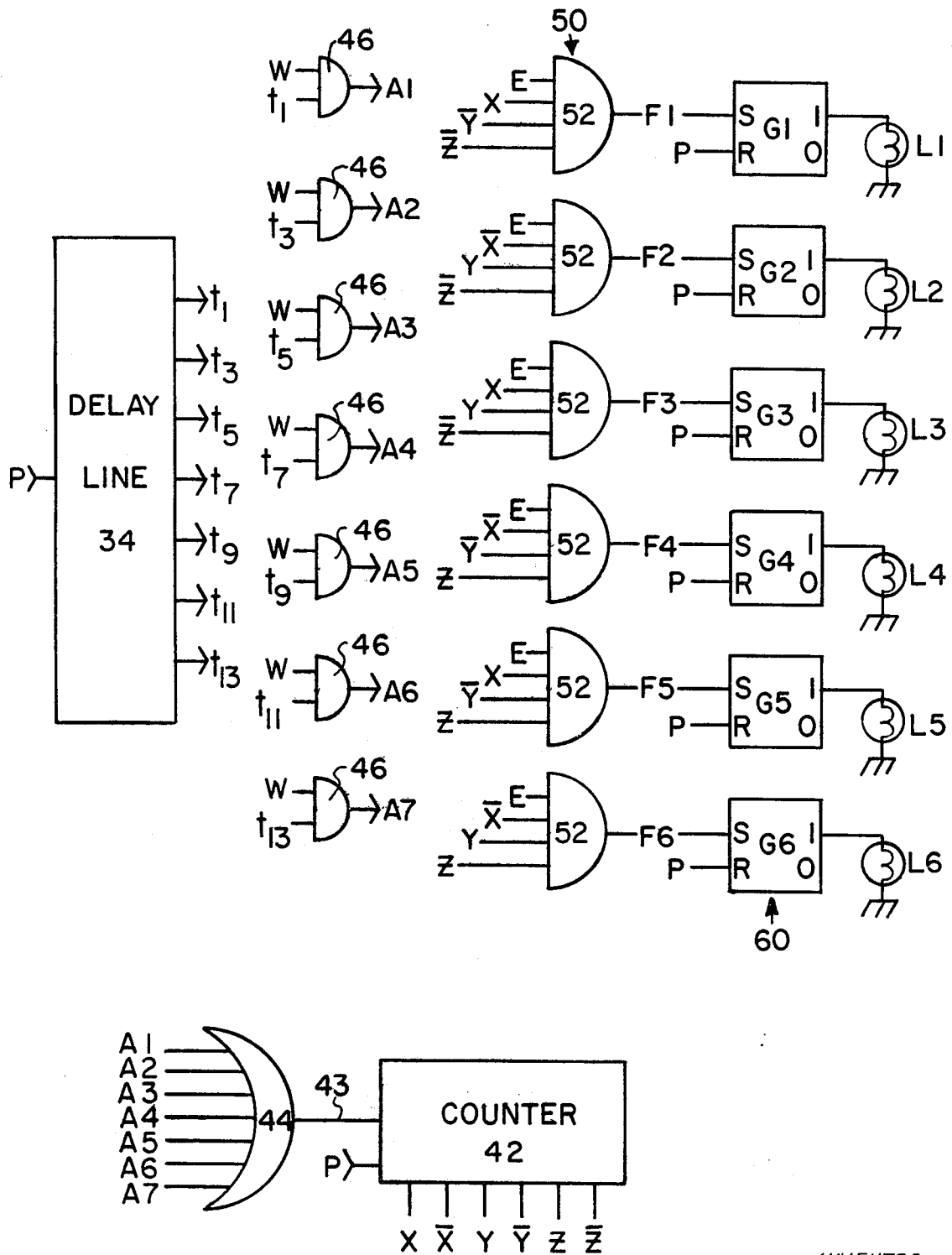


FIG. 4

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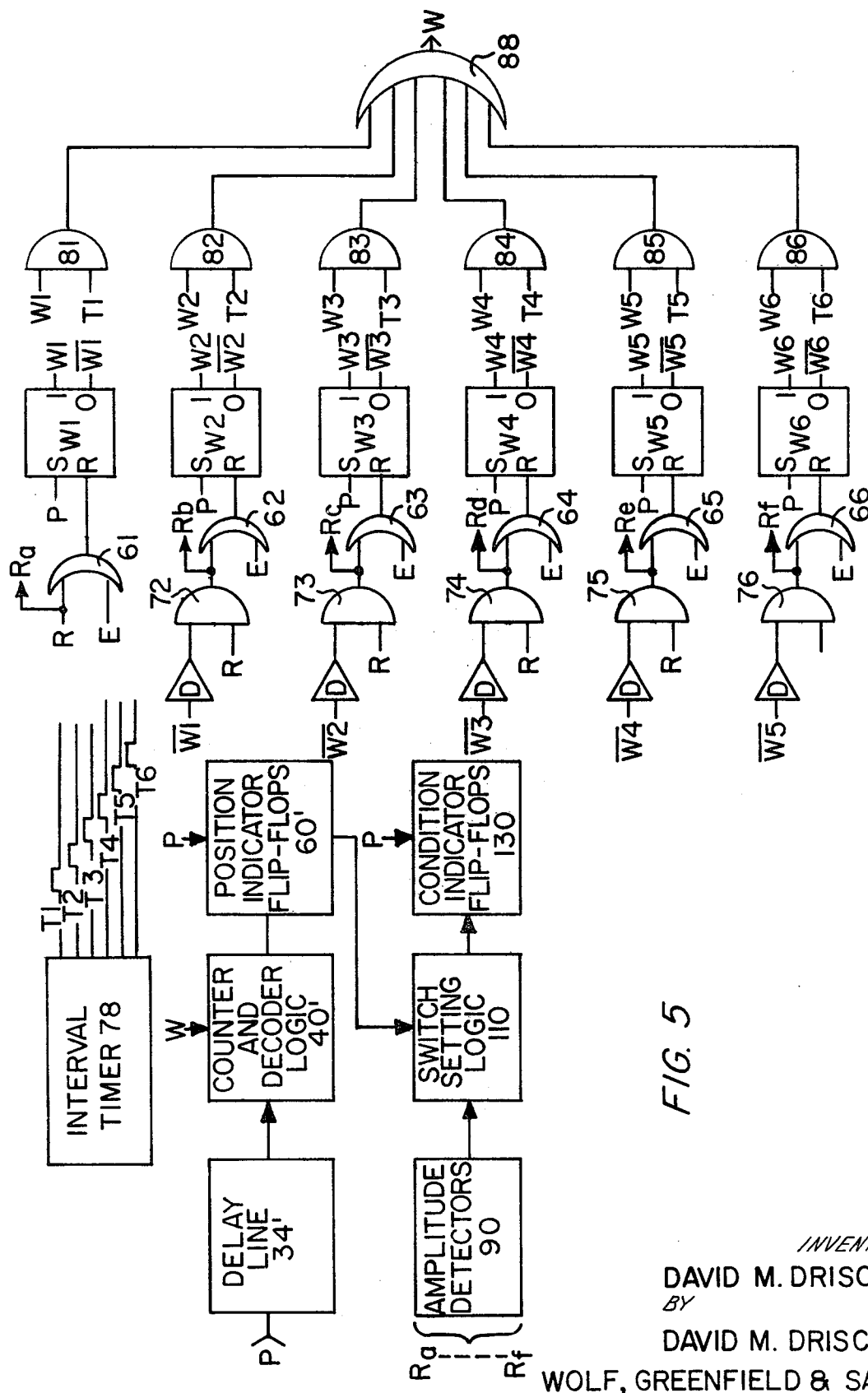
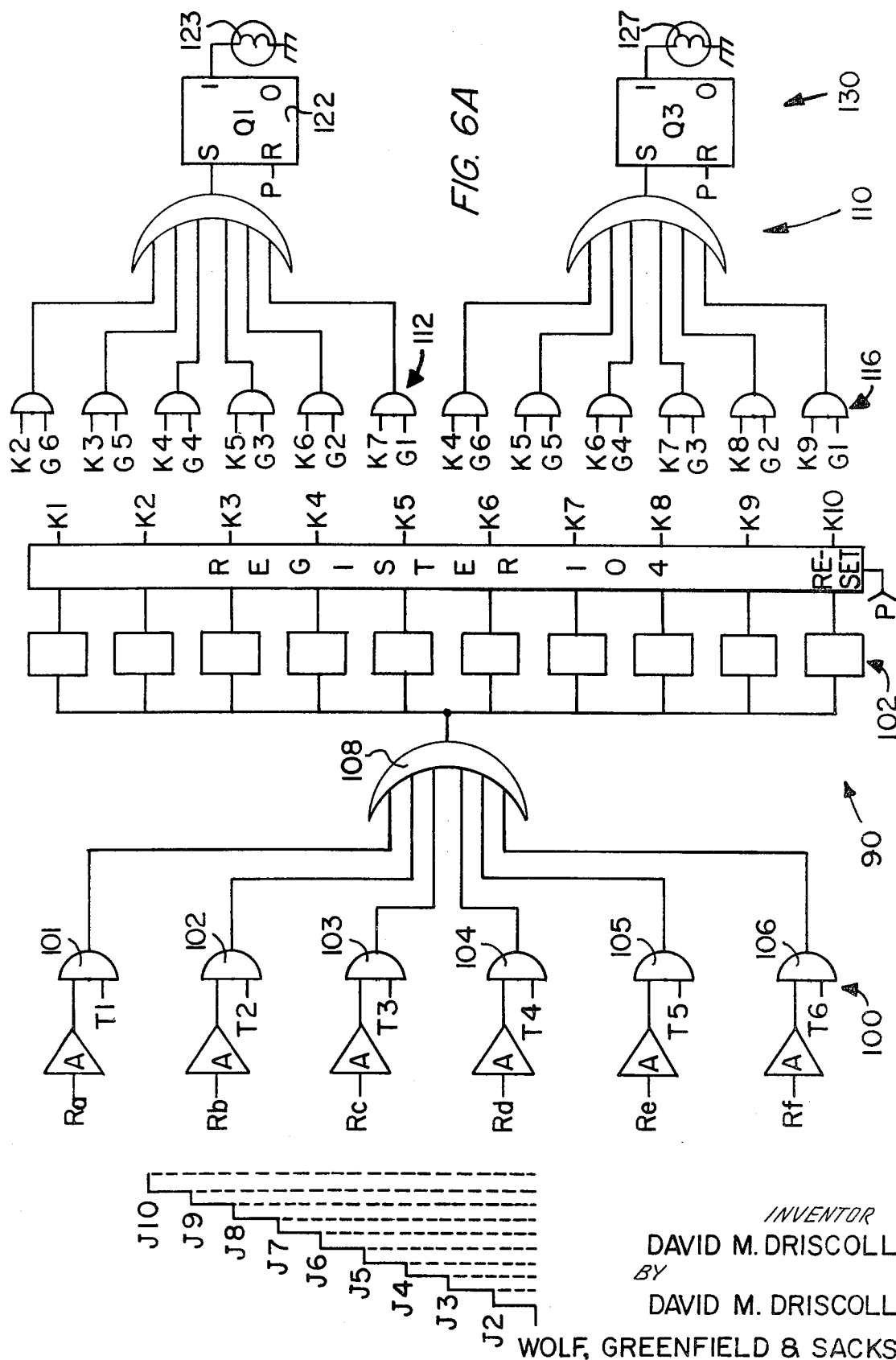


FIG. 5

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## SIGNALING AND INDICATING SYSTEM

## BACKGROUND OF THE INVENTION

The present invention relates in general to a signaling system preferably used on a relatively long limited access highway. More particularly, the present invention relates to a signaling and indicating system including memory circuitry for storing one or more signal conditions.

With the ever increasing number of multi-lane highways and freeways, it has become evident that signaling means should be provided along the highway. One system contemplates the use of a plurality of stations spaced along the highway to be actuated by a distressed motorist. Such signaling systems are particularly helpful when located along a relatively long, limited access highway where exits are spaced at relatively long distances apart.

One known signaling system uses conventional telephone communication means. One of the problems associated with this system is that the motorist in distress must be able to identify his position. Each station could be assigned a code number labelled on the station. However, the number would probably become obliterated, or vandals could tamper with the markings or remove them. Also, a transmitting means would have to be provided at each telephone station and a person at the central station would have to be continuously available to receive distress calls. In addition, such a telephone system is usually expensive and difficult to maintain.

In another known system, a cable is placed along the roadway and a plurality of spaced stations are coupled to the cable each including means for changing the impedance switched across the cable to thereby indicate different distress conditions. In this system, an oscilloscope is used to display the transmitted pulse and any reflected pulse that may occur from an actuated station. The time difference between the transmitted pulse and any reflected pulse is indicative of the position of the actuated station, and the amplitude of the return pulse may be used as an indication of the distress condition. One of the primary disadvantages with the use of an oscilloscope is, of course, the cost involved in providing such an expensive piece of equipment for merely monitoring pulses. Another disadvantage of this system is that there is not readily provided a quick indication of which station is signaling. Also, such a system does not provide a rapid indication of which distress condition is being signaled because it is difficult to correctly read amplitude differences on an oscilloscope. The inherent attenuation associated with the cable makes the problem even more complex.

Accordingly, it is one important object of the present invention to provide an improved signaling system including a central control station and a plurality of remote call stations, preferably for use along a roadway or highway.

Another object of the present invention is to provide a signaling and indicating system comprising a plurality of remote stations including switching means, each of which is capable of being separately manually actuated, and wherein the central control station includes means for logically indicating the actuation of one or more of the switching means.

A further object of the present invention is to provide a signaling and indicating system in accordance with the preceding object and further comprising means for indicating which distress condition has been selected by a motorist actuating a switching means.

## SUMMARY OF THE INVENTION

To accomplish these and other objects, the signaling system of the invention, preferably adopted for use along a highway, includes an electrically conductive cable having a predetermined characteristic impedance. A central control station is coupled to the cables and is adapted to transmit a pulse that may or may not be reflected from one of a plurality of stations coupled to the cable at predetermined distances along the cable. Each station comprises a switching means which is capable of altering the characteristic impedance of the cable to

cause a pulse transmitted therealong to be at least partially reflected. The central control station includes a pulse generating means that generates a pulse at a predetermined repetition rate. Detection electronics is coupled to the cable at the central station for receiving the reflected pulse from one or more of the remote stations, and for storing an indication of which station or stations have been actuated.

In another embodiment of the invention the detection electronics which forms a part of the central control station comprises means for monitoring the plurality of stations and for registering a call from more than one remote station. This embodiment, in addition to providing means for indicating which station has called, provides amplitude detection means in association with logic means to determine which one of a different set of impedances has been selected at the remote station.

Numerous other objects, features and advantages of the invention should now become apparent upon a reading of the following detailed description in conjunction with the accompanying drawings in which:

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a schematic block diagram of a central control station and a plurality of remote stations, in accordance with the present invention.

FIG. 1B is a preferred embodiment of one of the stations of FIG. 1A.

FIG. 2 is a block diagram of one embodiment of the detection electronics shown in FIG. 1A.

FIG. 3 is a timing diagram associated with the logic block diagram of FIG. 2.

FIG. 4 is a logic block diagram including the counter and decoder logic and indicator flip-flops of FIG. 2.

FIG. 5 is a schematic block diagram of another embodiment of detection electronics for the central control station.

FIG. 6A and B is a logic block diagram including the amplitude detectors, switch setting logic and indicator flip-flops depicted in FIG. 5.

## DETAILED DESCRIPTION

Referring now to FIG. 1A, there is illustrated schematically a cable 20 which may be a conventional coaxial cable having an inner conductor 21 coupled to pulse generator 12 and an outer shield conductor preferably grounded, as shown. Cable 20 has stations I through VI coupled thereto in the embodiment of FIG. 1A. Each of these stations may be spaced equidistant from its adjacent station. The cable 20 is terminated at 24 in a conventional manner such as by coupling a resistor across the cable having a resistance equal to the characteristic impedance of the cable. In FIG. 1A this resistance (not shown) would be terminated to ground. An illustrative embodiment of one of the stations, referred to as station N, is shown in detail in FIG. 1B and discussed hereafter.

Generator 12 feeds a pulse to cable 20 which is transmitted therealong and also feeds the same pulse via line 13 to blocking circuit 14. In one embodiment of the invention, pulse generator 12 may generate a 100-nanosecond width pulse at a repetition rate of 1 kilocycle. Pulse generator 12 also couples a P pulse by way of line 17 to central station detecting electronics 16. The P pulses are transmitted at the same time on lines 13 and 17.

Blocking circuit 14 is provided so that the logic circuitry of detection electronics 16 can distinguish a transmitted pulse (P pulse) from a return (R) pulse. Blocking circuit 14 may include one or more monostable multivibrators and may be of conventional design. The P pulse on line 17 is coupled directly to the P inputs of electronics 16. However, the P pulse on line 13 is inhibited (not present on line 15) by blocking circuit 14. Thus, only return (R) pulses are transmitted to electronics 16, via line 15 from cable 20. Detection electronics 16 is discussed in more detail hereinafter with reference to FIGS. 2-6.

Referring now to FIG. 1B, there is shown a station N constructed according to the invention. Station N comprises a switch means including a rotary switch 26 which is illustratively shown as having five separate positions. A wiper arm connects from the common contact 26C to one of the contacts 26A, 26B, 26D, 26E, or 26F. The switch 26 is adapted to switch different impedances across cable 20 so that different amplitude reflection pulses are caused to propagate back along cable 20 to detection electronics 16.

In FIG. 1B, the terminal 26A is open and is considered to be the off condition of rotary switch 26, wherein no impedance is shunted across cable 20. The resistors R1, R2, and R3 and R4 connected from the terminals 26B, 26D, 26E and 26F, respectively, to one of the conductors of cable 20. Typical values for resistors R1-R4 may be 250 ohms, 500 ohms, 750 ohms and 1,000 ohms, respectively.

Referring now to FIG. 2, there is shown one embodiment for the central station detection electronics 16 of FIG. 1A. In FIG. 2, the pulses from generator 12 are referred to as P pulses while the first reflected pulse from one of the stations I-VI is illustrated as the R (return) pulse.

In FIG. 2, the width (W) flip-flop 30 has a set input to which the P pulse is coupled and a reset input to which the R pulse is coupled by way of OR gate 32. When a P pulse is generated by pulse generator 12, flip-flop 30 becomes set and its W output goes high. If a return pulse is sensed by the detection electronics, OR gate 32 is enabled and flip-flop 30 becomes reset at the time that the R pulse occurs. Thus, the W output pulse width is indicative of the time difference between the sending of the P pulse and the receipt of the R pulse. This time difference can be converted quite readily into a distance, knowing at what intervals the stations are spaced. Therefore, the location of the station which was actuated can be determined. OR gate 32 may also be enabled by the E pulse which also resets flip-flop 30.

The delay line 34 receives a P pulse and generates sequential output pulses at one microsecond intervals, for example. Delay line 34 may be of conventional design and has its outputs  $t_1$ ,  $t_3$ ,  $t_5$ ,  $t_7$ ,  $t_9$ ,  $t_{11}$  and  $t_{13}$  coupled to counter and decoder logic 40. These latter outputs of delay line 34 are spaced at 2-microsecond intervals.

Considering that there are six stations with a 1-microsecond delay between adjacent stations, the last station would have a return pulse at 12 microseconds after the P pulse. If no R pulse is generated then the E pulse is used to reset flip-flop 30, and for other purposes discussed later. The  $t_{13}$  output of delay line 34 is coupled to monostable multivibrator 36 and generates an E pulse that may have a width of one microsecond. In FIG. 2, the E pulse enables OR gate 32, resets flip-flop 30, thus conditioning the electronics 16 for the next P pulse.

FIG. 3 depicts the  $t_1$ ,  $t_3$ ,  $t_5$ ,  $t_7$ ,  $t_9$ ,  $t_{11}$  and  $t_{13}$  outputs of delay line 34. These output timing pulses monitor the output of the W flip-flop to ultimately determine when the W output reverts to its reset condition. As indicated, in FIG. 2, the delay line outputs are coupled along with the W output to counter and decoder logic unit 40. The output of unit 40 is in turn coupled to indicator flip-flop 60 which also has the P pulse coupled thereto. The P pulse coupled to indicator flip-flops 60 is used as a reset pulse for the flip-flops comprising this unit 60. The details of units 40 and 60 are discussed in more detail hereinafter with reference to FIG. 4.

Referring to FIG. 3, there is shown a timing diagram associated with FIGS. 2 and 4. FIG. 3 shows the P pulse, the output of the W flip-flop, and the odd numbered timing pulses  $t_1$ - $t_{13}$  from delay line 34. The P pulse is illustrated as occurring at time  $T_0$ , and the stations I-VI may be considered as spaced so that the return pulses are received at two microsecond intervals from selected stations. It is evident from FIG. 3 that the  $t_1$ - $t_{13}$  pulses are used as sample or strobe pulses that monitor the W output one microsecond before it might be reset, thereby sensing for how long the W output is high and when the W output goes low. For example, if a P pulse were generated and an R pulse were returned from station II, the  $t_1$

and  $t_3$  outputs would detect a high level at those times, but the  $t_5$  and subsequent pulses would detect a low level of the W pulse thereafter.

Referring now to FIG. 4, there is shown delay line 34, counter and decoder logic unit 40 and indicator flip-flop unit 60. The delay line 34 has an input from the P pulse generator 12 and includes a plurality of outputs designated as  $t_1$ ,  $t_3$ ,  $t_5$ ,  $t_7$ ,  $t_9$ ,  $t_{11}$  and  $t_{13}$ . In this embodiment, the delay line could be a delay line having a total delay of 15 microseconds where the  $t_{15}$  pulse, or the last of the delay line pulses, is used to generate the E pulse shown in FIG. 2.

The counter and decoder logic unit 40 includes a counter 42 which is a three-stage counter in the embodiment of FIG. 4. The three stages of counter 42 are referred to as the X, the Y and the Z stage. FIG. 4 also shows the  $\bar{X}$ ,  $\bar{Y}$ , and  $\bar{Z}$  negation outputs. Counter 42 is reset by a P pulse on its reset line. The incrementing of counter 42 occurs by pulses received over line 43 from OR gate 44. OR gate 44 is adapted to have seven inputs labeled as inputs A1 through A7 generated from the logic of unit 40.

The unit 40 includes a series of AND gates 46, each of which has an output from the W flip-flop of FIG. 2, and an output from one of the  $t_1$ - $t_{13}$  outputs of delay line 34. For instance, the uppermost AND gate 46 has an input from the W flip-flop and one from the  $t_1$  output of delay line 34. The output of this AND gate 46 is designated as A1. Similarly, the other AND gates 46 have an input from the W flip-flop 30, and inputs from the  $t_3$ ,  $t_5$ ,  $t_7$ ,  $t_9$ ,  $t_{11}$  and  $t_{13}$  outputs of delay line 34 respectively. These outputs from gates 46 are referred to as outputs A1-A7.

In the operation of the circuitry of FIG. 4, when the return pulse occurs the W flip-flop is reset and the W output has a predetermined width dependent upon the station that was actuated. For example, referring to FIG. 3, if station II has been actuated, the W output width is 4 microseconds. The two AND gates 46 having the inputs  $t_1$ ,  $t_3$ , are enabled and generate corresponding pulses A1 and A2. The other outputs A3-A7 are inhibited because the W output is low at time  $t_5$  and thereafter. As the W output becomes wider, more A output pulses are sequentially generated.

The outputs A1-A7 are all coupled to OR gate 44. If, for example, only the A1 and A2 pulses were generated then only two pulses would be sequentially coupled by way of line 43 to counter 42. These two pulses would increment counter 42 to a count of two ( $\bar{X}$ , Y,  $\bar{Z}$ .)

In accordance with the foregoing example, the output of counter 42 is decoded by logic 50 which comprises a number (six) of AND gates 52. These gates 52 each have three inputs connected in a conventional style from counter 42 to decode the output of counter 42. Each gate 52 also receives an enabling E input. If a count of two were registered by counter 42 the X output stage would be a ZERO, the Y output stage would be a ONE, and the Z output stage would be a ZERO. Thus, when the E pulse occurred, the gate 52 having the F2 output would be enabled. Because the counter can assume only one state at a time, none of the other F1, F3-F6 outputs could be high. If the return pulse occurred at a later time, one of the other F3-F6 outputs could be high instead of the F2 output.

FIG. 4 also shows indicator flip-flop unit 60 which comprises a series of six indicator flip-flops labeled as flip-flops G1-G6. These flip-flops correspond to the six stations I-VI. The outputs F1-F6 connect to the set inputs of the flip-flops G1-G6. The reset input to each of these flip-flops is activated by the P pulse. The outputs of these G1-G6 flip-flops each couple to indicator lights L1-L6, respectively. Thus, when the F2 output goes high, for example, the G2 flip-flop gets set and the L2 indicator light illuminates indicating that it was station II that created the impedance mismatch causing a return pulse that reset the W flip-flop at the 4 microsecond interval.

Referring again to FIG. 1B, there is shown a number of different resistors R1-R4 that are capable of causing different amplitude return pulses. In the embodiment of FIGS. 2-4, it is

obvious that the amplitude of the return pulse has not been specifically detected, only the time of occurrence of the pulse. In the embodiment discussed with reference to FIGS. 5 and 6, the different positions of switch 26 may cause different amplitude return pulses. The switch 26 could be used to designate different distress conditions, such as an "out of gas" condition, or an "accident" condition.

Referring now to FIG. 5, there are six flip-flops which are designated as flip-flops W1-W6. In this embodiment, these six flip-flops essentially replace the width flip-flop 30 of FIG. 2, and provide the capability of detecting concurrent calls from all six stations. In the disclosed embodiment, a time sharing technique is used wherein each of the flip-flops W1-W6 is sequentially monitored.

The set (S) inputs of each of these flip-flops W1-W6 is coupled from the P output of generator 12. The reset (R) inputs to each of these flip-flops W1-W6 is coupled from logic 70 which controls the resetting of each flip-flop in sequence. The resetting is dependent upon the occurrence of a reflected pulse and a condition where the previous W flip-flop has been just previously reset.

Logic 70 comprises OR gates 61-66 each of which has an output that couples to the reset (R) input of flip-flops W1-W6, respectively. One of the inputs to each of these OR gates 61-66 is the E input, which is generated from delay line 34' and may be identical to that shown in FIG. 2. The E input is the reset signal for logic 70. The other input to the OR gates 62-66 couple from the output of AND gates 72-76, respectively. The second input to OR gate 61 is the R input which when it occurs is coupled from cable 20. The AND gates 72-76 each have an R input and an input coupled by way of a delay circuit from the negation output of the previous W flip-flop. For example, AND gate 73 has an R input and an input via a delay circuit from the W2 negation output (W2). The outputs of OR gates 72-76 are referred to as the R<sub>0</sub>-R<sub>7</sub> outputs, respectively. The R input to gate 61 is referred to as the R<sub>0</sub> input.

In the operation of the circuitry of FIG. 5, the R<sub>0</sub> output can only go high (true) when the W1 flip-flop has been set and subsequently reset. The resetting of W1 flip-flop occurs by the first return pulse. By the time the second return pulse occurs, the W1 output is high and gate 72 only is enabled. The delay circuit is provided at the input to each of these AND gates 72-76 to insure that these gates are not prematurely enabled. If six return pulses are received from all six stations, the gates 72-76 are enabled in sequence and the flip-flops W1-W6 would be set and reset, in sequence, by return pulses.

Referring still to FIG. 5, there is shown an interval timer 78 which may be of conventional design, and is adapted, in the disclosed embodiment, to have six outputs labeled T1-T6. In one embodiment these outputs were high (true) for a period of five seconds and the total time lapse for all six intervals was thus thirty seconds. The T1-T6 outputs from interval timer 78 are shown coupled to interval logic 80. Interval logic 80 comprises AND gates 81-86 which have inputs T1-T6 coupled thereto, respectively. The gates 81-86 are thus enabled in sequence, with only one gate being enabled at a time and for a duration of five seconds. The second input to each of these gates 81-86 are coupled from the W1-W6 flip-flops, respectively, of the associated W1-W6 flip-flops. Thus, during interval T1, the W1 flip-flop is monitored. With this type of arrangement, if only one return pulse is being received, and thus only the W1 flip-flop is set. Gate 81 will have two high inputs and OR gate 88 will be enabled for the duration of the W1 pulse. The other AND gates 82-86 will be enabled during intervals T2-T6 respectively, but if only one return pulse is sensed the outputs of gates 82-86 remain high (are non-information bearing) during the time a return pulse would be expected.

In FIG. 5, there is shown a delay line 34' and a counter and decoder logic 40'. The P pulse from the pulse generator (see FIG. 1) is coupled to delay line 34', and the output of delay line 34 is coupled to counter and decoder logic 40'. Logic 40' 75

also has an input W which is coupled from the output of OR gate 88. Both delay line 34' and logic 40' may be identical in design to the embodiment shown in FIG. 4. Also, the position indicator flip-flops 60' may be identical to flip-flops 60 shown in FIG. 4.

With the embodiment of FIG. 5, in addition to providing an indication of the position of a selected station by means of flip-flops 60', the condition of the switch setting at each station may be monitored by amplitude detection means. Thus, the embodiment of FIG. 5 includes amplitude detector 90 which senses the amplitude of return pulses. The output of detector 90 couples to switch setting logic 110 which also has inputs from the indicator flip-flops 60'. The outputs of switch setting logic 110 couple to condition indicator flip-flops 130 which also have an input from the P output of generator 12.

Referring now to FIG. 6, in particular, there is shown amplitude detector 90, switch setting logic 110, and condition indicator flip-flops 130. To simplify the discussion of this embodiment, it is assumed that the return pulses are integer multiple of a basic amplitude level. In FIG. 6, these levels are shown as levels J2-J10. For example, the J2 amplitude level could be ten millivolts, and each subsequent level could be also a multiple of the J2 amplitude. In the discussion of this embodiment, it is also assumed that the attenuation along the cable is equal to one-half amplitude change per station, or in other words, a ten millivolt attenuation is realized for a pulse traveling back and forth between adjacent stations.

In FIG. 6, the amplitude detector 90 comprises input logic 100. Logic 100 includes a plurality of AND gates 101-106 which each have an output coupled to OR gate 108. Logic 100 is used to steer the correct return pulse to the threshold discriminators 102. Each AND gate 101-106 has one input coupled from the outputs T1-T6, respectively, of interval timer 78. The R input to each of these AND gates 101-106 couples by way of a constant gain amplifier from the reflection inputs R<sub>0</sub>-R<sub>7</sub> threshold discriminators 102. For example, if the device is operating during time T<sub>2</sub> and an R<sub>0</sub> pulse is received, gate 102 is enabled and the R<sub>0</sub> pulse only is passed by way of OR gate 108 to the threshold discriminators 102.

The threshold discriminators 102 are adapted to sense the amplitude of the pulse from OR gate 108 and determine which of the plurality of separate discriminators comprising this discriminator group 102, is detecting the return pulse. Only one such discriminator should be activated as only one amplitude pulse at a time is received. The output of discriminators 102 couples to register 104 which may be a series of flip-flops one of which will be set corresponding to the threshold discriminator that was actuated. The resetting of register 104 occurs by way of a P pulse to the reset input. The outputs of register 104 are designated as outputs K1-K10. One of these K outputs should be high corresponding to the J amplitude that was reflected and detected by the detection electronics.

FIG. 6 also shows the switch setting logic 110. This logic 110 has inputs from output register 104 and also from the G flip-flops that comprise indicator flip-flops 60'. These G outputs to logic 110 may be the same as shown in FIG. 4 and are identically designated. The switch setting logic 110 comprises separate groups of AND gates 112, 114, 116 and 118. Each of these groups contain six AND gates.

The switch setting logic 110 determines which of four separate and distinct switch actuations took place at a selected station. The logic relies upon the determination firstly of which station has been actuated, and secondly what particular amplitude was detected from this station. For example, if an amplitude of K10 (corresponding to amplitude J10) were indicated in register 104 this could only mean that the first condition of station I is activated. However, a K7 output from register 104 may mean either that the fourth position of station I was selected or the first position of station IV etc. The logic 110 determines which of these conditions has occurred by first sensing the station that was activated. Thus, if station IV were actuated and the G4 flip-flop set, then logic 110 determines

that it is condition 1 and not condition 4 that is actuated at the switch located at station IV.

AND gates group 112 of logic 110, for example, includes six AND gates each having an output that couples to an OR gate. The output of the OR gate connects to the set input of flip-flop 122 which indicates the condition 1 of an actuated station. An indicator lamp 123 is coupled to the output of flip-flop 122 (Q1 flip-flop). The resetting of flip-flop 122 is by way of a P pulse. The logic and gates comprising group 112 indicate that flip-flop 122 is set when G1 is set (true) and a K7 amplitude pulse is received. The other inputs, namely G2 and K6; G3 and K5; G4 and K4; G5 and K3; G6 and K2 are the other input combinations that cause the setting of flip-flop 122. The other flip-flops shown in FIG. 6 have different input logic designed to provide for their setting under the appropriate conditions.

Thus, in the embodiment of FIGS. 5 and 6 indicator lights are provided for depicting (1) which station has been selected (switched on) by a motorist, and (2) to which position (condition) the selected station has been turned by the motorist. When the system is properly calibrated, no other visual displays, such as a cathode ray tube are necessary. Also, the display according to the invention can be monitored quickly and accurately even by an unskilled person.

Other changes in the illustrated embodiments of the invention are equally apparent to those skilled in the art. It is therefore not intended that the invention be limited to the precise structures here illustrated and described, but rather that the invention be defined by the appended claims and that within their scope be included those structures which do not materially depart from the invention.

What is claimed is:

1. A signaling system including an electrically conductive cable having a characteristic impedance comprising,  
a plurality of switching means coupled to said cable at predetermined intervals therealong,  
means coupled to said cable and remote from said switching means for transmitting an electrical pulse along said cable,  
each said switching means including means capable of varying the impedance at said switching means to thereby cause at least part of said transmitted pulse to be reflected when at least one of said switching means is actuated,  
means coupled to said cable for sensing said transmitted pulse and said reflected pulse from at least one of said switching means to thereby provide a signal which is a function of the time difference between the transmitted and reflected pulses,  
and means responsive to said means for sensing for storing an indication of said actuated switching means of said plurality of switching means,  
said means for sensing comprises bistable means responsive to said transmitted pulse to establish a first state of said bistable means and responsive to said reflected pulse to establish a second state of said bistable means,  
said bistable means remaining in said first state for a time duration indicative of the occurrence of said reflected pulse and thereby indicative of the position of the actuated switching means.

2. A signaling system as set forth in claim 1 wherein said means for sensing includes a plurality of bistable means each

having an indicator means associated therewith at least one of which is energized when one of the switching means is activated, means for detecting the amplitude of said reflected pulse, and a plurality of condition bistable means responsive to both said means for detecting the amplitude of said reflected pulse and said plurality of bistable means, each said condition bistable means having an indicator means associated therewith at least one of which is energized when one of the switching means is activated, each said switching means having a plurality of different impedance positions and at least one of said indicator means associated with said condition bistable means being energized thereby indicating the position selected of said actuated switching means.

3. A signaling system as set forth in claim 1 wherein said means for sensing further comprises a clock and decoder logic, said decoder logic including a plurality of AND gates each responsive to both an output of said clock and the state of said bistable means for enabling at least one of said AND gates, the total number of said gates being enabled indicative of the position of the actuated switching means.

4. A signaling system as set forth in claim 3 wherein said means for sensing further comprises counter means having a count input coupled from the output of each AND gate and adapted to count the number of enabled AND gates.

5. A signaling system as set forth in claim 4 wherein said means for sensing further comprises counter decoder means coupled to the output of said counter means for selectively decoding the count in said counter means after said counter means has finished counting.

6. A signaling system as set forth in claim 1 wherein said means for storing comprises a plurality of bistable circuits each having an indicator light coupled to an output thereof.

7. A signaling system as set forth in claim 1 wherein said means for sensing comprises a plurality of bistable means each responsive to said transmitted pulse to establish a first state of said bistable means and responsive to said reflected pulse to establish a second state of said bistable means,

said bistable means remaining in said first state for a time duration indicative of the occurrence of said reflected pulse and thereby indicative of the position of the actuated switching means,  
and means for detecting the amplitude of said reflected pulse.

8. A signaling system as set forth in claim 7 comprising an interval timer having sequential time outputs and a plurality of timer logic gates, responsive to both said interval timer outputs and said plurality of bistable means for sequentially sensing the output of each of said plurality of bistable means.

9. A signaling system as set forth in claim 7 comprising a register coupled from said amplitude detection means for storing a bistable indication of the amplitude of said reflected pulse.

10. A signaling system as set forth in claim 9 comprising a plurality of condition bistable circuits responsive to both said register and the condition of said means for storing an indication of said actuated switching means for sequentially causing one of said condition bistable circuits to assume a stored state indicative of the position selected of said actuated switching means.

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