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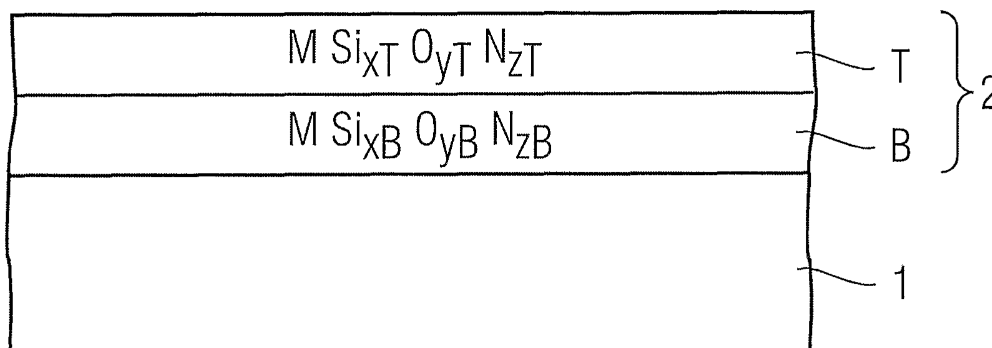
(54) Title: HIGH-K DIELECTRIC FILM, METHOD OF FORMING THE SAME AND RELATED SEMICONDUCTOR DEVICE



(57) Abstract: A high-k dielectric film, a method of forming the same and related semiconductor device are provided, wherein a bottom layer (B) of metal -silicon-oxynitride having a first nitrogen content (zB) and a first silicon content (xB), and a top layer (T) of metal -silicon-oxynitride having a second nitrogen content (zT) and a second silicon content (xT) are formed in such a way that the second nitrogen content (zT) is higher than the first nitrogen content (zB) and the second silicon content (xT) is higher than the first silicon content (xB).Thus, a dielectric film (2) with excellent leakage characteristics and a very high dielectric constant is formed.

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Description

High-k dielectric film, method of forming the same and related semiconductor device

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The present invention relates to a high-k dielectric film, a method of forming the same and related semiconductor devices, and in particular to high-k dielectric films related to a gate dielectric for field effect semiconductor devices or a
10 capacitor dielectric for trench capacitors in integrated circuits.

For forming semiconductor devices like CMOS devices (Complementary Metal Oxide Semiconductor), MOSFET devices (Metal Ox-
15 ide Semiconductor Field Effect Transistor) or high memory devices such as DRAMs (Dynamic Random Access Memories), it is often necessary to form a thin, high dielectric constant (high-k) film onto a substrate, such as a silicon wafer. A variety of techniques has been developed to form such thin
20 films on a semiconductor wafer.

In the past, gate dielectric layers have been formed using silicon dioxide. The scaling down of the above described devices, however, has increased the demand for gate dielec-
25 trics with a higher dielectric constant than silicon dioxide. This is necessary to reach ultra thin oxide equivalent thicknesses (EOT, Equivalent Oxide Thickness) without compromising gate leakage current.

30 In detail, as semiconductor devices have scaled to smaller dimensions, effective gate dielectric thickness has gotten thinner. The continued scaling of conventional gate dielectrics, such as SiO_2 and SiO_xN_y, has almost reached the fundamental limits of very high gate leakage current, due to di-
35 rect tunneling, which is not acceptable in a scaled device requirement of a low leakage current. In order to suppress the high leakage current, several high-k films of transition

metal oxide and silicate, such as HfO_2, ZrO_2, Hf-aluminate, Zr-aluminate, Zr-silicate, Hf-silicate and a lanthanide oxide like La_2O_3, Pr_2O_3, and Gd_2O_3, have been studied in replacement of SiO_2 and SiO_xN_y.

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However, these conventional materials have turned out to show a plurality of disadvantages. According to S. OHMI, et al., "Rare earth metal oxide gate thin films prepared by E-beam deposition", International Workshop on Gate Insulator 2001,
10 Tokyo, Japan, it is known that ZrO_2 or HfO_2 has shown micro crystal formation, resulting in high leakage current.

Furthermore, from J. H. LEE, et al., "Poly-Si gate CMOSFETs with HfO_2-Al_2O_3 laminate gate dielectric for low power appli-
15 cations", Tech. Dig. VLSI, page 84, 2002, it is known that HfO_2-Al_2O_3 laminate or Hf-aluminate have serious mobility degradation due to fixed charges in the high-k dielectric film.

Moreover, TAKESHI, YAMAGUCHI, et al., "Additional scattering
20 effects for mobility degradation in Hf-silicate gate MISFETs" Tech. Dig. IEDM 2002 reports that in case of Zr-silicate or Hf-silicate, phase separation of the film into HfO_2 and SiO_2 regions by the high temperature anneal induces also mobility degradation.

25

For lanthanide oxides, leakage current results have indicated that lanthanide oxides may be possible candidates of future dielectrics. However, according to H. IWAI, et al., "Advanced gate dielectric materials for Sub-100nm CMOS", Tech. Dig.
30 IEDM 2002, it is reported that these lanthanide oxides also form interfacial layers on Si substrates after subsequent thermal annealing, which may indicate thermal instability of these lanthanide oxides.

35 Moreover, an impurity penetration such as boron penetration from e.g. a gate layer to a Si substrate is a further problem to be solved by these high-k dielectric films. Even though

nitrogen incorporation on $HfSi_xO_y$ has been known to suppress such a e.g. boron penetration and improve thermal stability, it was also reported that the very high Si content of Si/[Si+Hf] ratio of over 80 % in $HfSi_xO_yN_z$ is required to prevent flat band voltage shift, resulting in seriously reducing dielectric constant of the film even with a high nitrogen content of 30 atomic percent (see M. KOYAMA, et al. "Effects of nitrogen in HfSiON gate dielectric on the electrical and thermal characteristics", Tech. Dig. IEDM 2002, 34-1). This low-k dielectric film of the very high Si content $HfSi_xO_yN_z$ is the almost same conventional SiO_xN_y in terms of dielectric constant and is not meaningful any more in view of replacement of the SiO_xN_y. Other technical problems of the formation of respective films on Si substrate are that a high nitrogen concentration at the interface between the dielectric layer and the Si substrate can be induced by subsequent high thermal annealing to degrade mobility.

It is, therefore, a need to provide an improved high-k dielectric film, a method of forming the same and related semiconductor devices.

In accordance with the present invention, a high-k dielectric film for a semiconductor device being formed on a substrate comprises at least a bottom layer of metal-silicon-oxynitride having a first nitrogen content and a first silicon content, and a top layer of metal-silicon-oxynitride having a second nitrogen content and a second silicon content, wherein said second nitrogen content of the top layer is higher than said first nitrogen content of the bottom layer and said second silicon content of the top layer is higher than said first silicon content of the bottom layer.

According to one embodiment, the high-k dielectric film constitutes a multilayer stack comprising at least one middle layer of metal-silicon-oxynitride being formed between said bottom layer and said top layer having a further nitrogen

content and a further silicon content wherein the respective further nitrogen and silicon contents are between said respective first and second nitrogen and silicon contents.

5 According to a preferred embodiment of the present invention, a thickness of the top layer is equal to or lower than the sum of thicknesses of the remaining layers in the high-k dielectric film.

10 The method of forming a high-k dielectric film comprises the steps of forming a bottom layer of metal-silicon-oxynitride having a first nitrogen content and a first silicon content on a substrate, and forming a top layer of metal-silicon-oxynitride having a second nitrogen content and a second
15 silicon content, wherein said second nitrogen content is higher than said first nitrogen content and said second silicon content is higher than said first silicon content of the respective layers.

20 In order to further improve a mobility particularly when used as a gate dielectric in field effect transistors, the method further includes the step of forming a substrate interface layer of silicon-oxide on the substrate before forming the bottom layer.

25

Further, at least one middle layer of metal-silicon-oxynitride having a further nitrogen content and a further silicon content is formed on the bottom layer, wherein the respective further nitrogen content and the further silicon content is
30 higher than that of the preceding layer.

In an alternative embodiment, the method of forming a high-k dielectric film comprises the steps of forming a pre-bottom layer of metal-silicon-oxide having a first silicon content
35 on a substrate, forming a pre-top layer of metal-silicon-oxide having a second silicon content, wherein the second silicon content is higher than the first silicon content, and

performing N_2 plasma treatment to convert said pre-bottom layer to a metal-silicon-oxynitride bottom layer having a first nitrogen content and said pre-top layer to a metal-silicon-oxynitride top layer having a second nitrogen content, wherein said second nitrogen content is higher than said first nitrogen content.

Also in this alternative embodiment at least one pre-middle layer of metal-silicon-oxide having a further silicon content is formed, wherein the respective further silicon content is higher than that of the preceding layer, and wherein during the N_2 plasma treatment at least one pre-middle layer is converted to at least one metal-silicon-oxynitride middle layer having a further nitrogen content, wherein the respective further nitrogen content is higher than that of the preceding layer.

The objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

Figures 1A and 1B are partial cross-sectional views showing essential steps for producing a high-k dielectric film according to a first embodiment;

Figure 2 is a partial cross-sectional view of the high-k dielectric film according to a second embodiment;

Figures 3A to 3D are partial cross-sectional views showing essential steps for producing a high-k dielectric film according to a third embodiment;

Figure 4 is a partial cross-sectional view of a field effect semiconductor device using the high-k dielectric film; and

Figure 5 is a partial cross-sectional view of a trench capacitor using the high-k dielectric film.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed. On the contrary, the intention is to cover all modification, equivalents and alternatives falling within the spirit and scope of the present invention.

Figures 1A and 1B show partial cross-sections illustrating essential steps for producing a high-k dielectric film according to a first embodiment of the present invention.

According to Figure 1A a monocrystalline Si substrate 1 is used as semiconductor substrate, on the surface of which a bottom layer B of metal-silicon-oxynitride ($MSi_{xB}O_{yB}N_{zB}$) is formed by layer deposition methods.

According to Figure 1B on the surface of the bottom layer B a top layer T is formed by the same metal-silicon-oxynitride, however, having different silicon content and nitrogen content. In detail, the deposited top layer T constitutes $MSi_{xT}O_{yT}N_{zT}$ having a second nitrogen content zT and a second silicon content xT. The first and second nitrogen contents of the bottom and top layer B and T as well as the first and second silicon contents xB and xT are selected in such a way that the second nitrogen content zT of the top layer T is higher than the first nitrogen content zB of the bottom layer and the second silicon content xT of the top layer T is higher than the first silicon content xB of the bottom layer.

The indices x, y and z or xB, yB and zB or xT, yT and zT in the $MSi_xO_yN_z$ layers are real positive values indicating atomic percentage in a molecular. Nitrogen atomic percentage in respective layer is calculated by $(z/(1+x+y+z))\times 100$. Usually,

Si and M (metal) concentrations are presented by $(x/(1+x)) \times 100$ and $(1/(1+x)) \times 100$, respectively.

Thus, the shown bilayer stack according to Figure 1B constitutes a new high-k dielectric film 2 having improved characteristics. In detail, the high-nitrogen-content top layer T of the bilayer stack plays a key role to effectively prevent diffusion of e.g. boron from a boron-doped poly-Si electrode (not shown) into the field effect device channel, whereas the low-nitrogen-content bottom layer B is helpful against mobility degradation within this channel and/or the substrate 1. Moreover, since a decrease of Si content in metal-silicon-oxynitrides is related to an increase of the metal content and, in turn, an increase of the dielectric constant the bilayer stack according to the first embodiment provides a higher dielectric constant than the prior art of the similar high-Si-content metal-silicon-oxynitride. Thus, it is possible to further scale down an effective oxide thickness (EOT), while leakage particularly caused by direct tunneling is prohibited.

According to the present invention, Si and N concentrations in the top layer T need to be higher than those in the bottom layer B, e.g. $xT > xB$, $zT > zB$. A ratio of N and Si in the top layer T with respect to the bottom layer B depends further on what metal-silicon-oxides are considered. In case the metal M in the metal-silicon-oxynitride layer is Hf, which is $HfSi_xO_yN_z$, the Si/(Hf+Si) ratio of $HfSi_xO_yN_z$ needs to be in the range of 70 % to 95 % with N concentration of as high as 30 atomic percentage. Thus, for a fixed Si and N concentration in the top layer T using Hf as metal, N and Si contents of the bottom layer B need to be lower than those of the top layer T, with N atomic percentage in the range from 15 % to 25 % and a Si/(Hf+Si) ratio in the range from 20 % to 60 %.

Concerning the thickness of the different layers, it is noted that the top layer T should have a lower thickness than the

thickness of the sum of the other layers within the high-k dielectric film 2 or the same. That is, the top layer T according to the bilayer structure of the first embodiment should be thinner or equal to the bottom layer B.

After formation of the high-k dielectric film 2, an anneal process (at a temperature of over 600°C in N_2 or other gas) is helpful to densify the layer stack and to reduce defects in order to improve the quality of the high-k dielectric film 2 (particularly to improve the leakage current characteristics).

Figure 2 shows a partial cross-sectional view of the high-k dielectric film according to a second embodiment, wherein same reference numbers refer to same or corresponding layers and a repeated description of these layers is omitted.

According to the second embodiment, a substrate interface layer I is formed on the surface of the substrate 1 while the respective further layers of the high-k dielectric film 2 are formed on the surface of this substrate interface layer I. In case of a Si substrate 1 this substrate interface layer constitutes preferably a silicon oxide, which further increases the mobility within the substrate and reduces defects at the surface of the substrate 1.

Besides the shown bilayer $MSi_xO_yN_z$ stack according to the first and second embodiment having a bottom layer and a top layer of metal-silicon-oxynitride, also at least a further metal layer of metal-silicon-oxynitride could be formed between said bottom layer B and said top layer T having a further nitrogen content and a further silicon content, wherein a respective further nitrogen content and a further silicon content is between said first and second nitrogen and silicon contents of the bottom layer B and top layer T. In particular, the further nitrogen content and the further silicon content of a respectively formed middle layer is higher than

the respective nitrogen and silicon contents of a metal-silicon-oxynitride layer formed in a preceding step.

The thickness of the top layer T is again equal to or lower than the sum of thicknesses of the remaining layers in the high-k dielectric film or multilayer stack, i.e. the bottom layer and the further middle layers.

Concerning the preferred method to form the above-mentioned metal-silicon-oxynitride layers, physical vapor deposition (PVD) is one of the methods to deposit various $MSi_xO_yN_z$ layers. As one embodiment of this invention, co-sputtering of metal, such as Hf, Zr, La, Pr, Gd and other lanthanide metals, and silicon in an $Ar/N_2/O_2$ ambient is considered to form metal-silicon-oxynitride films. Nitrogen concentration and silicon concentration in these metal-silicon-oxynitrides can be controlled by N_2 flow and silicon sputtering rate. High nitrogen content metal-silicon-oxynitride with a small amount of silicon can be obtained using high-nitrogen flow during the co-sputtering of Si.

As one of the examples in the basic concept of this invention, a high nitrogen content and high silicon content metal-silicon-oxynitride at the top part of the high-k dielectric film 2 and a lower nitrogen content and a lower silicon content at the bottom part of the high-k dielectric film 2 can be formed to keep the interface of the high-k dielectric film 2 and (a not shown) poly-Si electrode formed usually on the top of the high-k dielectric film 2 thermally stable. Poly-Si electrode deposition usually is performed using SiH_4 or Si_2H_6 which may induce reduction of metal-O and metal-N bonds by hydrogen coming from SiH_4 or Si_2H_6, probably generating defects and, in turn, resulting in high leakage current. High nitrogen concentrations and high silicon concentrations in metal-silicon-oxynitride suppress reaction between hydrogen and the high-k dielectric film during a respective poly-Si deposition due to a number of Si-N and Si-O bonds in the

place of metal-O and metal-N bonds. Similar advantages result when using a metallic material instead of poly-Si as an electrode formed on the surface of the high-k dielectric film 2.

5 Thus, $ZrSi_xO_yN_z$, $HfSi_xO_yN_z$, $LaSi_xO_yN_z$, $PrSi_xO_yN_z$, $GdSi_xO_yN_z$, $DySi_xO_yN_z$, and other nitrogen incorporated lanthanide-silicates can be formed as high-k dielectric films.

Figures 3A to 3D show partial cross-sectional views illus-
10 trating essential steps for producing a high-k dielectric film according to a third embodiment of the present invention, wherein same reference numbers refer to same or corresponding layers as in Figures 1 and 2, and, therefore, a repeated description of these layers is omitted in the follow-
15 ing.

According to the third embodiment a triple layer stack is formed by an alternative method to provide the high-k dielectric film 2.

20

According to Figure 3A, again a substrate interface layer I is formed directly on the surface of the substrate 1 preferably by a thermal process. Thus, a SiO_2-substrate interface layer I is formed on the Si substrate 1. Then a pre-bottom
25 layer B1 of metal-silicon-oxide having a low first silicon content xB is formed preferably by deposition on the substrate interface layer I.

According to Figure 3B a pre-middle layer M1 of metal-
30 silicon-oxide having a further silicon content xM is deposited on the pre-bottom layer B1 having the first silicon content xB. Again, the further silicon content xM of the further layer or the pre-middle layer M1 is higher than that of the bottom layer B1 or (if a plurality of middle layers are to be
35 used) is higher than that of the preceding layer.

According to Figure 3C a pre-top layer T1 of metal-silicon-oxide having a second silicon content xT is formed on the at least one pre-middle layer M1. Again, the second silicon content xT of the pre-top layer T1 is higher than the that of the pre-middle layer M1 which is higher than that of the pre-bottom layer B1.

Furthermore, an N_2 plasma treatment is made to the metal-silicon-oxide layers forming SiN bond rather than metal-N bond so that, as Si content in the different layer is different, also nitrogen contents after N_2 plasma treatment is different, respectively.

In particular, it is known that $HfSi_xO_y$ can be formed by various deposition methods, such as MOCVD (Metal Organic Chemical Vapor Deposition), PVD (Physical Vapor Deposition) and ALD (Atomic Layer Deposition). In the case of MOCVD $HfSi_xO_y$, two precursors, $Hf[N(C_2H_5)_2]_4$ for Hf and $Si[N(CH_3)_2]_4$ for Si, flow into a reactor together with O_2 to deposit $HfSi_xO_y$. SiO_2 mole fraction in $HfSi_xO_y$ can be controlled by process parameters, such as temperature, pressure and both precursor flow rates, during the silicate deposition.

Increase of the temperature from 325°C to 650°C was found to increase SiO_2 mole fraction in $HfSi_xO_y$ from about 20 % to 65 %. Change of process pressure from 400Pa (3 Torr) to 1065 Pa (8 Torr) results in increasing SiO_2 mole fraction from 30 % to 45 %.

In the basic concept of this invention, the third embodiment of this invention uses MOCVD $HfSi_xO_y$ as sequence for depositing low SiO_2 content $HfSi_{xB}O_{yB}$ and high SiO_2 content $HfSi_{xT}O_{yT}$ are deposited at the bottom part and at the top part of the high-k dielectric film 2 and then followed by N_2 plasma treatment. After N_2 plasma nitration, the top layer T of the film 2 shows a high nitrogen content and the bottom layer B a low nitrogen content.

In consideration of MOCVD Zr silicate instead of MOCVD Hf silicate, precursors are requested to simply change to $Zr[N(C_2H_5)_2]_4$ and $Si[N(CH_3)_2]_4$ for Zr silicate.

5

This embodiment of the Hf or Zr silicon-oxynitride stack using MOCVD Hf silicate or Zr silicate can be extended to for MOCVD lanthanide silicates even though various lanthanide MOCVD processes are possible.

10

Thus, according to Figure 3D after performing N_2 plasma treatment, the pre-bottom layer B1, the pre-middle layer M1 and the pre-top layer T1 are converted to a respective metal-silicon-oxynitride bottom layer B, middle layer M and top

15 layer T.

Again, an annealing process after N_2 plasma treatment can be considered to release the damage of plasma on the high-k dielectric film 2, to densify the high-k dielectric film and to

20 reduce defects as well as impurities in the high-k film stack.

Figure 4 shows a partial cross-sectional view of a semiconductor device comprising a field effect transistor using the

25 high-k dielectric film as a gate dielectric.

According to Figure 4 a source region S, a drain region D and a channel region between the source and drain region are provided in a semiconductor substrate 1. The high-k dielectric

30 film 2, according to the present invention, is used as gate dielectric and formed on the channel region while a gate layer is formed on said gate dielectric 2. Furthermore, spacer SP at the side walls of the gate stack could be provided to form the source and drain regions S and D. While the

35 gate layer 3 preferably comprises a poly-Si, it could also constitute a metal gate, thereby improving the electrical characteristics of the semiconductor device.

Figure 5 shows a partial cross-sectional view of a semiconductor device wherein the high-k dielectric film is used as a capacitor dielectric.

According to Figure 5, in order to realize so-called trench capacitors e.g. in DRAM (Dynamic Random Access Memory) semiconductor devices, a deep trench or hole is provided within the silicon substrate 1. On the surface of the trench or hole the high-k dielectric film 2 is provided after forming a second electrode 5 in the substrate 1 in the vicinity of the lower part of the trench. A filling material 4 is used as a first electrode of the resulting capacitor which is usually highly doped poly-Si or a deposited metal.

Thus, the new high-k dielectric film essentially improves the electric characteristics of semiconductor devices thereby enabling further integration densities.

It will be appreciated to those skilled in the art having the benefit of this disclosure that this invention is believed to provide a high-k dielectric film, a method for forming the same as well as related semiconductor devices having an improved leakage current by reduced tunneling currents as well as improved diffusion barrier characteristics. Further modifications and alternative embodiments of various aspects of the invention will be apparent to those skilled in the art in view of this description.

Reference List

1	substrate
2	high-k dielectric film
3	gate layer
4	first electrode
5	second electrode
B	bottom layer

M middle layer
T top layer
B1 pre-bottom layer
M1 pre-middle layer
5 T1 pre-top layer
I substrate interface layer
S source region
D drain region
SP spacer

Claims

1. High-k dielectric film for a semiconductor device being formed on a substrate (1) and comprising at least:
5 a bottom layer (B) of metal-silicon-oxynitride having a first nitrogen content (zB) and a first silicon content (xB); and a top layer (T) of metal-silicon-oxynitride having a second nitrogen content (zT) and a second silicon content (xT), wherein
10 said second nitrogen content (zT) of the top layer (T) is higher than said first nitrogen content (zB) of the bottom layer (B) and
said second silicon content (xT) of the top layer (T) is higher than said first silicon content (xB) of the bottom
15 layer (B).

2. High-k dielectric film according to claim 1, characterized by
a substrate interface layer (I) of silicon-oxide being formed
20 between said substrate (1) and said bottom layer (B).

3. High-k dielectric film according to claim 1 or 2, characterized by
at least one middle layer (M) of metal-silicon-oxynitride be-
25 ing formed between said bottom layer (B) and said top layer (T) having a further nitrogen content (zM) and a further silicon content (xM), wherein said respective further nitrogen content (zM) and further silicon content (xM) is between said first and second nitrogen and silicon contents (zT, zB,
30 xT, xB).

4. High-k dielectric film according to any of claims 1 to 3, characterized in that
said bottom, middle and/or top layers consist of the same
35 metal-silicon-oxynitride.

5. High-k dielectric film according to any of claims 1 to 4, characterized in that
said metal-silicon-oxynitride is $ZrSi_xO_yN_z$, $HfSi_xO_yN_z$, $LaSi_xO_yN_z$, $PrSi_xO_yN_z$, $GdSi_xO_yN_z$ or $DySi_xO_yN_z$, wherein x, y and z are real positive values indicating atomic percent~~age~~ in a molecular.

6. High-k dielectric film according to any of claims 1 to 5, characterized in that
a thickness of the top layer (T) is equal to or lower than the sum of thicknesses of the remaining layers in the high-k dielectric film (2).

7. Semiconductor device comprising a field effect transistor with a source region (S), a drain region (D) and a channel region provided in a semiconductor substrate (1), a gate dielectric (2) formed on said channel region, and a gate layer (3) formed on said gate dielectric, wherein said gate dielectric (2) consists of a high-k dielectric film according to any of claims 1 to 6.

8. Semiconductor device comprising a trench capacitor with a first electrode (4), a capacitor dielectric (2) and a second electrode (5) formed in a semiconductor substrate (1), wherein said capacitor dielectric (2) consists of a high-k dielectric film according to any of claims 1 to 6.

9. Method of forming a high-k dielectric film comprising the steps:
a) forming a bottom layer (B) of metal-silicon-oxynitride having a first nitrogen content (zB) and a first silicon content (xB) on a substrate (1);
b) forming a top layer (T) of metal-silicon-oxynitride having a second nitrogen content (zB) and a second silicon content (xT), wherein

said second nitrogen content (zT) of the top layer (T) is higher than said first nitrogen content (zB) of the bottom layer (B) and
said second silicon content (xT) of the top layer (T) is
5 higher than said first silicon content (xB) of the bottom layer (B).

10. Method according to claim 9, characterized by the further step of
10 forming a substrate interface layer (I) of silicon-oxide on said substrate (1) before forming said bottom layer (B).

11. Method according to claim 9 or 10, characterized by the further step of
15 forming at least one middle layer (M) of metal-silicon-oxynitride having a further nitrogen content (zM) and further silicon content (xM) on said bottom layer (B), wherein a respective further nitrogen content (zM) and a further silicon content (xM) is higher than that of the preceding layer.
20

12. Method according to any of claims 9 to 11, characterized in that
said bottom, middle and/or top layers (B, M, T) are formed by co-sputtering of metal and silicon in $Ar/N_2/O_2$ ambient,
25 wherein nitrogen and silicon concentration are controlled by N_2 flow and Si sputtering rate.

13. Method of forming a high-k dielectric film comprising the steps of:
30 a) forming a pre-bottom layer (B1) of metal-silicon-oxide having a first silicon content (xB) on a substrate (1);
b) forming a pre-top layer (T1) of metal-silicon-oxide having a second silicon content (xT), wherein
said second silicon content (xT) of the pre-top layer (T1) is
35 higher than said first silicon content (xB) of the pre-bottom layer (B1); and
c) performing N2 plasma treatment to convert

said pre-bottom layer (B1) to a metal-silicon-oxynitride bottom layer (B) having a first nitrogen content (zB) and said pre-top layer (T1) to a metal-silicon-oxynitride top layer (T) having a second nitrogen content (zT), wherein said second nitrogen content (zT) of the top layer (T) is higher than said first nitrogen content (zB) of the bottom layer (B).

14. Method according to claim 12, characterized by the further step of
forming at least one pre-middle layer (M1) of metal-silicon-oxide having a further silicon content (xM), wherein a respective further silicon content (xM) is higher than that of the preceding layer and wherein in step c) during the N_2 plasma treatment said at least one pre-middle layer (M1) is converted to at least one metal-silicon-oxynitride middle layer (M) having a further nitrogen content (zM), wherein said respective further nitrogen content (zM) is higher than that of the preceding layer.

15. Method according to any of claims 12 or 13, characterized in that
said pre-bottom, pre-middle and/or pre-top layers (B1, M1, T1) are formed by MOCVD, PVD and/or ALD.

16. Method according to any of claims 12 to 14, characterized by the further step of
forming a substrate interface layer (I) of silicon oxide on said substrate (1) before forming said pre-bottom layer (B1) in step a).

17. Method according to any of claims 9 to 16, characterized by the further step of
performing an anneal step at least for said said bottom, middle and/or top layers (B, M, T).

18. Method according to any of claims 9 to 17, characterized in that
said metal-silicon-oxynitride is $ZrSi_xO_yN_z$, $HfSi_xO_yN_z$, La-$Si_xO_yN_z$, $PrSi_xO_yN_z$, $GdSi_xO_yN_z$ or $DySi_xO_yN_z$, wherein x, y and z
5 are real positive values indicating atomic percentage in a molecular.

FIG 1A

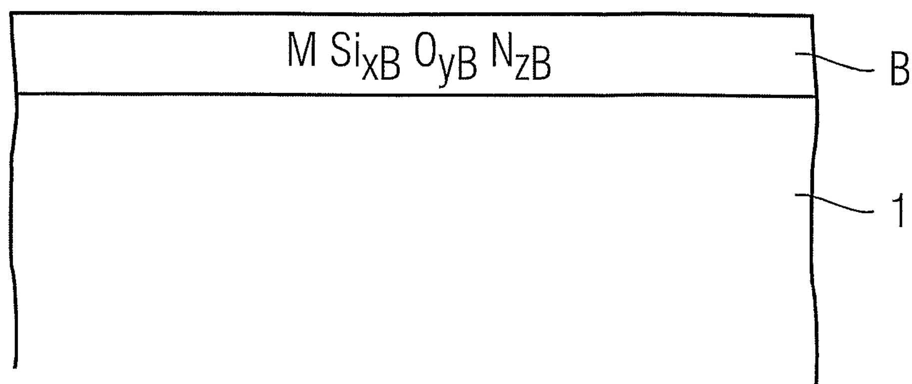


FIG 1B

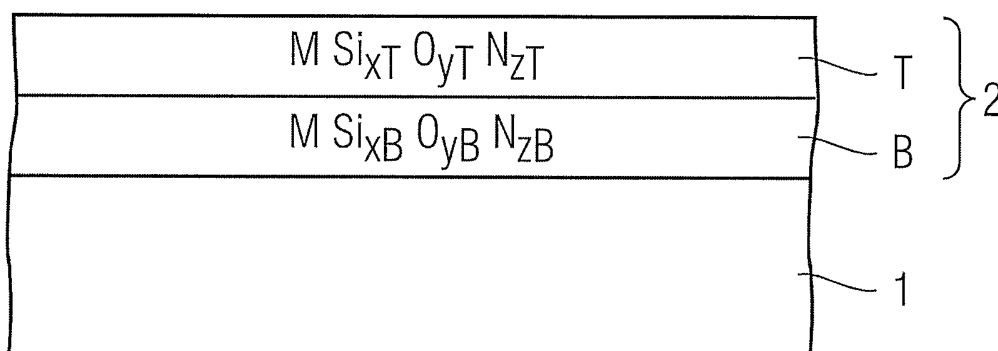
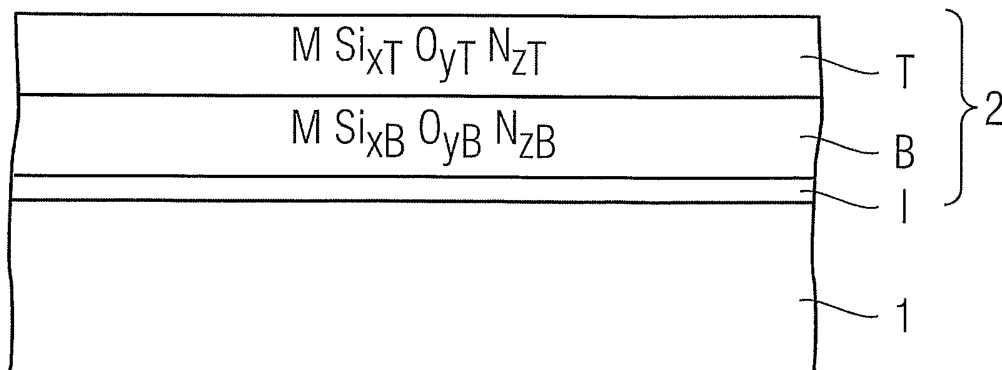


FIG 2



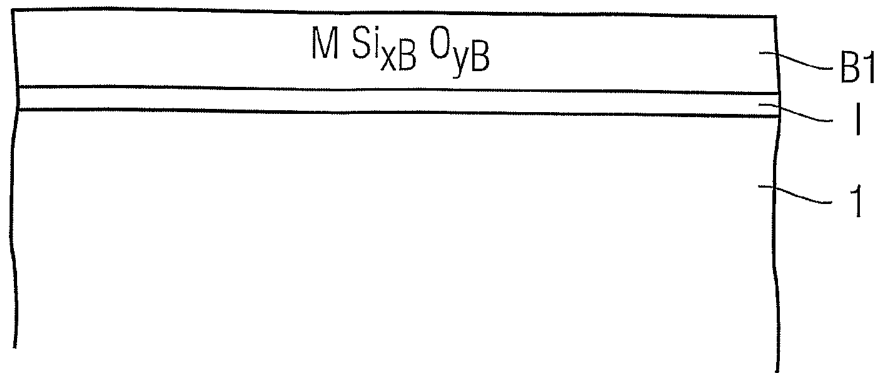


FIG 3A
M Si$_{xB}$ O$_{yB}$
B1
I
1

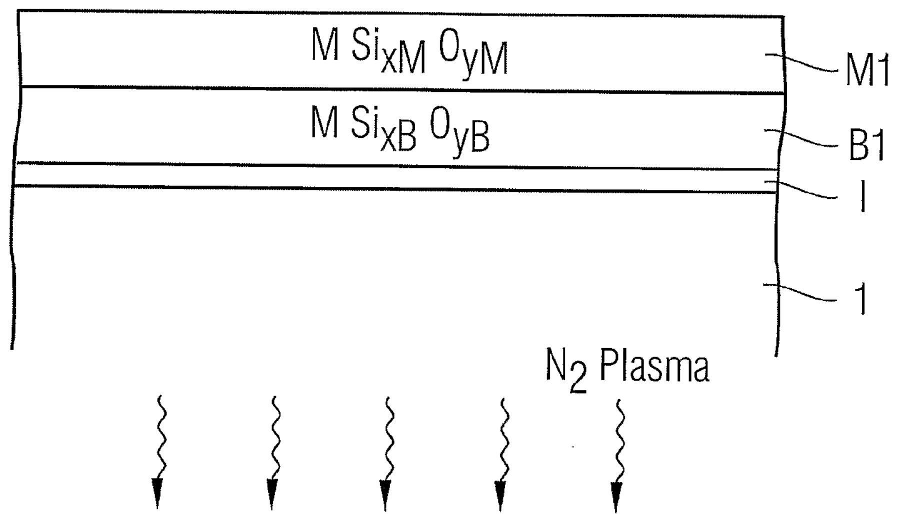


FIG 3B
M Si$_{xM}$ O$_{yM}$
M1
M Si$_{xB}$ O$_{yB}$
B1
I
1
N$_2$ Plasma

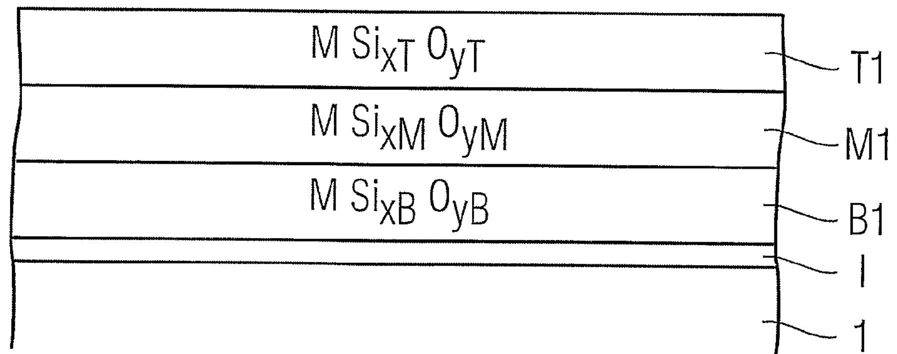


FIG 3C
M Si$_{xT}$ O$_{yT}$
T1
M Si$_{xM}$ O$_{yM}$
M1
M Si$_{xB}$ O$_{yB}$
B1
I
1

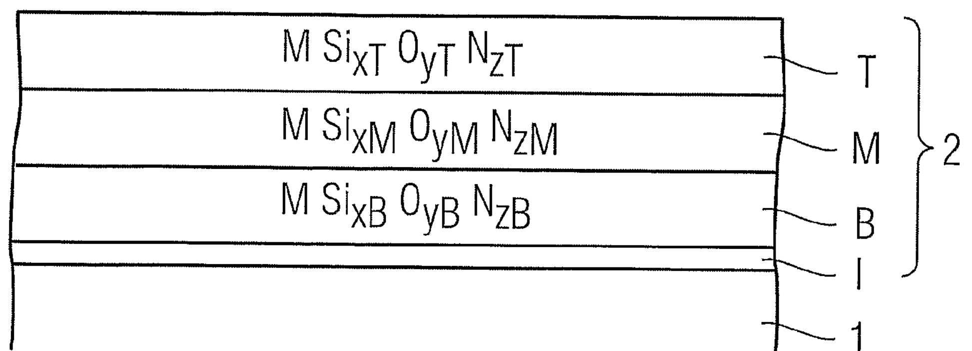


FIG 3D
M Si$_{xT}$ O$_{yT}$ N$_{zT}$
T
M Si$_{xM}$ O$_{yM}$ N$_{zM}$
M
M Si$_{xB}$ O$_{yB}$ N$_{zB}$
B
I
1
2

FIG 4

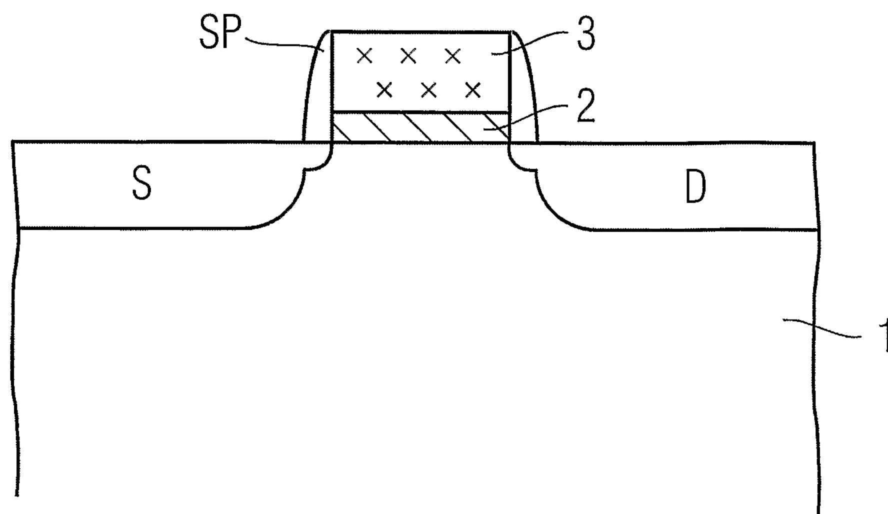
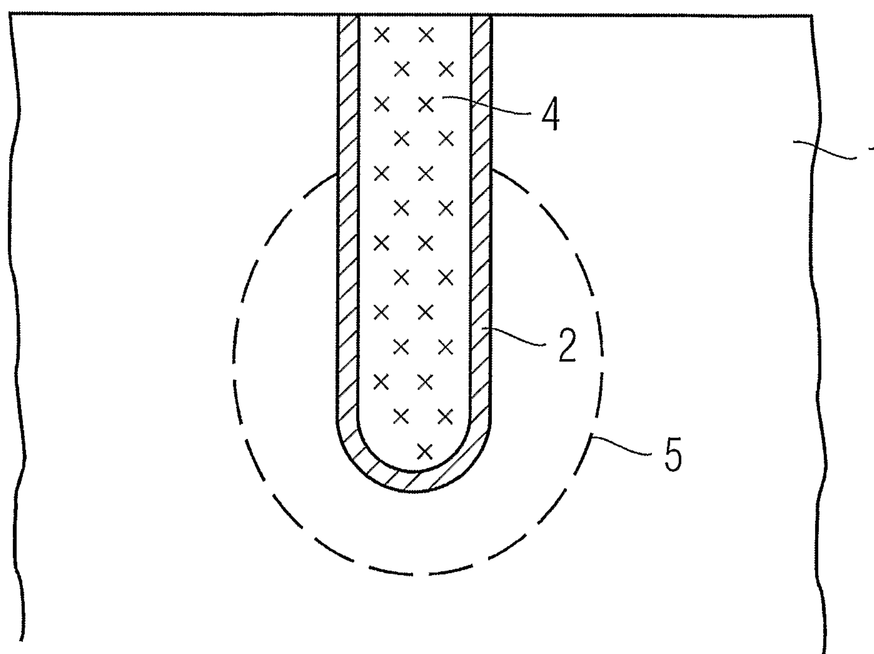


FIG 5



INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 03/50352

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/28 H01L29/51

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KOYAMA M ET AL: "Effects of nitrogen in HfSiON gate dielectric on the electrical and thermal characteristics" INTERNATIONAL ELECTRON DEVICES MEETING 2002. IEDM. TECHNICAL DIGEST. SAN FRANCISCO, CA, DEC. 8 - 11, 2002, NEW YORK, NY: IEEE, US, 8 December 2002 (2002-12-08), pages 849-852, XP010626172 ISBN: 0-7803-7462-2 cited in the application the whole document ---	1-18

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
2 March 2004	11/03/2004

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

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PCT/EP 03/50352

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	SHANWARE A ET AL: "Reliability evaluation of HfSiON gate dielectric film with 12.8 A/spl deg/ SiO2 equivalent thickness" INTERNATIONAL ELECTRON DEVICES MEETING 2001. IEDM. TECHNICAL DIGEST. WASHINGTON, DC, DEC. 2 - 5, 2001, NEW YORK, NY: IEEE, US, 2 December 2001 (2001-12-02), pages 661-664, XP010575093 ISBN: 0-7803-7050-3 the whole document ---	1-18
A	ROTONDARO A L P ET AL: "ADVANCED CMOS TRANSISTORS WITH A NOVEL HFSION GATE DIELECTRIC" 2002 SYMPOSIUM ON VLSI TECHNOLOGY. DIGEST OF TECHNICAL PAPERS. HONOLULU, JUNE 11 - 13, 2002, SYMPOSIUM ON VLSI TECHNOLOGY, NEW YORK, NY: IEEE, US, 11 June 2002 (2002-06-11), pages 148-149, XP001109853 ISBN: 0-7803-7312-X the whole document ---	1-18
A	VISOKAY M.R. ET AL: "Application of HfSiON as a gate dielectric material" APPLIED PHYSICS LETTERS, vol. 80, no. 17, 29 April 2002 (2002-04-29), pages 3183-3185, XP002264995 the whole document ---	1-18
A	EP 1 271 632 A (MATSUSHITA ELECTRIC IND CO LTD) 2 January 2003 (2003-01-02) the whole document ---	1-18
A	WO 01 66832 A (ASM INC) 13 September 2001 (2001-09-13) abstract ---	1-18
A	QUEVEDO-LOPEZ M. A. ET AL: "Effect of N incorporation on boron penetration from p+ polycrystalline-Si through HFSixOy films" APPLIED PHYSICS LETTERS, vol. 82, no. 26, 30 June 2003 (2003-06-30), pages 4669-4671, XP002264996 the whole document ---	1-18
A	US 6 291 866 B1 (WILK GLEN D ET AL) 18 September 2001 (2001-09-18) the whole document ---	1-18
	-/--	

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 03/50352

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 013 553 A (WILK GLEN D ET AL) 11 January 2000 (2000-01-11) the whole document	1-18

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP 03/50352

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
EP 1271632	A	02-01-2003	JP	2002314074	A	25-10-2002
			EP	1271632	A1	02-01-2003
			CN	1457508	T	19-11-2003
			WO	02063668	A1	15-08-2002
			TW	546734	B	11-08-2003
			US	2003092238	A1	15-05-2003
WO 0166832	A	13-09-2001	AU	4538801	A	17-09-2001
			EP	1266054	A2	18-12-2002
			JP	2003526218	T	02-09-2003
			TW	490739	B	11-06-2002
			WO	0166832	A2	13-09-2001
			US	2003032281	A1	13-02-2003
			US	2003129826	A1	10-07-2003
			US	2001041250	A1	15-11-2001
US 6291866	B1	18-09-2001	US	6013553	A	11-01-2000
			JP	2000058832	A	25-02-2000
			TW	402779	B	21-08-2000
			US	6020243	A	01-02-2000
			US	6291867	B1	18-09-2001
			US	2001024853	A1	27-09-2001
US 6013553	A	11-01-2000	JP	2000058832	A	25-02-2000
			US	6291866	B1	18-09-2001
			TW	402779	B	21-08-2000
			US	6020243	A	01-02-2000
			US	6291867	B1	18-09-2001
			US	2001024853	A1	27-09-2001