(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
2 July 2015 (02.07.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/099748 A1

(51) International Patent Classification:
G11C 11/4074 (2006.01) *G11C 16/30* (2006.01)

(21) International Application Number:
PCT/US2013/077884

(22) International Filing Date:
26 December 2013 (26.12.2013)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard MS:, RNB-4-150, Santa Clara, CA 95052 (US).

(72) Inventors: **HWANG, Seung**; 14555 NW Werner Lane, Portland, OR 97227 (US). **RUSU, Stefan**; 2200 Mission College Blvd., Santa Clara, CA 95054 (US). **KARL, Eric, A.**; 1001 NW Lovejoy Street, Unit 403, Portland, OR 97209 (US). **KOO, Kyung-hoae**; 11424 NW Permian Drive, Portland, OR 97229 (US).

(74) Agents: **MUGHAL, Usman, A.** et al.; Blakely, Sokoloff, Taylor & Zafman, 1279 Oakmead Parkway, Sunnyvale, CA 94085-4040 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

WO 2015/099748 A1

(54) Title: APPARATUS AND METHOD FOR REDUCING OPERATING SUPPLY VOLTAGE USING ADAPTIVE REGISTER FILE KEEPER

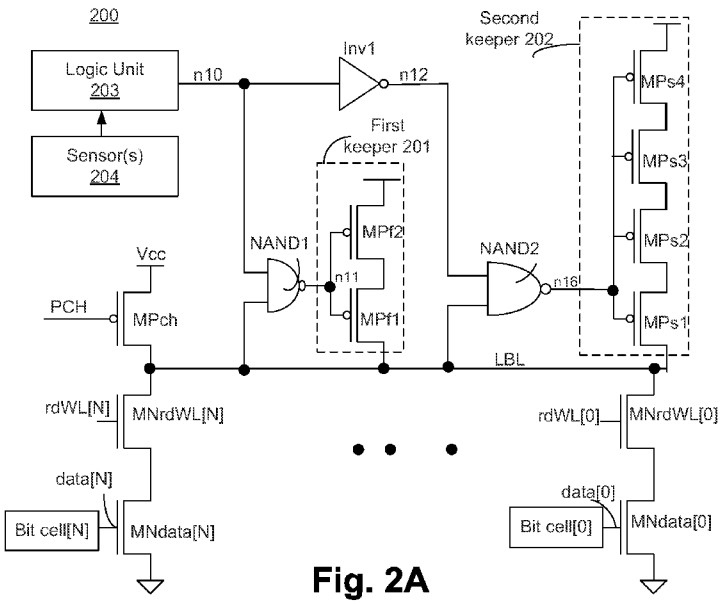

Fig. 2A

(57) Abstract: Described is an apparatus which comprises a bit line (BL); a first keeper of first strength coupled to the BL; a second keeper of second strength different from first strength, the second keeper coupled to BL; and a logic unit to enable one of first or second keepers according to one or more environmental conditions. Described is an apparatus which comprises: BL, a keeper coupled to the BL, the keeper having at least two transistor coupled in series; a delay unit to provide a first control signal for enabling or disabling one of the at least two transistors of the keeper; and a logic unit to bypass the delay unit and to provide a second control signal for enabling or disabling one of the at least two transistors of the keeper according to one or more environmental conditions.

APPARATUS AND METHOD FOR REDUCING OPERATING SUPPLY VOLTAGE USING ADAPTIVE REGISTER FILE KEEPER

BACKGROUND

[0001] Low power supply (Vcc) Register File (RF) and ROM (Read Only Memory) designs are used for low power processors and/or computers systems. However, circuit behavior of such circuits is non-linear in the low voltage region and can limit the minimum operating voltage (MinVCC) of the computer system.

[0002] RF/ROM MinVCC read circuitry is generally constrained by a delay failure mechanism and a noise/leakage failure mechanism. The delay and noise failure mechanisms that can limit MinVCC are anti-correlated i.e., using a weak or delayed keeper circuit on a read path to improve delay can degrade noise immunity whereas a strong keeper to deal with noise degrades the read delay constrained MinVCC.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The embodiments of the disclosure will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the disclosure, which, however, should not be taken to limit the disclosure to the specific embodiments, but are for explanation and understanding only.

[0004] **Fig. 1A** illustrates a traditional Register File (RF) with a keeper on the local bit line (LBL).

[0005] **Fig. 1B** illustrates a plot showing behavior of voltage on LBL node for **Fig. 1A** during evaluation and precharge phases for read '1' operation.

[0006] **Fig. 1C** illustrates an RF with ROMs (Read Only Memories).

[0007] **Fig. 2A** illustrates an apparatus having an RF/ROM with an adaptive keeper, according to one embodiment of the disclosure.

[0008] **Fig. 2B** illustrates a plot showing behavior of voltage on LBL node for **Fig. 2A** during evaluation and precharge phases for read '1' operation, according to one embodiment of the disclosure.

[0009] **Fig. 3A** illustrates an apparatus having an RF/ROM with logic to delay initiation of keeper operation, according to one embodiment of the disclosure.

[0010] **Fig. 3B** illustrates a plot showing discharge behavior of voltage on LBL node for **Fig. 3A** during read 0 evaluation phase, according to one embodiment of the disclosure.

[0011] **Fig. 3C** illustrates a plot showing droop behavior of voltage on LBL node for **Fig. 3A** during read 1 evaluation phase, according to one embodiment of the disclosure.

[0012] **Fig. 4A** illustrates an apparatus having an RF with logic to select one of adaptive keeper circuits of **Fig. 2A** or **Fig. 3A**, according to one embodiment of the disclosure.

[0013] **Fig. 4B** illustrates an apparatus having a ROM with logic to select one of adaptive keeper circuits of **Fig. 2A** or **Fig. 3A**, according to one embodiment of the disclosure.

[0014] **Fig. 5** illustrates a flowchart of a method to enable use of adaptive keeper circuits of **Fig. 2A** and/or **Fig. 3A**, according to one embodiment of the disclosure.

[0015] **Fig. 6** illustrates a processor with RF/ROM having adaptive keeper circuits of **Fig. 2A** and/or **Fig. 3A**, according to one embodiment of the disclosure.

[0016] **Fig. 7** is a smart device or a computer system or an SoC (System-on-Chip) with an RF/ROM having an adaptive keeper, according to one embodiment of the disclosure.

DETAILED DESCRIPTION

[0017] **Fig. 1A** illustrates a traditional Register File (RF) 100 with a keeper on the local bit line (LBL). In this example, RF 100 consists of 'N' bit-cells (where 'N' is an integer). Each bit-cell is a 8T bit-cell having an SRAM based 6T cell coupled to 2T discharge path, where 'T' refers to transistor.

[0018] For example, the bit-cell[N] includes six transistors (i.e., 6T) which are n-type transistors MN1, MN0, and n-type transistors of inverter inv1 and inv2; and p-type transistors of inverters inv1 and inv2. Inverters inv1 and inv2 form the cross-coupled memory unit. N-type transistors MN1 and MN0 are access transistors. Access transistor MN1 is coupled to BL (bit line) and node n1 while access transistor MN0 is coupled to BL# (i.e., an inverse of BL) and node n0. Gate

terminals of MN1 and MN0 are controlled by wrWL (i.e., write word line) signals. Transistors MNdata[N] and MNrdWL[N] are the other two transistors to form the 8T RF bit-cell.

[0019] Gate terminal of n-type MNdata[N] is coupled to node n0 (same as data[N]), source terminal of MNdata[N] is coupled to ground, and drain terminal of MNdata[N] is coupled to source terminal of MNrdWL[N]. Gate terminal of MNrdWL[N] is controlled by rdWL[N] (i.e., read word line). Drain terminal of MNrdWL[N] is coupled to local bit line (LBL) node. Likewise, each discharge path has a corresponding 6T SRAM bit-cell coupled to it. For example, discharge path with n-type transistors MNrdWL[0] (controllable by rdWL[0]) and MNdata[0] (controllable by data[0]) have a 6T SRAM cell that provides data[0].

[0020] RF also consists of precharge pull-up p-type device MPch which is controllable by PCH (precharge signal). MPch drain node is coupled to LBL node while source node is coupled to Vcc. A keeper, having transistors p-type MP1, MP2, and MP3 coupled in series, is coupled to node LBL. The keeper is turned ON or OFF by inverter inv3 which receives input from LBL.

[0021] As discussed above, RF/ROM MinVCC read circuitry is generally constrained by a delay failure mechanism and a noise/leakage failure mechanism. The delay and noise failure mechanisms that can limit MinVCC are anti-correlated i.e., using a weak or delayed keeper circuit on a read path to improve delay can degrade noise immunity whereas a strong keeper to deal with noise degrades the read delay constrained MinVCC.

[0022] Typically, to design an optimal keeper for both MinVCC limiters, the RF/ROM circuit is simulated at various process corners (i.e., fast and slow corners), and temperatures (i.e., cold, medium, and hot). Based on simulation results, a reliable keeper across all the possible cases is selected. In this current solution, keeper is biased to either improve delay or improve noise with a fuse option to mitigate the opposite problem (i.e., delay problem if biased to noise, and noise problem if biased to delay).

[0023] The strength of keeper devices MP1, MP2, and MP3 can be selectively adjusted by fuse options which statically program the keeper's strength per wafer, die, or processing core after testing. Testing and setting keeper strength

per die or core in HVM (high volume manufacturing), however, can increase manufacturing cost and may be prohibitive in many cases. Another issue with the setting static keeper is aging impact on p-type MP1, MP2, and MP3 devices of the keeper. PMOS device performance measured by Idsat or Vt (i.e., threshold voltage) is sharply degraded by NBTI (i.e., PMOS aging), up to several hundred milli-volt Vt increase, especially in the small devices which are typically used for implementing the keeper.

[0024] Turbo performance mode for processors, which results in the worst aging stress where both Vcc and temperature are high, is a technique for achieving high performance in power-constrained processors. But, unfortunately Turbo performance mode results in excessive NBTI/aging Vt increase. The PMOS aging/Vt increase can be manifested as a noise failure. Therefore mitigating aging induced PMOS degradation may be desirable for reliable RF/ROM design. Current RF and ROM designs use static fuse options for enabling a stronger keeper to mitigate aging effects.

[0025] The RF/ROM LBL of **Fig. 1A** is sustained by the keeper after MPch device is turned OFF (i.e., evaluation phase). If the voltage on LBL node is flipped to '0' by noise or high leakage, a false evaluation occurs which can cause a system functional failure. The common solution to this problem is to implement a stronger keeper even though it increases pull-down delay and contention during true '0' evaluation. When fabricated with fast/leaky material and operating at high temperature, the RF/ROM read circuit 100 is very susceptible to this noise failure and requires a strong keeper. With the conventional static keeper method, this strong keeper induces very slow discharge delay at low voltage and significantly increases performance-constrained MinVCC of the circuit 100 in the slow process material.

[0026] **Fig. 1B** illustrates a plot 120 showing behavior of voltage on LBL node for **Fig. 1A** during evaluation and precharge phases for read '1' operation. It is pointed out that those elements of **Fig. 1B** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0027] Here, x-axis is time and y-axis is voltage. The bold waveform is PCH which controls MPch. When PCH is low, LBL is precharged by MPch which is turned ON. When PCH is high, LBL is evaluated by one of the 'N' discharge paths. The dotted waveform is the voltage on node LBL. In this example, during evaluation phase, keeper is turned ON but it is not strong enough to maintain change on LBL node i.e., voltage on LBL node begins to decay. During precharge phase, MPch precharges LBL node back to Vcc level. Here, labels for signals and nodes are interchangeably used. For example, LBL is used to refer to LBL node or LBL signal depending on the context of the sentence.

[0028] **Fig. 1C** illustrates an RF 130 with ROMs (Read Only Memories). It is pointed out that those elements of **Fig. 1C** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. In **Fig. 1C**, third transistor in the stack (i.e., MNdata[N:0]) of **Fig. 1A** is replaced by a connection to VSS or VREF or a floating node to form ROM. The discharge path (e.g., transistors MNrdWL[0]-[N] and MNdata[0]-[N] can replaced with transistors 131 and/or 132. Transistor 131 is an n-type transistor controllable by WL and coupled to LBL node. The discharge path (e.g., transistors MNrdWL[0]-[N] and MNdata[0]-[N] can also be replaced with transistor 132. Transistor 132 is an n-type transistor controllable by WL and coupled to a supply (e.g., Vref) or left floating instead of being connected to ground.

[0029] RF circuit is increasingly used for the high speed dense memory applications. For example, RF circuit is used for core (e.g., Intel's x86® based processors) and graphics application like GT and display engines to boost the performance. ROM circuits are used extensively in the core, system agent, and in various SoC intellectual property (IP) blocks. As the device count sharply increases, the stringent requirement for low power and small die area is challenging. To lower RF MinVCC, save power, and mitigate aging effects, the embodiments use adaptive keepers. Here, adaptive keeper refers to dynamically varying keeper strength and/or adjusting delay to keeper control signal.

[0030] In the following description, numerous details are discussed to provide a more thorough explanation of embodiments of the present disclosure. It

will be apparent, however, to one skilled in the art, that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring embodiments of the present disclosure.

[0031] Note that in the corresponding drawings of the embodiments, signals are represented with lines. Some lines may be thicker, to indicate more constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. Such indications are not intended to be limiting. Rather, the lines are used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit or a logical unit. Any represented signal, as dictated by design needs or preferences, may actually comprise one or more signals that may travel in either direction and may be implemented with any suitable type of signal scheme.

[0032] Throughout the specification, and in the claims, the term "connected" means a direct electrical connection between the things that are connected, without any intermediary devices. The term "coupled" means either a direct electrical connection between the things that are connected or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function. The term "signal" means at least one current signal, voltage signal or data/clock signal. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0033] The term “scaling” generally refers to converting a design (schematic and layout) from one process technology to another process technology. The term “scaling” generally also refers to downsizing layout and devices within the same technology node. The terms “substantially,” “close,” “approximately,” “near,” “about,” generally refer to being within +/- 20% of a target value.

[0034] Unless otherwise specified the use of the ordinal adjectives “first,” “second,” and “third,” etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0035] For purposes of the embodiments, the transistors are metal oxide semiconductor (MOS) transistors, which include drain, source, gate, and bulk terminals. The transistors also include Tri-Gate and FinFET transistors. Source and drain terminals may be identical terminals and are interchangeably used herein. Those skilled in the art will appreciate that other transistors, for example, Bi-polar junction transistors—BJT PNP/NPN, BiCMOS, CMOS, eFET, etc., may be used without departing from the scope of the disclosure. The term "MN" indicates a n-type transistor (e.g., NMOS, NPN BJT, etc.) and the term "MP" indicates a p-type transistor (e.g., PMOS, PNP BJT, etc.).

[0036] The term "power state" or "power mode" generally refers to performance level of the processor or SoC (System-on-Chip). Power states may be defined by Advanced Configuration and Power Interface (ACPI) specification, Revision 5.0, Published November 23, 2011. However, the embodiments are not limited to ACPI power states. Other standards and non-standards defining power state may also be used.

[0037] **Fig. 2A** illustrates an apparatus 200 having RF with an adaptive keeper, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 2A** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. **Fig. 2A** is described with reference to **Fig. 1A**.

[0038] In one embodiment, apparatus 200 comprises a first keeper 201, second keeper 202, Logic Unit 203, Sensor(s) 204, logic gates (e.g., NAND1 and NAND2), precharge device MPch, and 'N' RF bit-cells. RF bit-cells are same as the 'N' RF bit-cells of **Fig. 1A**, and precharge device MPch is the same as the precharge device MPch of **Fig. 1A**.

[0039] Referring back to **Fig. 2A**, in one embodiment, first keeper 201 has a keeper strength which is stronger than the keeper strength of second keeper 202. In one embodiment, first keeper 201 comprises p-type transistors MPf1 and MPf2 coupled together in series such that drain terminal of MPf1 is coupled to LBL node and source terminal of MPf2 is coupled to power supply (Vcc). In embodiment, gate terminals of MPf2 and MPf1 are coupled together. In one embodiment, output of NAND1 gate drives gate terminals of MPf1 and MPf2. In one embodiment,

NAND1 gate is a two input logic gate, having first input coupled to LBL and second input coupled to node n10 (i.e., output of Logic Unit 203).

[0040] In one embodiment, second keeper 202 has weaker keeper strength than the keeper strength of first keeper 201. In one embodiment, second keeper 202 comprises p-type transistors MPs1, MPs2, MPs3, and MPs4 coupled together in series such that drain terminal of MPs1 is coupled to LBL node and source terminal of MPs4 is coupled to power supply (Vcc). While the embodiments of first keeper 201 and second keeper 202 illustrates two and four p-type devices coupled in series, respectively, any number of p-type devices can be used so long as first keeper 201 is stronger than second keeper 202.

[0041] In embodiment, gate terminals of MPs1, MPs2, MPs3, and MPs4 are coupled together. In one embodiment, output of NAND2 gate drives gate terminals of MPs1, MPs2, MPs3, and MPs4. In one embodiment, NAND2 gate is a two input logic gate, having first input coupled to LBL and second input coupled to node n12 (i.e., output of inverter inv1). Here, labels for signals and nodes are interchangeably used. For example, n12 is used to refer to signal n12 or node n12 depending on context of the sentence. In one embodiment, inverter inv1 receives signal n10 and generates signal n12, which is an inverted version of n10.

[0042] In one embodiment, one or more Sensors 204 sense one or more attributes of apparatus 200. For example, one or more Sensors 204 includes a temperature sensor to sense temperature of apparatus 200. In one embodiment, Logic Unit 203 compares the sensed temperature relating to a predetermined threshold (e.g., 50°C) and generates a signal n10 to enable or disable first or second keeper (201 and 202). In one embodiment, signal n10 can be set by a fuse signal to select one of the first or second keepers. For example, when the die having apparatus 200 is formed from slow process material, then second keeper 202 is enabled and first keeper 201 is disabled by a fuse signal.

[0043] **Fig. 2B** illustrates a plot 220 showing behavior of voltage on LBL node for **Fig. 2A** during read '1' evaluation and precharge phases, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 2B** having the same reference numbers (or names) as the elements of any other figure

can operate or function in any manner similar to that described, but are not limited to such. **Fig. 2B** is described with reference to **Fig. 2A**.

[0044] Here, x-axis is time and y-axis is voltage. The bold waveform is PCH and the dotted waveform is voltage on node LBL. In one embodiment, high phase of PCH is the Evaluation Phase in which voltage on node LBL is evaluated. In one embodiment, low phase of PCH is the precharge phase in which charge on LBL node is charged to substantially the level of Vcc. In one embodiment, during Evaluation Phase, depending on output of Sensor(s) 204, Logic Unit 203 selects one of first or second keeper (201 or 202). For example, for high temperatures (e.g., greater than 50F), first keeper 201 is enabled and second keeper 202 is disabled. For low temperatures (e.g., lower than 50°C), first keeper 201 is disabled and second keeper 202 is enabled.

[0045] In one embodiment, LBL is sustained by a keeper (either first keeper 201 or second keeper 202) after pre-charge device MPch is turned-off (i.e., during evaluation phase). If the voltage on LBL node is flipped to '0' by noise or high leakage, a false evaluation occurs which can cause a system functional failure. This failure scenario is mitigated by enabling one of the first or second keepers (201 and 202) depending on output of Sensor(s) 204. For example, first keeper 201 may be enabled to implement a stronger keeper even though it increases pull-down delay and contention during true '0' evaluation.

[0046] When apparatus 200 is fabricated with fast/leaky material and operates at high temperature, the RF/ROM read circuit is very susceptible to this noise failure and requires a strong keeper. With the conventional static keeper method discussed with reference to **Figs. 1A-B**, this strong keeper induces very slow discharge delay at low voltage and significantly increases performance-constrained MinVCC of the circuits in the slow material. The embodiment of **Fig. 2A** uses adaptive keeper which enables lowering of RF/ROM MinVCC by providing the optimum keeper strength such as strong keeper (i.e., first keeper 201) for noise at hot temperature (e.g., greater than 50°C) and weak keeper (i.e., second keeper 202) at cold temperature (e.g., less than 50°C).

[0047] **Fig. 3A** illustrates an apparatus 300 with an RF/ROM with logic to delay initiation of keeper operation, according to one embodiment of the disclosure.

It is pointed out that those elements of **Fig. 3A** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. **Fig. 3A** is described with reference to **Fig. 1A** and **Fig. 2A**.

[0048] In one embodiment, apparatus 300 comprises keeper 301, Delay Unit 302, Multiplexer (Mux) 303, Logic Unit 304, and Sensor(s) 204. In this embodiment, keeper 301 is coupled to LBL node and power supply. In one embodiment, keeper 301 is substantially the same as second keeper 202 of **Fig. 2A**.

[0049] Referring back to **Fig. 3A**, in one embodiment, gate terminal of MPs4 is controlled by signal ken which is either an output "dk" of Delay Unit 302 or input "Keeper_in" of Delay Unit 302. In one embodiment, output select of Logic Unit 304 determines whether ken is derived from "dk" or "Keeper_in." In one embodiment, Logic Unit 304 generates the select signal according to outputs of one or more Sensor(s) 204. In one embodiment, output of inverter inv1 is coupled to gate terminals of MPs1, MPs2, and MPs3. In one embodiment, Delay Unit 302 comprises a chain of delay stages coupled together in series. In one embodiment, number of delay stages in Delay Unit 302 is programmable by software or hardware (e.g., fuse).

[0050] In this embodiment, apparatus 300 tradeoffs the noise/leakage MinVCC with delay/contention MinVCC using the delayed keeper circuit formed from keeper 301, Delay Unit 302, Mux 303, Logic Unit 304, and Sensor(s) 204. In one embodiment, the delayed keeper circuit is operable to prevent read delay degradation on very slow silicon/process material without compromising on leakage/noise MinVCC under high temperature conditions. In one embodiment, "ken" signal can disable the entire stack of transistors in keeper 301 to prevent contention current between the p-type transistor stack and the read pull down n-type stack in the selected bit cell. Here, the read pull-down n-type stack is formed from any n-type stack of MNrdWL[N]-MNdata[N]. In one embodiment, after a delay through Delay Unit 302, the stack in keeper 301 can be enabled to avoid leakage related failures that could occur on a longer access period.

[0051] In one embodiment, Logic Unit 304 is a power control unit (PCU) which monitors one or more Sensor(s) 204 and controls many aspects of the

processor having the apparatus of the embodiments. A PCU may be a microcontroller which controls voltage, frequency, and power of the processor. In one embodiment, for systems without a PCU, a local thermal sensor may be added to generate "select" signal. In one embodiment, the local thermal sensor may be a small and simple thermal sensor which is able to detect whether the processor having the apparatus of the embodiments is the hot vs. cold. In one such embodiment, accuracy of the thermal sensors can be coarse.

[0052] In one embodiment, for a low leakage RF/ROM, "select" signal is set to '0' by Logic Unit 304 and "ken" is coupled to "dk." In this embodiment, the delayed 4-stack keeper is enabled. In one embodiment, LBL is floated during "delay" time in **Fig 3B** and it speeds up true evaluation, faster than static keeper. In low leakage RF/ROM, LBL floating around ¼*phase time in this example produces slight LBL droop as shown in **Fig. 3C** and does not cause a functional failure, flip to bit 0. In one embodiment, the adaptive RF/ROM keeper is enabled in the high leakage RF/ROM circuits. In one embodiment, Logic 304 selects "Keeper_in" at hot temperature and selects "dk" in cold temperature. In one embodiment, low cost thermal sensors can be sprinkled across the chip/processor to determine "select" signal. In such an embodiment, Logic 304 enables to take into account the expected temperature variation across the die.

[0053] In one embodiment, at low temperature, n10 signal is driven to '0' to turn-on the weak keeper (i.e., second keeper 202). In one embodiment, delay is improved at low Vcc and MinVCC is lowered. As the local temperature rises and enters into the hot region, (e.g., 50°C), the local thermal sensor triggers n10 signal to '1' to enable the strong keeper (i.e., first keeper 201). In this embodiment, noise immunity is enhanced by the strong keeper (i.e., first keeper 201) and noise MinVCC is improved.

[0054] In one embodiment, keeper 301 stack includes a single transistor in the stack coupled to power supply and LBL. That single transistor may have multiple transistors coupled in parallel to it, but the stack height is one. In one embodiment, the single transistor is controllable by logic gate (e.g., NAND gate) instead of inverter inv1 such that output of the logic gate is coupled to the gate terminal of the single transistor. In this embodiment, one input terminal of the logic

gate is coupled to LBL and the other input terminal of the logic gate is coupled to "ken."

[0055] **Table 1** illustrates the operation of the adaptive keeper and the MinVCC improvement, according to one embodiment. The measurements in **Table 1** correspond to Delay and Noise in mV. The Delay and Noise are shown for traditional keeper (e.g., of **Fig. 1A**) using two stack and four stack of p-type devices in its keeper. **Table 1** also shows type of keeper enabled for apparatus 200, and the associated MinVCC. The last row shows the improvement in MinVCC using the embodiments over traditional architecture of **Fig. 1A**.

Table 1: Adaptive Keeper setting and MinVCC at different temperatures

Temperature (°C)		**0**		**50**		**100**	
Measurement		**Delay (mV)**	**Noise (mV)**	**Delay (mV)**	**Noise (mV)**	**Delay (mV)**	**Noise (mV)**
Traditional Keeper	**Two Stack**	**720**	490	670	570	640	620
	Four Stack	580	570	540	660	480	**1000**
Embodiment (e.g., 200)	**Keeper Type**	**Second Keeper 202**		**First or Second Keeper (201 or 202)**		**First Keeper 201**	
	MinVCC	580		660		640	
	Improvement over traditional Keeper	140 (i.e., 720-580)		10 (i.e., 670-660)		360 (i.e., 1000-640)	

[0056] **Table 1** shows that without adaptive RF/ROM keeper, MinVCC of 2-stack and 4-stack is limited by 720mV/delay and 1000mV/noise, respectively. With the introduction of adaptive RF/ROM keeper of apparatus 200, the highest MinVCC across the full temperature range is 660 mV in this example, so the overall gain is 60mV (720-660). The actual MinVCC gain at each temperature can be more than overall gain, for example, 360mV (i.e., 1000-640) at hot temperature and 140mV (i.e., 720-580) at cold temperature.

[0057] **Fig. 3B** illustrates a plot 320 showing discharge behavior of voltage on LBL node for **Fig. 3A** during read 0 evaluation phase, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 3B**

having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0058] Here, x-axis is time and y-axis is voltage. Plot 320 shows waveforms PCH, LBL (using static keeper), LBL (using delayed keeper 301), and "ken." LBL waveform for static keeper is similar to LBL waveform of plot 120 during read1 evaluation phase i.e., when Mux 303 selects "Keeper_in" for "ken." Near the end of the Evaluation Phase, charge on LBL (that determines the voltage on LBL node) decays to ground. In this embodiment, when Mux 303 selects "dk" for "ken" during Evaluation Phase (i.e., when PCH is high), keeper 301 is not immediately turned ON, but its turn on is delayed by late arrival of signal "ken." The delay in "ken" is determined by delay of Delay Unit 302.

[0059] The embodiment of **Fig. 3A** expands the effective process margin to balance the low voltage read performance vs. leakage and noise related failures on RF/ROM bit lines using keeper circuit feedback. In one embodiment, sensor circuits (i.e., Sensor(s) 204) can detect the relative process corner, temperature, or voltage conditions on die and switch between static keeper circuit strength (i.e., by selecting "Keeper_in" for "ken" by Mux 303) or the length of delay in a delayed keeper implementation (i.e., by selecting "dk" for "ken" by Mux 303).

[0060] **Fig. 3C** illustrates a plot 330 showing droop behavior of voltage on LBL node for **Fig. 3A** during read 1 evaluation phase, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 3C** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0061] Here, x-axis is time and y-axis is voltage. Plot 330 shows waveforms PCH, LBL (using static keeper), LBL (using delayed keeper 301), and ken. LBL waveform for static keeper is flat during read 1 evaluation phase i.e., when Mux 303 selects "Keeper_in" for "ken." LBL experiences a small droop because of the delay in enabling keeper 301 via "ken" signal.

[0062] **Fig. 4A** illustrates an apparatus 400 having an RF with logic to select one of adaptive keeper circuits of **Fig. 2A** or **Fig. 3A**, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 4** having the same

reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0063] Apparatus 400 comprises multiplexer (Mux) 401, inverter inv1, NAND3 gate, and other components described with reference to **Fig. 2A** and **Fig. 3A**. In one embodiment, Mux 401 selects between adaptive keeper circuit of **Fig. 2A** or **Fig. 3A**. For example, when select is logically high, signal n14 is coupled to node n15 which controls NAND2 to control delayed enabling of second keeper 202. In one embodiment, when select is logically low, signal n12 is coupled to node n15 which controls static enabling of second keeper 202.

[0064] In one embodiment, when first keeper 201 is enabled, second keeper 202 is disabled. For example, when n10 is logically high, then NAND1 enables first keeper 201 to be controlled by LBL. In this example, n12 is logical low which, when coupled to node n15 via Mux 401, causes NAND2 to disable second keeper 202. In one embodiment, when second keeper 202 is disabled NAND3 also causes signal n14 to become logical low. In such an embodiment, it does not matter whether select signal of Mux 401 couples n14 to n15 or n12 to n15.

[0065] In one embodiment, when second keeper 202 is enabled, first keeper 201 is disabled. For example, when n10 is logically low, then NAND1 disables first keeper 201. In this example, n12 is logical high which, when coupled to node n15 via Mux 401, causes NAND2 to enable second keeper 202. In one embodiment, when second keeper 202 is enabled, output n16 of NAND2 is controlled by LBL. In one embodiment, when n15 is logically high, NAND3 is controlled by n13. In such an embodiment, depending on select signal of Mux 401, second keeper 202 is controlled by either delayed "Keeper_in" signal (i.e., Mux 401 couples nodes n14 to n15) or is controlled statically by output of Logic Unit 203 (i.e., Mux 401 couples nodes n12 to n15).

[0066] **Fig. 4B** illustrates an apparatus 420 having a ROM with logic to select one of adaptive keeper circuits of **Fig. 2A** or **Fig. 3A**, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 4B** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0067] So as not to obscure the embodiment, **Fig. 4B** is similar to **Fig. 4A** except that RF cells are replaced with ROM cells. In one embodiment, ROM cells n-type transistors WNWL[0]-[N] are used to replace RF n-type stack MNrdWL[0]-[N] and MNdata[0]-[N]. In one embodiment, each of the WNWL[0]-[N] is controllable by a wordline WL signal. In one embodiment, each of WNWL[0]-[N] receives a corresponding WL signal. For example, WNWL[0] is controllable by WL[0], WNWL[N] is controllable by WL[N]. In one embodiment, each of the n-type transistors WNWL[0]-[N] have a drain terminal coupled to LBL and a source terminal coupled to either ground or a reference voltage Vref (as indicated by the dashed line). The remaining operation is similar to the one discussed with reference to **Fig. 4A**.

[0068] In one embodiment, Second keeper 202 stack includes a single transistor in the stack coupled to power supply and LBL. That single transistor may have multiple transistors coupled in parallel to it, but the stack height is one. In one embodiment, the single transistor is controllable by NAND2 such that output n16 of NAND2 is coupled to the gate terminal of the single transistor. In one embodiment, the strength of the single transistor can be made different from the strength of First keeper 201 by adjusting size (W/L) of the single transistor to adjust its threshold voltage. For example, channel length of the single transistor in Second keeper 202 may be different from the channel length of the transistors in First keeper 201.

[0069] **Fig. 5** illustrates a flowchart 500 of a method to enable use of adaptive keeper circuits of **Fig. 2A** and/or **Fig. 3A**, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 5** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0070] Although the blocks in the flowcharts with reference to **Fig 5** are shown in a particular order, the order of the actions can be modified. Thus, the illustrated embodiments can be performed in a different order, and some actions/blocks may be performed in parallel. Some of the blocks and/or operations listed in **Fig. 5** are optional in accordance with certain embodiments. The numbering of the blocks presented is for the sake of clarity and is not intended to prescribe an order of operations in which the various blocks must occur.

Additionally, operations from the various flows may be utilized in a variety of combinations.

[0071] At block 501, wafer having dies (which have apparatus 200, 300, or 400) is tested using one or more method to determine whether wafer is fabricated using fast, slow, or typical process material. A fast process has transistors that operate at faster speed than the similar me transistors formed from a slow or typical process under same conditions. A typical process has transistors that operate at faster speed than the similar me transistors formed from a slow process under same conditions.

[0072] At block 502, a determination is made whether the wafer is made of fast process material. If it is determined that wafer is not made of fast process material, then the process of flowchart 500 proceeds to block 503. At block 503, weaker keeper (i.e., second keeper 202 or 301) is enabled and stronger keeper (i.e., first keeper 201) is disabled. In one embodiment, second keeper 301 is enabled to be controlled by delayed keeper signal ken (or dk). When weaker keeper is enabled, Delay MinVCC of the circuit is lowered by helping the true evaluation.

[0073] In one embodiment, the determination of block 502 is made by using a device leakage sensor or ring oscillator in dies of wafer having the embodiments. For example, delay or frequency of ring oscillator is used to determine slow or fast material. If the oscillating frequency of ring oscillator is above a predefined threshold then the wafer material is considered fast else it is considered slow. In one embodiment, the local process corner (fast or slow) is determined from reading local ring oscillators only once at power on of the processor/die. In one embodiment, when it is determined that wafer is a slow process material based wafer, then the process of flowchart 500 proceeds to block 503.

[0074] At block 504, adaptive (or dynamic) keeper apparatus is enabled. In this embodiment, Logic Unit 203 is operable to select either first or second keeper (201 or 202/301) according to outputs of one or more Sensors 204. In one embodiment, adaptive RF/ROM keeper is turned on for arrays in fast material to dynamically switch keeper strength. At block 505, Logic Unit 203 monitors outputs of one or more Sensors 204. In this example, the sensor is a thermal/temperature sensor.

[0075] In other embodiments, other types of sensors may be used. For example, in addition to the thermal sensor and power control unit (PCU) controller, other sensors can be used to define a control scheme for keeper strength, including, but not limited to: on-die voltage sensors, on-die oscillators tuned to be sensitive to process parameters such as leakage, threshold voltage, saturation or linear transistor currents or ratios of the mentioned parameters, discrete sensors generating reference voltages based upon drive current ratios, leakage ratios or threshold voltage ratios.

[0076] At block 506, a determination is made by Logic Unit 203 based on output of one or more Sensors 204 whether temperature of the die (having the apparatus of the embodiments) is above a predetermined threshold (e.g., 50°C). In one embodiment, if it is determined that the temperature is above the predetermined threshold (i.e., temperature is hot) then the process proceeds to block 507. At block 507, Logic Unit 203 selects a stronger keeper (i.e., first keeper 201) to prevent a false evaluation of '0' due to leakage/noise. In this embodiment, weaker keeper (i.e., second keeper 202) is disabled. In such an embodiment, MinVCC, which is limited by leakage/noise, is reduced by using the static strong first keeper 201. The process then continues to block 505 and temperature is again monitored by Logic Unit 203.

[0077] As temperature drops below the predetermined threshold, the process proceeds from block 506 to block 508. At block 508, Logic Unit 203 disables the strong first keeper 201 and enables the weaker or delayed keeper (i.e., second keeper 202/301). MinVCC, which is limited by delay at cold temperature, is significantly improved by the weakened keeper (i.e., second keeper 202/301). In one embodiment, switching keeper due to change in temperature allows longer off-state of p-type keeper and improves aging MinVCC degradation significantly (e.g., 1-2% off-state can lower the p-type device aging by approx. 40%). The process then continues to block 505 and temperature is again monitored by Logic Unit 203.

[0078] **Fig. 6** illustrates a processor 601 with adaptive keeper circuits of **Fig. 2A** and/or **Fig. 3A**, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 6** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0079] In one embodiment, processor 601 comprises PCU 602, and two cores—Core 1 and Core 2. The embodiments are not limited to any number of cores. In one embodiment, Core 1 comprises power management agent 1(PMA1), one or more sensor1(s), read only memory 1 (ROM1) and register file 1 (RF1). In one embodiment, Sensor1 is the same as Sensor(s) 204. ROM1 and/or RF1 are like the apparatus of ROM and/or RF with adaptive keepers of the embodiments. In one embodiment, Core 2 comprises PMA2, one or more Sensor2(s), ROM2 and RF2. In one embodiment, Sensor2 is the same as Sensor(s) 204. ROM2 and/or RF2 are like the apparatus of ROM and/or RF with adaptive keepers of the embodiments.

[0080] In one embodiment, for systems having an on-die PCU like PCU 602, information about local process corner and temperature is already available to the PCU which can be used to determine n10 signal from a local PMA (e.g., PMA1/2). In one embodiment, a core may have more register files than on-die thermal sensors. In such an embodiment, the RF/ROM arrays of the embodiments are grouped in clusters that assume similar process and temperature conditions and share the same keeper enable signal (e.g., signal n10).

[0081] In one embodiment, for RF/ROM arrays of the embodiments that are far from the thermal sensors, PCU 602 averages the thermal readouts from several thermal sensors (e.g., Sensor(s) 204) to determine an average local temperature. In one embodiment, the temperature information is updated in real time, but in a slow loop (e.g., 1ms) since local temperature is slow changing. In such an embodiment, Logic 203 updates the selection of first and/or second keeper after a long time (e.g., 1ms).

[0082] **Fig. 7** is a smart device or a computer system or an SoC (System-on-Chip) with adaptive keeper, according to one embodiment of the disclosure. **Fig. 7** is a smart device or a computer system or an SoC (System-on-Chip) 1600 with power regulator with continuous controlled mode regulation of supply for multiple adjustable loads, according to one embodiment of the disclosure. It is pointed out that those elements of **Fig. 7** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0083] **Fig. 7** illustrates a block diagram of an embodiment of a mobile device in which flat surface interface connectors could be used. In one embodiment, computing device 1600 represents a mobile computing device, such as a computing tablet, a mobile phone or smart-phone, a wireless-enabled e-reader, or other wireless mobile device. It will be understood that certain components are shown generally, and not all components of such a device are shown in computing device 1600.

[0084] In one embodiment, computing device 1600 includes a first processor 1610 with adaptive keeper, according to the embodiments. In one embodiment, computing device 1600 includes a second processor 1690 with adaptive keeper, according to the embodiments discussed herein. In one embodiment, second processor 1690 is optional. Other blocks of the computing device 1600 with I/O drivers may also include adaptive keeper of the embodiments. The various embodiments of the present disclosure may also comprise a network interface within 1670 such as a wireless interface so that a system embodiment may be incorporated into a wireless device, for example, cell phone or personal digital assistant.

[0085] In one embodiment, processor 1610 can include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. The processing operations performed by processor 1610 include the execution of an operating platform or operating system on which applications and/or device functions are executed. The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, and/or operations related to connecting the computing device 1600 to another device. The processing operations may also include operations related to audio I/O and/or display I/O.

[0086] In one embodiment, computing device 1600 includes audio subsystem 1620, which represents hardware (e.g., audio hardware and audio circuits) and software (e.g., drivers, codecs) components associated with providing audio functions to the computing device. Audio functions can include speaker and/or headphone output, as well as microphone input. Devices for such functions

can be integrated into computing device 1600, or connected to the computing device 1600. In one embodiment, a user interacts with the computing device 1600 by providing audio commands that are received and processed by processor 1610.

[0087] Display subsystem 1630 represents hardware (e.g., display devices) and software (e.g., drivers) components that provide a visual and/or tactile display for a user to interact with the computing device 1600. Display subsystem 1630 includes display interface 1632, which includes the particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 1632 includes logic separate from processor 1610 to perform at least some processing related to the display. In one embodiment, display subsystem 1630 includes a touch screen (or touch pad) device that provides both output and input to a user.

[0088] I/O controller 1640 represents hardware devices and software components related to interaction with a user. I/O controller 1640 is operable to manage hardware that is part of audio subsystem 1620 and/or display subsystem 1630. Additionally, I/O controller 1640 illustrates a connection point for additional devices that connect to computing device 1600 through which a user might interact with the system. For example, devices that can be attached to the computing device 1600 might include microphone devices, speaker or stereo systems, video systems or other display devices, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

[0089] As mentioned above, I/O controller 1640 can interact with audio subsystem 1620 and/or display subsystem 1630. For example, input through a microphone or other audio device can provide input or commands for one or more applications or functions of the computing device 1600. Additionally, audio output can be provided instead of, or in addition to display output. In another example, if display subsystem 1630 includes a touch screen, the display device also acts as an input device, which can be at least partially managed by I/O controller 1640. There can also be additional buttons or switches on the computing device 1600 to provide I/O functions managed by I/O controller 1640.

[0090] In one embodiment, I/O controller 1640 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, or other

hardware that can be included in the computing device 1600. The input can be part of direct user interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

[0091] In one embodiment, computing device 1600 includes power management 1650 that manages battery power usage, charging of the battery, and features related to power saving operation. Memory subsystem 1660 includes memory devices for storing information in computing device 1600. Memory can include nonvolatile (state does not change if power to the memory device is interrupted) and/or volatile (state is indeterminate if power to the memory device is interrupted) memory devices. Memory subsystem 1660 can store application data, user data, music, photos, documents, or other data, as well as system data (whether long-term or temporary) related to the execution of the applications and functions of the computing device 1600.

[0092] Elements of embodiments are also provided as a machine-readable medium (e.g., memory 1660) for storing the computer-executable instructions (e.g., instructions to implement any other processes discussed herein). The machine-readable medium (e.g., memory 1660) may include, but is not limited to, flash memory, optical disks, CD-ROMs, DVD ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, phase change memory (PCM), or other types of machine-readable media suitable for storing electronic or computer-executable instructions. For example, embodiments of the disclosure may be downloaded as a computer program (e.g., BIOS) which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals via a communication link (e.g., a modem or network connection).

[0093] Connectivity 1670 includes hardware devices (e.g., wireless and/or wired connectors and communication hardware) and software components (e.g., drivers, protocol stacks) to enable the computing device 1600 to communicate with external devices. The computing device 1600 could be separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

[0094] Connectivity 1670 can include multiple different types of connectivity. To generalize, the computing device 1600 is illustrated with cellular connectivity 1672 and wireless connectivity 1674. Cellular connectivity 1672 refers generally to cellular network connectivity provided by wireless carriers, such as provided via GSM (global system for mobile communications) or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, or other cellular service standards. Wireless connectivity (or wireless interface) 1674 refers to wireless connectivity that is not cellular, and can include personal area networks (such as Bluetooth, Near Field, etc.), local area networks (such as Wi-Fi), and/or wide area networks (such as WiMax), or other wireless communication.

[0095] Peripheral connections 1680 include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that the computing device 1600 could both be a peripheral device ("to" 1682) to other computing devices, as well as have peripheral devices ("from" 1684) connected to it. The computing device 1600 commonly has a "docking" connector to connect to other computing devices for purposes such as managing (e.g., downloading and/or uploading, changing, synchronizing) content on computing device 1600. Additionally, a docking connector can allow computing device 1600 to connect to certain peripherals that allow the computing device 1600 to control content output, for example, to audiovisual or other systems.

[0096] In addition to a proprietary docking connector or other proprietary connection hardware, the computing device 1600 can make peripheral connections 1680 via common or standards-based connectors. Common types can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware interfaces), DisplayPort including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other types.

[0097] Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The

various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure, or characteristic "may," "might," or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

[0098] Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.

[0099] While the disclosure has been described in conjunction with specific embodiments thereof, many alternatives, modifications and variations of such embodiments will be apparent to those of ordinary skill in the art in light of the foregoing description. For example, other memory architectures e.g., Dynamic RAM (DRAM) may use the embodiments discussed. The embodiments of the disclosure are intended to embrace all such alternatives, modifications, and variations as to fall within the broad scope of the appended claims.

[00100] In addition, well known power/ground connections to integrated circuit (IC) chips and other components may or may not be shown within the presented figures, for simplicity of illustration and discussion, and so as not to obscure the disclosure. Further, arrangements may be shown in block diagram form in order to avoid obscuring the disclosure, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the present disclosure is to be implemented (i.e., such specifics should be well within purview of one skilled in the art). Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the disclosure, it should be apparent to one skilled in the art that the disclosure can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

[00101] The following examples pertain to further embodiments. Specifics in the examples may be used anywhere in one or more embodiments. All optional features of the apparatus described herein may also be implemented with respect to a method or process.

[00102] For example, an apparatus is provided which comprises: a bit line (BL); a first keeper of first strength coupled to the BL; a second keeper of second strength different from first strength, the second keeper coupled to BL; and a logic unit to enable one of the first or second keepers according to one or more environmental conditions. The apparatus further comprises a temperature sensor to generate an output for controlling the logic unit. In one embodiment, each of the first and second keepers comprises a stack of transistors, wherein the stack of transistors for the first keeper is shorter than the stack of transistors of the second keeper.

[00103] In one embodiment, the logic unit is operable to enable the first keeper and disable the second keeper when a sensor output from a sensor is above a first threshold level. In one embodiment, the logic unit is operable to enable the second keeper and disable the first keeper when the sensor output is below a second threshold level. In one embodiment, the first and second threshold levels are substantially the same. In one embodiment, the first threshold is higher than the second threshold such that the first threshold indicates a temperature higher than a temperature indicated by the second threshold.

[00104] In one embodiment, the sensor is one of: a temperature sensor; a voltage sensor; or a ring oscillator. In one embodiment, the apparatus further comprises a power control unit to sense the one or more environmental conditions. In one embodiment, the apparatus further comprises: a first transistor operable to precharge the BL; and a second transistor coupled to the BL, the second transistor controllable by a word line signal. In one embodiment, the apparatus further comprises: a third transistor coupled in series with the second transistor, the third transistor having a gate terminal coupled to a memory cell._In one embodiment, the wordline is a read wordline, and where the memory cell is an SRAM bit-cell.

[00105] In another example, a system is provided which comprises: a memory unit; a processor coupled to the memory unit, the processor having a

register file according to the apparatus described above. In one embodiment, the system further comprises wireless interface for allowing the processor to communicate with another device. In one embodiment, the system further comprises a display unit. In one embodiment, the display unit is a touch screen.

[00106] In another example, an apparatus is provided which comprises: a bit line (BL); a keeper coupled to the BL, the keeper having at least two transistor coupled in series; a delay unit to provide a first control signal for enabling or disabling one of the at least two transistors of the keeper; and a logic unit to bypass the delay unit and to provide a second control signal for enabling or disabling one of the at least two transistors of the keeper according to one or more environmental conditions.

[00107] In one embodiment, the logic unit is operable to provide the first control signal from the delay unit to the one of the at least two transistors of the keeper when a sensor output from a sensor is below a threshold level. In one embodiment, the logic unit is operable to provide the second control signal instead of the first control signal to the one of the at least two transistors of the keeper when the sensor output is above or equal to the threshold level. In one embodiment, the sensor is one of: a temperature sensor; a voltage sensor; or a ring oscillator.

[00108] In one embodiment, a power control unit to sense the one or more environmental conditions. In one embodiment, the apparatus further comprises: a first transistor operable to precharge the BL; and a second transistor coupled to the BL, the second transistor controllable by a word line signal. In one embodiment, the apparatus further comprises: a third transistor coupled in series with the second transistor, the third transistor having a gate terminal coupled to a memory cell. In one embodiment, the wordline is a read wordline, and where the memory cell is an SRAM bit-cell.

[00109] In another example, a system is provided which comprises: a memory unit; a processor coupled to the memory unit, the processor having a register file according to the apparatus described above. In one embodiment, the system further comprises wireless interface for allowing the processor to communicate with another device. In one embodiment, the system further comprises a display unit. In one embodiment, the display unit is a touch screen.

[00110] In another example, an apparatus is provided which comprises: a bit line (BL); a keeper coupled to the BL, the keeper having a transistor; a delay unit to provide a first control signal for enabling or disabling the transistor of the keeper; and a logic unit to bypass the delay unit and to provide a second control signal for enabling or disabling the transistor of the keeper according to one or more environmental conditions. In one embodiment, the logic unit is operable to provide the first control signal from the delay unit to the transistor of the keeper when a sensor output from a sensor is below a threshold level.

[00111] In one embodiment, the logic unit is operable to provide the second control signal instead of the first control signal to the transistor of the keeper when the sensor output is above or equal to the threshold level. In one embodiment, the sensor is one of: a temperature sensor; a voltage sensor; or a ring oscillator.

[00112] In another example, a system is provided which comprises: a memory unit; a processor coupled to the memory unit, the processor having a register file according to the apparatus described above. In one embodiment, the system further comprises wireless interface for allowing the processor to communicate with another device. In one embodiment, the system further comprises a display unit. In one embodiment, the display unit is a touch screen.

[00113] In another example, a method is provided which comprises: monitoring one or more environmental conditions of a processor; determining whether the one or more environmental conditions is above a threshold level; enabling a first keeper of first strength, the first keeper coupled to a local bit line (LBL), when it is determined that the one or more environmental conditions is above a threshold level; and enabling a second keeper of second strength different from first strength, and disabling the first keeper, the second keeper coupled to the LBL, when it is determined that the one or more environmental conditions is below the threshold level.

[00114] In one embodiment, the method further comprises: testing a wafer having the processor to determine whether the processor is fabricated on a slow or a fast process; and enabling or disabling the first or second keepers according to whether the processor was fabricated on a slow or a fast process, the fast process having transistors operating at a faster speed than transistors in the slow process

under same conditions. In one embodiment, the method further comprises: enabling the second keeper and disabling the first keeper when it is determined that the processor is fabricated on a slow process.

[00115] An abstract is provided that will allow the reader to ascertain the nature and gist of the technical disclosure. The abstract is submitted with the understanding that it will not be used to limit the scope or meaning of the claims. The following claims are hereby incorporated into the detailed description, with each claim standing on its own as a separate embodiment.

CLAIMS

We claim:

1. An apparatus comprising:

   a bit line (BL);

   a first keeper of first strength coupled to the BL;

   a second keeper of second strength different from first strength, the second keeper coupled to BL; and

   a logic unit to enable one of the first or second keepers according to one or more environmental conditions.

2. The apparatus of claim 1 further comprises a temperature sensor to generate an output for controlling the logic unit.

3. The apparatus of claim 1, wherein each of the first and second keepers comprises a stack of transistors, wherein the stack of transistors for the first keeper is shorter than the stack of transistors of the second keeper.

4. The apparatus of claim 3, wherein the logic unit is operable to enable the first keeper and disable the second keeper when a sensor output from a sensor is above a first threshold level.

5. The apparatus of claim 4, wherein the logic unit is operable to enable the second keeper and disable the first keeper when the sensor output is below a second threshold level.

6. The apparatus of claim 5, wherein the first and second threshold levels are substantially the same.

7. The apparatus of claim 5, wherein the first threshold is higher than the second threshold such that the first threshold indicates a temperature higher than a temperature indicated by the second threshold.

8. The apparatus of claim 4, wherein the sensor is one of:

a temperature sensor;

a voltage sensor; or

a ring oscillator.

9. The apparatus of claim 1 further comprises a power control unit to sense the one or more environmental conditions.

10. The apparatus of claim 1 further comprises:

a first transistor operable to precharge the BL; and

a second transistor coupled to the BL, the second transistor controllable by a word line signal.

11. The apparatus of claim 10 further comprises:

a third transistor coupled in series with the second transistor, the third transistor having a gate terminal coupled to a memory cell.

12. The apparatus of claim 11, wherein the wordline is a read wordline, and where the memory cell is an SRAM bit-cell.

13. An apparatus comprising:

a bit line (BL);

a keeper coupled to the BL, the keeper having at least two transistor coupled in series;

a delay unit to provide a first control signal for enabling or disabling one of the at least two transistors of the keeper; and

a logic unit to bypass the delay unit and to provide a second control signal for enabling or disabling one of the at least two transistors of the keeper according to one or more environmental conditions.

14. The apparatus of claim 13, wherein the logic unit is operable to provide the first control signal from the delay unit to the one of the at least two transistors of the keeper when a sensor output from a sensor is below a threshold level.

15. The apparatus of claim 14, wherein the logic unit is operable to provide the second control signal instead of the first control signal to the one of the at least two transistors of the keeper when the sensor output is above or equal to the threshold level.

16. The apparatus of claim 14, wherein the sensor is one of:
a temperature sensor;
a voltage sensor; or
a ring oscillator.

17. The apparatus of claim 13 further comprises a power control unit to sense the one or more environmental conditions.

18. The apparatus of claim 13 further comprises:
a first transistor operable to precharge the BL; and
a second transistor coupled to the BL, the second transistor controllable by a word line signal.

19. The apparatus of claim 18 further comprises:
a third transistor coupled in series with the second transistor, the third transistor having a gate terminal coupled to a memory cell.

20. The apparatus of claim 18, wherein the wordline is a read wordline, and where the memory cell is an SRAM bit-cell.

21. An apparatus comprising:
a bit line (BL);

a keeper coupled to the BL, the keeper having a transistor;

a delay unit to provide a first control signal for enabling or disabling the transistor of the keeper; and

a logic unit to bypass the delay unit and to provide a second control signal for enabling or disabling the transistor of the keeper according to one or more environmental conditions.

22. The apparatus of claim 21, wherein the logic unit is operable to provide the first control signal from the delay unit to the transistor of the keeper when a sensor output from a sensor is below a threshold level.

23. The apparatus of claim 22, wherein the logic unit is operable to provide the second control signal instead of the first control signal to the transistor of the keeper when the sensor output is above or equal to the threshold level.

24. The apparatus of claim 22, wherein the sensor is one of:

a temperature sensor;

a voltage sensor; or

a ring oscillator.

25. A method comprising:

monitoring one or more environmental conditions of a processor;

determining whether the one or more environmental conditions is above a threshold level;

enabling a first keeper of first strength, the first keeper coupled to a local bit line (LBL), when it is determined that the one or more environmental conditions is above a threshold level; and

enabling a second keeper of second strength different from first strength, and disabling the first keeper, the second keeper coupled to the LBL, when it is determined that the one or more environmental conditions is below the threshold level.

26. The method of claim 25 further comprises:

testing a wafer having the processor to determine whether the processor is fabricated on a slow or a fast process; and

enabling or disabling the first or second keepers according to whether the processor was fabricated on a slow or a fast process, the fast process having transistors operating at a faster speed than transistors in the slow process under same conditions.

27. The method of claim 26 further comprises:

enabling the second keeper and disabling the first keeper when it is determined that the processor is fabricated on a slow process.

28. A system comprising:

a memory unit;

a processor coupled to the memory unit, the processor having a register file according to any one of apparatus claims 1 to 11; and

a wireless interface for allowing the processor to communicate with another device.

29. A system comprising:

a memory unit;

a processor coupled to the memory unit, the processor having a an apparatus according to any one of apparatus claims 12 to 18; and

a wireless interface for allowing the processor to communicate with another device.

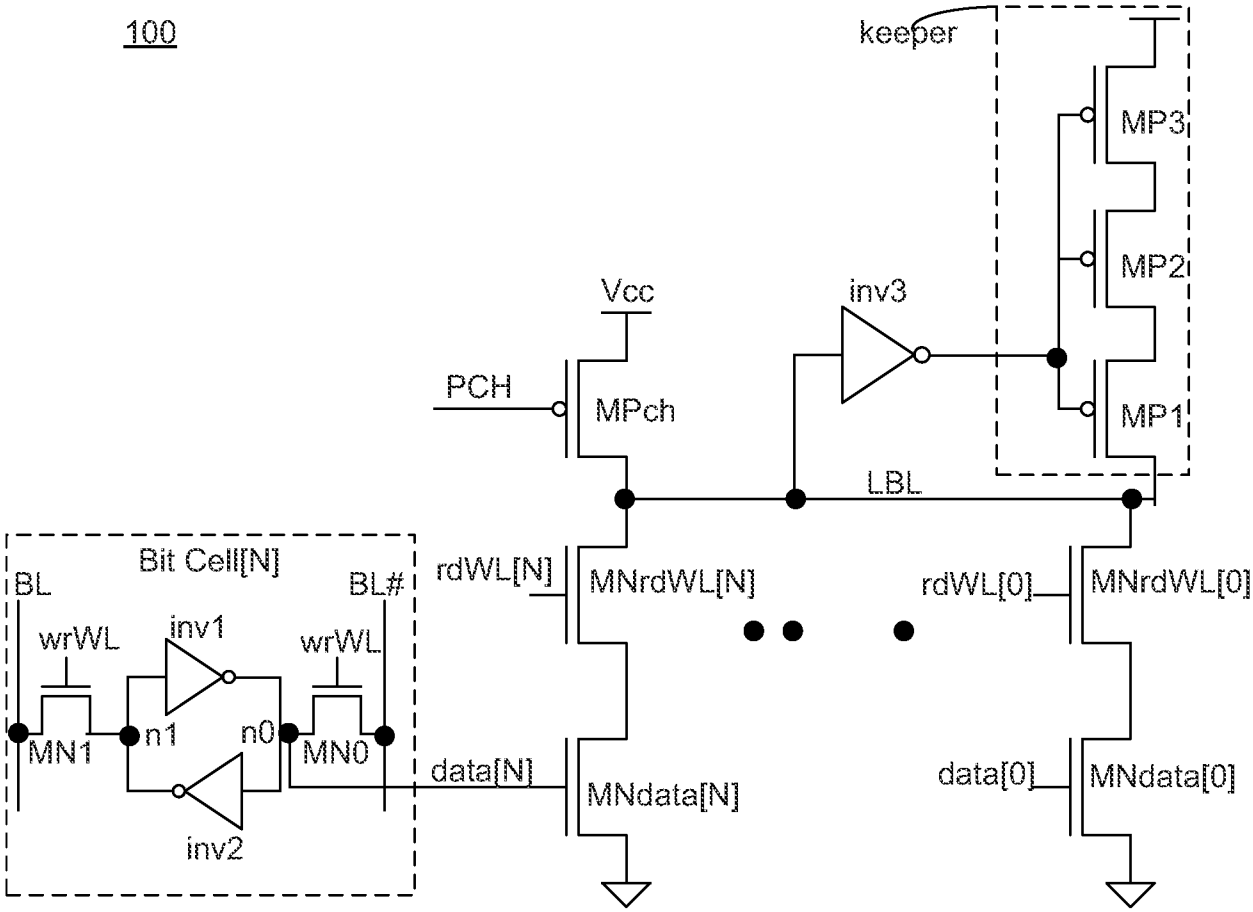

Fig. 1A (prior art)

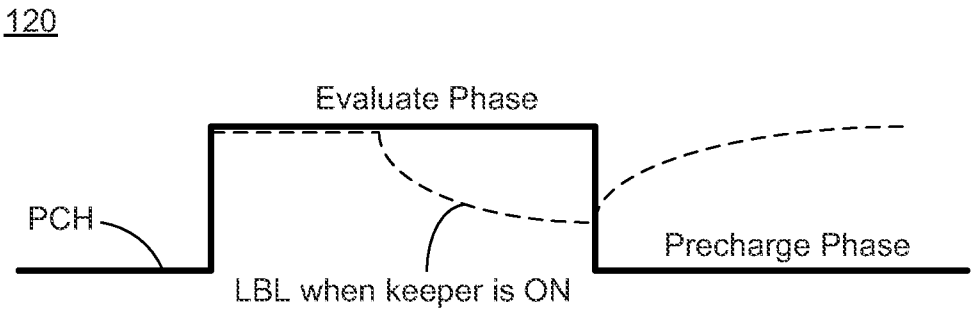

Fig. 1B (prior art)

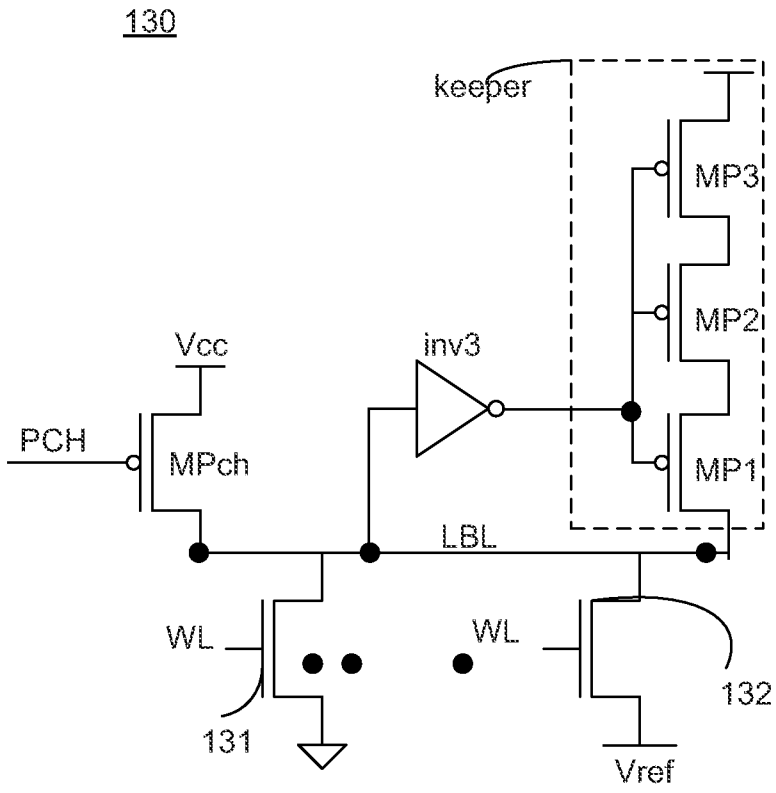

Fig. 1C (prior art)

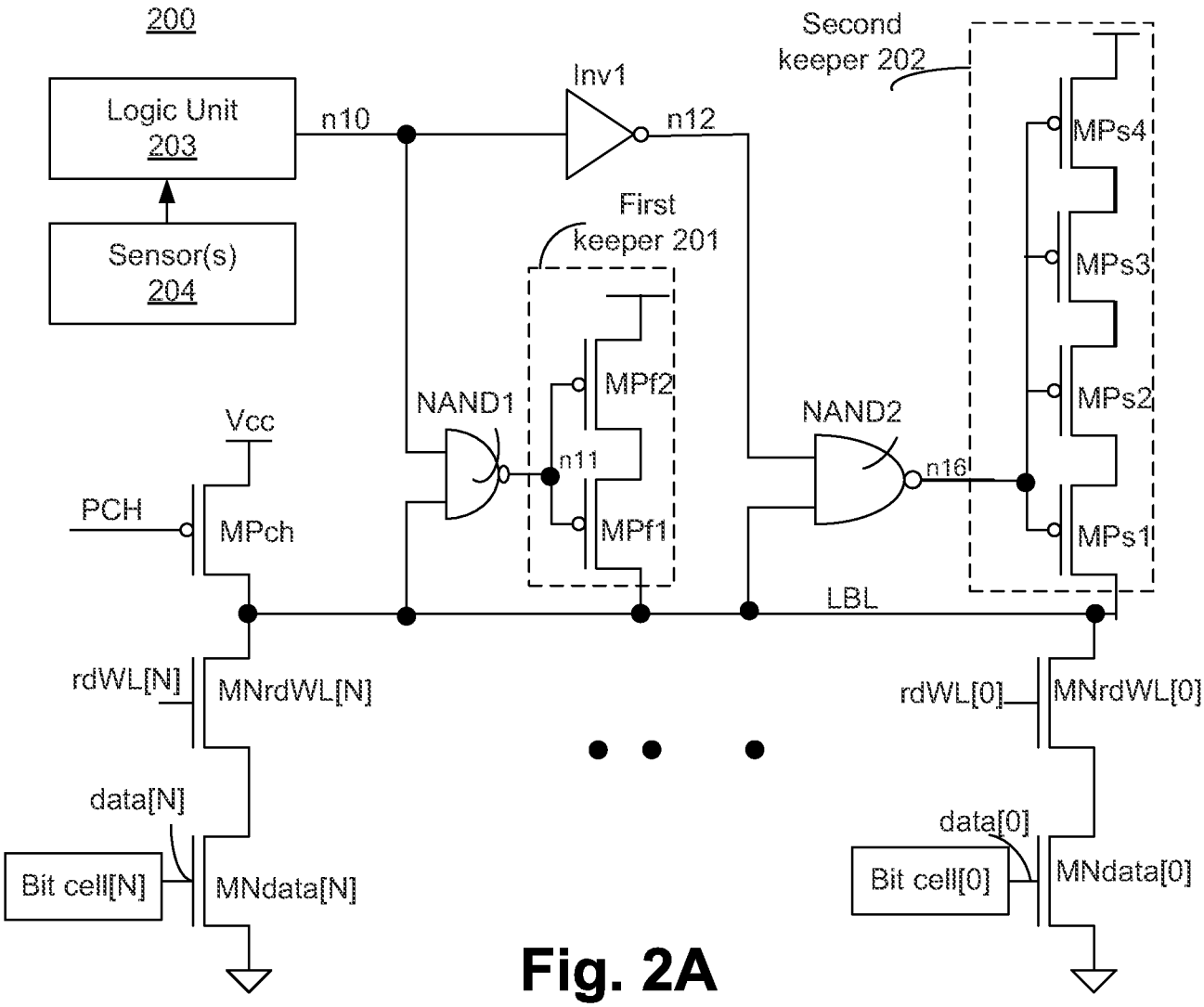
200
Logic Unit
203
Sensor(s)
204
n10
Inv1
n12
Second
keeper 202
First
keeper 201
MPs4
MPs3
MPs2
MPs1
MPf2
MPf1
NAND1
NAND2
n11
n16
Vcc
PCH
MPch
LBL
rdWL[N]
MNrdWL[N]
rdWL[0]
MNrdWL[0]
data[N]
Bit cell[N]
MNdata[N]
data[0]
Bit cell[0]
MNdata[0]

Fig. 2A

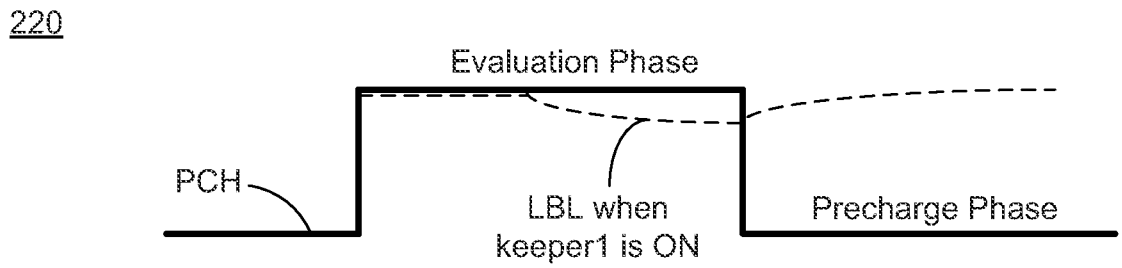
220
Evaluation Phase
PCH
LBL when
keeper1 is ON
Precharge Phase

Fig. 2B

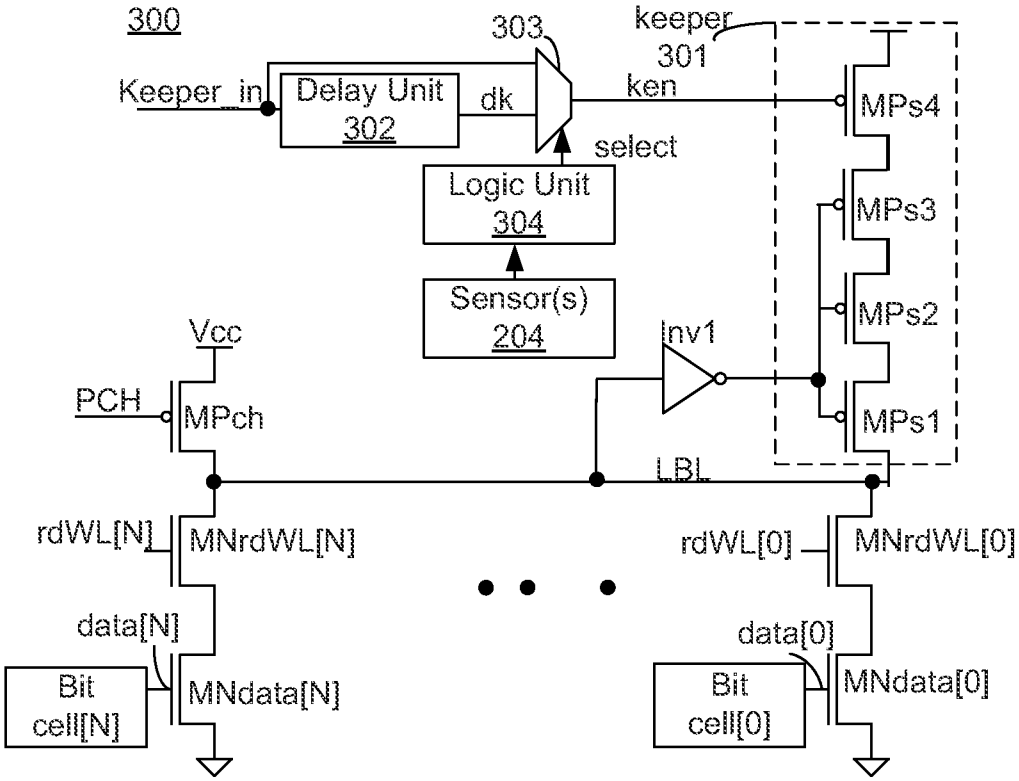

Fig. 3A

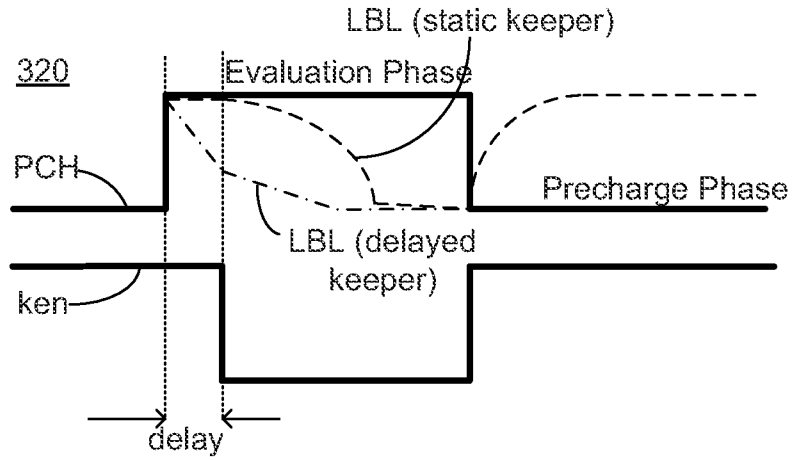

Fig. 3B

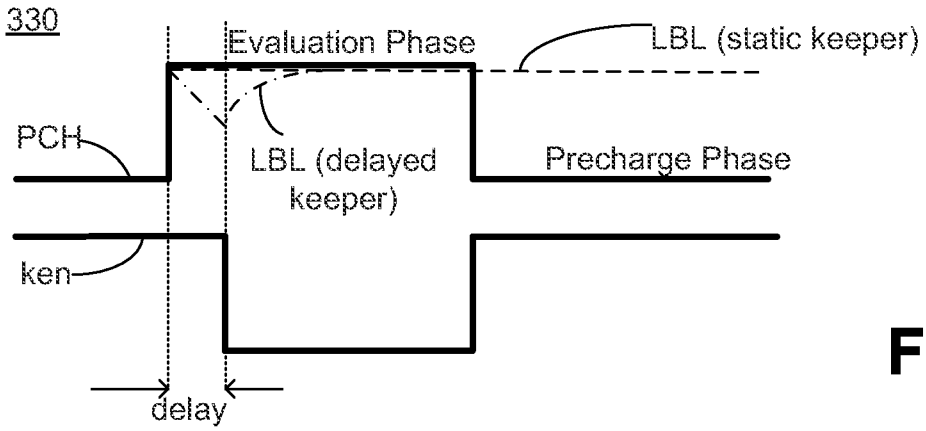

Fig. 3C

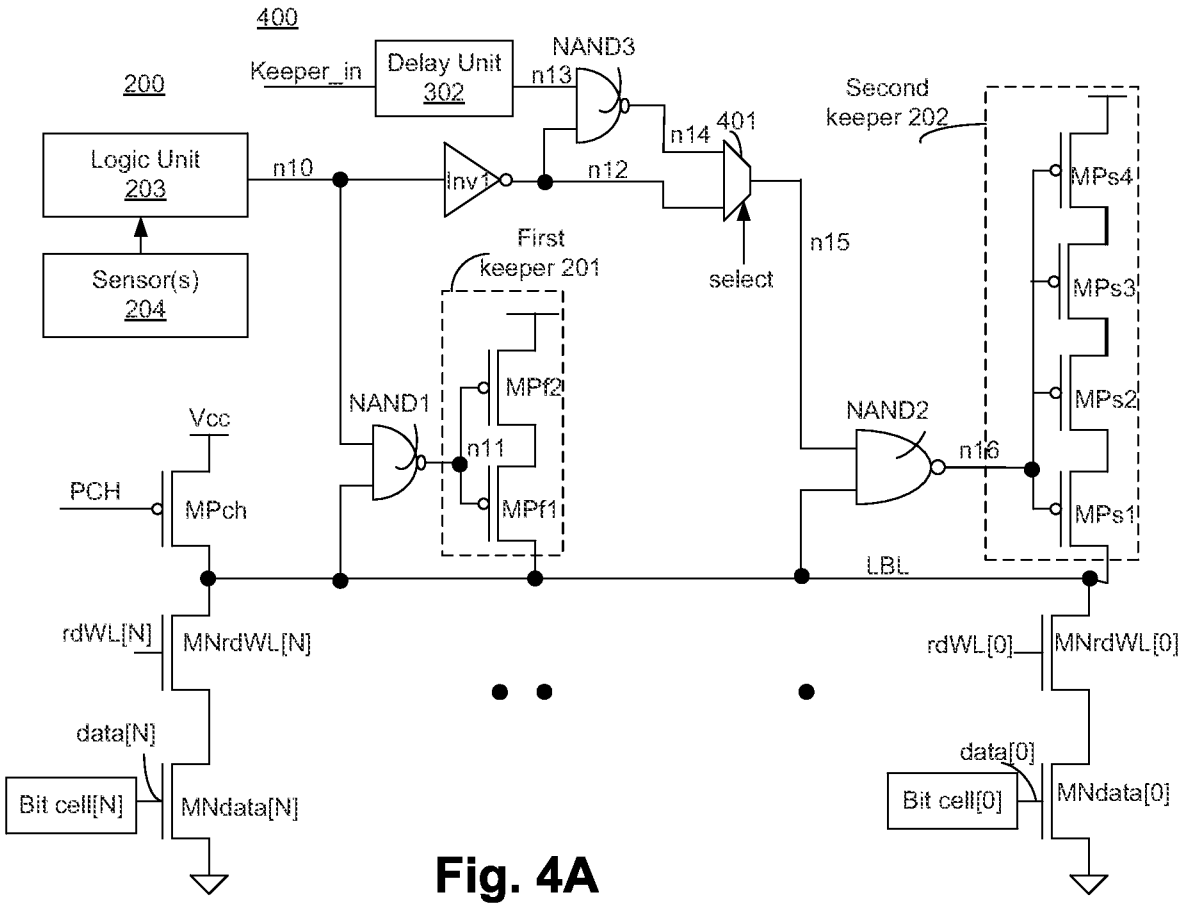
400
200
Keeper_in
Delay Unit
302
NAND3
n13
n14
401
Second
keeper 202
Logic Unit
203
n10
Inv1
n12
Sensor(s)
204
First
keeper 201
select
n15
MPs4
MPs3
MPs2
MPs1
MPf2
NAND1
NAND2
n16
Vcc
PCH
MPch
n11
MPf1
LBL
rdWL[N]
MNrdWL[N]
rdWL[0]
MNrdWL[0]
data[N]
data[0]
Bit cell[N]
MNdata[N]
Bit cell[0]
MNdata[0]

Fig. 4A

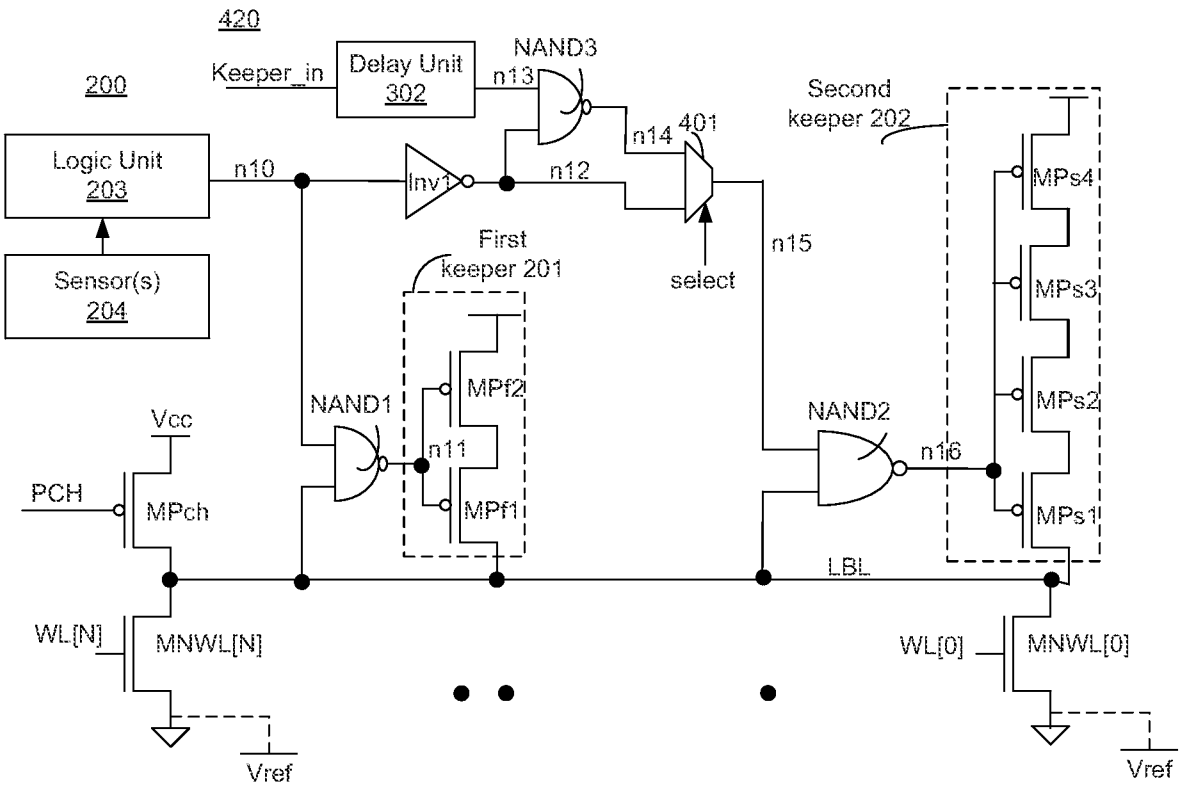
420
200
Keeper_in
Delay Unit
302
NAND3
n13
Logic Unit
203
n10
Inv1
n12
n14
401
Second
keeper 202
Sensor(s)
204
First
keeper 201
select
n15
MPs4
MPs3
MPs2
MPs1
MPf2
MPf1
NAND1
NAND2
n11
n16
Vcc
PCH
MPch
LBL
WL[N]
MNWL[N]
WL[0]
MNWL[0]
Vref
Vref

Fig. 4B

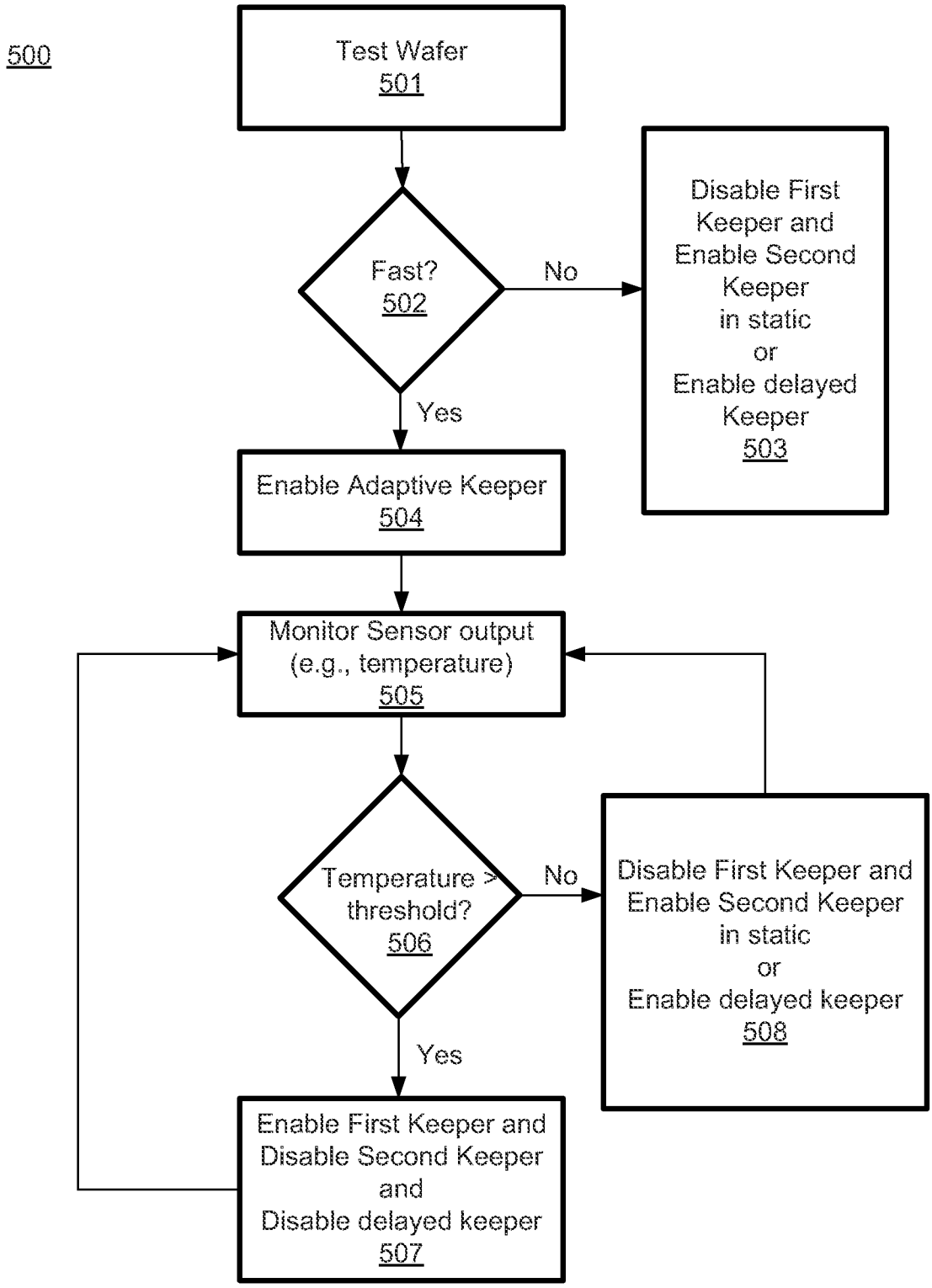
500
Test Wafer
501
Fast?
502
No
Disable First Keeper and Enable Second Keeper in static or Enable delayed Keeper
503
Yes
Enable Adaptive Keeper
504
Monitor Sensor output (e.g., temperature)
505
Temperature > threshold?
506
No
Disable First Keeper and Enable Second Keeper in static or Enable delayed keeper
508
Yes
Enable First Keeper and Disable Second Keeper and Disable delayed keeper
507

Fig. 5

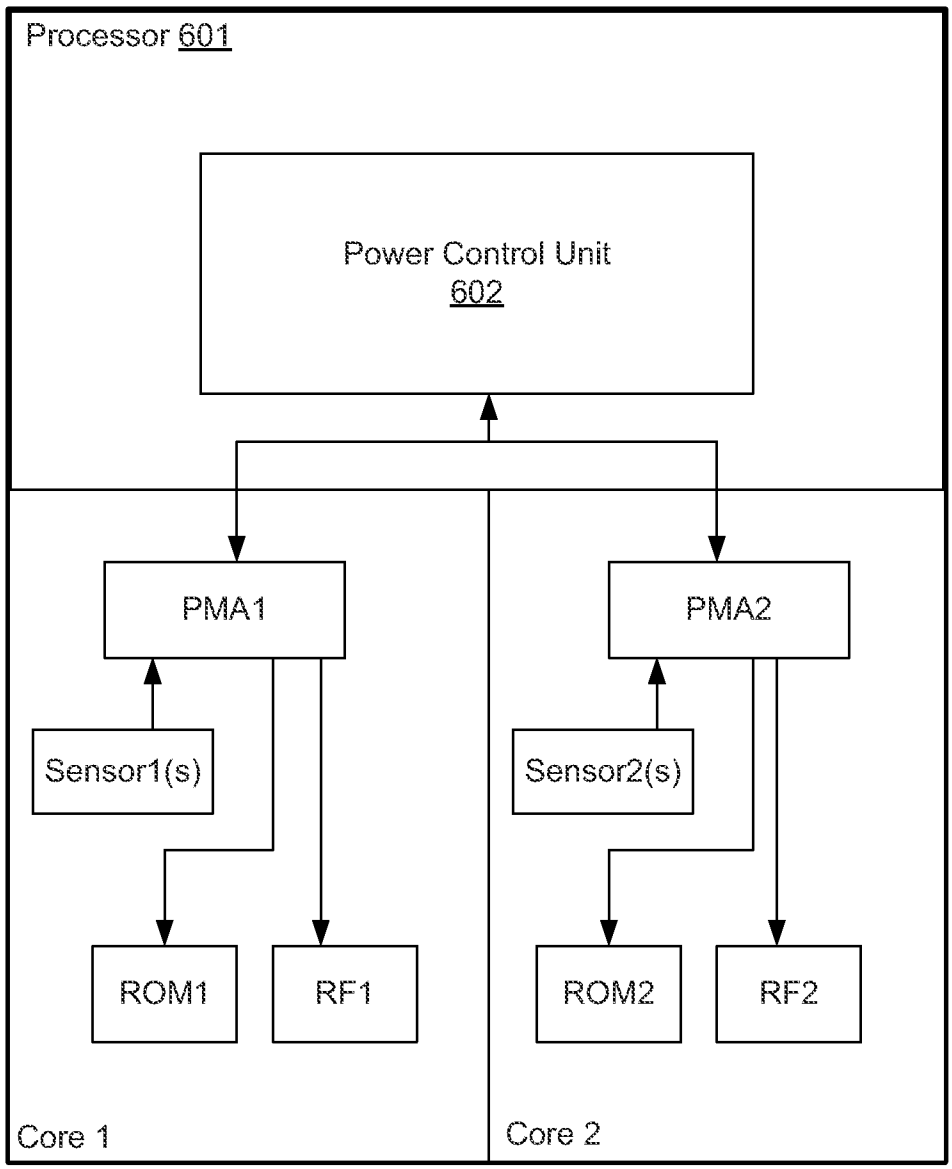
Processor 601
Power Control Unit
602
PMA1
PMA2
Sensor1(s)
Sensor2(s)
ROM1
RF1
ROM2
RF2
Core 1
Core 2

Fig. 6

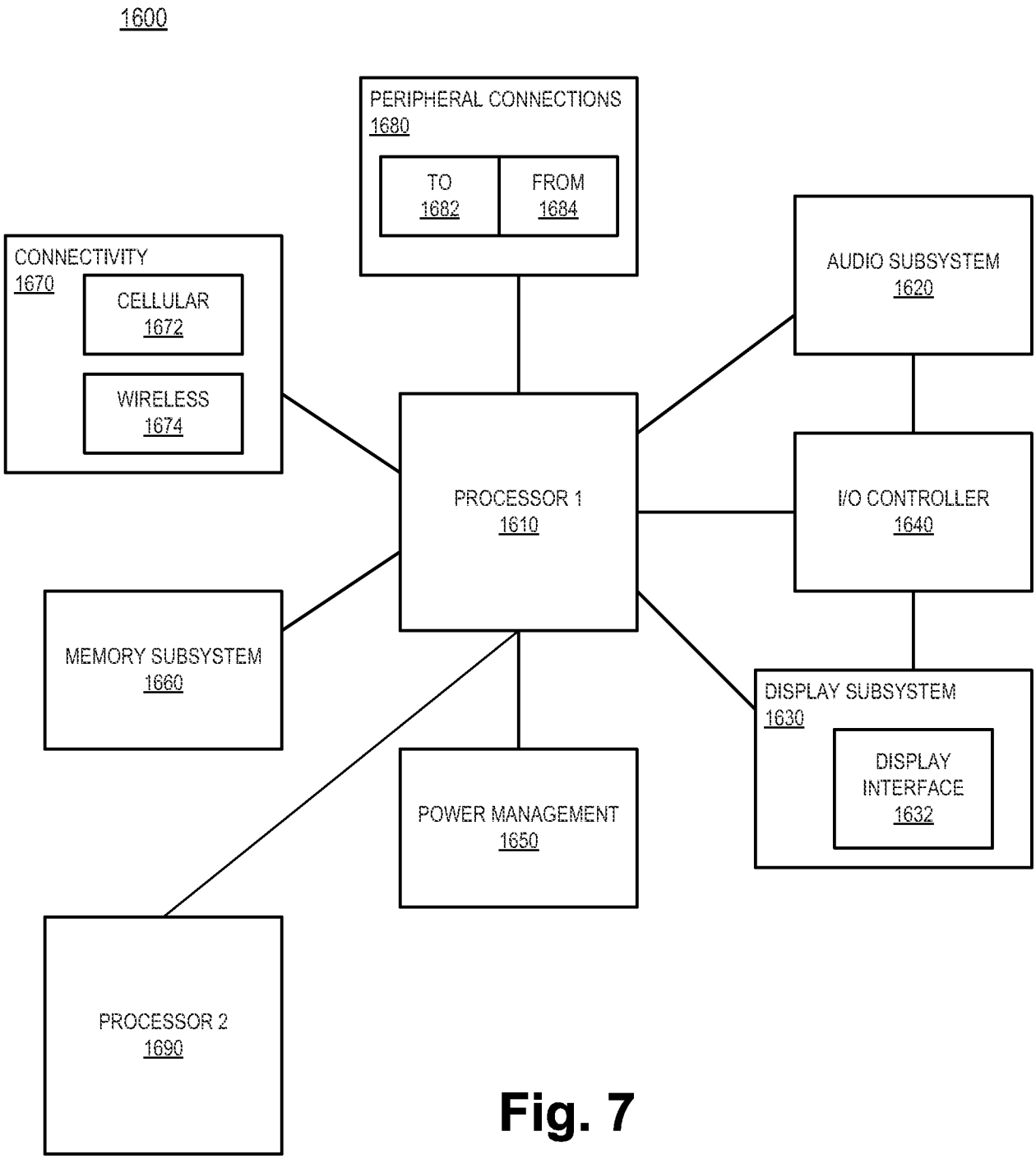
1600
PERIPHERAL CONNECTIONS
1680
TO
1682
FROM
1684
CONNECTIVITY
1670
CELLULAR
1672
WIRELESS
1674
AUDIO SUBSYSTEM
1620
PROCESSOR 1
1610
I/O CONTROLLER
1640
MEMORY SUBSYSTEM
1660
DISPLAY SUBSYSTEM
1630
DISPLAY
INTERFACE
1632
POWER MANAGEMENT
1650
PROCESSOR 2
1690

Fig. 7

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2013/077884

A. CLASSIFICATION OF SUBJECT MATTER

G11C 11/4074 *(2006.01)*
G11C 16/30 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 11/00-11/4074, 16/00-16/30, H03L 7/00-7/087, G05F 1/00-1/40, 11/00, H03K 3/00-3/84, 19/00-19/084

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/0146013 A1 (INTEL CORPORATION) 28.06.2007, paragraphs [0008]-[0012], [0016]-[0017], [0020]-[0022], [0025]	1-9, 25-28
Y		10-12, 16-17, 24
X	US 2010/0327909 (INTEL CORPORATION) 30.12.2010, paragraphs [0010], [0013], [0017]-[0021], [0024], [0028]-[0029], [0033]	13-15, 18-23, 29
Y		10-12, 16-17, 24
A	US 2011/0188314 A1 (TIEN-CHIEN KUO et al) 04.08.2011	1-29

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03 September 2014 (03.09.2014)	11 September 2014 (11.09.2014)

Name and mailing address of the ISA/RU:
FIPS,
Russia, 123995, Moscow, G-59, GSP-5,
Berezhkovskaya nab., 30-1
Facsimile No. +7 (499) 243-33-37

Authorized officer

D. Glazkov

Telephone No. (499) 240-25-91