



(51) International Patent Classification:

H01L 27/1157 (2017.01) H01L 27/11582 (2017.01)

(21) International Application Number:

PCT/CN2019/096195

(22) International Filing Date:

16 July 2019 (16.07.2019)

(25) Filing Language:

English

(26) Publication Language:

English

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(81) Designated States (unless otherwise indicated, for every

kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every

kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,

(54) Title: SELF-ALIGNED CONTACTS IN THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME

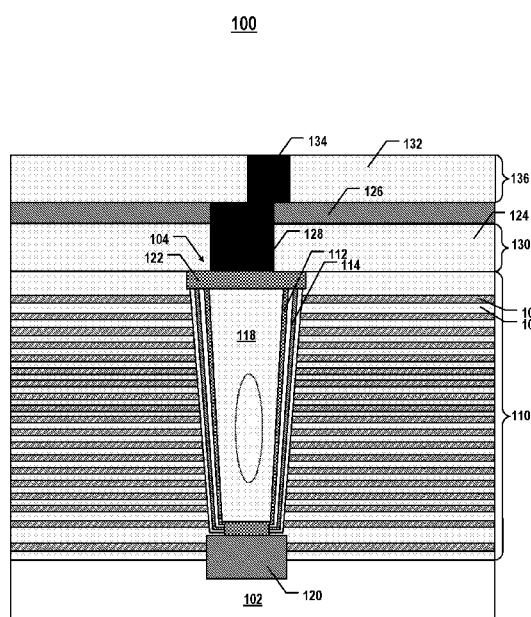


FIG. 1A

(57) Abstract: Embodiments of 3D memory devices and methods for forming the same are disclosed. In an example, a 3D memory device includes a substrate, a memory stack including interleaved conductive layers and dielectric layers above the substrate, a structure extending vertically through the memory stack, a first dielectric layer on the memory stack, an etch stop layer on the first dielectric layer, a second dielectric layer on the etch stop layer, a first contact through the etch stop layer and the first dielectric layer and in contact with an upper end of the structure, and a second contact through the second dielectric layer and in contact with at least an upper end of the first contact.

TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

SELF-ALIGNED CONTACTS IN THREE-DIMENSIONAL MEMORY DEVICES AND METHODS FOR FORMING THE SAME

BACKGROUND

[0001] Embodiments of the present disclosure relate to three-dimensional (3D) memory devices and fabrication methods thereof.

[0002] Planar memory cells are scaled to smaller sizes by improving process technology, circuit design, programming algorithm, and fabrication process. However, as feature sizes of the memory cells approach a lower limit, planar process and fabrication techniques become challenging and costly. As a result, memory density for planar memory cells approaches an upper limit.

[0003] A 3D memory architecture can address the density limitation in planar memory cells. The 3D memory architecture includes a memory array and peripheral devices for controlling signals to and from the memory array.

SUMMARY

[0004] Embodiments of 3D memory devices and methods for forming the same are disclosed herein.

[0005] In one example, a 3D memory device includes a substrate, a memory stack including interleaved conductive layers and dielectric layers above the substrate, a structure extending vertically through the memory stack, a first dielectric layer on the memory stack, an etch stop layer on the first dielectric layer, a second dielectric layer on the etch stop layer, a first contact through the etch stop layer and the first dielectric layer and in contact with an upper end of the structure, and a second contact through the second dielectric layer and in contact with at least an upper end of the first contact.

[0006] In another example, a method for forming a 3D memory device is disclosed. A structure extending vertically through a memory stack including interleaved conductive layers and dielectric layers is formed above a substrate. A first dielectric layer is formed on the memory stack. An etch stop layer is formed on the first dielectric layer. A first contact is formed through the etch stop layer and the first dielectric layer and in contact with an upper end of the structure. A second dielectric layer is formed on the etch stop

- 2 -

layer. A second contact is formed through the second dielectric layer and in contact with at least an upper end of the first contact.

[0007] In still another example, a method for forming a 3D memory device is disclosed. A channel structure extending vertically through a memory stack including interleaved conductive layers and dielectric layers is formed above a substrate. A first silicon oxide layer is deposited on the memory stack. A silicon nitride layer is deposited on the first silicon oxide layer. A first contact opening is etched through the silicon nitride layer and the first silicon oxide layer until being stopped by an upper end of the channel structure. The first contact opening is filled with a metal material to form a first contact in contact with the upper end of the channel structure. A second silicon oxide layer is deposited on the silicon nitride layer. A second contact opening is etched through the second silicon oxide layer until being stopped by an upper end of the first contact and the silicon nitride layer. The second contact opening is filled with the metal material to form the second contact in contact with the upper end of the first contact and the silicon nitride layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.

[0009] FIG. 1A illustrates a cross-section of an exemplary 3D memory device with self-aligned contacts, according to some embodiments of the present disclosure.

[0010] FIG. 1B illustrates a cross-section of another exemplary 3D memory device with self-aligned contacts, according to some embodiments of the present disclosure.

[0011] FIGs. 2A–2F illustrate a fabrication process for forming an exemplary 3D memory device with self-aligned contacts, according to some embodiments of the present disclosure.

[0012] FIG. 3 illustrates a flowchart of a method for forming an exemplary 3D memory device with self-aligned contacts, according to some embodiments of the present disclosure.

[0013] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

[0014] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.

[0015] It is noted that references in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” “some embodiments,” etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to effect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0016] In general, terminology may be understood at least in part from usage in context. For example, the term “one or more” as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as “a,” “an,” or “the,” again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term “based on” may be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0017] It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something but also includes the meaning of “on” something with an intermediate feature or a layer therebetween, and that “above” or “over” not only means the meaning of “above” or “over” something but can also include the meaning it is “above” or “over” something with no intermediate feature or layer therebetween (i.e., directly on something).

- [0018]** Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.
- [0019]** As used herein, the term “substrate” refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.
- [0020]** As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which interconnect lines and/or via contacts are formed) and one or more dielectric layers.
- [0021]** As used herein, the term “nominal/nominally” refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term “about” indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term

- 5 -

“about” can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., $\pm 10\%$, $\pm 20\%$, or $\pm 30\%$ of the value).

[0022] As used herein, the term “3D memory device” refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as “memory strings,” such as NAND memory strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term “vertical/vertically” means nominally perpendicular to the lateral surface of a substrate.

[0023] In 3D memory devices fabrication, it is often necessary to achieve precise alignment and overlay control between structures fabricated at different lithographic stages. Tighter alignment tolerances and overlay issues become exasperated as the memory density and interconnect density continue increasing. For example, the misalignment and partial overlap of contacts in different layers may cause yield loss due to a short circuit with the misaligned contact.

[0024] Various embodiments in accordance with the present disclosure provide self-aligned contacts in 3D memory devices with relaxed alignment and overlay constraints. As a result, short circuits with misaligned contacts can be prevented to minimize yield loss. The self-aligned contacts are applicable to various interconnect structures in 3D memory devices, such as the local contacts (known as “C1”) and the contacts right above (known as “V0”) for channel structures and slit structures (e.g., functioning as array common source “ACS”).

[0025] FIG. 1A illustrates a cross-section of an exemplary 3D memory device 100 with self-aligned contacts, according to some embodiments of the present disclosure. 3D memory device 100 can include a substrate 102, which can include silicon (e.g., single crystalline silicon), silicon germanium (SiGe), gallium arsenide (GaAs), germanium (Ge), silicon on insulator (SOI), germanium on insulator (GOI), or any other suitable materials. In some embodiments, substrate 102 is a thinned substrate (e.g., a semiconductor layer), which was thinned by grinding, etching, chemical mechanical polishing (CMP), or any combination thereof.

[0026] 3D memory device 100 can be part of a monolithic 3D memory device. The term “monolithic” means that the components (e.g., the peripheral device and memory array device) of the 3D memory device are formed on a single substrate. For monolithic 3D

- 6 -

memory devices, the fabrication encounters additional restrictions due to the convolution of the peripheral device processing and the memory array device processing. For example, the fabrication of the memory array device (e.g., NAND memory strings) is constrained by the thermal budget associated with the peripheral devices that have been formed or to be formed on the same substrate.

[0027] Alternatively, 3D memory device 100 can be part of a non-monolithic 3D memory device, in which components (e.g., the peripheral device and memory array device) can be formed separately on different substrates and then bonded, for example, in a face-to-face manner. In some embodiments, the memory array device substrate (e.g., substrate 102) remains as the substrate of the bonded non-monolithic 3D memory device, and the peripheral device (e.g., including any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of 3D memory device 100, such as page buffers, decoders, and latches; not shown) is flipped and faces down toward the memory array device (e.g., NAND memory strings) for hybrid bonding. It is understood that in some embodiments, the memory array device substrate (e.g., substrate 102) is flipped and faces down toward the peripheral device (not shown) for hybrid bonding, so that in the bonded non-monolithic 3D memory device, the memory array device is above the peripheral device. The memory array device substrate (e.g., substrate 102) can be a thinned substrate (which is not the substrate of the bonded non-monolithic 3D memory device), and the back-end-of-line (BEOL) interconnects of the non-monolithic 3D memory device can be formed on the backside of the thinned memory array device substrate.

[0028] In some embodiments, 3D memory device 100 is a NAND Flash memory device in which memory cells are provided in the form of an array of NAND memory strings each extending vertically above substrate 102. The memory array device can include an array of channel structures 104 functioning as the array of NAND memory strings. As shown in FIG. 1, channel structure 104 can extend vertically through a plurality of pairs each including a conductive layer 106 and a dielectric layer 108. The interleaved conductive layers 106 and dielectric layers 108 are part of a memory stack 110. The number of the pairs of conductive layers 106 and dielectric layers 108 in memory stack 110 (e.g., 32, 64, 96, or 128) determines the number of memory cells in 3D memory device 100. It is understood that in some embodiments, memory stack 110 may have a

- 7 -

multi-deck architecture (not shown), which includes a plurality of memory decks stacked over one another. The numbers of the pairs of conductive layers 106 and dielectric layers 108 in each memory deck can be the same or different.

[0029] Memory stack 110 can include a plurality of interleaved conductive layers 106 and dielectric layers 108. Conductive layers 106 and dielectric layers 108 in memory stack 110 can alternate in the vertical direction. In other words, except the ones at the top or bottom of memory stack 110, each conductive layer 106 can be adjoined by two dielectric layers 108 on both sides, and each dielectric layer 108 can be adjoined by two conductive layers 106 on both sides. Conductive layers 106 can include conductive materials including, but not limited to, tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), polysilicon, doped silicon, silicides, or any combination thereof. Each conductive layer 106 can be a gate electrode (gate line) surrounding channel structure 104 and can extend laterally as a word line. Dielectric layers 108 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.

[0030] As shown in FIG. 1, channel structure 104 can include a channel hole filled with a semiconductor layer (e.g., as a semiconductor channel 112) and a composite dielectric layer (e.g., as a memory film 114). In some embodiments, semiconductor channel 112 includes silicon, such as amorphous silicon, polysilicon, or single-crystal silicon. In some embodiments, memory film 114 is a composite layer including a tunneling layer, a storage layer (also known as a “charge trap layer”), and a blocking layer. The remaining space of channel structure 104 can be partially or fully filled with a capping layer 118 including dielectric materials, such as silicon oxide, and/or an air gap. Channel structure 104 can have a cylinder shape (e.g., a pillar shape). Capping layer 118, semiconductor channel 112, the tunneling layer, storage layer, and blocking layer of memory film 114 are arranged radially from the center toward the outer surface of the pillar in this order, according to some embodiments. The tunneling layer can include silicon oxide, silicon oxynitride, or any combination thereof. The storage layer can include silicon nitride, silicon oxynitride, silicon, or any combination thereof. The blocking layer can include silicon oxide, silicon oxynitride, high dielectric constant (high-k) dielectrics, or any combination thereof. In one example, memory film 114 can include a composite layer of silicon oxide/silicon oxynitride/silicon oxide (ONO).

[0031] In some embodiments, channel structure 104 further includes a semiconductor plug 120 in the lower portion (e.g., at the lower end) of channel structure 104. As used herein, the “upper end” of a component (e.g., channel structure 104) is the end farther away from substrate 102 in the y-direction, and the “lower end” of the component (e.g., channel structure 104) is the end closer to substrate 102 in the y-direction when substrate 102 is positioned in the lowest plane of 3D memory device 100. Semiconductor plug 120 can include a semiconductor material, such as silicon, which is epitaxially grown from substrate 102 in any suitable directions. It is understood that in some embodiments, semiconductor plug 120 includes single-crystal silicon, the same material of substrate 102. In other words, semiconductor plug 120 can include an epitaxially-grown semiconductor layer that is the same material as substrate 102. Semiconductor plug 120 can be below and in contact with the lower end of semiconductor channel 112. Semiconductor plug 120 can function as a channel controlled by a source select gate of the NAND memory string.

[0032] In some embodiments, channel structure 104 further includes a channel plug 122 in the upper portion (e.g., at the upper end) of channel structure 104. Channel plug 122 can be above and in contact with the upper end of semiconductor channel 112. Channel plug 122 can include semiconductor materials (e.g., polysilicon). In some embodiments, channel plug 122 includes an opening filled with a conductive layer, including a metal material such as tungsten. By covering the upper end of channel structure 104 during the fabrication of 3D memory device 100, channel plug 122 can function as an etch stop layer to prevent etching of dielectrics filled in channel structure 104. In some embodiments, channel plug 122 can function as the drain of the NAND memory string.

[0033] As shown in FIG. 1, 3D memory device 100 includes a local contact layer 130 on memory stack 110 as part of the interconnect structure. Local contact layer 130 can include a first dielectric layer 124 formed on memory stack 110. In some embodiments, first dielectric layer 124 is formed on the upper end of channel structure 104 and the top surface of memory stack 110 without any intervening layer. First dielectric layer 124 can include one or more interlayer dielectric (ILD) layers (also known as “intermetal dielectric (IMD) layers”). First dielectric layer 124 of local contact layer 130 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, low dielectric constant (low-k) dielectrics, or any combination thereof. In

some embodiments, the dielectric material of first dielectric layer 124 includes silicon oxide.

[0034] As shown in FIG. 1, 3D memory device 100 also includes an etch stop layer 126 on first dielectric layer 124 of local contact layer 130. In some embodiments, etch stop layer 126 is formed on the top surface of first dielectric layer 124 without any intervening layer. Etch stop layer 126 can include dielectric materials including, but not limited to, silicon nitride, silicon oxynitride, high dielectric constant (high-k) dielectrics, or any combination thereof. The high-k dielectrics can include aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), zirconium oxide (ZrO_2), to name a few. In some embodiments, etch stop layer 126 includes a dielectric material that is different from the dielectric material of first dielectric layer 124. For example, the dielectric material of etch stop layer 126 includes silicon nitride, and the dielectric material of first dielectric layer 124 includes silicon oxide. It is understood that in some embodiments, first dielectric layer 124 and etch stop layer 126 may have the same dielectric material.

[0035] Local contact layer 130 can include a plurality of interconnects (also referred to herein as “contacts”), including lateral interconnect lines and vertical interconnect access (via) contacts. As used herein, the term “interconnects” can broadly include any suitable types of interconnects, such as middle-end-of-line (MEOL) interconnects and back-end-of-line (BEOL) interconnects. The interconnects in local contact layer 130 are referred to herein as “local contacts” (also known as “C1”), which are in contact with a structure in memory stack 110 directly. As shown in FIG. 1, local contact layer 130 includes a first contact 128 (e.g., a local contact for channel structure 104) above and in contact with the upper end of channel structure 104 (e.g., channel plug 122). The local contacts, including first contact 128, in local contact layer 130 can include conductive materials including, but not limited to, Cu, Al, W, Co, silicides, or any combination thereof. In some embodiments, the conductive material of first contact 128 includes tungsten.

[0036] The local contacts, including first contact 128, in local contact layer 130 are formed through first dielectric layer 124. That is, local contact layer 130 can include first dielectric layer 124 and first contact 128 therethrough. As shown in FIG. 1, first contact 128 extends further through etch stop layer 126. That is, first contact 128 is formed through both first dielectric layer 124 and etch stop layer 126 and in contact with the

- 10 -

upper end of channel structure 104. In some embodiments, the upper end of first contact 128 is flush with the top surface of etch stop layer 126.

[0037] As shown in FIG. 1, 3D memory device 100 further includes an interconnect layer 136 on etch stop layer 126 as part of the interconnect structure. Interconnect layer 136 can include a second dielectric layer 132 formed on etch stop layer 126. In some embodiments, second dielectric layer 132 is formed on the top surface of etch stop layer 126 without any intervening layer. Second dielectric layer 132 can include one or more ILD layers. Second dielectric layer 132 of interconnect layer 136 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, low-k dielectrics, or any combination thereof. In some embodiments, the dielectric material of second dielectric layer 132 is the same as the dielectric material of first dielectric layer 124. For example, the dielectric material of first and second dielectric layers 124 and 132 includes silicon oxide.

[0038] In some embodiments, the dielectric material of second dielectric layer 132 is different from the dielectric material of etch stop layer 126. Moreover, in order for etch stop layer 126 to function (i.e., automatically stop the etching of second dielectric layer 132 when the etching reaches to etch stop layer 126), the etch selectivity between the dielectric material of second dielectric layer 132 and the dielectric material of etch stop layer 126 is not less than about 5:1, such as not less than 5:1 (e.g., 5:1, 6:1, 7:1, 8:1, 9:1, 10:1, 11:1, 12:1, 13:1, 14:1, 15:1, 16:1, 17:1, 18:1, 19:1, 20:1, 25:1, 30:1, 40:1, 50:1, 60:1, 70:1, 80:1, 90:1, 100:1, 200:1, 300:1, 400:1, 500:1, any range bounded by the lower end by any of these values, or in any range defined by any two of these values). In some embodiments, the dielectric material of second dielectric layer 132 includes silicon oxide, and the dielectric material of etch stop layer includes silicon nitride with an etch selectivity greater than 50:1 over silicon nitride.

[0039] Due to the structures (e.g., second dielectric layer 132 on etch stop layer 126) and materials (e.g., different dielectric materials with a high etch selectivity) of etch stop layer 126 and second dielectric layer 132, etching of second dielectric layer 132 for forming any contact therethrough is stopped by etch stop layer 126. As a result, interconnect layer 136 can include a plurality of self-aligned contacts (SACs, also known as “V0”) including a second contact 134 (e.g., a V0 via contact for channel structure 104) in contact with at least the upper end of first contact 128. The contacts, including second contact 134, in

- 11 -

interconnect layer 136 can include conductive materials including, but not limited to, Cu, Al, W, Co, silicides, or any combination thereof. In some embodiments, the conductive material of second contact 134 includes tungsten. In some embodiments, the critical dimension of first contact 128 is greater than the critical dimension of second contact 134. For example, the diameter of first contact 128 (e.g., a via contact) may be greater than the diameter of second contact 134 (e.g., a via contact). As a result, when second contact 134 is well aligned with first contact 128, second contact 134 can fully land on first contact 128 as part of the electrical connection for channel structure 104, for example, with a bit line.

[0040] The contacts, including second contact 134, in interconnect layer 136 are formed through second dielectric layer 132. That is, interconnect layer 136 can include second dielectric layer 132 and second contact 134 therethrough. As shown in FIG. 1, second contact 134 is formed through second dielectric layer 132 and in contact with the upper end of first contact 128 as well as the top surface of etch stop layer 126. In some embodiments, the lower end of second contact 134 is flush with the top surface of etch stop layer 126. That is, even if second contact 134 does not fully land on first contact 128 due to misalignment (e.g., as shown in FIG. 1), the portion of second contact 134 outside of first contact 128 cannot extend further through etch stop layer 126 to form a short circuit, for example, with components in memory stack 110 (e.g., conductive layers 106) after extending through first dielectric layer 124. As a result, the alignment margin and overlay control between first and second contacts 128 and 134 can be relaxed by the SAC scheme with etch stop layer 126. It is understood that in some embodiments, second contact 134 may be well aligned with first contact 128, such that second contact 134 fully lands on first contact 128 without being in contact with etch stop layer 126.

[0041] It is understood that the SAC scheme with etch stop layer 126 described above with respect to FIG. 1 is not limited to the interconnect structure for channel structure 104 and can be applied to the interconnect structures or any other suitable structures extending vertically through memory stack 110, such as slit structures, through array contacts (TACs), etc. FIG. 1B illustrates a cross-section of another exemplary 3D memory device 101 with self-aligned contacts, according to some embodiments of the present disclosure. Different from 3D memory device 100 described above in FIG. 1A, 3D memory device 101 in FIG. 1B further includes a slit structure 103 having an interconnect structure

- 12 -

employing the SAC scheme with etch stop layer 126. It is understood that the details of similar structures (e.g., materials, fabrication process, functions, etc.) in both 3D memory devices 100 and 101 may not be repeated below.

[0042] As shown in FIG. 1B, 3D memory device 101 further includes slit structure 103 extending vertically through interleaved conductive layers 106 and dielectric layers 108 of memory stack 110. Slit structure 103 can also extend laterally to separate memory stack 110 into multiple blocks. Slit structure 103 can include a slit opening that provides access for the chemical precursor to form conductive layers 106. In some embodiments, slit structure 103 includes a source conductive layer 105 having conductive materials including, but not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof. In some embodiments, source conductive layer 105 includes polysilicon in the lower portion of the slit opening and a metal (e.g., tungsten) in the upper portion of the slit opening. To electrically isolate source conductive layer 105 from conductive layers 106, slit structure 103 can further include a spacer 107 disposed along the sidewall of the slit opening and in etch-back recesses (not shown) abutting the sidewall of the slit opening. That is, spacer 107 can be formed between source conductive layer 105 and conductive layers 106 in memory stack 110. Spacer 107 can include one or more layers of dielectric materials, such as silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. In some embodiments, source conductive layer 105 of slit structure 103 works as the source contact of 3D memory device 101 and electrically connects to the source of the NAND memory string, e.g., an array common source (ACS) of the array of NAND memory strings. In some embodiments, slit structure 103 further includes a doped region 109 at its lower end in substrate 102 to reduce the resistance of the electrical connection with the ACS.

[0043] As shown in FIG. 1B, local contact layer 130 can further include another first contact 111 (e.g., the local contact for slit structure 103) through first dielectric layer 124 and in contact with the upper end of slit structure 103. Similar to first contact 128, another first contact 111 is formed through both etch stop layer 126 and first dielectric layer 124, according to some embodiments. The upper surface of another first contact 111 can be flush with the top surface of etch stop layer 126. Interconnect layer 136 can include another second contact 113 as another SAC with relaxed alignment margin and overlay control with another first contact 111 as described above in detail. The lower

surface of another second contact 113 can be flush with the top surface of etch stop layer 126. It is to be understood that the number of interconnect layers in 3D memory devices 100 and 101 is not limited by the examples in FIGs. 1A and 1B. Additional interconnect layer(s) with contacts can be formed using the SAC scheme disclosed herein.

[0044] FIGs. 2A–2F illustrate a fabrication process for forming an exemplary 3D memory device with self-aligned contacts, according to some embodiments of the present disclosure. FIG. 3 illustrates a flowchart of a method 300 for forming an exemplary 3D memory device with self-aligned contacts, according to some embodiments of the present disclosure. Examples of the 3D memory device depicted in FIGs. 2A–2F and 3 include 3D memory device 100 depicted in FIG. 1A. FIGs. 2A–2F and 3 will be described together. It is understood that the operations shown in method 300 are not exhaustive and that other operations can be performed as well before, after, or between any of the illustrated operations. Further, some of the operations may be performed simultaneously, or in a different order than shown in FIG. 3.

[0045] Referring to FIG. 3, method 300 starts at operation 302, in which a structure extending vertically through a memory stack including interleaved conductive layers and dielectric layers is formed above a substrate. The structure is a channel structure or a slit structure, according to some embodiments. The substrate can be a silicon substrate.

[0046] Referring to FIG. 2A, a memory stack 204 including a plurality pairs of a conductive layer 206 and a dielectric layer 208 is formed above a silicon substrate 202. In some embodiments, memory stack 204 is formed by a “gate-first” process in which dielectric layers 208 and conductive layers 206 are alternately deposited on silicon substrate 202 using one or more thin film deposition processes including, but not limited to, chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), or any combination thereof. In some embodiments, memory stack 204 is formed by a “gate-last” process in which a dielectric stack (not shown) including dielectric layers 208 and sacrificial layers (not shown) are alternately deposited on silicon substrate 202 using one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, or any combination thereof. Memory stack 204 can then be formed by a “gate-replacement” process, which replaces the sacrificial layers with conductive layers 206 using an etching process to remove the sacrificial layers and a thin

film deposition process to deposit conductive layers 206 at the places where the sacrificial layers were formed.

[0047] As illustrated in FIG. 2A, a channel structure 210 extending vertically through interleaved dielectric layers 208 and conductive layers 206 of memory stack 204 is formed above silicon substrate 202. It is understood that although channel structure 210 is illustrated, any other suitable structures that extending vertically through memory stack 204, including slit structures (e.g., slit structure 103 in FIG. 1B) may be applicable as well although the detailed fabrication processes for forming those structures as known in the art are not described herein. To form channel structure 210, a channel hole is first etched through memory stack 204 (or the dielectric stack) using wet etching and/or dry etching, such as deep-ion reactive etching (DRIE). In some embodiments, the channel hole of channel structure 210 extends further through the top portion of silicon substrate 202. As illustrated in FIG. 2A, a semiconductor plug 218 can be formed by filling the lower portion of the channel hole with single-crystal silicon epitaxially grown from silicon substrate 202 in any suitable directions (e.g., from the bottom surface and/or side surface). The fabrication processes for epitaxially growing semiconductor plug 218 can include, but not limited to, vapor-phase epitaxy (VPE), liquid-phase epitaxy (LPE), molecular-beam epitaxy (MPE), or any combinations thereof.

[0048] As illustrated in FIG. 2A, a memory film 212 (including a blocking layer, a storage layer, and a tunneling layer) and a semiconductor channel 214 are formed along the sidewall of the channel hole of channel structure 210 and above semiconductor plug 218. In some embodiments, memory film 212 is first deposited along the sidewall of the channel hole and above semiconductor plug 218, and semiconductor channel 214 is then deposited over memory film 212. The blocking layer, storage layer, and tunneling layer can be subsequently deposited in this order using one or more thin film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof, to form memory film 212. Semiconductor channel 214 can then be formed by depositing polysilicon on the tunneling layer using one or more thin film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof. Semiconductor channel 214 can be in contact with semiconductor plug 218 using, for example, a SONO punch process. In some embodiments, semiconductor channel 214 is deposited in the channel hole without completely filling the channel hole. As

- 15 -

illustrated in FIG. 2A, a capping layer 216, such as a silicon oxide layer, is formed in the channel hole to fully or partially fill the remaining space of the channel hole using one or more thin film deposition processes, such as CVD, PVD, ALD, electroplating, electroless plating, or any combination thereof.

[0049] As illustrated in FIG. 2A, a channel plug 220 is formed in the upper portion of the channel hole of channel structure 210. A recess can then be formed in the upper portion of the channel hole by wet etching and/or drying etching parts of memory film 212, semiconductor channel 214, and capping layer 216 in the upper portion of the channel hole. Channel plug 220 can then be formed by depositing semiconductor materials, such as polysilicon, and/or metals, such as tungsten, into the recess by one or more thin film deposition processes, such as CVD, PVD, ALD, electroplating, electroless plating, or any combination thereof. Channel structure 210 is thereby formed through memory stack 204 (or the dielectric stack).

[0050] Method 300 proceeds to operation 304, as illustrated in FIG. 3, in which a first dielectric layer is formed on the memory stack. In some embodiments, the first dielectric layer includes silicon oxide. As illustrated in FIG. 2A, a first dielectric layer 222 is formed on memory stack 204 (or the dielectric stack). First dielectric layer 222 can be formed by depositing dielectric materials, such as silicon oxide, using one or more thin film deposition processes, such as CVD, PVD, ALD, or any combination thereof, on the upper end of channel structure 210 and the top surface of memory stack 204 (or the dielectric stack).

[0051] Method 300 proceeds to operation 306, as illustrated in FIG. 3, in which an etch stop layer is formed on the first dielectric layer. The etch stop layer can include a dielectric material including at least one of silicon nitride, silicon oxynitride, or high-k dielectrics. In some embodiments, the dielectric material includes silicon nitride. As illustrated in FIG. 2A, an etch stop layer 224 is formed on first dielectric layer 222. Etch stop layer 224 can be formed by depositing dielectric materials, such as silicon nitride, using one or more thin film deposition processes, such as CVD, PVD, ALD, or any combination thereof, on the top surface of first dielectric layer 222.

[0052] Method 300 proceeds to operation 308, as illustrated in FIG. 3, in which a first contact is formed through the etch stop layer and the first dielectric layer and in contact with an upper end of the structure. In some embodiments, to form the first contact, a first

- 16 -

contact opening is etched through the etch stop layer and the first dielectric layer until being stopped by the structure, and the first contact opening is filled with a conductive material to form the first contact. In some embodiments, the conductive material includes a metal material, such as tungsten. In some embodiments, the upper end of the first contact is flush with a top surface of the etch stop layer.

[0053] As illustrated in FIG. 2A, an etch mask 226 is patterned on etch stop layer 224 with an etch opening 228 aligned with channel structure 210. Etch opening 228 can expose part of etch stop layer 224 that is to be removed later. Etch mask 226 can be patterned by first coating a photoresist layer using spin coating, followed by photolithography and photoresist development processes to form etch opening 228 aligned with channel structure 210. In some embodiments, a hard mask is patterned under the photoresist layer as part of etch mask 226 using wet etching and/or dry etching processes.

[0054] As illustrated in FIG. 2B, a first contact opening 230 is etched through etch stop layer 224 and first dielectric layer 222 until being stopped by the upper end of channel structure 210 (i.e., channel plug 220) using one or more wet etching and/or dry etching processes, such as RIE. First contact opening 230 can be etched from etch opening 228 (shown in FIG. 2A) of etch mask 226 as other areas of etch stop layer 224 and first dielectric layer 222 are covered by etch mask 226. As a result, the upper end of channel structure 210 can be exposed by first contact opening 230.

[0055] As illustrated in FIG. 2C, a first contact 232 is formed through etch stop layer 224 and first dielectric layer 222 and in contact with the upper end of channel structure 210 (i.e., channel plug 220). In some embodiments, to form first contact 232, first contact opening 230 (shown in FIG. 2B) is filled with a conductive material, such as a metal material (e.g., tungsten), using one or more thin film deposition processes, such as CVD, PVD, ALD, electroplating, electroless plating, or any combination thereof. A CMP process can be performed to remove the excess conductive material and planarize the top surface of etch stop layer 224.

[0056] Method 300 proceeds to operation 310, as illustrated in FIG. 3, in which a second dielectric layer is formed on the etch stop layer. In some embodiments, the second dielectric layer includes a dielectric material that is different from the dielectric material of the etch stop layer. In some embodiments, the etch selectivity between the dielectric

material of the second dielectric layer and the dielectric material of the etch stop layer is not less than about 5:1. For example, the dielectric material of the second dielectric layer may include silicon oxide.

[0057] As illustrated in FIG. 2D, a second dielectric layer 234 is formed on etch stop layer 224. Second dielectric layer 234 can be formed by depositing dielectric materials, such as silicon oxide, using one or more thin film deposition processes, such as CVD, PVD, ALD, or any combination thereof, on the top surface of etch stop layer 224.

[0058] Method 300 proceeds to operation 312, as illustrated in FIG. 3, in which a second contact is formed through the second dielectric layer and in contact with at least an upper end of the first contact. In some embodiments, to form the first contact, a second contact opening is etched through the second dielectric layer until being stopped by the first contact and the etch stop layer, and the second contact opening is filled with a conductive material to form the second contact in contact with the upper end of the first contact and the etch stop layer. In some embodiments, the conductive material includes a metal material, such as tungsten. In some embodiments, a lower end of the second contact is flush with the top surface of the etch stop layer. In some embodiments, a critical dimension of the first contact is greater than a critical dimension of the second contact.

[0059] As illustrated in FIG. 2D, an etch mask 236 is patterned on second dielectric layer 234 with an etch opening 238 aligned with first contact 232. Etch opening 238 can expose part of second dielectric layer 234 that is to be removed later. Etch mask 236 can be patterned by first coating a photoresist layer using spin coating, followed by photolithography and photoresist development processes to form etch opening 238 aligned with first contact 232. In some embodiments, a hard mask is patterned under the photoresist layer as part of etch mask 236 using wet etching and/or dry etching processes. It is understood that etch opening 238 may not be well aligned with first contact 232, for example, only partially overlapping with first contact 232.

[0060] As illustrated in FIG. 2E, a second contact opening 240 is etched through second dielectric layer 234 until being stopped by the upper end of first contact 232 using one or more wet etching and/or dry etching processes, such as RIE. Second contact opening 240 can be etched from etch opening 238 (shown in FIG. 2D) of etch mask 236 as other areas of second dielectric layer 234 are covered by etch mask 236. As a result, the upper end of first contact 232 can be exposed by second contact opening 240. It is understood that in

- 18 -

case etch opening 238 is not well aligned with first contact 232, for example, only partially overlapping with first contact 232, second contact opening 240 is etched through second dielectric layer 234 until being stopped by the upper end of first contact 232 as well as etch stop layer 224 due to the high etch selectivity (e.g., not less than about 5:1) between the dielectric materials of second dielectric layer 234 and etch stop layer 224 (e.g., silicon oxide and silicon nitride). That is, etch stop layer 224 can prevent the etching of second dielectric layer 234 to go further below to cause any short circuits after depositing a conductive material into second contact opening 240 even when etch opening 238 is not well aligned with first contact 232 in some cases, which relaxes the alignment margin when forming etch opening 238 and second contact opening 240.

[0061] As illustrated in FIG. 2F, a second contact 242 is formed through second dielectric layer 234 and in contact with the upper end of first contact 232. In some embodiments, to form second contact 242, second contact opening 240 (shown in FIG. 2E) is filled with a conductive material, such as a metal material (e.g., tungsten), using one or more thin film deposition processes, such as CVD, PVD, ALD, electroplating, electroless plating, or any combination thereof. In some embodiments, the critical dimension of first contact 232 is greater than the critical dimension of second contact 242. For example, the diameter of first contact 232 (e.g., a via contact) may be greater than the diameter of second contact 242 (e.g., a via contact). It is understood that in some embodiments, second contact 242 may be well aligned with first contact 232, such that second contact 242 may fully land on first contact 232 without being in contact with etch stop layer 224. It is further understood that even when second contact 242 is not well aligned with first contact 232, second contact 242 may land on first contact 232 and etch stop layer 224 without making any contact with structures below etch stop layer 224 to cause a short circuit.

[0062] According to one aspect of the present disclosure, a 3D memory device includes a substrate, a memory stack including interleaved conductive layers and dielectric layers above the substrate, a structure extending vertically through the memory stack, a first dielectric layer on the memory stack, an etch stop layer on the first dielectric layer, a second dielectric layer on the etch stop layer, a first contact through the etch stop layer and the first dielectric layer and in contact with an upper end of the structure, and a second contact through the second dielectric layer and in contact with at least an upper end of the first contact.

- [0063] In some embodiments, the second contact is in contact with the upper end of the first contact and the etch stop layer.
- [0064] In some embodiments, the second dielectric layer includes a first dielectric material, and the etch stop layer includes a second dielectric material different from the first dielectric material. In some embodiments, an etch selectivity between the first dielectric material and the second dielectric material is not less than about 5:1. In some embodiments, the first dielectric material includes silicon oxide. In some embodiments, the second dielectric material includes at least one of silicon nitride, silicon oxynitride, or high-k dielectrics.
- [0065] In some embodiments, the structure is a channel structure or a slit structure.
- [0066] In some embodiments, a critical dimension of the first contact is greater than a critical dimension of the second contact.
- [0067] In some embodiments, the upper end of the first contact is flush with a top surface of the etch stop layer. In some embodiments, a lower end of the second contact is flush with the top surface of the etch stop layer.
- [0068] According to another aspect of the present disclosure, a method for forming a 3D memory device is disclosed. A structure extending vertically through a memory stack including interleaved conductive layers and dielectric layers is formed above a substrate. A first dielectric layer is formed on the memory stack. An etch stop layer is formed on the first dielectric layer. A first contact is formed through the etch stop layer and the first dielectric layer and in contact with an upper end of the structure. A second dielectric layer is formed on the etch stop layer. A second contact is formed through the second dielectric layer and in contact with at least an upper end of the first contact.
- [0069] In some embodiments, to form the second contact, a second contact opening is etched through the second dielectric layer until being stopped by the first contact and the etch stop layer, and the second contact opening is filled with a conductive material to form the second contact in contact with the upper end of the first contact and the etch stop layer.
- [0070] In some embodiments, to form the first contact, a first contact opening is etched through the etch stop layer and the first dielectric layer until being stopped by the structure, and the first contact opening is filled with a conductive material to form the first contact.

- [0071] In some embodiments, the second dielectric layer includes a first dielectric material, and the etch stop layer includes a second dielectric material different from the first dielectric material. In some embodiments, an etch selectivity between the first dielectric material and the second dielectric material is not less than about 5:1. In some embodiments, the first dielectric material includes silicon oxide. In some embodiments, the second dielectric material includes at least one of silicon nitride, silicon oxynitride, or high-k dielectrics.
- [0072] In some embodiments, a critical dimension of the first contact is greater than a critical dimension of the second contact.
- [0073] In some embodiments, the upper end of the first contact is flush with a top surface of the etch stop layer. In some embodiments, a lower end of the second contact is flush with the top surface of the etch stop layer.
- [0074] According to still another aspect of the present disclosure, a method for forming a 3D memory device is disclosed. A channel structure extending vertically through a memory stack including interleaved conductive layers and dielectric layers is formed above a substrate. A first silicon oxide layer is deposited on the memory stack. A silicon nitride layer is deposited on the first silicon oxide layer. A first contact opening is etched through the silicon nitride layer and the first silicon oxide layer until being stopped by an upper end of the channel structure. The first contact opening is filled with a metal material to form a first contact in contact with the upper end of the channel structure. A second silicon oxide layer is deposited on the silicon nitride layer. A second contact opening is etched through the second silicon oxide layer until being stopped by an upper end of the first contact and the silicon nitride layer. The second contact opening is filled with the metal material to form the second contact in contact with the upper end of the first contact and the silicon nitride layer.
- [0075] In some embodiments, the metal material includes tungsten.
- [0076] In some embodiments, a critical dimension of the first contact is greater than a critical dimension of the second contact.
- [0077] In some embodiments, the upper end of the first contact is flush with a top surface of the etch stop layer. In some embodiments, a lower end of the second contact is flush with the top surface of the silicon nitride layer.

- [0078]** The foregoing description of the specific embodiments will so reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.
- [0079]** Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.
- [0080]** The Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.
- [0081]** The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A three-dimensional (3D) memory device, comprising:
 - a substrate;
 - a memory stack comprising interleaved conductive layers and dielectric layers above the substrate;
 - a structure extending vertically through the memory stack;
 - a first dielectric layer on the memory stack;
 - an etch stop layer on the first dielectric layer;
 - a second dielectric layer on the etch stop layer;
 - a first contact through the etch stop layer and the first dielectric layer and in contact with an upper end of the structure; and
 - a second contact through the second dielectric layer and in contact with at least an upper end of the first contact.
2. The 3D memory device of claim 1, wherein the second contact is in contact with the upper end of the first contact and the etch stop layer.
3. The 3D memory device of claim 1 or 2, wherein the second dielectric layer comprises a first dielectric material, and the etch stop layer comprises a second dielectric material different from the first dielectric material.
4. The 3D memory device of claim 3, wherein an etch selectivity between the first dielectric material and the second dielectric material is not less than about 5:1.
5. The 3D memory device of claim 3 or 4, wherein the first dielectric material comprises silicon oxide.
6. The 3D memory device of any one of claims 3-5, wherein the second dielectric material comprises at least one of silicon nitride, silicon oxynitride, or high dielectric constant (high-k) dielectrics.

- 23 -

7. The 3D memory device of any one of claims 1-6, wherein the structure is a channel structure or a slit structure.

8. The 3D memory device of any one of claims 1-7, wherein a critical dimension of the first contact is greater than a critical dimension of the second contact.

9. The 3D memory device of any one of claims 1-8, wherein the upper end of the first contact is flush with a top surface of the etch stop layer.

10. The 3D memory device of claim 9, wherein a lower end of the second contact is flush with the top surface of the etch stop layer.

11. A method for forming a three-dimensional (3D) memory device, comprising:
forming a structure extending vertically through a memory stack comprising interleaved conductive layers and dielectric layers above a substrate;
forming a first dielectric layer on the memory stack;
forming an etch stop layer on the first dielectric layer;
forming a first contact through the etch stop layer and the first dielectric layer and in contact with an upper end of the structure;
forming a second dielectric layer on the etch stop layer; and
forming a second contact through the second dielectric layer and in contact with at least an upper end of the first contact.

12. The method of claim 11, wherein forming the second contact comprises:
etching a second contact opening through the second dielectric layer until being stopped by the first contact and the etch stop layer; and
filling the second contact opening with a conductive material to form the second contact in contact with the upper end of the first contact and the etch stop layer.

13. The method of claim 11 or 12, wherein forming the first contact comprises:
etching a first contact opening through the etch stop layer and the first dielectric layer until being stopped by the structure; and

- 24 -

filling the first contact opening with a conductive material to form the first contact.

14. The method of any one of claims 11-13, wherein the second dielectric layer comprises a first dielectric material, and the etch stop layer comprises a second dielectric material different from the first dielectric material.

15. The method of claim 14, wherein an etch selectivity between the first dielectric material and the second dielectric material is not less than about 5:1.

16. The method of claim 14 or 15, wherein the first dielectric material comprises silicon oxide.

17. The method of any one of claims 14-16, wherein the second dielectric material comprises at least one of silicon nitride, silicon oxynitride, or high dielectric constant (high-k) dielectrics.

18. The method of any one of claims 11-17, wherein a critical dimension of the first contact is greater than a critical dimension of the second contact.

19. The method of any one of claims 11-18, wherein the upper end of the first contact is flush with a top surface of the etch stop layer.

20. The method of claim 19, wherein a lower end of the second contact is flush with the top surface of the etch stop layer.

21. A method for forming a three-dimensional (3D) memory device, comprising:
forming a channel structure extending vertically through a memory stack comprising interleaved conductive layers and dielectric layers above a substrate;
depositing a first silicon oxide layer on the memory stack;
depositing a silicon nitride layer on the first silicon oxide layer;
etching a first contact opening through the silicon nitride layer and the first silicon oxide layer until being stopped by an upper end of the channel structure;

- 25 -

filling the first contact opening with a metal material to form a first contact in contact with the upper end of the channel structure;

depositing a second silicon oxide layer on the silicon nitride layer;

etching a second contact opening through the second silicon oxide layer until being stopped by an upper end of the first contact and the silicon nitride layer; and

filling the second contact opening with the metal material to form the second contact in contact with the upper end of the first contact and the silicon nitride layer.

22. The method of claim 21, wherein the metal material comprises tungsten.

23. The method of claim 21 or 22, wherein a critical dimension of the first contact is greater than a critical dimension of the second contact.

24. The method of any one of claims 21-23, wherein the upper end of the first contact is flush with a top surface of the silicon nitride layer.

25. The method of claim 24, wherein a lower end of the second contact is flush with the top surface of the silicon nitride layer.

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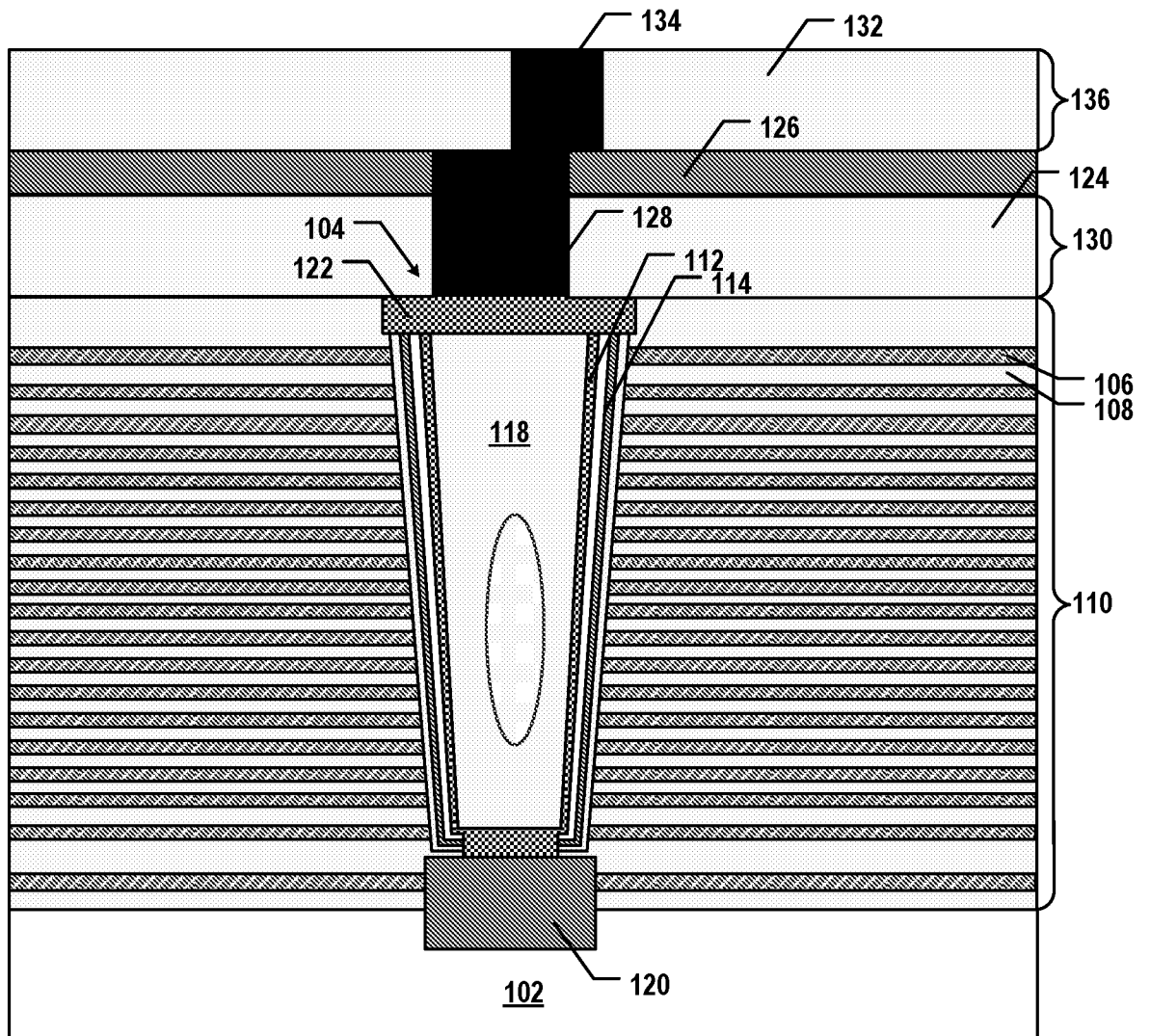


FIG. 1A

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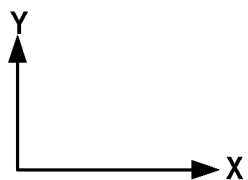
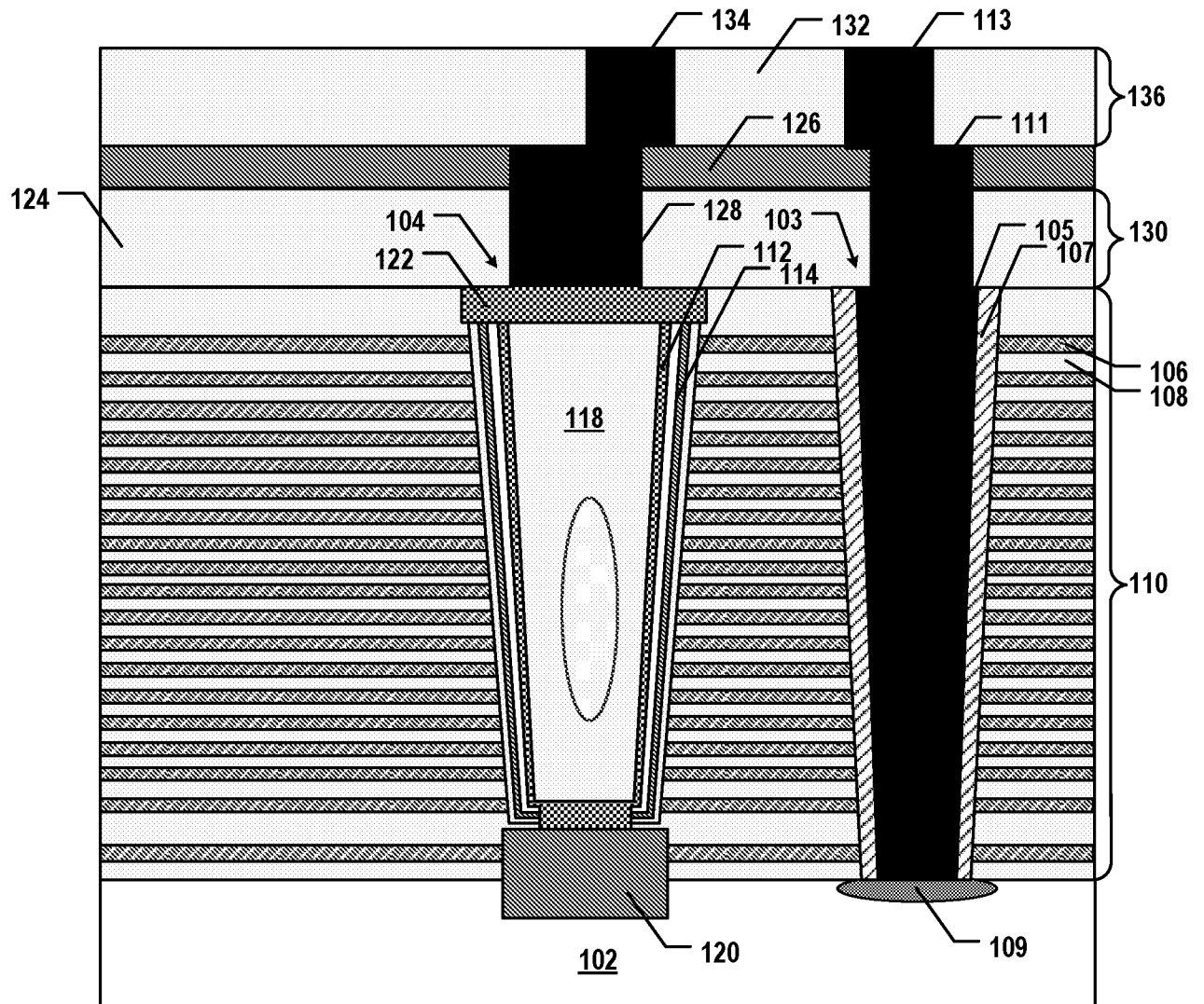
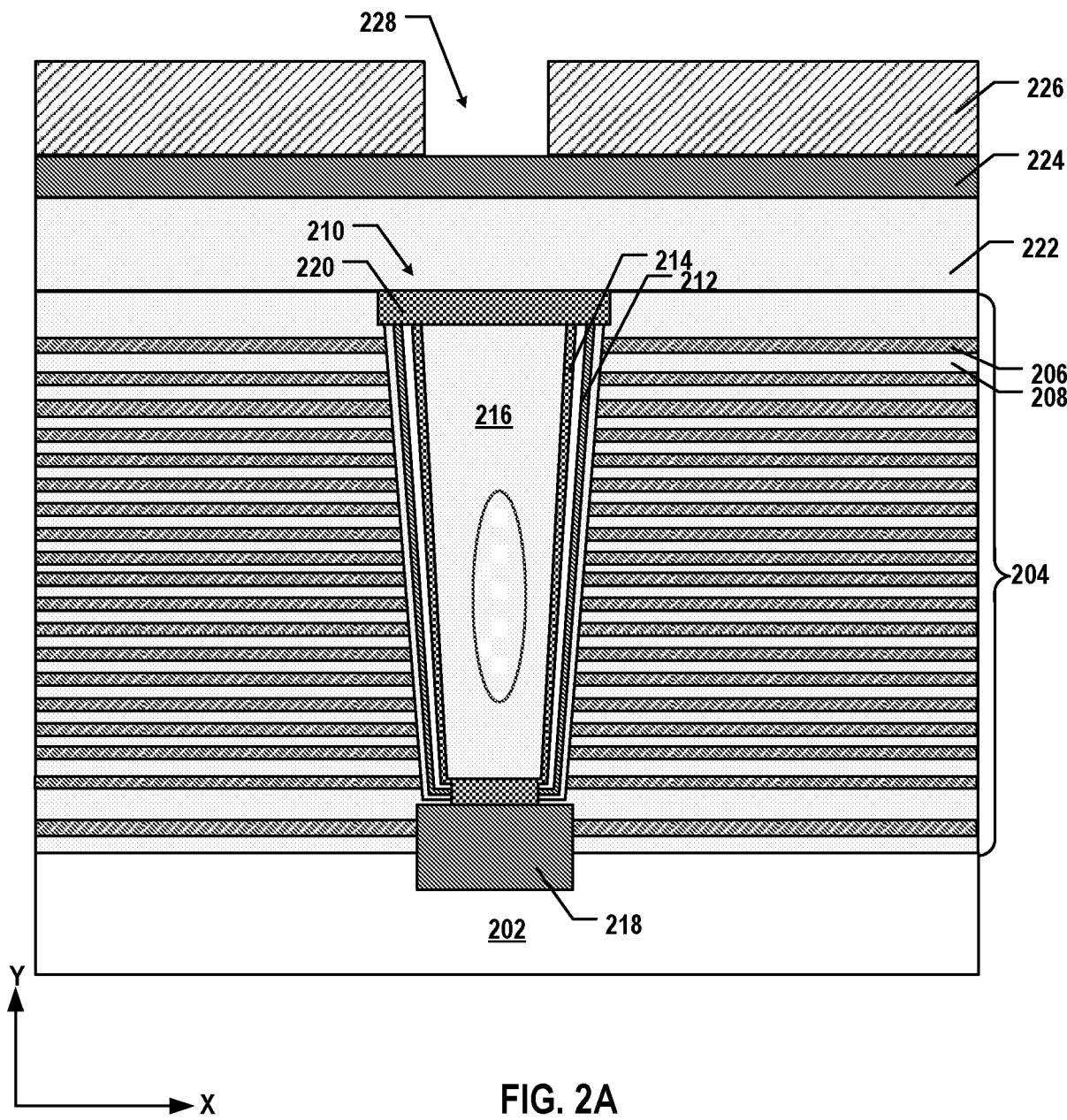
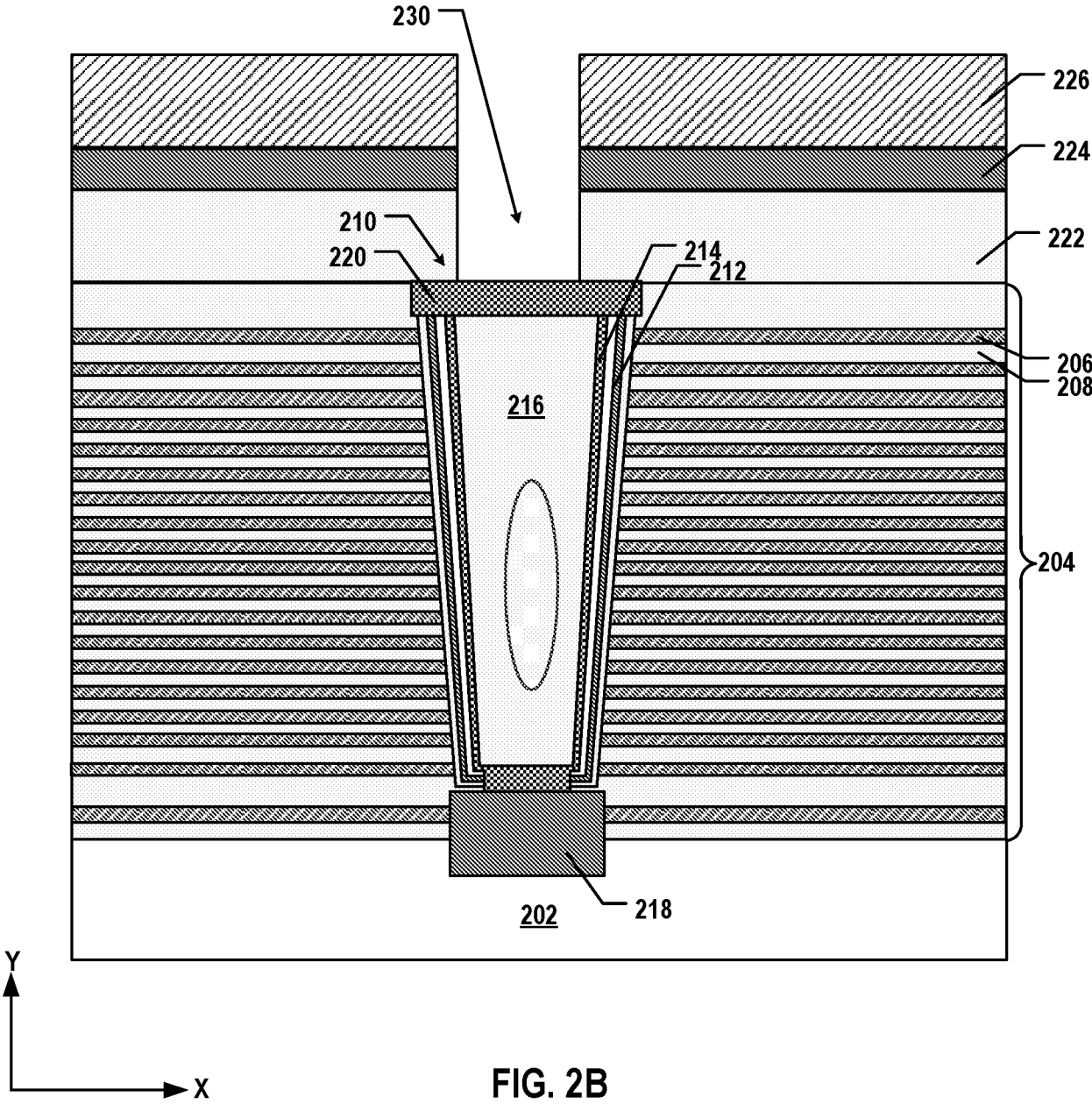
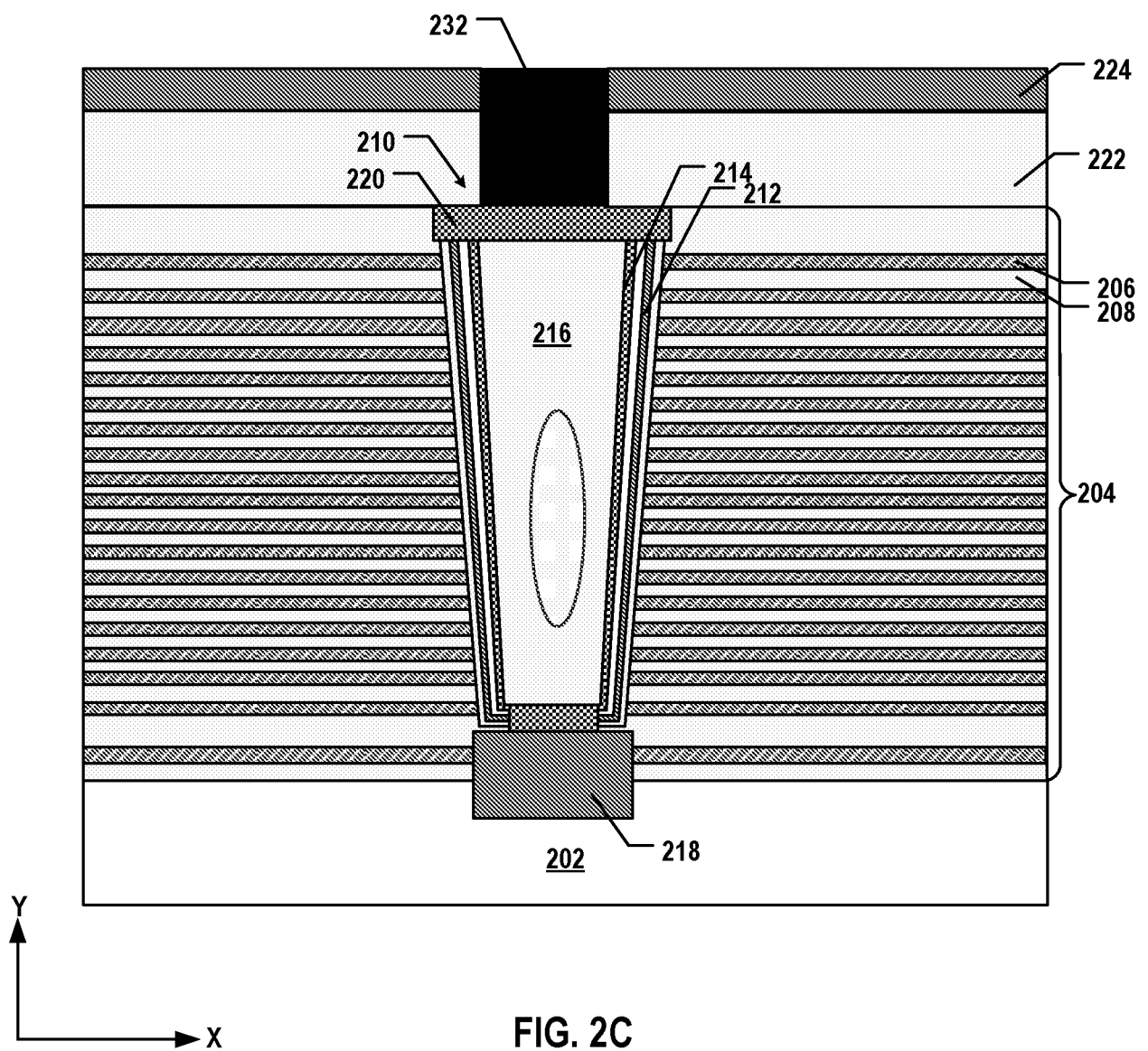
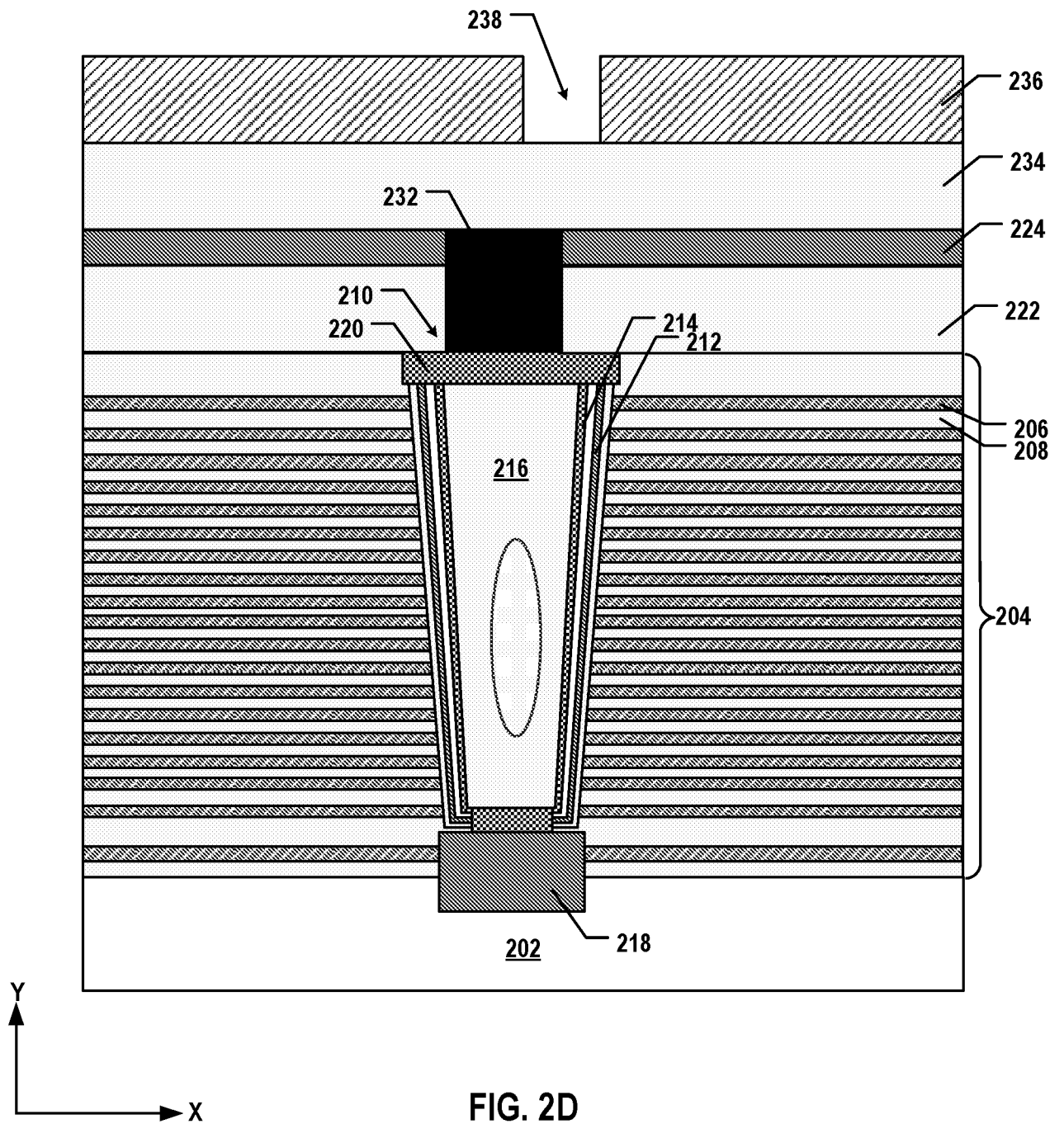


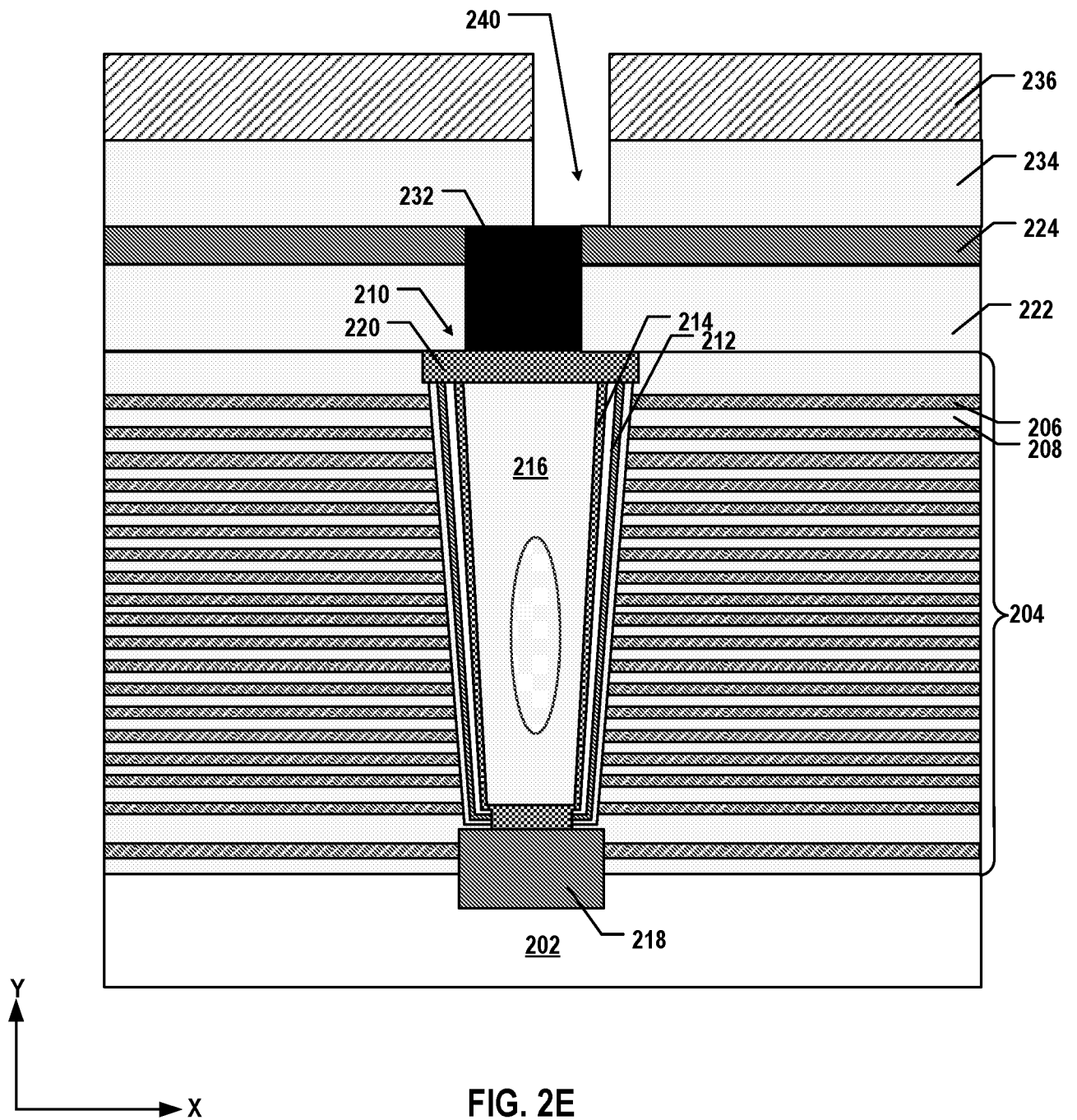
FIG. 1B

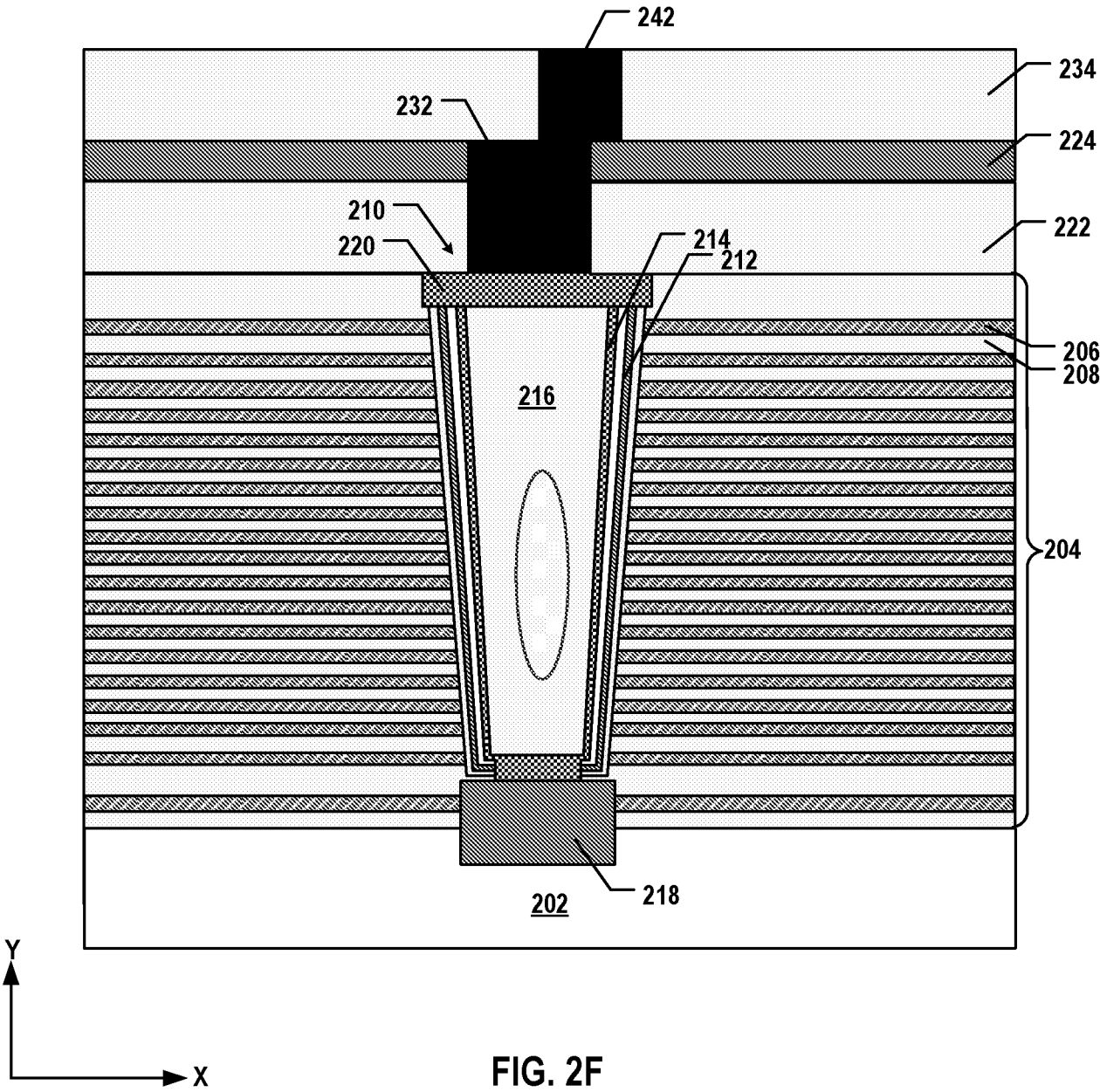












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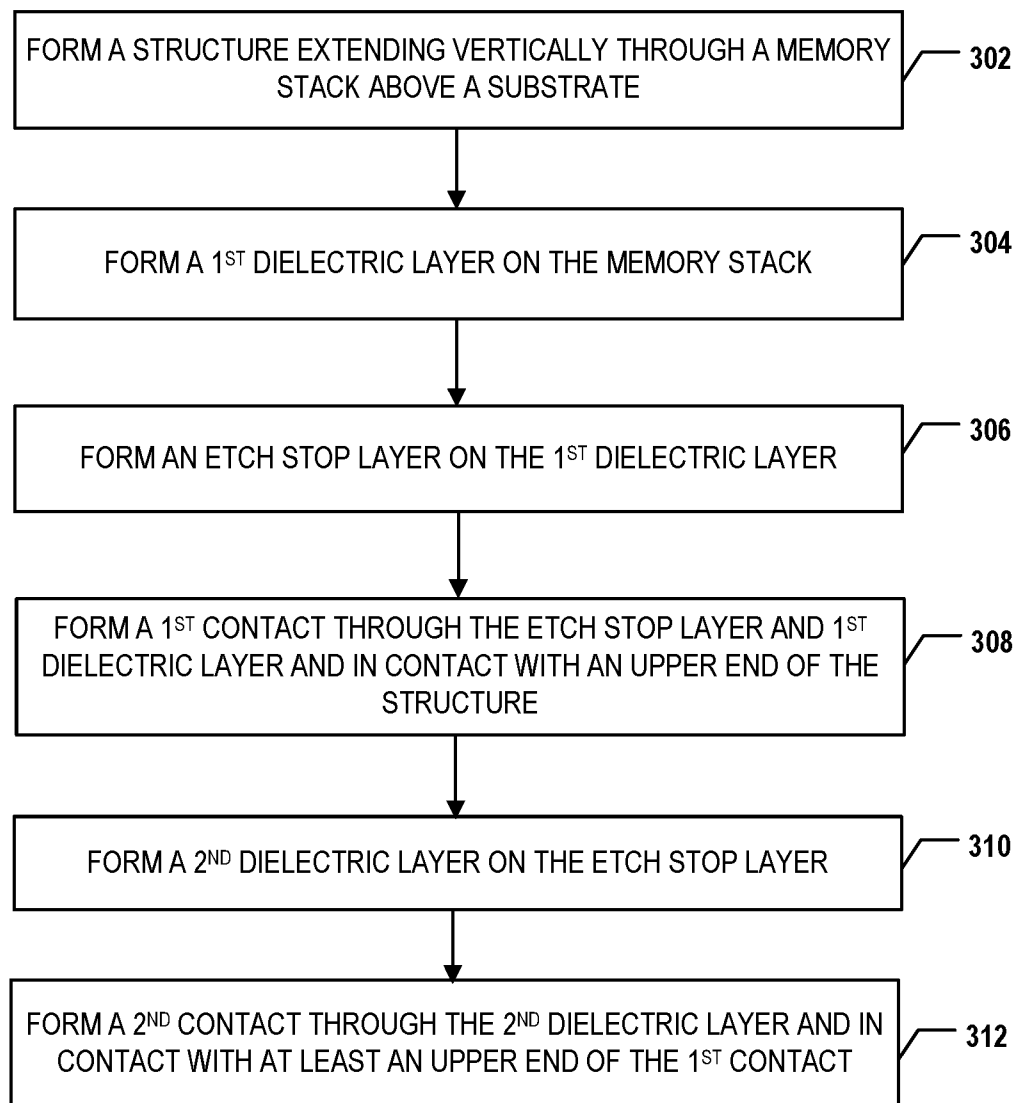


FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/096195

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/1157(2017.01)i; H01L 27/11582(2017.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC, CNPAT, CNKI, IEEE: 3D, memory, dielectric, etch, stop, contact, metal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2017025421 A1 (SANISK TECHNOLOGIES LLC) 26 January 2017 (2017-01-26) description, paragraphs [0032]-[0117], and figures 1-11	1-25
Y	CN 101330072 A (SAMSUNG ELECTRONICS CO., LTD.) 24 December 2008 (2008-12-24) description, page 5, line 12 to page 11, line 15, and figures 1-7B	1-25
A	CN 109314116 A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 05 February 2019 (2019-02-05) the whole document	1-25
A	CN 108511447 A (SAMSUNG ELECTRONICS CO., LTD.) 07 September 2018 (2018-09-07) the whole document	1-25

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

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“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

25 March 2020

Date of mailing of the international search report

20 April 2020

Name and mailing address of the ISA/CN

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LIN,Shaohua

Facsimile No. (86-10)62019451

Telephone No. 86-(10)-53961454

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2019/096195

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