(19) DANMARK

(10) **DK/EP 4264659 T3**

Patent- og Varemærkestyrelsen

(12) Oversættelse af europæisk patentskrift

(51) Int.Cl.: ***H 01 L 21/18 (2006.01)*** ***H 01 L 21/02 (2006.01)*** ***H 01 L 21/322 (2006.01)***

(45) Oversættelsen bekendtgjort den: **2025-02-03**

(80) Dato for Den Europæiske Patentmyndigheds bekendtgørelse om meddelelse af patentet: **2025-01-01**

(86) Europæisk ansøgning nr.: **21835348.0**

(86) Europæisk indleveringsdag: **2021-11-29**

(87) Den europæiske ansøgnings publiceringsdag: **2023-10-25**

(86) International ansøgning nr.: **FR2021052124**

(87) Internationalt publikationsnr.: **WO2022129726**

(30) Prioritet: **2020-12-15 FR 2013294**

(84) Designerede stater: **AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR**

(73) Patenthaver: **Commissariat à l'Energie Atomique et aux Energies Alternatives, 25 Rue Leblanc, Bat Le Ponant, 75015 Paris, Frankrig**
SOITEC, Parc Technologique des Fontaines , Chemin des Franques, 38190 Bernin, Frankrig

(72) Opfinder: **GAUDIN, Gweltaz, , 38190 BERNIN, Frankrig**
RADU, Ionut, , 38190 BERNIN, Frankrig
FOURNEL, Franck, , 38000 GRENOBLE, Frankrig
LANDRU, Didier, , 38190 BERNIN, Frankrig
WIDIEZ, Julie, , 38000 Grenoble, Frankrig

(74) Fuldmægtig i Danmark: **Novagraaf Brevets, Bâtiment O2, 2 rue Sarah Bernhardt CS90017, F-92665 Asnières-sur-Seine cedex, Frankrig**

(54) Benævnelse: **FREMGANGSMÅDE TIL FREMSTILLING AF EN HALVLEDERSTRUKTUR, DER OMFATTER ET GRÆNSEFLADEOMRÅDE, SOM INDBEFATTER AGGLOMERATER**

(56) Fremdragne publikationer:
FR-A1- 2 798 224
FR-A1- 3 006 236
FR-B1- 2 798 224
US-A1- 2015 303 316

METHOD FOR PRODUCING A SEMICONDUCTOR STRUCTURE COMPRISING AN INTERFACE REGION INCLUDING AGGLOMERATES

Description

Field of the invention

The present invention relates to the field of semiconductor materials for microelectronic components. It relates in particular to a method for producing a structure comprising a working semiconductor layer and a semiconductor carrier substrate, joined at an interface region wherein regions of direct contact between the layer and the carrier substrate, and agglomerates comprising a semiconductor material other than the semiconductor material(s) of the layer and of the carrier substrate, co-exist side by side.

Technological background of the invention

It is usual to form a semiconductor structure by transferring a working semiconductor layer, of low thickness and of high crystalline quality, onto a semiconductor carrier substrate of a lower crystalline quality. A well-known thin-layer transfer solution is the Smart Cut™ method, based on light-ion implantation and direct bonding at a bonding interface. In addition to economic advantages related to the streamlining of the high-quality material of the working layer, the semiconductor structure can also provide advantageous properties, for example due to the thermal or electrical conductivity or mechanical compatibility of the carrier substrate.

In the field of power electronics for example, it may also be advantageous to establish electrical conduction between the working layer and the carrier substrate, so as to form vertical components. For example, in the case of a structure comprising a useful layer of monocrystalline silicon carbide and a support substrate of lower quality silicon carbide (monocrystalline or polycrystalline), the bonding interface must have a resistivity that is as low as possible, preferentially less than 1 mohm.cm^2, or even less than 0.1 mohm.cm^2.

In other fields, even if high vertical electrical conductivity is not required, direct contact between the working layer and the carrier substrate is necessary to

guarantee electrical and/or thermal continuity, and/or very strong cohesion or mechanical strength.

Certain solutions of the prior art propose semiconductor-on-semiconductor bonding, by molecular adhesion, between the working layer and the carrier substrate. It is then required to manage the native oxide layers at the bonding interface, which prevent direct contact between the working layer and the carrier substrate. It is in particular possible to produce bonds of hydrophobic type, but from which it remains difficult to achieve a good interface quality.

F. Mu et al. (ECS Transactions, 86 (5) 3-21, 2018) implement direct bonding after activation of the surfaces to be joined by argon bombardment (SAB for "Surface Activation Bonding"): such a treatment prior to bonding generates a very high density of pendant bonds, which promote the formation of covalent bonds at the joining interface, and thus a high bonding energy. This method nevertheless has the drawback of generating an amorphous layer, at the joined surfaces, which particularly adversely affects the vertical electrical conduction between the thin layer and the carrier substrate. To overcome this problem, heavy doping of said surfaces is proposed in particular in document EP3168862. Other ways of bonding two substrates are described in FR 2 798 224 A1, US 2015/303316 A1 and FR 3 006 236 A1."

Object of the invention

The present invention relates to an alternative solution to those of the prior art, and aims to remedy all or some of the aforementioned drawbacks. It relates in particular to a method for producing a structure comprising a working semiconductor layer and a semiconductor carrier substrate, joined at an interface region comprising regions of direct contact between layer and carrier substrate, and agglomerates comprising a semiconductor material different from that (or those) of the layer and of the support substrate.

Brief description of the invention

The invention relates to a method for producing a semiconductor structure comprising the following steps:

a) providing a working layer made of a semiconductor material having a free face to be joined,

b) providing a carrier substrate made of a semiconductor material having a free face to be joined,

c) depositing a film composed of a semiconductor material different from that or those of the working layer and of the carrier substrate, having a thickness of less than 50 nm, on the free face to be joined of the working layer and/or on the free face to be joined of the carrier substrate,

d) forming an intermediate structure, comprising directly joining, along a bonding interface extending along a main plane, the free faces to be joined of the working layer and of the carrier substrate, respectively, the intermediate structure comprising an encapsulated film originating from the one or more film(s) deposited during step c),

e) annealing the intermediate structure at a temperature higher than or equal to a critical temperature, so as to bring about segmentation of the encapsulated film and form the semiconductor structure comprising an interface region between the working layer and the carrier substrate, said interface region comprising:

- regions of direct contact between the working layer and the carrier substrate, and
- agglomerates comprising the semiconductor material of the film, and having a thickness, along an axis normal to the main plane, of less than or equal to 250 nm; the regions of direct contact and the agglomerates being adjacent in the main plane.

According to other advantageous and non-limiting features of the invention, either individually or in any technically feasible combination:

- in step a), the free face to be joined of the working layer comprises a native oxide and/or, in step b), the free face to be joined of the carrier substrate comprises a native oxide,

- in step e), the agglomerates of the interface region trap the oxygen originating from the native oxide(s),

- step a) comprises an implantation of light species in a donor substrate, to form a buried fragile plane which delimits, with a front face of the donor substrate, the working layer,

- step a) comprises the formation of the donor substrate by epitaxy of a donor layer on an initial substrate, the implantation being carried out subsequently, in the donor layer,

- step d) comprises, after the direct joining giving rise to a bonded assembly comprising the donor substrate and the carrier substrate, a separation at the buried fragile plane, in order to form, on the one hand, the intermediate structure comprising the working layer, the encapsulated film and the carrier substrate, and on the other hand, the remainder of the donor substrate,

- the thickness of the film deposited in step c) is less than or equal to 10 nm, or less than or equal to 5 nm, or less than or equal to 3 nm, or less than or equal to 2 nm,

- the thickness of the film deposited in step c) is less than 10 nm, and the agglomerates have a thickness, along an axis normal to the main plane, of less than or equal to 50 nm,

- the critical temperature is between 500°C and 1800°C, depending on the nature of the semiconductor material of the film and of the semiconductor material(s) of the working layer and of the carrier substrate,

- the semiconductor material of the working layer is silicon carbide and has a monocrystalline, polycrystalline or amorphous structure,

- the semiconductor material of the carrier substrate is silicon carbide and has a monocrystalline, polycrystalline or amorphous structure,

- the semiconductor material of the film is selected from silicon or germanium,

- the agglomerates have a thickness of less than or equal to 40 nm, or even less than or equal to 30 nm,

- the agglomerates are in the form of first precipitates comprising the semiconductor material of the film, second precipitates comprising the semiconductor material of the film and oxygen, and/or cavities lined with a compound comprising the semiconductor material of the film and oxygen,

- the second precipitates have a substantially triangular shape in a transverse plane normal to the main plane,

- the agglomerates have lateral dimensions, in the main plane, between 5 nm and 500 nm.

The invention also relates to an electronic component produced on and/or in the working layer of a semi-conducting structure coming from the aforementioned production method. The semiconductor structure comprises:

– the working layer made of a semi-conductor material, extending in a main plane,

– a carrier substrate made of a semiconductor material,

– and an interface region between the working layer and the carrier substrate, extending parallel to the main plane, the interface region comprising regions of direct contact between the working layer and the carrier substrate, and agglomerates comprising a semiconductor material different from that or those of the working layer and of the carrier substrate, and having a thickness, along an axis normal to the main plane, of less than or equal to 250 nm; the regions of direct contact and the agglomerates being adjacent in the main plane.

According to a particular variant, the component comprises at least one electrical contact on and/or in the carrier substrate, at a rear face of the semiconductor structure for a power application.

Brief description of the drawings

Other features and advantages of the invention will emerge from the following detailed description of the invention with reference to the appended figures, wherein:

[Fig. 1] Figure 1 shows a carrier substrate according to the invention;

[Fig. 2a]

[Fig. 2b]

[Fig. 2c]

[Fig. 2d]

[Fig. 2e] Figures 2a to 2e show steps of a production method according to the invention;

[Fig. 3a]

[Fig. 3b]

[Fig. 3c]

[Fig. 3d] Figures 3a to 3d show variants of steps of a production method according to the invention;

[Fig. 4a]

[Fig. 4b] Figures 4a and 4b show, respectively, a graph I(V) (current as a function of voltage) comparing the electrical characteristics of an interface region of a semiconductor structure in accordance with the invention and those of a solid substrate, for different sizes of electrode patterns, and the arrangement of the electrodes on said structure to carry out such a measurement.

The same references in the figures may be used for elements of the same type. The figures are schematic depictions which, for the sake of readability, are not to scale. In particular, the thicknesses of the layers along the z-axis are not to scale relative to the lateral dimensions along the x-axis and the y-axis; and the relative thicknesses of the layers are not reflected in the figures.

Detailed description of the invention

The invention relates to a method for producing a semiconductor structure 100 comprising a working layer 10 made of monocrystalline semiconductor material, a carrier substrate 30 made of semiconductor material, and an interface region 20 between the working layer 10 and the carrier substrate 30 (Figure 1). Like the working layer 10, the interface region 20 extends parallel to the main plane (x, y).

Advantageously, and as is usually the case in the field of microelectronics, the semiconductor structure 100 is in the form of a circular wafer with a diameter of between 100 mm and 450 mm, and of total thickness typically between 300 microns and 1000 microns. It is understood that, in this case, the carrier substrate 30 and the working layer 10 also have such a circular shape. The front 100a and rear 100b faces of the wafer extend parallel to the main plane (x, y).

Many types of semiconductor structure 100 allowing vertical electrical conduction or direct contact between the working layer 10 and the carrier substrate 30 may be of interest for microelectronic applications: the nature of the materials making up the working layer 10 and the carrier substrate 30 can therefore be very varied.

By way of example, the semiconductor material of the useful layer 10 can be chosen from silicon carbide, silicon, gallium nitride, gallium arsenide, indium phosphide and silicon-germanium alloys. In general, the production of components on the working layer 10 requires a high crystalline quality of said layer 10: it is therefore preferentially chosen to be monocrystalline, with a quality grade, type and doping level adapted to the targeted application. Alternatively, the working layer 10 may of course have a polycrystalline or amorphous structure.

Also by way of example, the semiconductor material of the support substrate 30 can be chosen from silicon carbide, silicon, gallium nitride, gallium arsenide, indium phosphide and silicon-germanium alloys. It preferentially has a lower level of quality, essentially for economic reasons, and a monocrystalline, polycrystalline or amorphous structure. Its type and its doping level are chosen to respond to the targeted application.

The production method firstly comprises a step a) of providing the working layer 10 made of semiconductor material, preferentially monocrystalline (Figure 2a). In this step a), the working layer 10 has a free face 10a intended to be joined, during a

subsequent step of the method, also called front face 10a; it also has a rear face 10b opposite its front face 10a.

According to an advantageous embodiment, the useful layer 10 results from the transfer of a surface layer from a donor substrate 1, in particular a layer transfer based on the Smart Cut™ method.

Step a) can thus comprise an implantation of light species, for example hydrogen, helium or a combination of these two species, into a donor substrate 1, to form a buried fragile plane 11 which delimits, with a front face 10a of the donor substrate 1, the working layer 10 (Figure 3a).

According to a variant of this embodiment, step a) comprises the formation of the donor substrate 1 by epitaxy of a donor layer 1′ on an initial substrate, prior to the implantation of the light species (Figure 3b). This variant makes it possible to form a donor layer 1′ having the structural and electrical characteristics required for the intended application. In particular, an excellent crystal quality can be obtained by epitaxy, and in situ doping of the donor layer 1’ can be precisely controlled. The implantation of light species, to form the buried fragile plane 11, is then carried out in the donor layer 1′.

Alternatively, the working layer 10, provided in step a), may of course be formed from other known thin-film transfer techniques.

The production method according to the invention then comprises a step b) of providing a carrier substrate 30 made of semiconductor material (Figure 2b). The carrier substrate 30 has a free face 30a intended to be joined during a subsequent step of the method, also called front face 30a; it also has a rear face 30b.

The working layer 10 and the carrier substrate 30 may be formed of one or more materials chosen from those mentioned above.

The production method then comprises a step c) of depositing a film 2 made of a semiconductor material (called the second material), on the free face 10a to be joined of the working layer 10 or on the free face 30a to be joined of the carrier substrate 30 or even, as is shown in Figure 2c, on both of the free faces 10a, 30a

to be joined. The second material is different from the semiconductor material(s) of the useful layer 10 and the support substrate 30.

Preferentially, the second material is chosen for its particular affinity with oxygen; furthermore, it is not a compound of several elements and, by reacting with oxygen, it must generate a solid and non-gaseous compound.

The second material must be able to be deposited in an extremely thin layer and be compatible with a microelectronic component manufacturing line ("front end of line"). It may in particular be chosen from silicon, germanium, etc., depending on the nature of the working layer 10 and of the carrier substrate 30.

The film 2 has a thickness of less than 50 nm, preferentially less than or equal to 10 nm, less than or equal to 8 nm, less than or equal to 5 nm, or even less than or equal to 3 nm, or even less than or equal to 2 nm. For example, the deposited film 2 may have a thickness of the order of 0.5 nm, 1 nm, 2 nm, 3 nm, 4 nm, 5 nm, 8 nm, 9 nm, 10 nm, 11 nm, 12 nm, 13 nm, 15 nm, 20 nm, 30 nm or 40 nm.

Note that when a film 2 is deposited on the two free faces 10a, 30a, the total deposited thickness, that is to say the sum of the thicknesses of the film 2 deposited on one and the other free faces 10a, 30a is preferentially less than 50 nm, preferentially less than or equal to 10 nm, less than or equal to 8 nm, or even less than or equal to 5 nm. The total thickness of deposited film 2 is always kept low, so as to allow a segmentation of the film in the form of agglomerates 21, in a subsequent step of the method.

The film 2 is deposited under a controlled atmosphere. Depending on the nature of the deposited film 2, step c) is carried out at low temperatures or even ambient temperature, advantageously by a known chemical vapor deposition technique (assisted by plasma: PECVD, at sub-atmospheric pressure: LPCVD), or a sputtering technique using, in order to bombard the target, a neutral element or an element whose residual presence in the deposited film is not troublesome (Ar, Si, N, etc.).

The production method then comprises a step d) of forming an intermediate structure 150, which step comprises a joining of the free faces 10a, 30a

respectively of the working layer 10 and of the carrier substrate 30, at a bonding interface 15 extending along the main plane (x, y) (Figure 2d).

This direct bonding is preferably carried out by molecular-adhesion bonding, which consists in bringing the faces 10a, 30a to be joined into contact without adding any intermediate adhesive material. It may be direct bonding between the working layer 10 and the film 2, when the latter has been deposited only on the carrier substrate 30, or direct bonding between the carrier substrate 30 and the film 2, when the latter has been deposited only on the working layer 10, or even direct bonding between two films 2, when they were deposited on the working layer 10 and on the carrier substrate 30. The direct bonding can be carried out in an ambient atmosphere, or under a controlled atmosphere and in particular under a high vacuum of approximately 10^{-6} Pa or less.

Optionally, the deposition of step c) and the direct assembly of step d) are linked without breaking the vacuum, in-situ or in a multi-chamber equipment. By way of example, mention will be made of Atomic Diffusion Bonding BV7000 from the company Canon, wherein it is possible to successively carry out a direct deposition and bonding, by maintaining a controlled atmosphere.

With reference to the advantageous embodiment shown in Figures 3a to 3d, step d) comprising the direct joining of the free face 10a to be joined of the working layer 10 on the free face 30a to be joined of the carrier substrate 30, gives rise to a bonded assembly 200 that includes the donor substrate 1, the carrier substrate 30, and the bonding interface 15 (Figure 3c). Step d) further comprises a separation at the buried fragile plane 11, in order to form, on the one hand, the intermediate structure 150 comprising the working layer 10, the film(s) 2 and the carrier substrate 30, and on the other hand, the rest of the donor substrate 1' (Figure 3d). Such a separation can be carried out during a heat treatment capable of growing lenticular cavities ("platelets") and microcracks under pressure, induced by the implanted species, in the buried fragile plane 11. The separation can also be achieved by applying mechanical stress, or even by the combination of thermal and mechanical stresses, as is well known from the Smart Cut™ method.

Sequences for cleaning, smoothing, polishing or etching the separate face 10b of the working layer 10 and/or of the separate face 1''a of the rest of the donor substrate 1'' will be able to be operated so as to restore a good surface quality, in particular in terms of roughness, defectivity and other contaminations.

Regardless of the embodiment of the method, at the end of step d), the intermediate structure 150 has a front face 10b on the side of the working layer 10, a rear face 30b on the side of the carrier substrate 30, and an encapsulated film 2' between the working layer 10 and the carrier substrate 30. Note that the encapsulated film 2' corresponds to the film 2 when the latter has been deposited only on one of the free faces 10a, 30a, or corresponds to the two films 2 deposited respectively on the working layer 10 and on the carrier substrate 30.

The production method according to the invention then comprises a step e) of annealing the intermediate structure 150 at a temperature greater than or equal to a critical temperature, so as to bring about the segmentation of the encapsulated film 2' in the form of agglomerates 21 and to form an interface region 20 (Figure 2e) comprising:

- regions of direct contact 22 between the working layer 10 and the carrier substrate 30, in other words regions wherein there is a direct bond between the semiconductor materials of the working layer 10 and of the carrier substrate 30, and

- agglomerates 21 comprising the semi-conductor material of the film 2 (second material), and having a thickness, along an axis z normal to the main plane (x, y), low or very low, namely less than or equal to 250 nm, less than or equal to 50 nm, less than or equal to 40 nm, less than or equal to 30 nm, less than or equal to 20 nm, or even less than or equal to 10 nm. The agglomerates 21, distributed in the interface region 20, are disjoint or joined, the disjoint agglomerates 21 are separated from one another by regions of direct contact 22. The regions of direct contact 22 and the agglomerates 21 are adjacent in the main plane (x, y).

Step e) results in the formation of the semiconductor structure 100.

The term “critical temperature” is used to mean the temperature from which it will be energetically more favorable for the second material to form agglomerates 21 rather than to remain in the form of a very fine encapsulated film 2’. The annealing temperature of step e) must, on the other hand, be sufficient to allow the bonding of the regions of direct contact 22, between the agglomerates 21. The critical temperature is typically between 500°C and 1800°C, depending on the nature of the second material and of the semiconductor material(s) of the useful layer 10 and the support substrate 30.

The annealing step e) is therefore always carried out at a temperature greater than or equal to this critical temperature, and under neutral atmosphere, in particular under argon, argon/hydrogen or nitrogen.

Beyond the critical temperature, the system including the encapsulated film 2′ and the semi-conductor surfaces of the working layer 10 and of the carrier substrate 30 in contact with said film 2′ will optimize its surface energy by segmenting the encapsulated film 2′ in the form of agglomerates 21, and by creating regions of direct contact 22 between the semiconductor surfaces respectively of the working layer 10 and of the carrier substrate 30.

Furthermore, because the encapsulated film 2′ is extremely thin, semiconductor materials known to be stable at low or medium temperature only, can be used as the second material in semiconductor structures 100 in accordance with the invention capable of undergoing treatments at high (900°C-1100°C), or even very high (1200°C-1900°C) temperatures. Indeed, due to their precipitation in the form of agglomerates 21 of small dimensions and of very small thickness, they do not cause any deterioration of the structure 100 and in particular of the working layer 10. Mention will be made, for example, of agglomerates 21 comprising silicon in a structure 100 comprising a working layer 10 and a carrier substrate 30 made of SiC and intended to undergo epitaxy at a temperature of between 1600°C and 1800°C. Note that in this example, a complete segmentation of the film 2’ into agglomerates 21 is observed, at around 1700°C.

It is usual that, in step a), the free face 10a to be joined of the working layer 10 comprises a native oxide and/or, in step b), the free face 30a to be joined of the

carrier substrate 30 comprises such an oxide. The fact of not having to manage this native oxide often simplifies the manufacturing steps.

Thus, in step e) of the process according to the invention, the agglomerates 21 of the interface region 20 will be able to trap the oxygen obtained from the native oxide (s), and thus to eliminate any oxide of the interface between the working layer 10 and the carrier substrate 30, in the regions of direct contact 22.

Furthermore, it is possible that steps c) and/or d) of the method are carried out in an atmosphere comprising oxygen, which can release the manufacturing constraints: oxygen is then present at the bonding interface 15 in the intermediate structure 150.

In this case also, in step e), the agglomerates 21 of the interface region 20 will trap the oxygen of the bonding interface 15, thus avoiding the presence of oxygen in the regions of direct contact 22.

The production method as described therefore makes it possible to obtain a semiconductor structure 100 providing vertical electrical conduction and/or effective direct contact between the working layer 10 and the carrier substrate 30, via the interface region 20, thanks to the regions of direct contact 22 free of oxygen and/or native oxides. The very fine agglomerates 21 consist of the second material and optionally of oxygen, mainly trapped in the form of oxides.

In general, the agglomerates 21 are in the form of:

- first precipitates comprising the semiconductor material of the film 2 (second material), and/or

- second precipitates comprising the second material and oxygen (mainly in the form of oxides of said second material), and/or

- cavities whose internal walls are lined with a compound comprising the second material and oxygen (mainly in the form of oxides of said second material).

The interface region 20 with the agglomerates 21, adjacent to the regions of direct contact 22, ensures the mechanical strength and more generally the reliability of the working layer 10 and/or the components which will be produced on or in the latter.

The semiconductor structure 100 according to the invention guarantees good electrical conductivity and/or effective direct contact between the working layer 10 and the carrier substrate 30, via its interface region 20. In particular, the agglomerates 21, distributed in the interface region 20, in a median plane P substantially parallel to the main plane (x, y), are able to effectively trap the oxygen that may be present in the encapsulated film 2′ or to the bonding interface 15; the regions of direct contact 22 between the working layer 10 and the carrier substrate 30, devoid of native oxide residues in particular, allow electrical conduction and/or a vertical semi-conductor/semi-conductor contact that is effective and of good quality.

Furthermore, the agglomerates 21 and the regions of direct contact 22 ensure the mechanical continuity of the interface region 20 and provide excellent mechanical strength between the working layer 10 and the carrier substrate 30. The quality of the working layer 10 is therefore not affected by any holes or interface defects; note that the aforementioned cavities, when present, have dimensions and a density which do not negatively impact the quality and the resistance of the working layer 10.

On a median plane P of the interface region 20, the degree of coverage of the agglomerates 21 is typically between 1 % and 50 %, preferentially between 10 % and 40 %. The lateral dimensions (in the median plane P) of the agglomerates 21 are limited, typically of the order of 5 nm to 500 nm. In particular, when the thickness of the film 2 deposited in step c) is less than 10 nm, the lateral dimensions of the agglomerates 21 are about 5 nm to 150 nm and the thickness of the agglomerates 21 is less than or equal to 50 nm.

Among the agglomerates 21, the first precipitates and the cavities may have a lenticular or polygonal shape, and the second precipitates may have a substantially triangular shape, in a transverse plane normal to the main plane (x, y).

Example embodiment

The donor substrate 1 is of high-quality monocrystalline 4H-SiC and has a diameter of 150 mm. The donor substrate 1 is n-doped, with a resistivity of the order of 20mohm.cm. It is implanted through its front face 1a, a "C" face, with hydrogen ions at a dose of $5^E16/cm^2$ and an energy of 95 keV. Around the implantation depth, a buried fragile plane 11 is thus defined, delimiting, with the front face 10a of the donor substrate 1, the working layer 10.

The carrier substrate 30 is made of lower-quality monocrystalline 4H-SiC, of the same diameter as the donor substrate 1. It is n-doped with a resistivity of the order of 20 mohm.cm.

Both the substrates 1, 30 undergo cleaning sequences, in order to remove the particles and other surface contaminations. Both the substrates may comprise a native oxide on their surfaces.

The substrates 1, 30 are introduced into a first deposition chamber, integrated into direct bonding equipment. A silicon film 2 having a thickness of 1 nm is deposited on each of the front faces 10a, 30a (free faces to be joined) of the substrates 1, 30 under a secondary vacuum, at 10^{-6} Pa and room temperature, by sputtering.

The substrates 1, 30 are introduced into a second bonding chamber in order to be joined at their front faces 10a, 30a by bringing the films 2 deposited on the donor substrate 1 and on the support substrate 30, respectively, into direct contact. The atmosphere in the bonding chamber is the same as that in the deposition chamber, but could optionally be different: for example, the substrates may be removed from the first chamber, returned to the ambient atmosphere, then introduced into bonding equipment separate from the deposition chamber. Indeed, the method according to the invention greatly relieves the constraints related to the presence of oxygen, for example in the form of native oxides, in or on the films to be joined.

After assembly, the bonded assembly 200 comprises the donor substrate 1 bonded to the carrier substrate 30 via a bonding interface 15, and the encapsulated film 2' formed of the two films 2 deposited and buried between the two substrates 1, 30. The encapsulated film 2' has a thickness of about 2 nm.

The bonded assembly 200 is subjected to a heat treatment to cause separation at the buried fragile plane 11, at a temperature of about 900°C, for 30 minutes. The intermediate structure 150 including a working layer 10 having a thickness of 500 nm is then obtained, arranged on the encapsulated film 2', itself arranged on the carrier substrate 30. Cleaning and polishing sequences are applied so as to restore the right level of defectiveness and roughness to the surface 10b of the working layer 10.

Finally, annealing at 1900°C for 30 min is applied to the intermediate structure 150, previously provided with a protective layer on its front face 10b (also free face 10b of the working layer 10 in the intermediate structure 150). At the end of this annealing, the structure 100 according to the invention is obtained: the interface region 20 is formed with agglomerates 21 comprising silicon and oxygen (mainly in SiOx form), separated by regions of direct contact 20 between working layer 10 and carrier substrate 30. Such an interface region 20 gives the structure 100 a good vertical electrical conductivity, close to that of a solid SiC substrate having a resistivity of 20 mohm.cm.

The interface zone 20 has a resistivity of less than or equal to 0.1 mohm.cm^2. This is apparent in the graph of Figure 4a which shows the curves of current as a function of voltage I(V) for simple components comprising two metal contact electrodes 41, 42 of different sizes (between 50 microns and 230 microns in diameter); these electrode sizes (patterns) are shown on the graph of Figure 4a. In the case of the structure 100 according to the invention, the measurement of I(V) is made at two electrodes 41, 42 between which the current path passes through the interface zone 20, due to the presence of trenches 40 between the electrodes 41, 42 which cross said interface zone 20 (Figure 4b). A resistivity of the interface zone 20 of approximately 0.0076 mohm.cm^2 was extracted. For comparison and reference, electrodes 51, 52 are also deposited on the support substrate 30: the associated I(V) curves are denoted “bulk” on the graph of Figure 4a.

The agglomerates 21 in this structure 100 have a thickness of 5 nm to 15 nm and an average diameter on the same order of magnitude. The degree of coverage of the agglomerates 21, in a median plane P of the interface region 20 is about 20 %.

It should be noted that annealing temperatures (step e), other than 1900°C, were also applied to the intermediate structure 150 described in the above example, for example 1370°C. A resistivity of the interface region 20 of about 0.032 mohm.cm^2 was extracted, that is, clearly less than 0.1 mohm.cm^2.

Of course, this example is not limiting and numerous other semiconductor structures 100 according to the invention can be produced, based on different combinations of materials for the working layer 10, the film 2 and the carrier substrate 30, while adhering to the conditions set out above for the formation of the interface region 20.

Electronic components can be produced on and/or in the working layer 10 of a semiconductor structure 100 according to the invention. These components may in particular address power applications, photovoltaic applications or light-emitting diodes.

The components may comprise at least one electrical contact on and/or in the carrier substrate 30, at a rear face 100b of the semiconductor structure 100, in particular for power applications. By way of non-limiting examples, these power components may comprise transistors, diodes, thyristors or passive components (capacitors, inductors, etc.), etc.

Of course, the invention is not limited to the embodiments and examples described, and implementation variants may be applied thereto without departing from the scope of the invention as defined by the claims.

PATENTKRAV

1. Fremgangsmåde til fremstilling af en halvlederstruktur (100), hvilken fremgangsmåde omfatter følgende trin:

a) tilvejebringelse af et nyttelag (10), som er fremstillet af et halvledermateriale og har en fri flade (10a), der skal sammenføjes,

b) tilvejebringelse af et bærersubstrat (30), som er fremstillet af et halvledermateriale og har en fri flade (30a), der skal sammenføjes,

c) afsætning af en film (2), bestående af et halvledermateriale, der er forskelligt fra nyttelagets (10) og bærersubstratets (30) materiale eller materialer og har en tykkelse på mindre end 50 nm, på nyttelagets (10) frie flade (10a), der skal sammenføjes, og/eller på bærersubstratets (30) frie flade (30a), der skal sammenføjes,

d) dannelse af en mellemstruktur (150), hvilket omfatter direkte sammenføjning, langs en klæbegrænseflade (15), der strækker sig langs et hovedplan (x,y), af henholdsvis nyttelagets (10) og bærersubstratets (30) frie flader, der skal sammenføjes, hvor mellemstrukturen (150) omfatter en indkapslet film (2'), som stammer fra den ene eller flere film (2), der afsættes i løbet af trin c),

e) annealing af mellemstrukturen (150) ved en temperatur, der er højere end eller lig med en kritisk temperatur, med henblik på at frembringe segmentering af den indkapslede film (2') og danne halvlederstrukturen (100), der omfatter et grænsefladeområde (20) mellem nyttelaget (10) og bærersubstratet (30), hvilket grænsefladeområde (20) omfatter:

- områder (22) med direkte kontakt mellem nyttelaget (10) og bærersubstratet (30) og

- agglomerater (21), der omfatter filmens (2) halvledermateriale og har en tykkelse, langs en akse (z) vinkelret på hovedplanet (x,y), på mindre end eller lig med 250 nm; hvor områderne (22) med direkte kontakt og agglomeraterne (21) støder op til hinanden i hovedplanet (x,y).

2. Fremstillingsfremgangsmåde ifølge det foregående krav, hvor:

- nyttelagets (10) frie flade (10a), der skal sammenføjes, i trin a) omfatter et nativt oxid, og/eller bærersubstratets (30) frie flade (30a), der skal sammenføjes, i trin b) omfatter et nativt oxid,

- grænsefladeområdets (20) agglomerater (21) i trin e) indfanger oxygenet, som stammer fra det eller de native oxider.

3. Fremstillingsfremgangsmåde ifølge et af de foregående krav, hvor trin a) omfatter en implantation af lette species i et donorsubstrat (1) til dannelse af et skjult fragilt plan (11), der med en forreste flade (10a) af donorsubstratet (1), afgrænser nyttelaget (10).

4. Fremstillingsfremgangsmåde ifølge det foregående krav, hvor trin a) omfatter dannelse af donorsubstratet (1) ved epitaksi af et donorlag (1') på et udgangssubstrat, hvor implantationen efterfølgende udføres i donorlaget (1').

5. Fremstillingsfremgangsmåde ifølge et af de to foregående krav, hvor trin d), efter den direkte samling, som giver anledning til en sammenklæbet samling (200), der omfatter donorsubstratet (1) og bærersubstratet (30), omfatter en separering at det skjulte fragile plan (11) med henblik på at danne mellemstrukturen (150), der omfatter nyttelaget (10), den indkapslede film (2') og bærersubstratet (30), og at danne resten af donorsubstratet (1").

6. Fremstillingsfremgangsmåde ifølge et af de foregående krav, hvor tykkelsen af den afsatte film (2) i trin c) er mindre end eller lig med 10 nm, eller mindre end eller lig med 5 nm, eller mindre end eller lig med 3 nm eller mindre end eller lig med 2 nm.

7. Fremstillingsfremgangsmåde ifølge det foregående krav, hvor tykkelsen af den afsatte film (2) i trin c) er mindre end 10 nm, og agglomeraterne (21) har en tykkelse, langs en akse (z) vinkelret på hovedplanet (x,y), på mindre end eller lig med 50 nm.

8. Fremstillingsfremgangsmåde ifølge et af de foregående krav, hvor den kritiske temperatur er mellem 500 °C og 1.800 °C, afhængigt af beskaffenheden af

filmens (2) halvledermateriale og nyttelagets (10) og bærersubstratets (30) halvledermateriale(-er).

9. Fremstillingsfremgangsmåde ifølge et af de foregående krav, hvor nyttelagets (10) halvledermateriale er siliciumcarbid og har en monokrystallinsk, polykrystallinsk eller amorf struktur.

10. Fremstillingsfremgangsmåde ifølge et af de foregående krav, hvor bærersubstratets (30) halvledermateriale er siliciumcarbid og har en monokrystallinsk, polykrystallinsk eller amorf struktur.

11. Fremstillingsfremgangsmåde ifølge et af de foregående krav, hvor filmens (2) halvledermateriale er valgt blandt silicium eller germanium.

12. Fremstillingsfremgangsmåde ifølge et af de foregående krav, hvor agglomeraterne (21) har en tykkelse på mindre end eller lig med 40 nm eller mindre end eller lig med 30 nm.

13. Fremstillingsfremgangsmåde ifølge et af de foregående krav, hvor agglomeraterne (21) er i form af:

- første præcipitater, der omfatter filmens (2) halvledermateriale,

- sekundære præcipitater, der omfatter filmens (2) halvledermateriale og oxygen, og/eller

- hulrum, der er beklædt med en forbindelse, der omfatter filmens (2) halvledermateriale og oxygen.

14. Fremstillingsfremgangsmåde ifølge det foregående krav, hvor de sekundære præcipitater har en i det væsentlige triangulær form i et tværgående plan vinkelret på hovedplanet (x,y).

15. Elektronisk komponent, der er fremstillet på og/eller i et nyttelag (10) i en halvlederstruktur (100) som følge af fremstillingsfremgangsmåden ifølge et af de foregående krav, hvor halvlederstrukturen (100) omfatter:

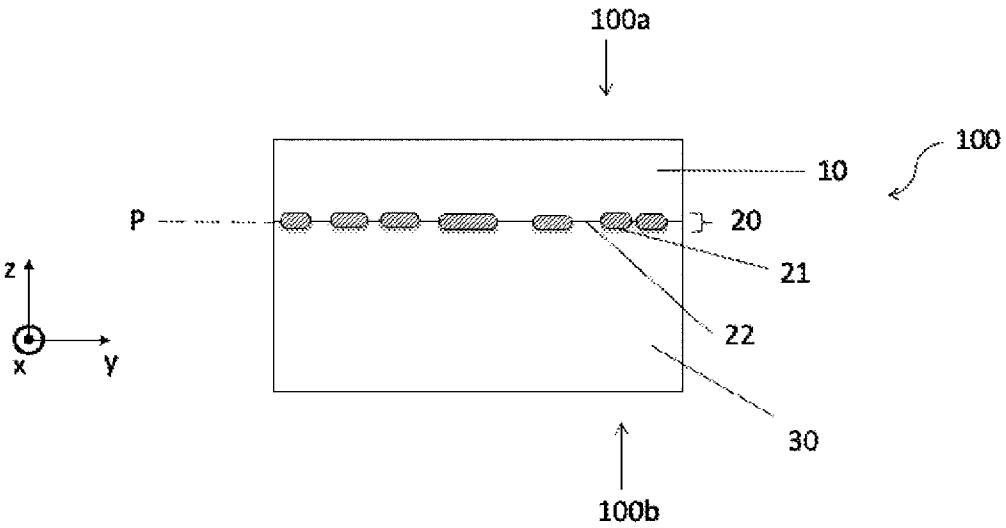
- nyttelaget (10), der er fremstillet af et halvledermateriale og strækker sig i et hovedplan (x,y),

- et bærersubstrat (30), der er fremstillet af et halvledermateriale,

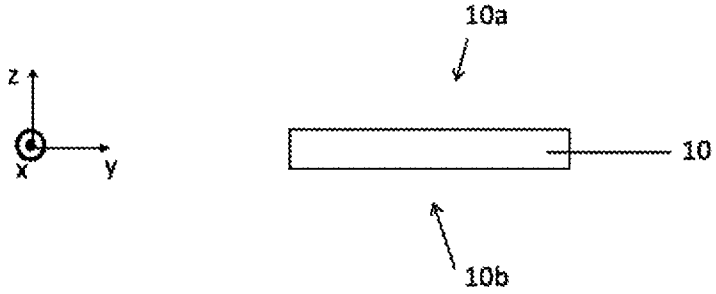
- og et grænsefladeområde (20) mellem nyttelaget (10) og bærersubstratet (30), der strækker sig parallelt med hovedplanet (x,y), hvor grænsefladeområdet (20) omfatter områder (22) med direkte kontakt mellem nyttelaget (10) og bærersubstratet (30) og agglomerater (21), der omfatter et halvledermateriale, som er forskelligt fra nyttelagets (10) og bærersubstratets (30) materiale eller materialer og har en tykkelse, langs en akse (z) vinkelret på hovedplanet (x,y), på mindre end eller lig med 250 nm; hvor områderne (22) med direkte kontakt og agglomeraterne (21) støder op til hinanden i hovedplanet (x,y).

16. Elektronisk komponent ifølge det foregående krav, der på en bagflade af halvlederstrukturen (100) omfatter mindst én elektrisk kontakt på og/eller i bærersubstratet (30) til en effektanvendelse.

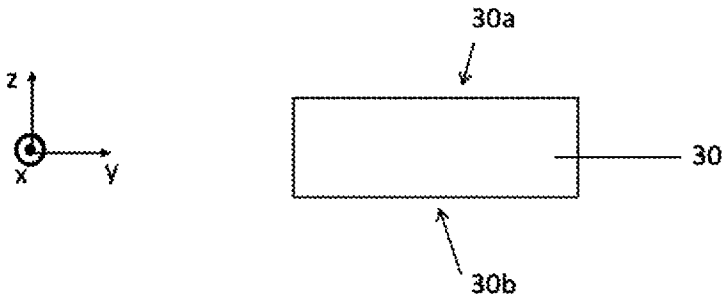
[Fig. 1]



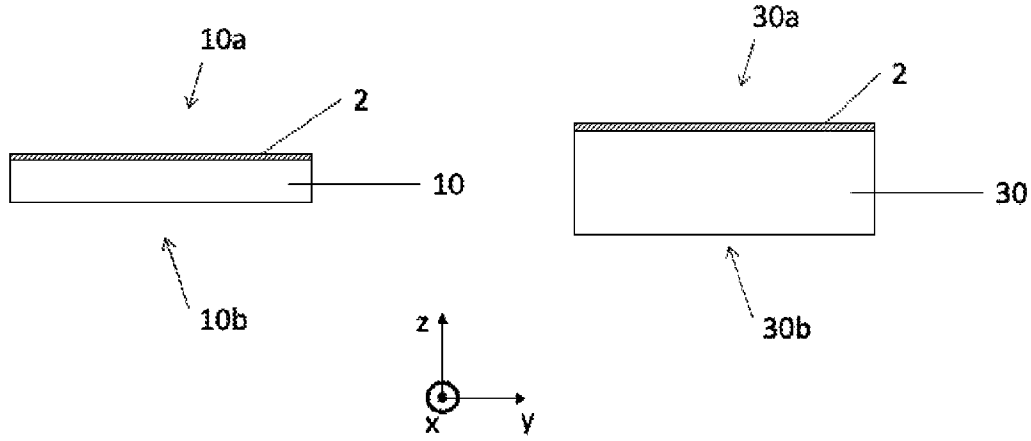
[Fig. 2a]



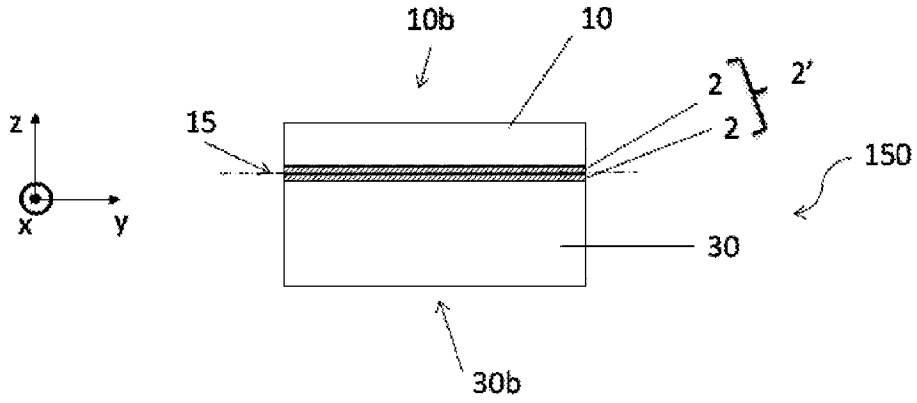
[Fig. 2b]



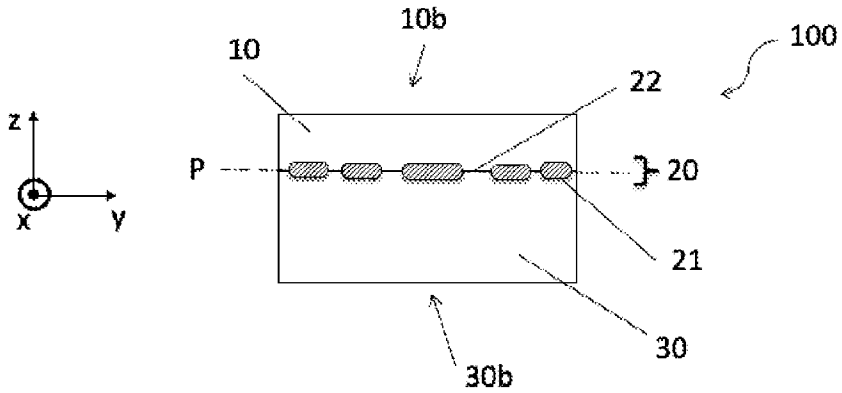
[Fig. 2c]



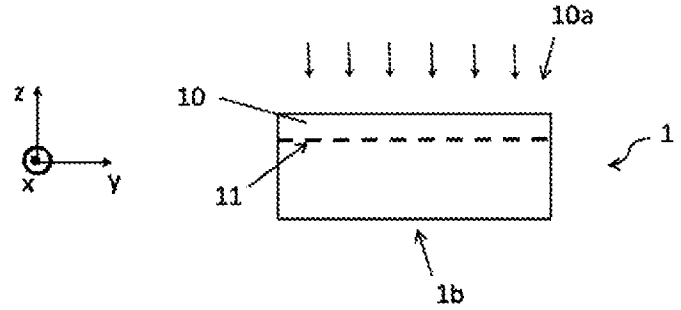
[Fig. 2d]



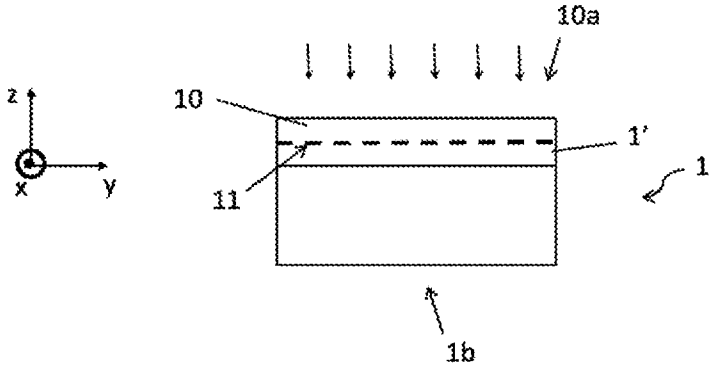
[Fig. 2e]



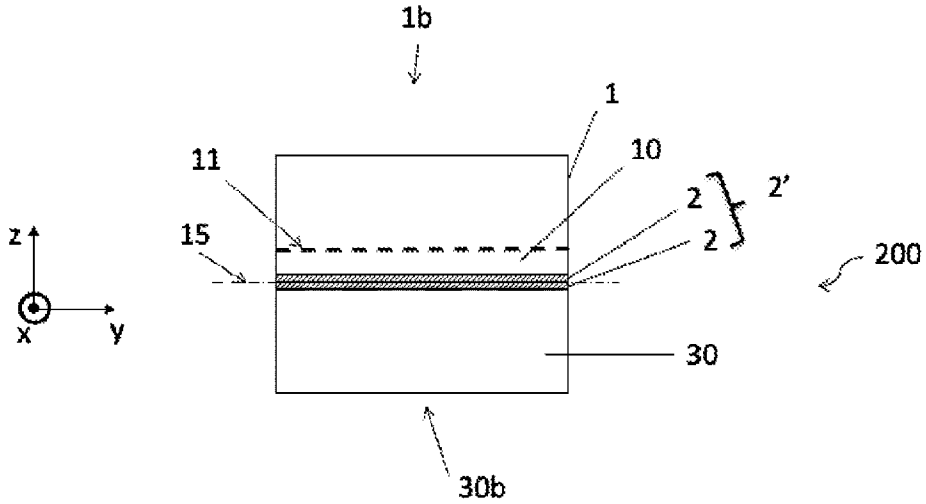
[Fig. 3a]



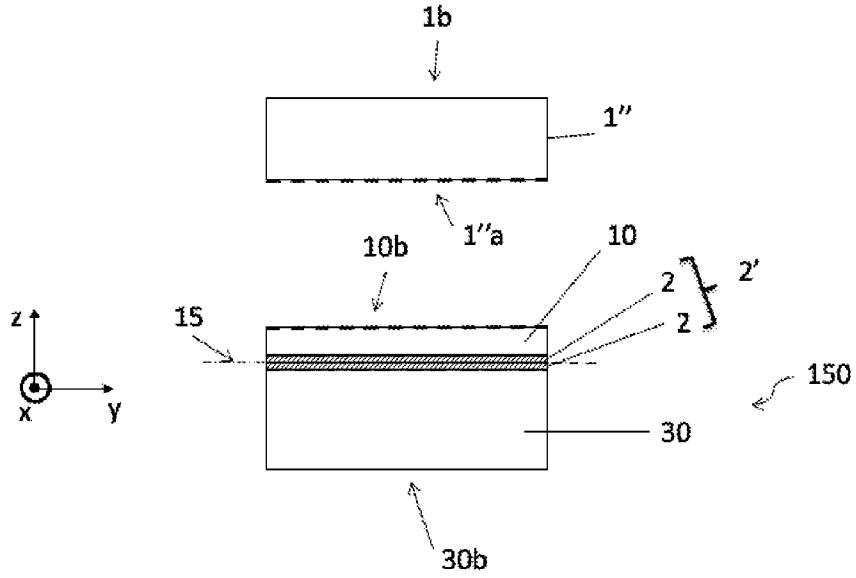
[Fig. 3b]



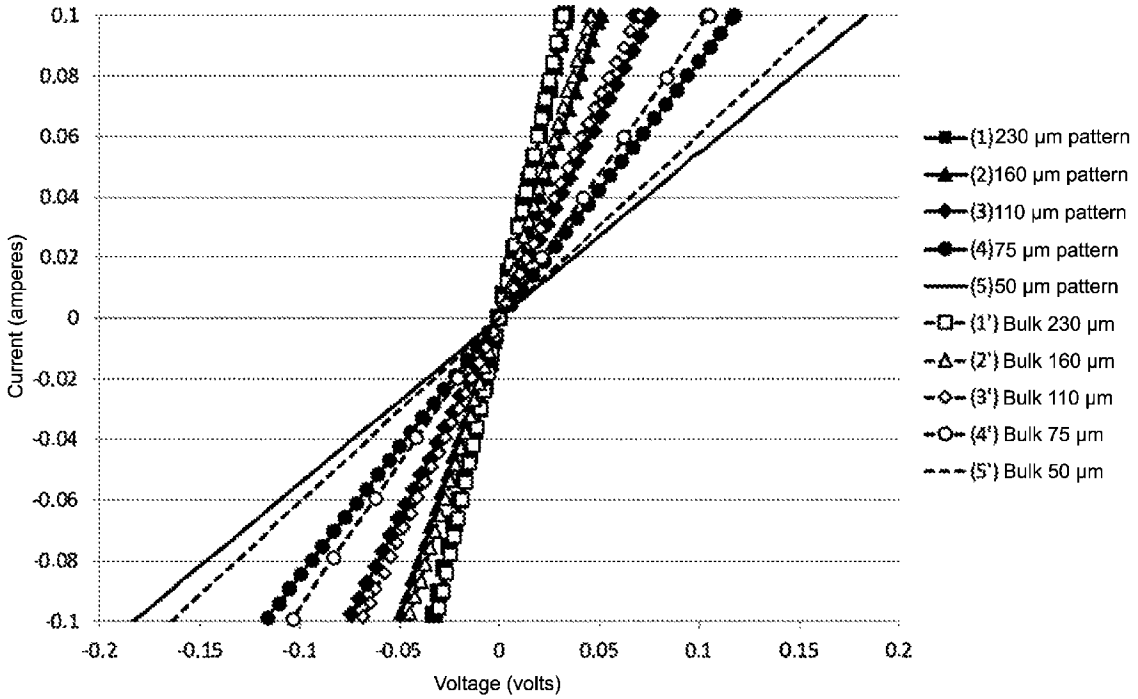
[Fig. 3c]



[Fig. 3d]


1b
1''
1''a
10b
10
2
2'
2
15
150
30
30b
z
x
y

[Fig. 4a]


0.1
0.08
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
-0.08
-0.1
Current (amperes)
-0.2
-0.15
-0.1
-0.05
0
0.05
0.1
0.15
0.2
Voltage (volts)
(1)230 µm pattern
(2)160 µm pattern
(3)110 µm pattern
(4)75 µm pattern
(5)50 µm pattern
(1') Bulk 230 µm
(2') Bulk 160 µm
(3') Bulk 110 µm
(4') Bulk 75 µm
(5') Bulk 50 µm

[Fig. 4b]