The present invention provides a Via Code Mask read-only memory comprising an array of transistors, and a plurality of bit lines and word lines, wherein the transistors in each row of the array are connected in series by connection of a drain/source of one transistor with a drain/source of another transistor. Both ends of the series of the transistors in each row of the array are connected to a supply voltage together. Each one of the bit lines is selectively connected to drain(s)/source(s) of one or more transistors in one corresponding column. Each one of the word lines connects together gates of the transistors in one corresponding row.
FIG. 1 (PRIOR ART)
FIG. 2
VI A CODE MASK ROM

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a Mask read-only memory (Mask ROM), and particularly to a VIA Code Mask ROM having a smaller circuit area.

[0003] 2. Description of the Prior Art

[0004] Mask ROM is a basic kind of ROM. In manufacturing of a Mask ROM, the connections within the array of the memory cells for storing particular information are determined by a mask. Thus, to manufacture a ROM for storing different information, only the mask need be modified rather than the whole process of manufacturing the ROM.

[0005] Referring to FIG. 1, a traditional Mask ROM comprises a row address decoder 101 receiving a row address 104, a column address decoder 102 receiving a column address 105 and having an output 106, and an array 103 of memory cells. The array 103 of memory cells comprises an array of transistors 111–114, 4 bit lines C1–C4 connected to the column address decoder 102 and 4 word lines R1–R4 connected to the row address decoder 101. In the array of the transistors 111–114, the connections between the transistors 111–114 and the bit lines C1–C4 are carried out by Via Code and shown in FIG. 1, wherein a black dot on the intersection of two crossed lines represents an electrical connection.

[0006] The operation of the traditional Mask ROM in FIG. 1 will be explained below. Initially, given that the voltage level on each of the word lines R1–R4 is lower than the threshold voltage, all the transistors 111–114 are turned off and the voltage level on each of the bit lines C1–C4 represents a “1” (logic high). When receiving the row address 104, the row address decoder 101 pulls up the voltage level on one of the word lines R1–R4 accordingly, to turn on a corresponding row of transistors. Specifically, if the word line R1 is selected, the voltage level thereon is pulled up to be higher than the threshold voltage and the transistors 111–114 are turned on. Since the bit lines C1, C3 and C4 are connected to the drains/sources of the transistor 111, 113 and 114, the logic levels of bit lines C1, C2, C3 and C4 are 0, 1, 0 and 0, respectively, when the word line R1 is selected.

[0007] Afterwords, the column address decoder 101 receives the column address 105 and accordingly selects a voltage level from one of the bit lines C1–C4 as the output 106. Therefore, the output 106 can be a value selected from the 16 values (0, 1, 0, 0), (0, 1, 0, 1), (1, 0, 1, 0), (0, 0, 0, 0) according to the row and column address 104 and 105. That is to say, the Mask ROM in FIG. 1 is a 16-bit ROM.

[0008] Generally, there are two kinds of code used to carry out the connections between the transistors and the bit lines. They are Buried P+ Code and Via Code. In a Buried P+ Code Mask ROM, the Buried P+ Code is under the gate of a transistor so that it is possible for two adjacent transistors to have a common drain/source. However, in a Via Code Mask ROM, the Via Code is under the drain/source of a transistor so that a common drain/source for two adjacent transistors is not practicable. Thus makes the required circuit area for the Via Code Mask ROM larger than that for the Buried P+ Code Mask ROM.

SUMMARY OF THE INVENTION

[0009] In order to solve the above problem, it is therefore one object of the invention to provide a Via Code Mask ROM with a smaller circuit area.

[0010] The present invention provides a Via Code Mask read-only memory comprising an array of transistors, and a plurality of bit lines and word lines, wherein the transistors in each row of the array are connected in series by connection of a drain/source of one transistor with a drain/source of another transistor. Both ends of the series of the transistors in each row of the array are connected to a supply voltage together. Each one of the bit lines is selectively connected to drain(s)/source(s) of one or more transistors in one corresponding column. Each one of the word lines connects together gates of the transistors in one corresponding row.

[0011] Accordingly, in the present invention, most of the transistors are placed at the spaces between two adjacent bit lines. People skilled in the art will appreciate that there is sufficient space between two adjacent bit lines. Thus, there is no need for an additional circuit area for the transistors, which makes the whole circuit area of a Via Code Mask ROM smaller.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings, given by way of illustration only and thus not intended to be limiting of the present invention.

[0013] FIG. 1 is a block diagram showing a circuit of a traditional Mask ROM;

[0014] FIG. 2 is a block diagram showing a circuit of a Via Code Mask ROM according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] FIG. 2 is a block diagram showing a circuit of a Via Code Mask ROM according to the invention. The Mask ROM shown in FIG. 1 and FIG. 2 are both 16-bit ROMs and store the same information. The distinction between them is the configuration of the array of the transistors.
Referring to FIG. 2, according to one embodiment of the invention, a Via Code Mask ROM comprises a row address decoder 201 receiving a row address 204, a column address decoder 202 receiving a column address 205 and having an output 206, and an array 203 of memory cells. The array 203 of memory cells comprises an array of transistors 211–245, 4 bit lines C1–C4 connected to the column address decoder 202 and 4 word lines R1–R4 connected to the row address decoder 201. In the array of the transistors 211–245, it is noted that the transistors in one row, transistors 211–215 for example, are connected in series by connection of a drain/source of one transistor with a drain/source of another transistor. In addition, both ends of the series of the transistors in one row are connected to a supply voltage Vss (not shown) or ground together. The connections between the transistors 211–244 and the bit lines C1–C4 are carried out by Via Code and —shown in FIG. 2, wherein a black dot on the intersection of two crossed lines represents an electrical connection.

What is claimed is:
1. A Via Code Mask read-only memory, comprising:
   an array of transistors, wherein by connection of a drain/source of one transistor with a drain/source of another transistor, the transistors in each row of the array are connected in series, and both ends of the series of the transistors in each row of the array are connected to a supply voltage together;
   a plurality of bit lines, wherein each one of the bit lines is selectively connected to drain(s)/source(s) of one or more transistors in one corresponding column; and
   a plurality of word lines, wherein each one of the word lines connects together gates of the transistors in one corresponding row.
2. The Via Code Mask read-only memory as claimed in claim 1, wherein the supply voltage is a ground voltage.
3. The Via Code Mask read-only memory as claimed in claim 1, wherein the connections between the bit lines and drain(s)/source(s) of the transistors are carried out by Via Code.
4. A Via Code Mask read-only memory, comprising:
   an array of memory cells comprising:
   an array of transistors, wherein by connection of a drain/source of one transistor with a drain/source of another transistor, the transistors in each row of the array are connected in series, and both ends of the series of the transistors in each row of the array are connected to a supply voltage together;
   a plurality of bit lines, wherein each one of the bit lines is selectively connected to drain(s)/source(s) of one or more transistors in one corresponding column; and
   a plurality of word lines, wherein each one of the word lines connects together gates of the transistors in one corresponding row;
a row address decoder receiving a row address and accordingly turning on all the transistors in one of the columns of the array through one of the corresponding word lines; and

a column address decoder receiving a column address, selecting one of the bit lines accordingly and outputting a voltage on the selected bit line.

5. The Via Code Mask read-only memory as claimed in claim 4, wherein the supply voltage is a ground voltage.

6. The Via Code Mask read-only memory as claimed in claim 4, wherein the connections between the bit lines and drain(s)/source(s) of the transistors are carried out by Via Code.