US 20170033184A1

(19) United States

(12) Patent Application Publication

(10) Pub. No.: US 2017/0033184 A1

He et al.

(43) Pub. Date: Feb. 2, 2017

(54) SEMICONDUCTOR DEVICE INCLUDING FIN HAVING CONDENSED CHANNEL REGION

(71) Applicant: **International Business Machines Corporation**, Armonk, NY (US)

(72) Inventors: **Hong He**, Schenectady, NY (US); **Effendi Leobandung**, Stormville, NY (US); **Gen Tsutsui**, Albany, NY (US); **Tenko Yamashita**, Schenectady, NY (US)

(21) Appl. No.: **14/809,688**

(22) Filed: **Jul. 27, 2015**

Publication Classification

(51) Int. Cl.

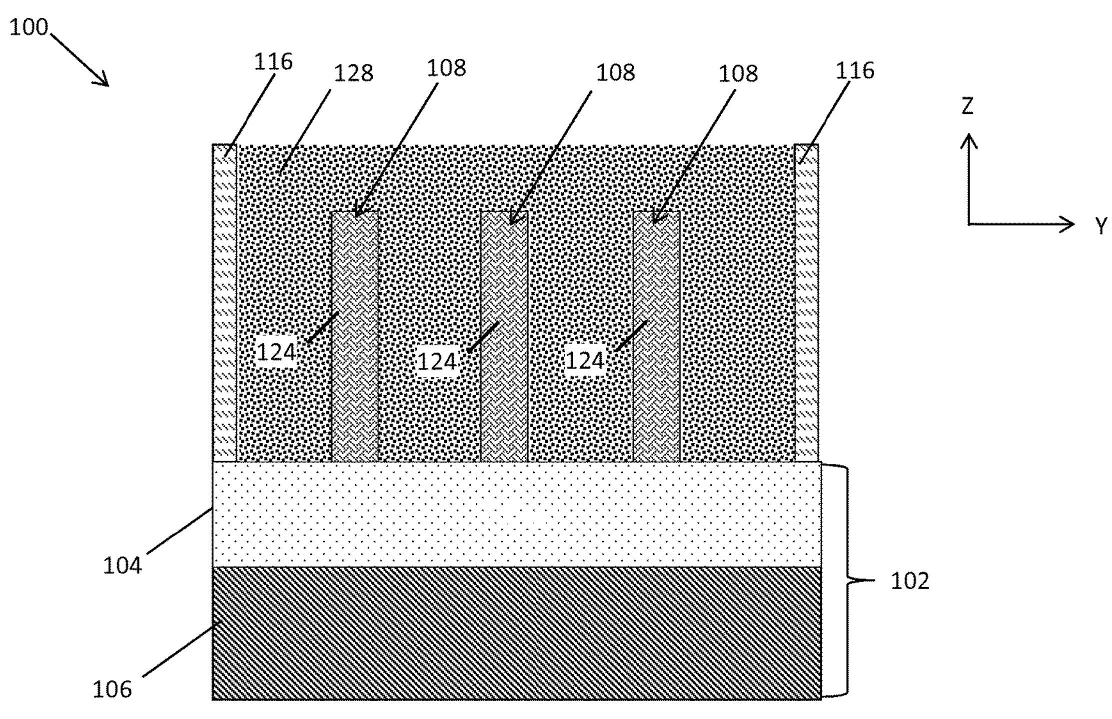
H01L 29/165	(2006.01)
H01L 21/311	(2006.01)
H01L 29/49	(2006.01)
H01L 29/78	(2006.01)
H01L 29/51	(2006.01)
H01L 29/66	(2006.01)
H01L 21/283	(2006.01)

(52) U.S. Cl.

CPC ***H01L 29/165*** (2013.01); ***H01L 29/6681*** (2013.01); ***H01L 21/31116*** (2013.01); ***H01L 21/283*** (2013.01); ***H01L 29/785*** (2013.01); ***H01L 29/518*** (2013.01); ***H01L 29/495*** (2013.01)

(57) **ABSTRACT**

A finFET semiconductor device includes at least one semiconductor fin on an upper surface of a substrate. The semiconductor fin includes a channel region interposed between opposing source/drain regions. A gate stack is on the upper surface of the substrate and wraps around sidewalls and an upper surface of only the channel region. The channel region further includes a condensed portion formed of a first semiconductor material and a second semiconductor material. The source/drain regions are formed of the first semiconductor material while excluding the second semiconductor material.



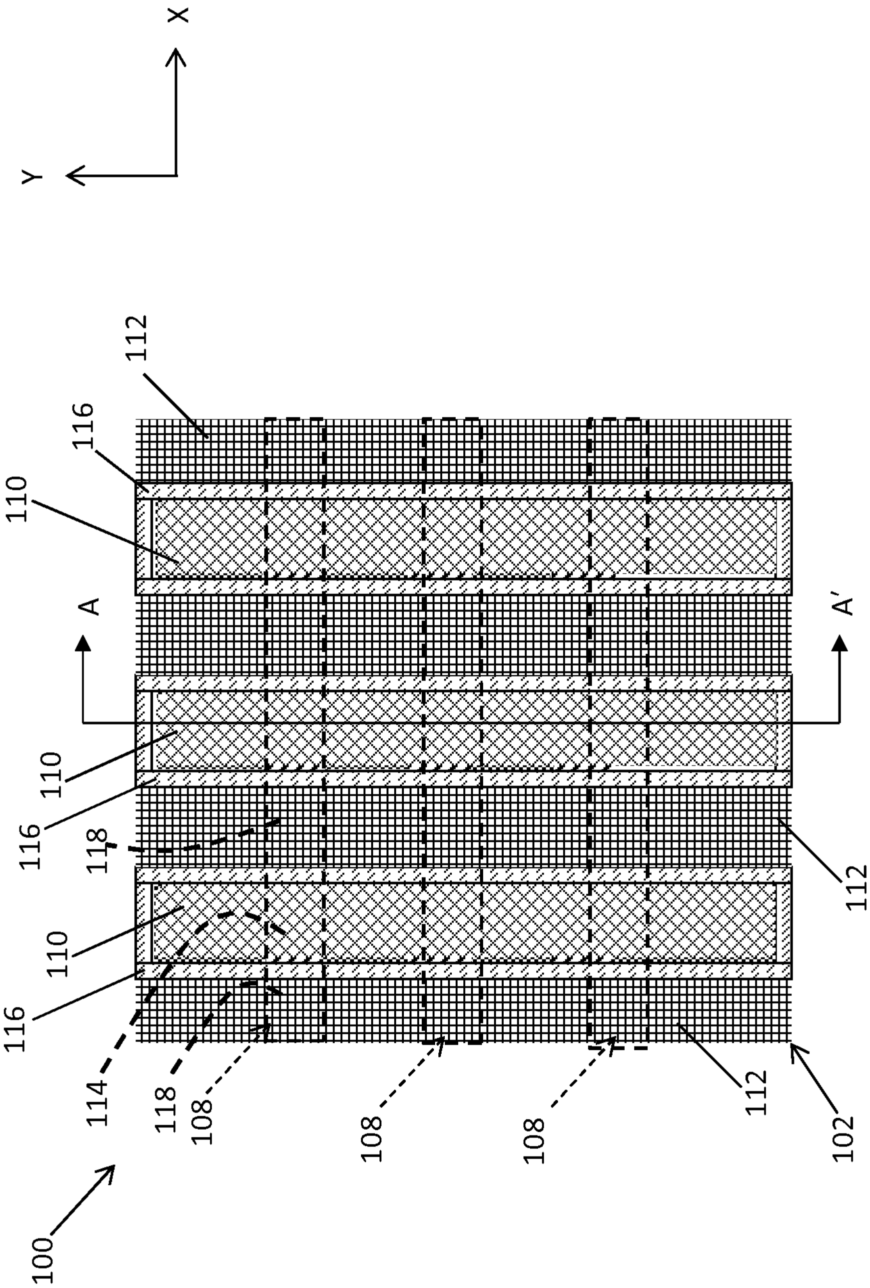

X
Y
112
116
110
A
A'
110
116
118
112
110
116
114
118
108
108
108
112
102
100

FIG. 1A

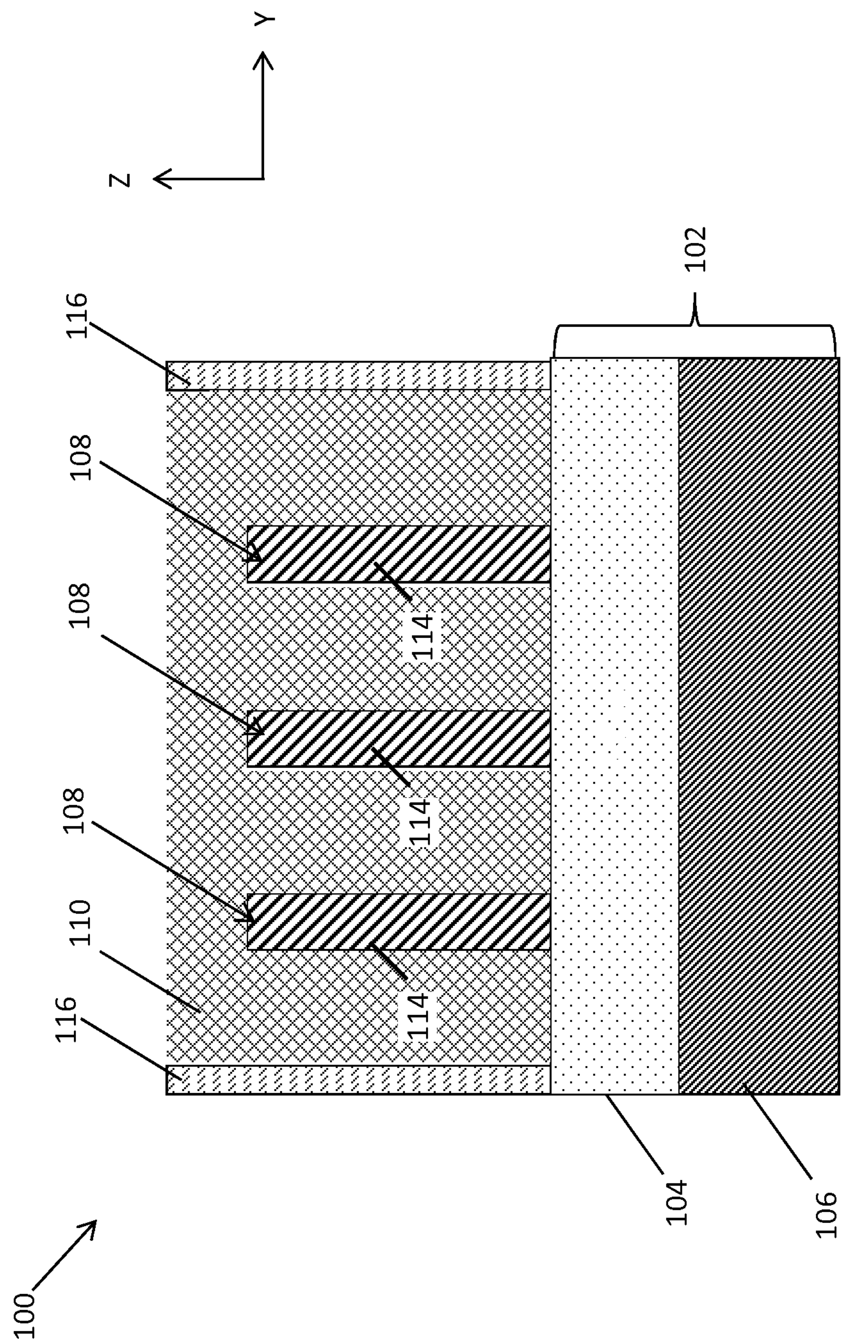


FIG. 1B

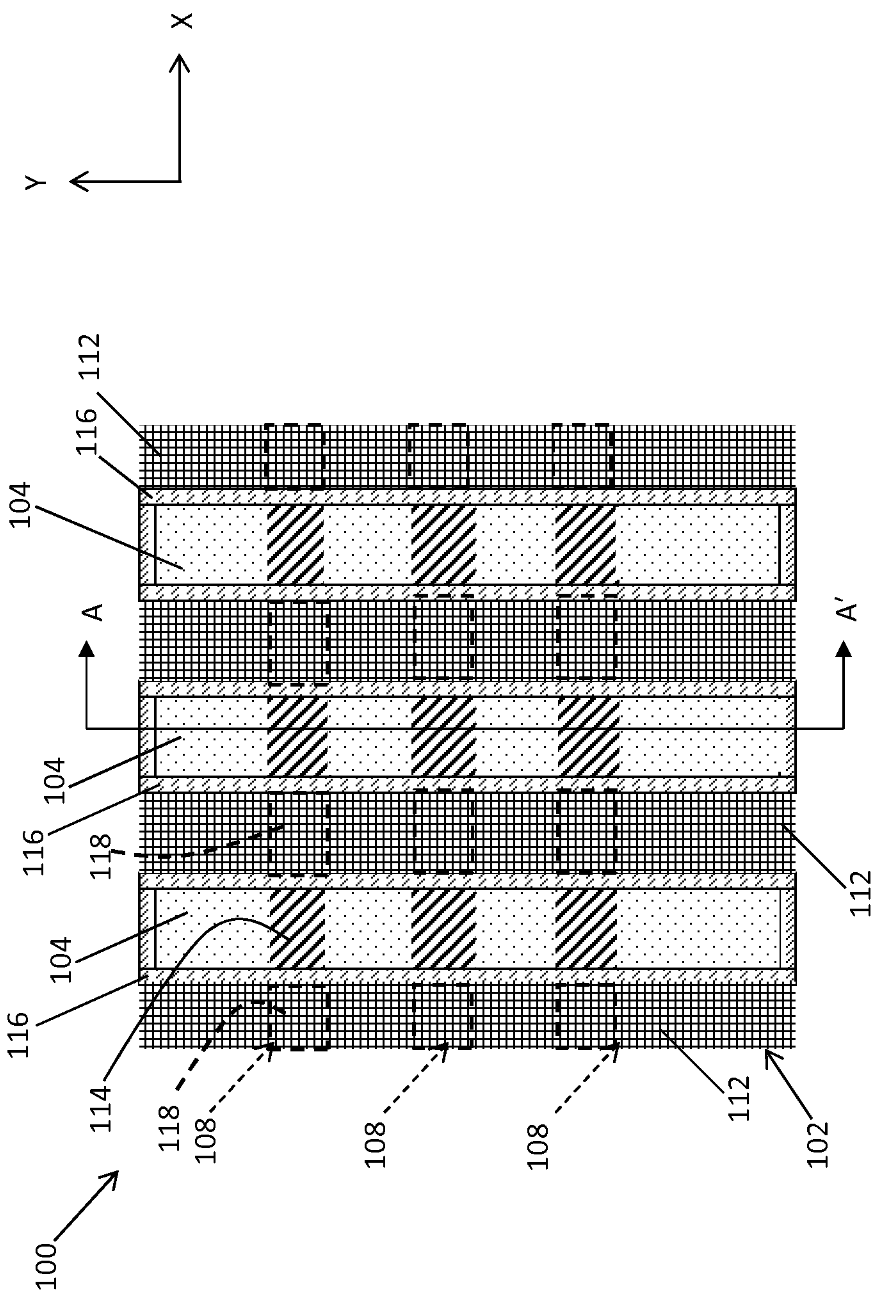

X
Y
112
116
104
A
A′
104
116
118
112
104
116
114
118
108
108
108
112
102
100

FIG. 2A

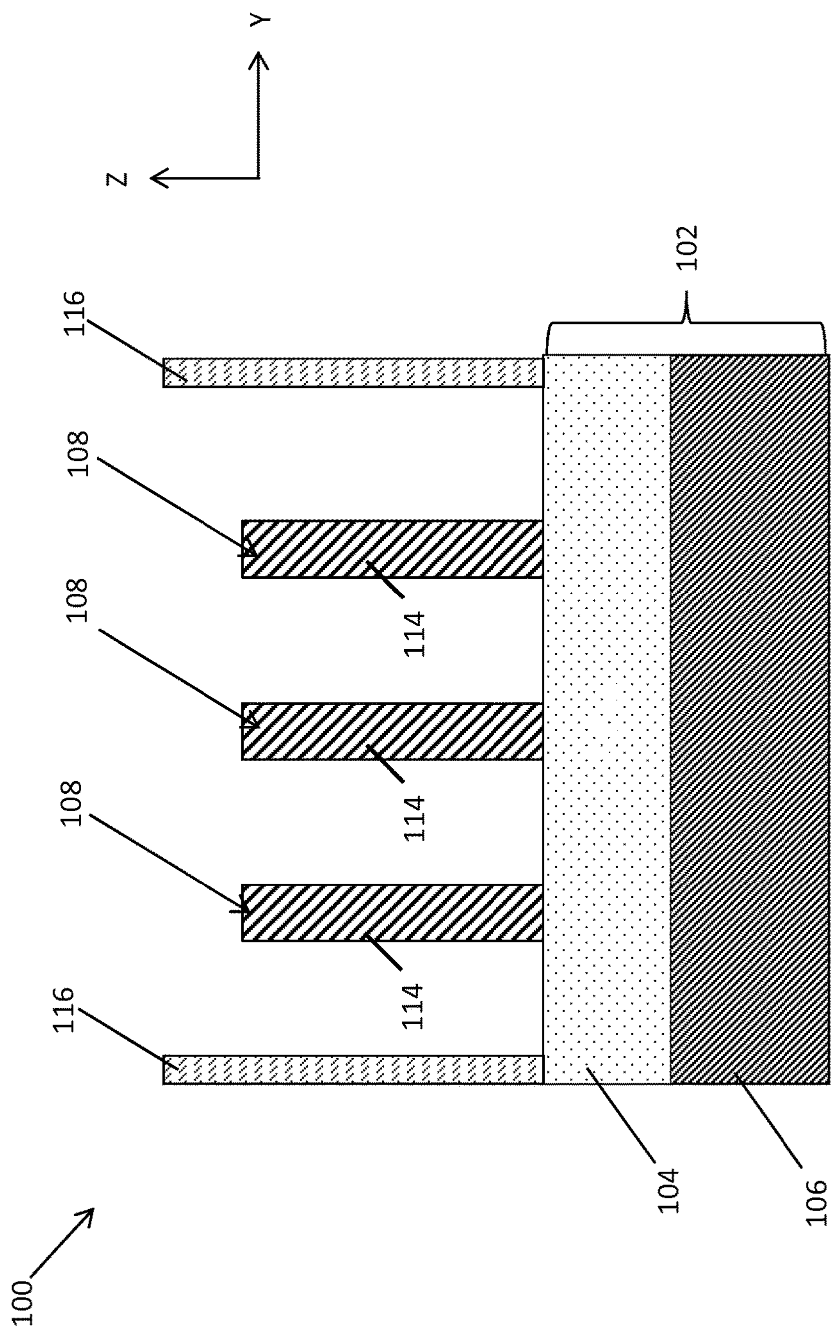


FIG. 2B

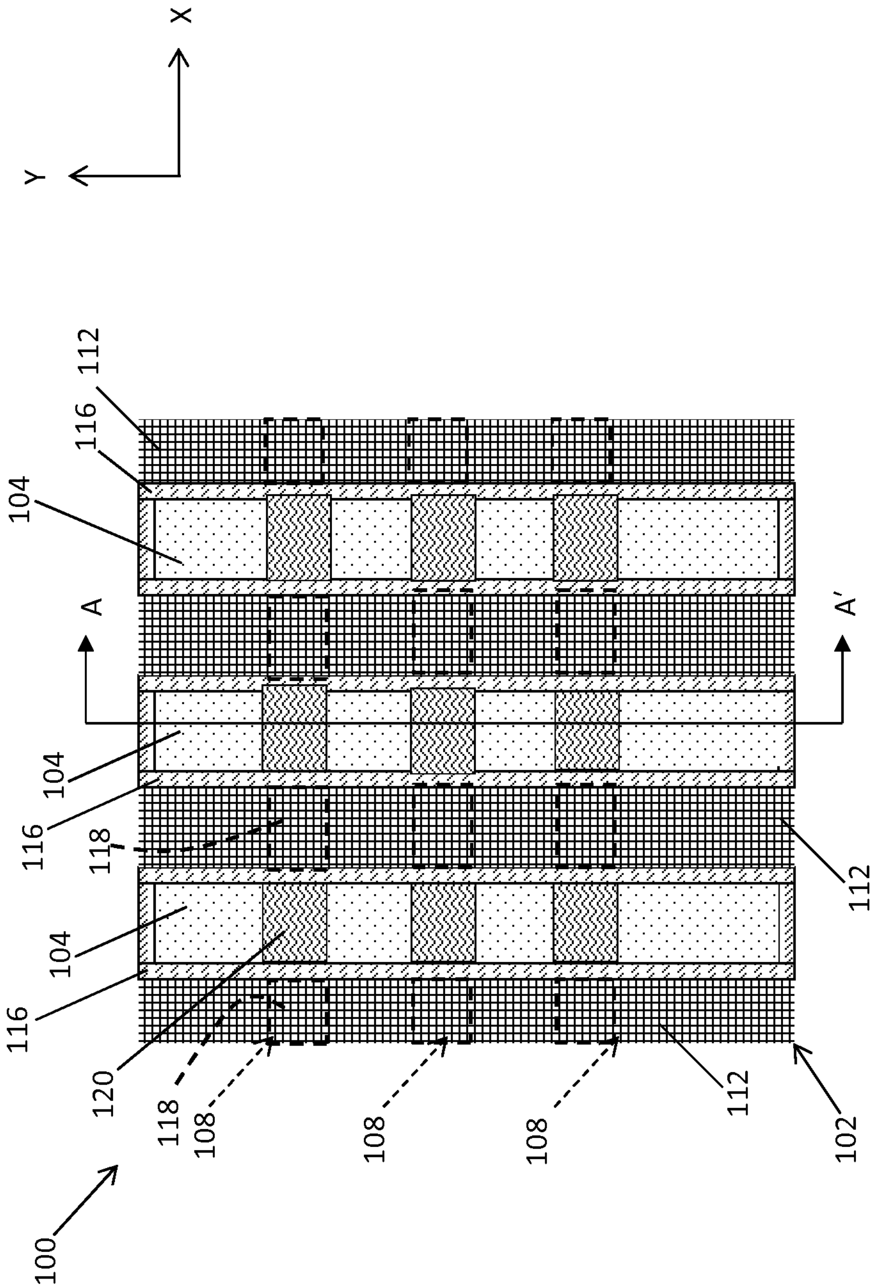

X
Y
112
116
104
A
A'
104
116
118
112
104
116
120
118
108
108
108
112
102
100

FIG. 3A

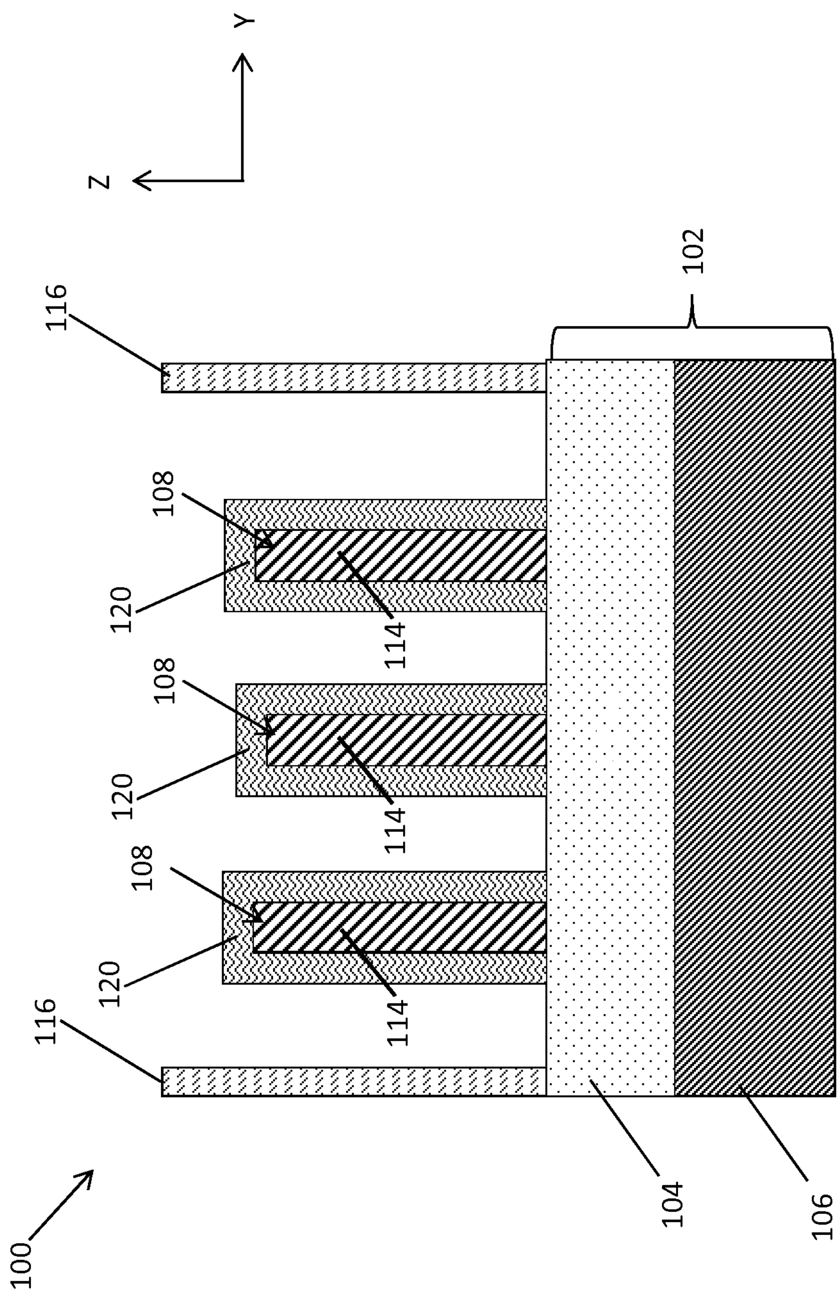


FIG. 3B

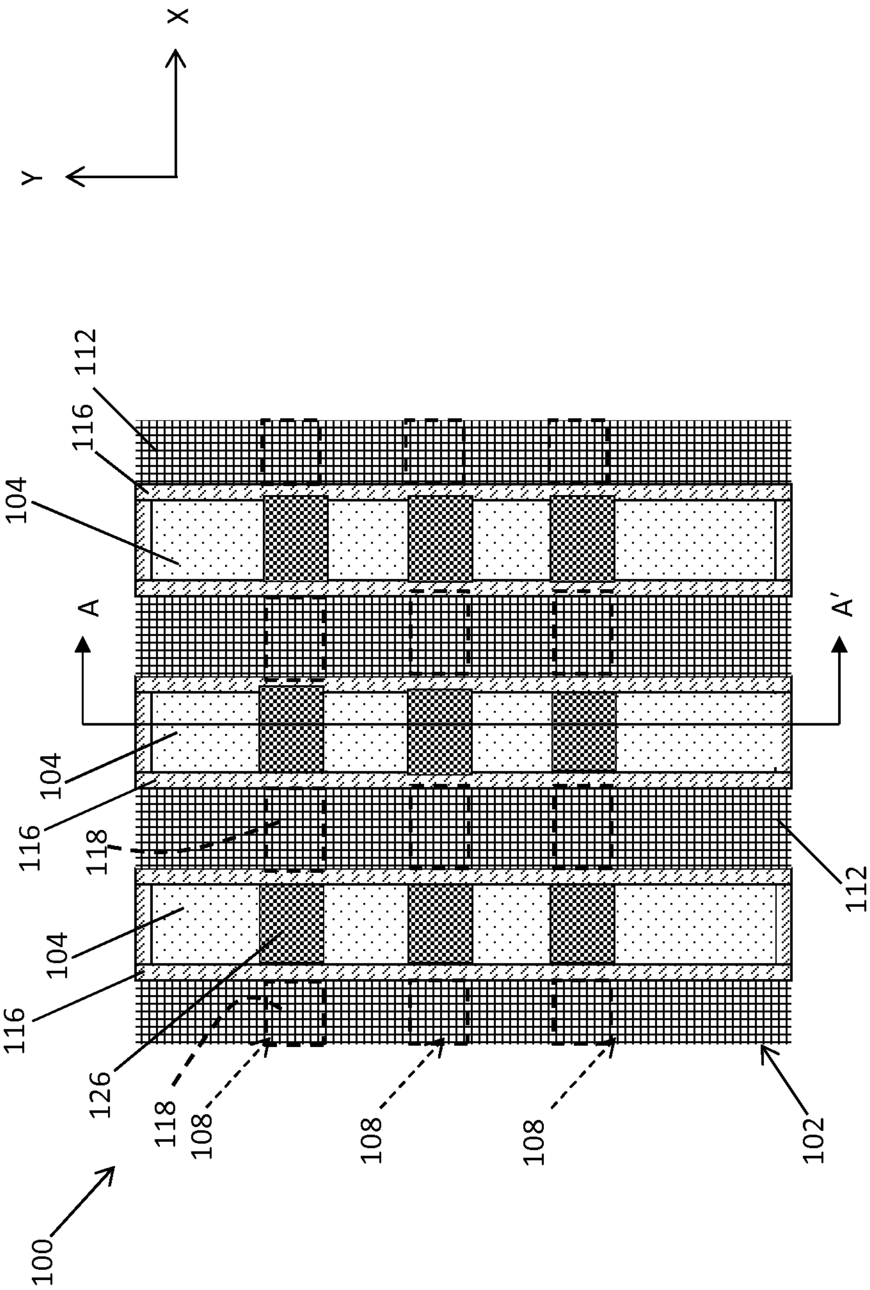

X
Y
112
116
104
A
A′
104
116
118
112
104
116
126
118
108
108
108
102
100

FIG. 4A

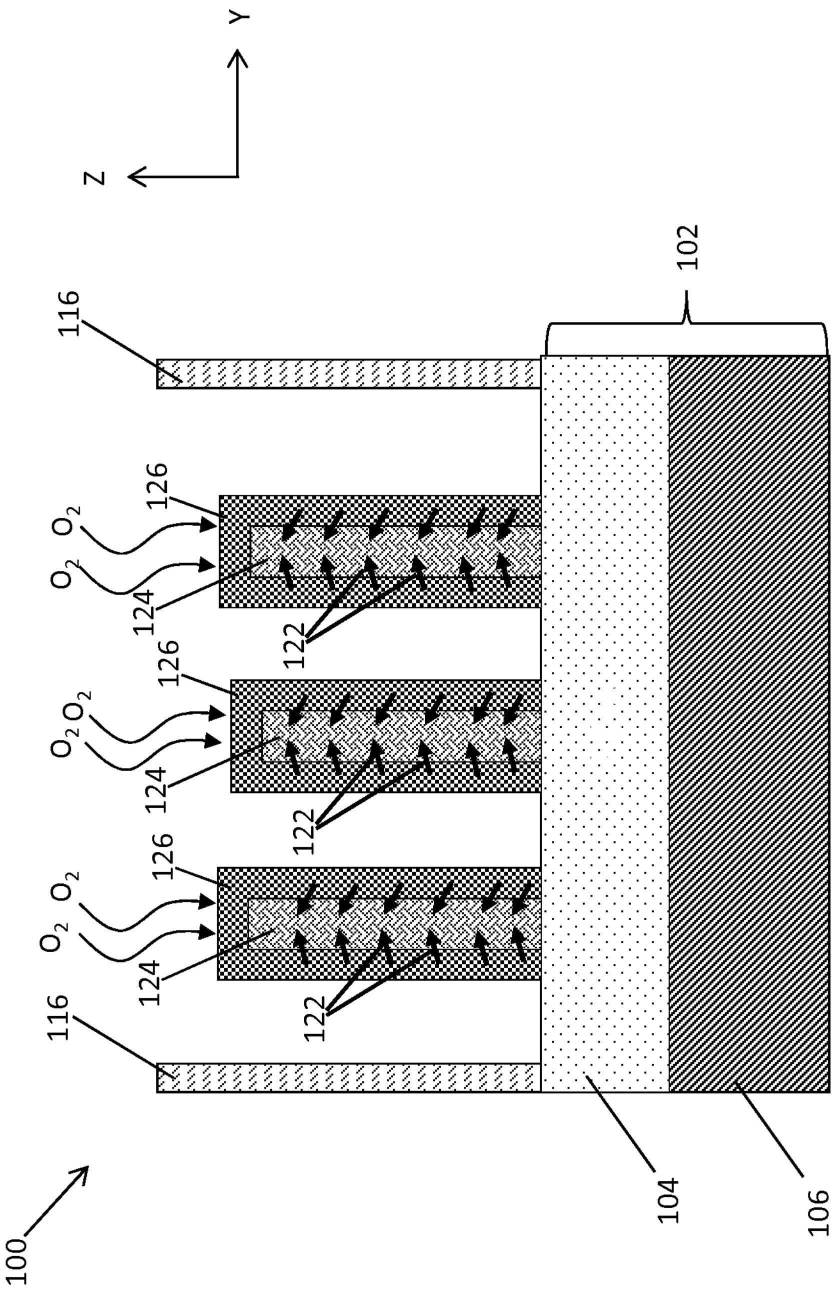


FIG. 4B

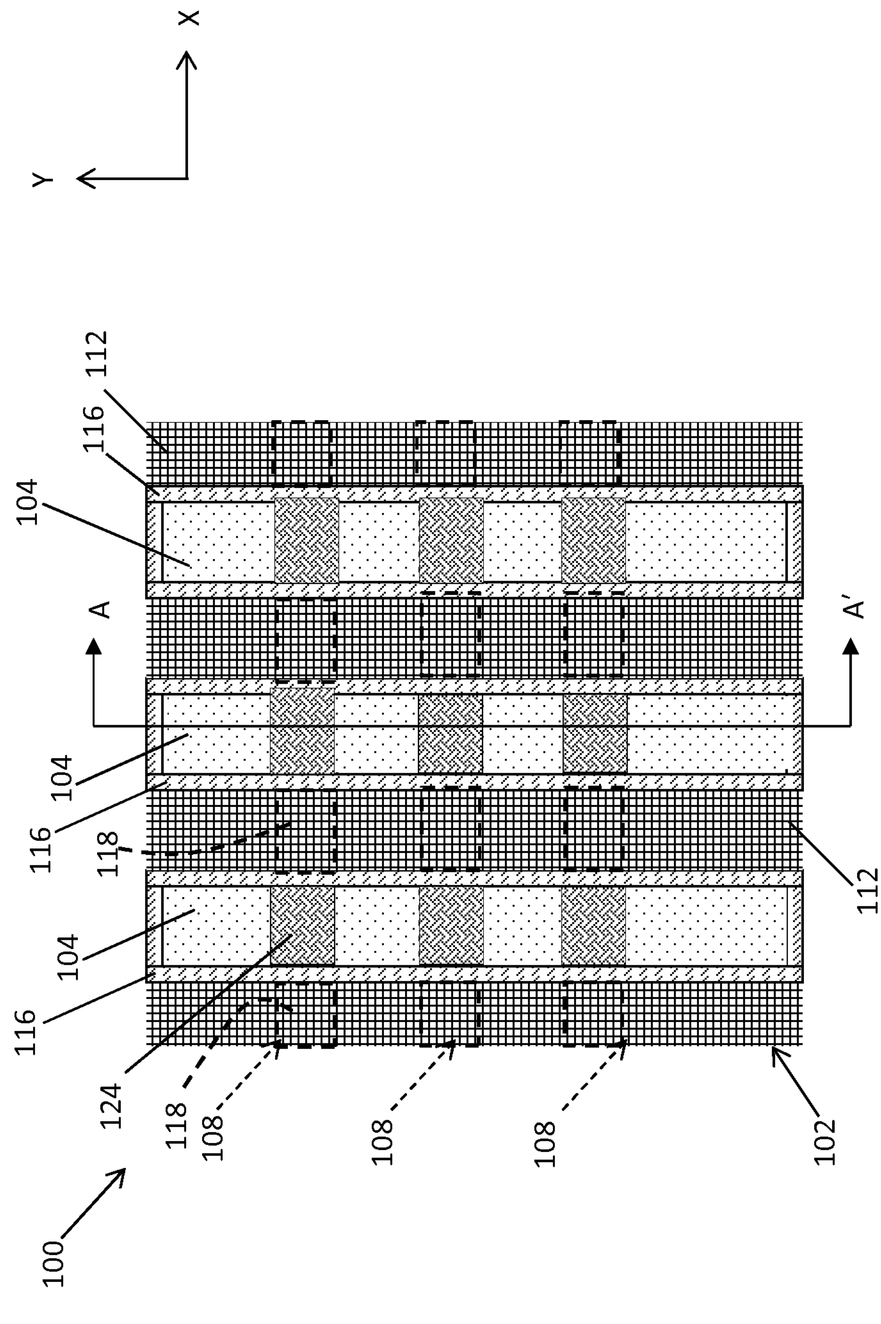

X
Y
112
116
104
A
A'
104
116
118
112
104
116
124
118
108
108
108
102
100

FIG. 5A

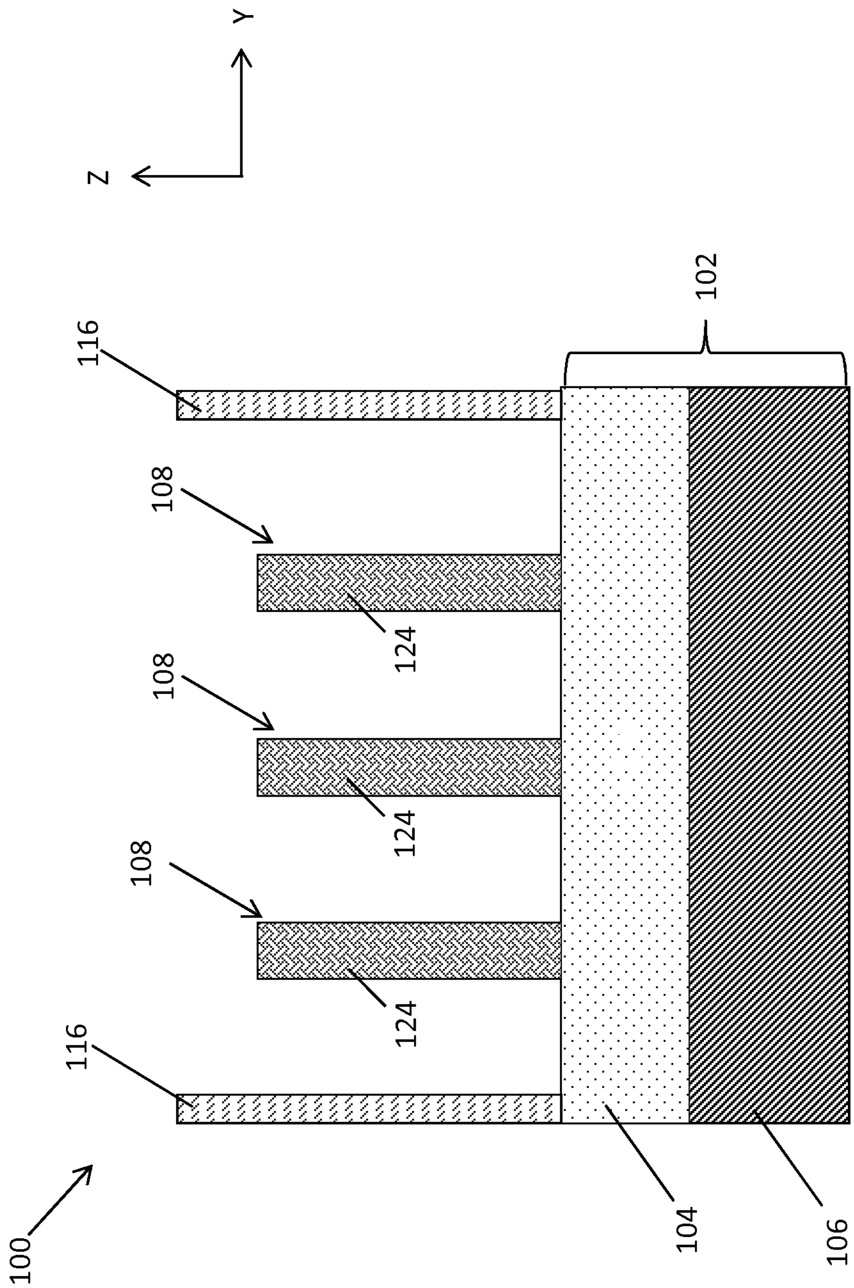


FIG. 5B

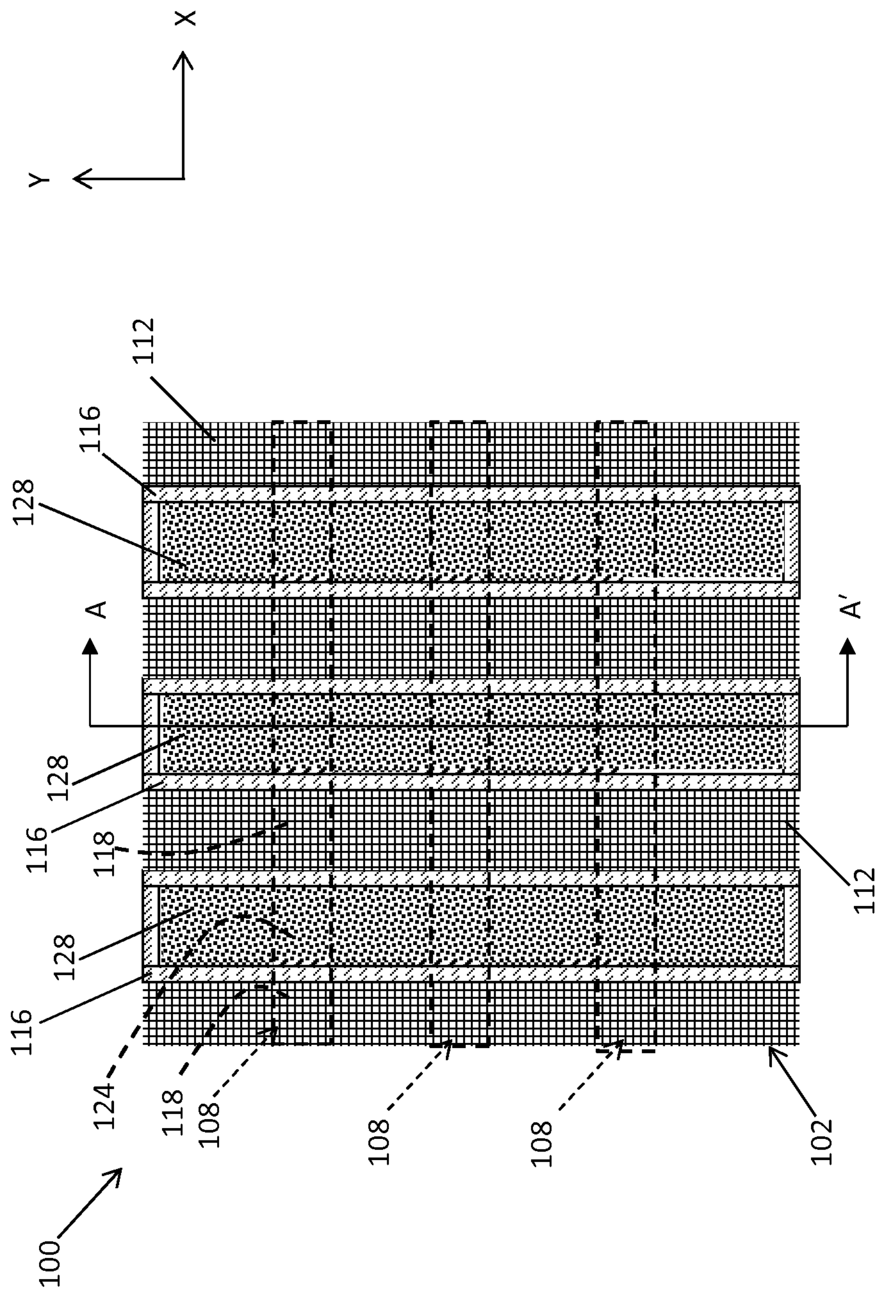

X
Y
112
116
128
A
A'
128
116
118
112
128
116
124
118
108
108
108
102
100

FIG. 6A

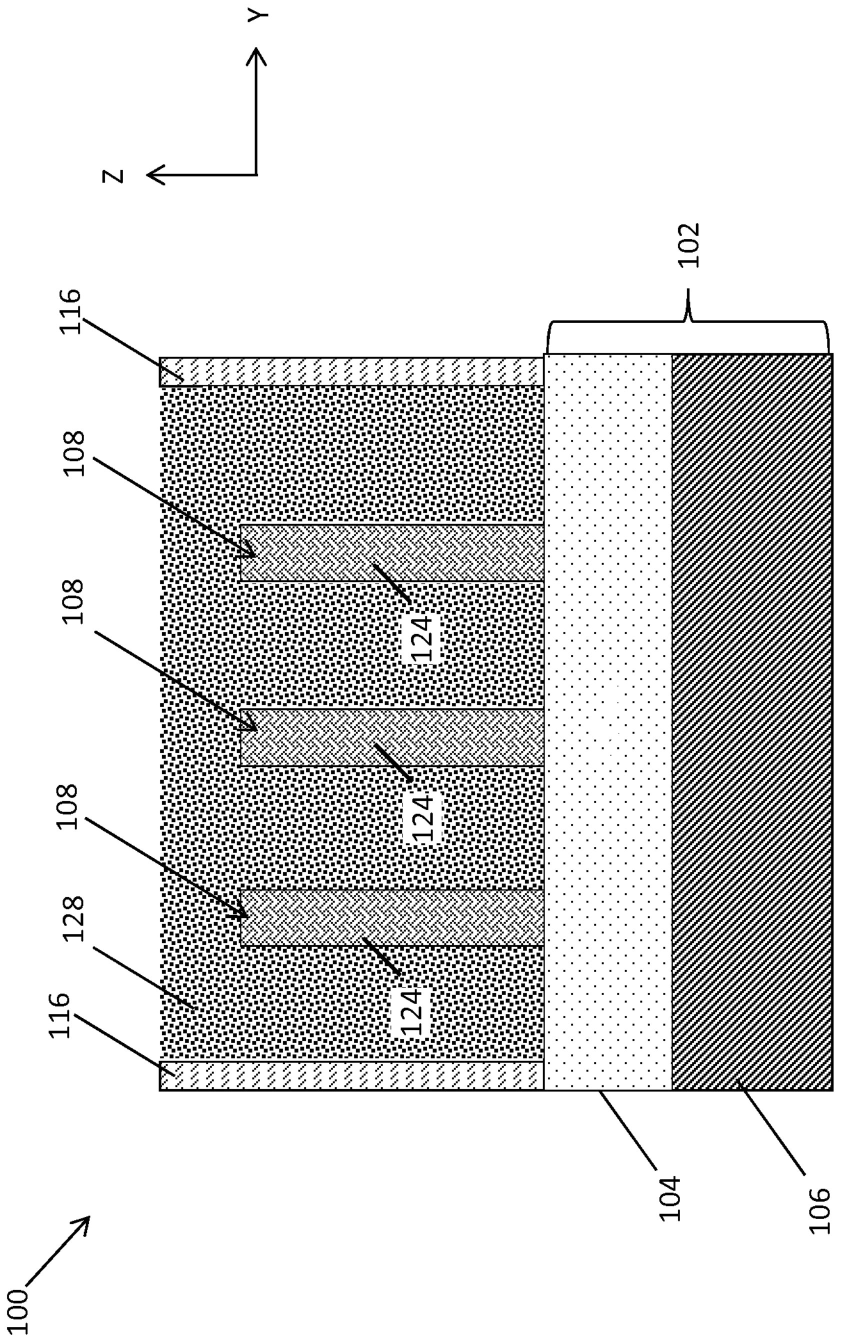


FIG. 6B

SEMICONDUCTOR DEVICE INCLUDING FIN HAVING CONDENSED CHANNEL REGION

BACKGROUND

[0001] The present invention relates to semiconductor devices, and more specifically, to fin-type field effect transistor (finFET) devices.

[0002] Recent semiconductor fabrication methods have been developed to replace pure silicon (Si) fins with silicon germanium (SiGe) fins, especially in p-type finFET devices. Forming the fins from SiGe reduces the threshold voltage (Vt) of the semiconductor device, thereby increasing the drive current that flows through the channel. Further, SiGe material provides higher carrier mobility than Si. Accordingly, SiGe fins may have improve hole mobility performance with respect to Si fins. Conventional methods use an ion implantation process that drives Ge ions into the fin to form a SiGe fin. However, these conventional ion implantation methods may damage the fin and reduce overall performance of the finFET device.

SUMMARY

[0003] According to a non-limiting embodiment, a finFET semiconductor device includes at least one semiconductor fin on an upper surface of a substrate. The semiconductor fin includes a channel region interposed between opposing source/drain regions. A gate stack is on the upper surface of the substrate and wraps around sidewalls and an upper surface of only the channel region. The channel region further includes a condensed portion formed of a first semiconductor material and a second semiconductor material. Unlike the channel region, the source/drain regions are formed of the first semiconductor material while excluding the second semiconductor material.

[0004] According to another non-limiting embodiment, a method of fabricating a finFET device comprises forming, on an upper surface of a semiconductor substrate, at least one semiconductor fin comprising a first semiconductor material. The at least one semiconductor fin has a channel region interposed between opposing source/drain regions. The method further includes forming a flowable insulator layer on the source/drain regions, and forming a dummy gate stack on the channel region. The method further includes selectively removing the dummy gate stack with respect to the flowable insulator layer to expose the channel region. The method further includes performing a condensation process to selectively transform the exposed channel region into a second semiconductor material different from the first semiconductor material so as to increase carrier mobility conductivity of the channel region, while maintaining the first semiconductor material of the source/drain regions.

[0005] Additional features are realized through the techniques of the present invention. Other embodiments are described in detail herein and are considered a part of the claimed invention. For a better understanding of the invention with the features, refer to the description and to the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The forgoing features are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[0007] FIG. **1**A illustrates an intermediate semiconductor device in a first orientation including a plurality of semiconductor fins including source/drain regions covered by a flowable insulator material and a channel region covered by a dummy gate stack according to a non-limiting embodiment;

[0008] FIG. **1**B illustrates the semiconductor device according to a second orientation;

[0009] FIG. **2**A illustrates the semiconductor device of FIGS. **1**A-**1**B in the first orientation following removal of the dummy gate stack to expose the channel regions of the fins;

[0010] FIG. **2**B illustrates the semiconductor device of FIG. **2**A in the second orientation;

[0011] FIG. **3**A illustrates the semiconductor device of FIGS. **2**A-**2**B in the first orientation after growing a condenser layer on the sidewalls and an upper surface of the channel regions;

[0012] FIG. **3**B illustrates the semiconductor device of FIG. **3**A in the second orientation;

[0013] FIG. **4**A illustrates the semiconductor device of FIGS. **3**A-**3**B in the first orientation undergoing a condensation processes so as to drive a donor material into the channel regions and oxidize the condenser layer;

[0014] FIG. **4**B illustrates the semiconductor device of FIG. **4**A in the second orientation;

[0015] FIG. **5**A illustrates the semiconductor device of FIGS. **4**A-**4**B in the first orientation after selectively removing the oxidized condenser layer from the condensed channel regions of the fins;

[0016] FIG. **5**B illustrates the semiconductor device of FIG. **5**A in the second orientation;

[0017] FIG. **6**A illustrates the semiconductor device of FIGS. **5**A-**5**B in the first orientation after forming a planarized metal gate structure that wraps around the condensed channel region of the fins; and

[0018] FIG. **6**B illustrates the semiconductor device of FIG. **6**A in the second orientation.

DETAILED DESCRIPTION

[0019] The transistor gain of semiconductor devices such as finFET devices, for example, is proportional to the mobility of the majority carrier traveling through the channel region. The current carrying capability, and therefore the performance of a finFET device is proportional to the mobility of the majority carrier in the channel. Traditional finFET devices include one or more semiconductor fins formed of silicon (Si). However, studies of semiconductor materials have shown that silicon germanium (SiGe) provides increased hole mobility, which are the majority carriers in a P-channel field effect transistor (i.e., PFET devices). Various non-limiting embodiments of the invention provide a finFET device including one or more fins having a SiGe condensed channel region. In this manner, hole mobility through the channel region of the fin is improved so as to enhance the overall performance of the finFET device.

[0020] With reference now to FIGS. **1**A-**1**B, a semiconductor structure **100** which serves as a starting point for fabricating a finFET device in accordance with an exemplary embodiment is shown. The semiconductor structure **100** includes a semiconductor substrate **102** extending along a first axis (e.g., X-axis) to define a length, a second axis (e.g., Y axis) to define a width, and a third axis (Z-axis) to define a height. The substrate **102** is formed as a semiconductor-on-insulator (SOI) substrate, for example, including a buried insulator layer **104** (FIG. **1**B) formed on an upper surface of a bulk substrate layer **106**. The buried insulator layer **104** is formed of, for example, silicon dioxide (SiO_2) and the bulk substrate layer **106** is formed, for example, of silicon (Si). The buried insulator layer **104** has a vertical thickness (e.g., height) ranging from, for example, approximately 0.5 nanometers to approximately 200 nm. An active semiconductor layer (not shown) formed atop the buried insulator layer **104** is patterned to form one or more semiconductor fins **108**, as further illustrated in FIG. **1**B. According to a non-limiting embodiment, the semiconductor fins **108** are initially formed of silicon (Si). Various fin fabrications can be used to form the semiconductor fins **108** such as, for example, a sidewall image transfer (SIT) process. The semiconductor fins **108** extend along the X-axis to define a fin length, the Y-axis to define a fin width, and the Z-axis to define a fin height. The fin width ranges from approximately 3 nm to approximately 10 nm, the fin length ranges from approximately 50 nm to approximately 2000 nm, and the fin height ranges from ranges from approximately 20 nm to approximately 60 nm.

[0021] As further illustrated in FIGS. **1**A-**1**B, the semiconductor fins **108** are covered by one or more dummy gate stacks **110** and a flowable insulator layer **112** (FIG. **1**A). The dummy gate stacks **110** are formed on an upper surface of the buried insulator layer **104** and wrap around the channel region **114** of the semiconductor fins **108**. According to at least one embodiment, the dummy gate stacks **110** are formed, for example, of an amorphous or polysilicon material. The dummy gate stacks **110** extend along the Y-axis to define a gate width, the X-axis to define a gate length, and the Z-axis to define a gate height. The gate width ranges from approximately 50 nm to approximately 2000 nm, the gate length ranges from approximately 15 nm to approximately 500 nm, and the gate height ranges from approximately 50 nm to approximately 150 nm. Although not illustrated, the dummy gate stack **110** may further include a gate oxide layer (not shown). The gate oxide layer is interposed between the dummy gate stack **110** and the fin **108**. The gate oxide layer may be formed as a dummy gate oxide layer, with the intention of being replaced by a high-k gate oxide layer or metal gate layer as understood by one of ordinary skill in the art. In addition, gate spacers **116** are formed on sidewalls of each dummy gate stack **110**. In this manner, the gate spacers **116** are interposed between the dummy gate stacks **110** and the flowable insulator layer **112**. The gate spacers **116** are formed from, for example, silicon nitride (SiN).

[0022] The flowable insulator layer **112** is formed atop the buried insulator layer **104** and covers the source/drain (S/D) regions **118** of the semiconductor fins **108**. The flowable insulator layer **112** is formed, for example, of SiO_2. The flowable insulator layer **112** has a vertical thickness (e.g., height) ranging from approximately 50 nm to approximately 150 nm. Although not illustrated, it should be appreciated that an epitaxially grown semiconductor layer formed of Si, for example, may be grown from sidewalls and upper surfaces of the S/D regions **118** of the semiconductor fins **108** prior to forming the flowable insulator layer **112**. The epitaxially grown semiconductor layer is configured to merge the S/D regions **118** of each semiconductor fin **108** as understood by one of ordinary skill in the art.

[0023] Turning to FIGS. **2**A-**2**B, the semiconductor device **100** is illustrated following removal of the dummy gate stack **110**. Removal of the dummy gate stack **110** exposes the channel portion **114** of the semiconductor fins **108** and the underlying buried insulator layer **104**. The dummy gate stack **110** may be removed (i.e., pulled) using various etching processes such as, an ammonium hydroxide etching process, for example, which is implemented in well-known replacement metal gate fabrication processes. Since source/drain regions **118** are covered by the gate spacers **116** and flowable insulator layer **112**, no additional masking layers are necessary to remove the dummy gate stack **110**.

[0024] Referring now to FIGS. **3**A-**3**B, a condenser layer **120** is epitaxially deposited on sidewalls and an upper surface of the channel region **114**. According to an embodiment, the condenser layer **120** is formed using an epitaxial deposition process to ensure sufficient contact between the condenser and the surfaces of the fins **108**. The epitaxial growth process is selective to semiconductor materials such as, for example, silicon (Si). In this manner, the condenser layer **120** grows readily on the exposed semiconductor (e.g., Si) material of the channel region **114**, while avoiding growth on the exposed buried insulator layer **104**. According to a non-limiting embodiment, the condenser layer has a thickness ranging from approximately 1 nm to approximately 5 nm.

[0025] The condenser layer **120** may include a donor material (not shown in FIGS. **3**A-**3**B) which, when driven into the semiconductor material of fins **108**, increases carrier mobility through the channel regions **114** without increasing or substantially increasing the dimensions of the fins **108**. According to a non-limiting embodiment, the donor material includes germanium (Ge) whereby a SiGe condenser layer **120** is epitaxially grown on the sidewalls and upper surface of the channel region **114**. The concentration of Ge donor material included in the condenser layer **120** ranges, for example, from approximately 50 to approximately 90. Since source/drain regions **118** are covered by the gate spacers **116** and flowable insulator layer **112**, no additional masking layers are necessary to protect the source/drain regions **118** when epitaxially growing the condenser layer **120** on the channel regions **114** of the fins **108**.

[0026] Turning to FIGS. **4**A-**4**B, a condensation process is performed to drive or push donor material from the condenser layer **120** into the channel region **114** of the fins **108**. According to a non-limiting embodiment, the condensation process includes exposing the channel region **114** to ions capable of condensing the channel region **114** into a second semiconductor material different from the initial semiconductor layer of the fins (e.g., Si). For example, the exposed channel region **114** is exposed to oxygen (O_2) ions, for example, at a temperature of approximately 600 degrees Celsius for a time period of approximately 15 minutes. In this manner, the condenser layer **120** is oxidized and the released donor material **122** is driven into the channel region **114** so as to condense the channel region **114**, i.e., chemically transform the first semiconductor material into the second semiconductor material.

[0027] According to at least one embodiment, if the condenser layer **120** is formed of SiGe, and the fins **108** are formed of Si, then Ge donor material **122** is released from the condenser layer **120** and driven into the channel region

114 during the condensation process. As a result, the composition of the fins **108** is altered as the donor material **122** is diffused into the first semiconductor material (e.g., Si) of the exposed channel region **114**. In this manner the fin channel regions **114** are condensed, i.e., chemically transformed, into a condensed channel region **124** such as, for example, a SiGe channel region **124**. According to a non-limiting embodiment, the concentration of Ge contained in the condensed channel region **124** is greater than 50% of the Si contained in the condensed channel region. Condensing the channel regions of the fins may also induce a strain in the fins. In the case where the channel region **124** is formed of SiGe, for example, the condensation process may induce a compressive strain in the SiGe. The S/D regions **118** are not condensed and remain comprising their initial semiconductor material (e.g., Si) since they are covered by the flowable insulator layer **112**. In the case where the channel regions **124** are formed from SiGe, for example, maintaining the S/D regions **118** as Si achieves a bandgap offset between Si and SiGe, thereby increasing carrier velocity which increases current and overall device performance. Following the oxidation process, the condenser layer **120** in chemically transformed into an oxidized layer **126** as further illustrated in FIGS. **4**A-**4**B. If the condenser layer **120** is formed of SiGe, then the resulting oxidized layer **126** is formed, for example, of SiO_2.

[0028] Referring now to FIGS. **5**A-**5**B, the semiconductor device **100** is illustrated following removal of the oxidized layer (previously identified as numeral **126**) from the surfaces of the condensed channel region **124**. According to a non-limiting embodiment, a reactive ion etching (RIE) process selective to the gate spacer material (e.g., SiN) and the condensed fin material (SiGe) is performed to selectively remove the oxidized layer. The flowable insulator layer **112** is formed with a thickness so as to serve as a buffer when removing the oxidized layer. Accordingly, a portion of the flowable insulator layer **112** is permitted to be etched while still adequately protecting the S/D regions **118**. According to a non-limiting embodiment, the thickness of oxidized layer **126** is limited to around 10 nm, for example. In this manner, S/D channel shorting between the buried insulator layer **104** and the S/D regions **118** may be prevented even if a portion of the buried insulator layer **104** is recessed when etching away the oxidized layers **126** from the fins **108**.

[0029] Turning now to FIGS. **6**A-**6**B, the semiconductor device **100** is illustrated after depositing a metal gate structure **128** between the gate spacers **116** and atop the buried insulator layer **104**. The metal gate structure **128** wraps around the sidewalls and the upper surface of the condensed channel region **124** so as to serve as a gate electrode as understood by one of ordinary skill in the art. The metal gate structure **128** can be formed of various metal gate materials including, but not limited to, tungsten (W).

[0030] Although not illustrated, it should be appreciated that the metal gate structure **128** may include one or more work function metal layers including, but not limited to, a titanium nitride (TiN) liner and a tantalum nitride (TaN) liner, formed on sidewalls of the metal gate structure **128** as understood by one of ordinary skill in the art. As mentioned earlier, a gate dielectric layer (e.g., a high-k gate dielectric layer) may be disposed atop the buried insulator layer **104**. In this case, it should be appreciated that the metal gate structure **128** includes the metal gate material, the gate dielectric layer, and the work function metals. It should also be appreciated that a chemical-mechanical planarization (CMP) process may be performed after depositing the metal gate structure **128**. In this manner, the upper surface of the metal gate structure **128** is formed flush with the upper surface of the gate sidewalls **106** as further illustrated in FIGS. **6**A-**6**B.

[0031] Accordingly, at least one embodiment described above provides a finFET device including one or more semiconductor fins having a SiGe condensed channel region. In this manner, hole mobility through the channel region of the fins is improved compared to conventional finFET devices. For example, the hole mobility through the channel region may be approximately 3 times higher compared to conventional semiconductor fins having channel regions formed solely of silicon, e.g., Si<100> or Si<110>. In this manner, a finFET device according to at least one embodiment of the invention provides a finFET device having improved overall device performance compared to conventional finFET devices.

[0032] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

[0033] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one more other features, integers, steps, operations, element components, and/or groups thereof.

[0034] The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The embodiment was chosen and described in order to best explain the principles of the inventive teachings and the practical application, and to enable others of ordinary skill in the art to understand the invention for various embodiments with various modifications as are suited to the particular use contemplated.

[0035] The flow diagrams depicted herein are just one example. There may be many variations to this diagram or the operations described therein without departing from the spirit of the invention. For instance, the operations may be performed in a differing order or operations may be added, deleted or modified. All of these variations are considered a part of the claimed invention.

[0036] While various embodiments have been described, it will be understood that those skilled in the art, both now and in the future, may make various modifications which fall within the scope of the claims which follow. These claims should be construed to maintain the proper protection for the invention first described.

1.-**12**. (canceled)

13. A finFET semiconductor device, comprising:

at least one semiconductor fin on an upper surface of a substrate, the at least one semiconductor fin including a channel region interposed between opposing source/drain regions being integral with the at least one semiconductor fins so as to directly contact the source/drain regions; and

a gate stack on the upper surface of the substrate and wrapping around sidewalls and an upper surface of only the channel region;

gate spacers formed on sidewalls of the gate stack,

wherein the channel region includes a condensed portion comprising a first semiconductor material and a second semiconductor material, and the source/drain regions comprise the first semiconductor material while excluding the second semiconductor material, the condensed portion directly contacting the gate spacers.

14. The finFET semiconductor device of claim **13**, wherein the first semiconductor material is silicon (Si).

15. The finFET semiconductor device of claim **14**, wherein the second semiconductor material is germanium (Ge).

16. The finFET semiconductor device of claim **15**, wherein a concentration of Ge contained in the condensed channel portion ranges from approximately 50 to approximately 90.

17. The finFET semiconductor device of claim **15**, further comprising gate spacers formed on sidewalls of the gate stack.

18. The finFET semiconductor device of claim **13**, wherein the condensed portion does not extend beyond the gate spacers.

19. The finFET semiconductor device of claim **18**, wherein the gate spacers comprise silicon nitride (SiN).

20. The finFET semiconductor device of claim **19**, wherein the gate stack comprises a metal material.

21. The finFET semiconductor device of claim **13**, wherein a single junction is between the channel region and a first source/drain region among the opposing source/drain regions, and a single junction is between the channel region and a second source/drain region among the opposing source/drain regions.

* * * * *