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(54) LOW VOLTAGE HIGH DENSITY TRENCH-GATED POWER DEVICE WITH UNIFORMLY DOPED CHANNEL AND ITS EDGE TERMINATION TECHNIQUE

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Publication Classification

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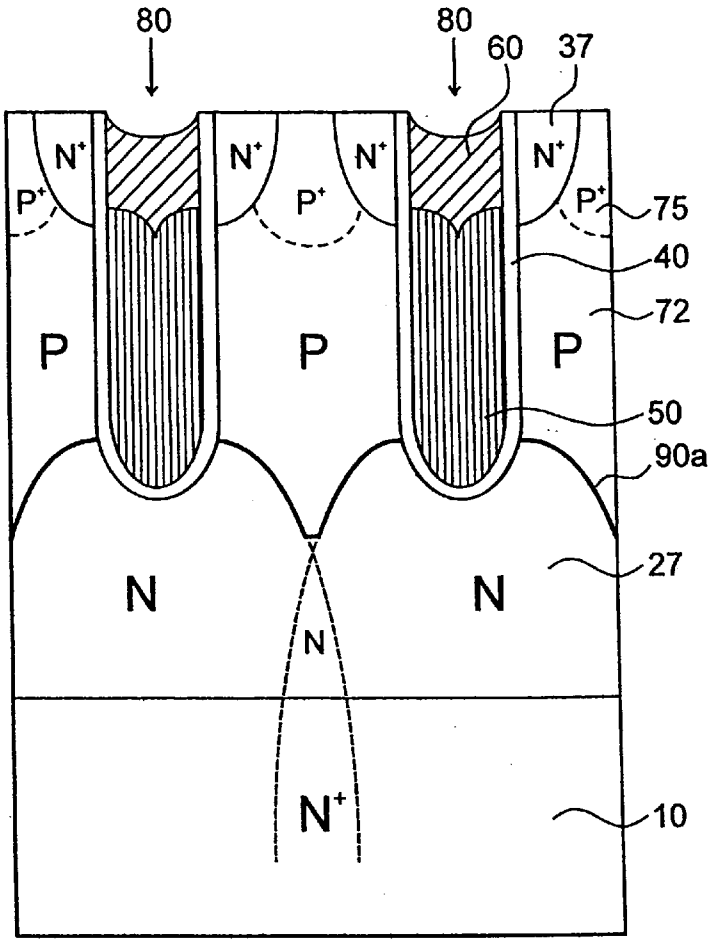
(52) **U.S. Cl.** **438/268**

(57) **ABSTRACT**

Merging together the drift regions in a low-power trench MOSFET device via a dopant implant through the bottom of the trench permits use of a very small cell pitch, resulting in a very high channel density and a uniformly doped channel and a consequent significant reduction in the channel resistance. By properly choosing the implant dose and the annealing parameters of the drift region, the channel length of the device can be closely controlled, and the channel doping may be made highly uniform. In comparison with a conventional device, the threshold voltage is reduced, the channel resistance is lowered, and the drift region on-resistance is also lowered. Implementing the merged drift regions requires incorporation of a new edge termination design, so that the PN junction formed by the P epi-layer and the N^+ substrate can be terminated at the edge of the die.



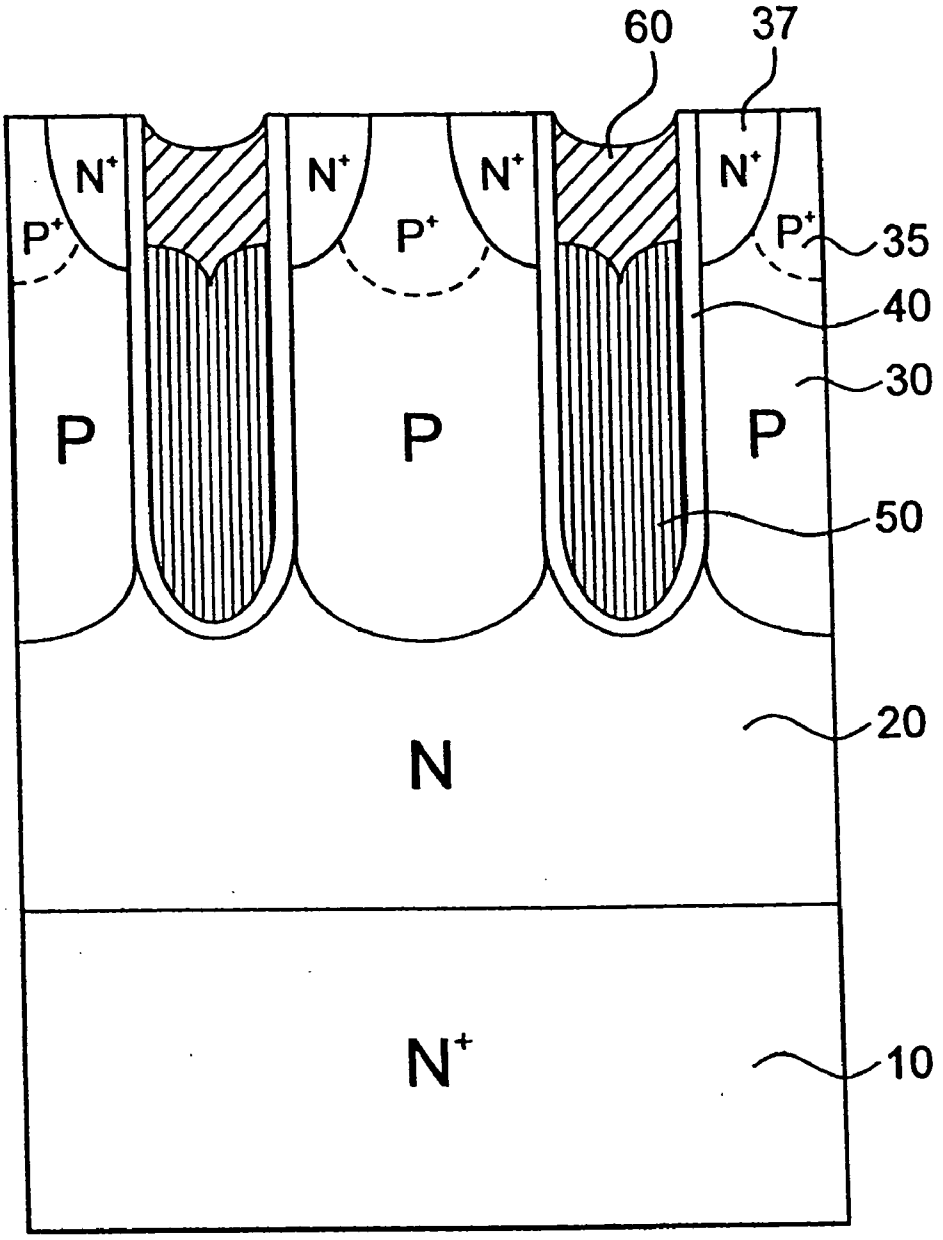


Fig. 1

(PRIOR ART)

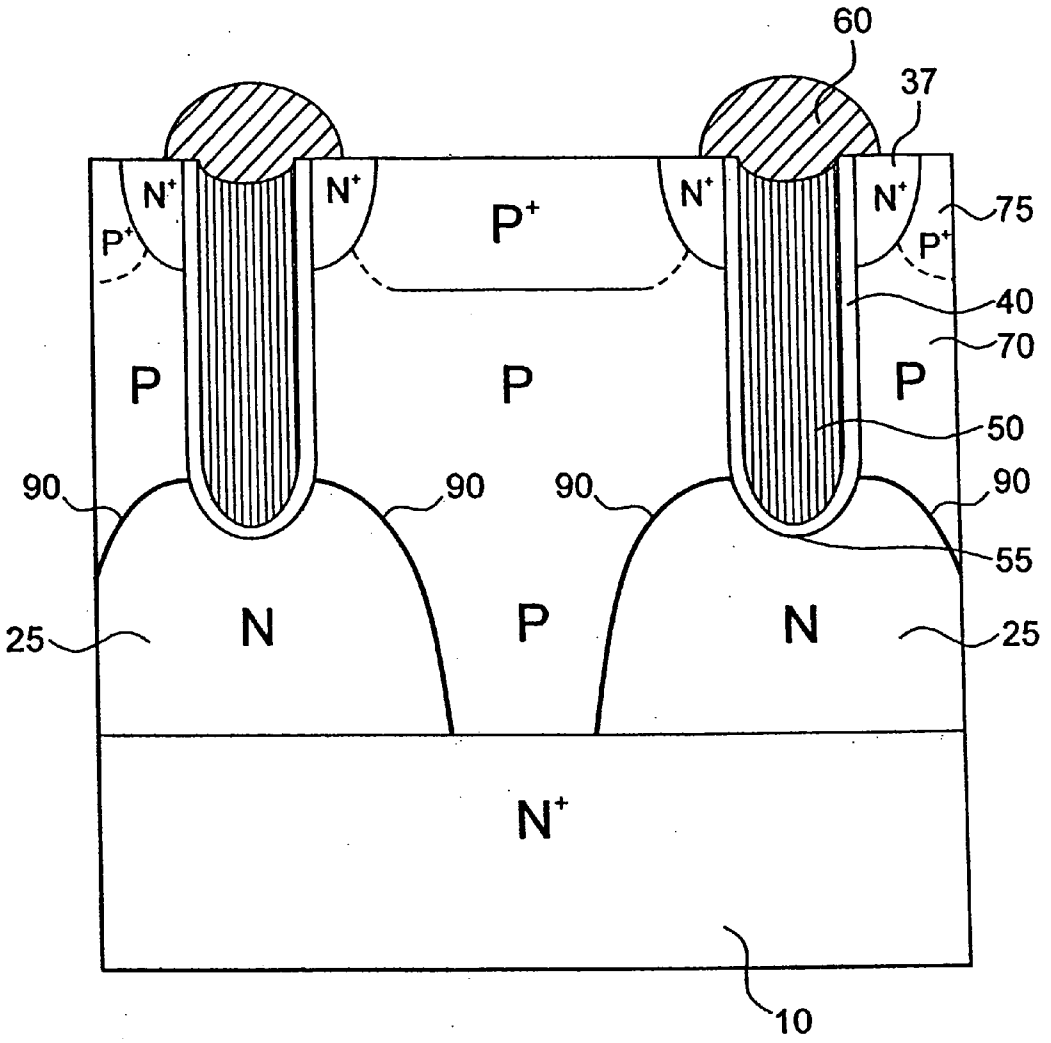


Fig. 2

(PRIOR ART)

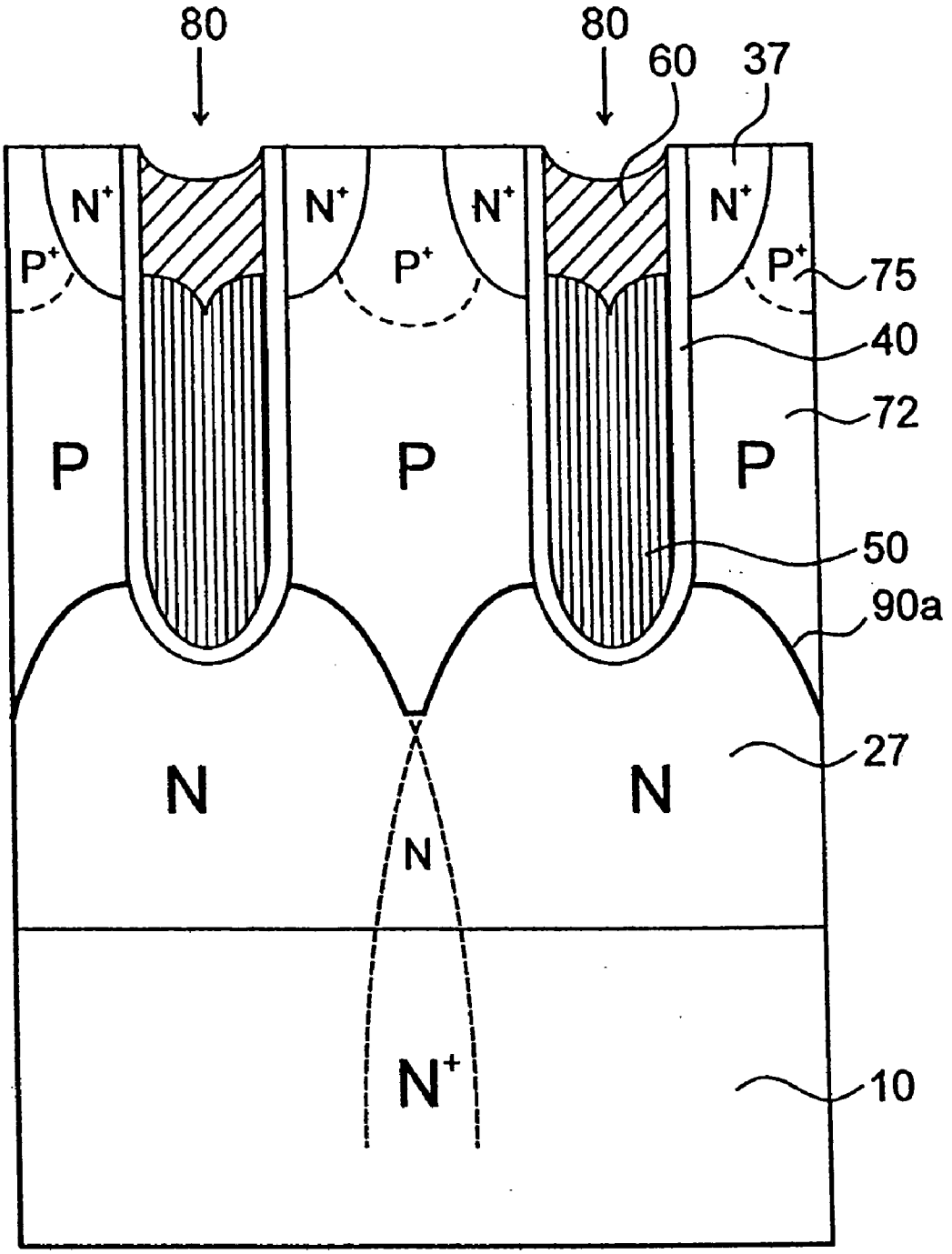


Fig. 3

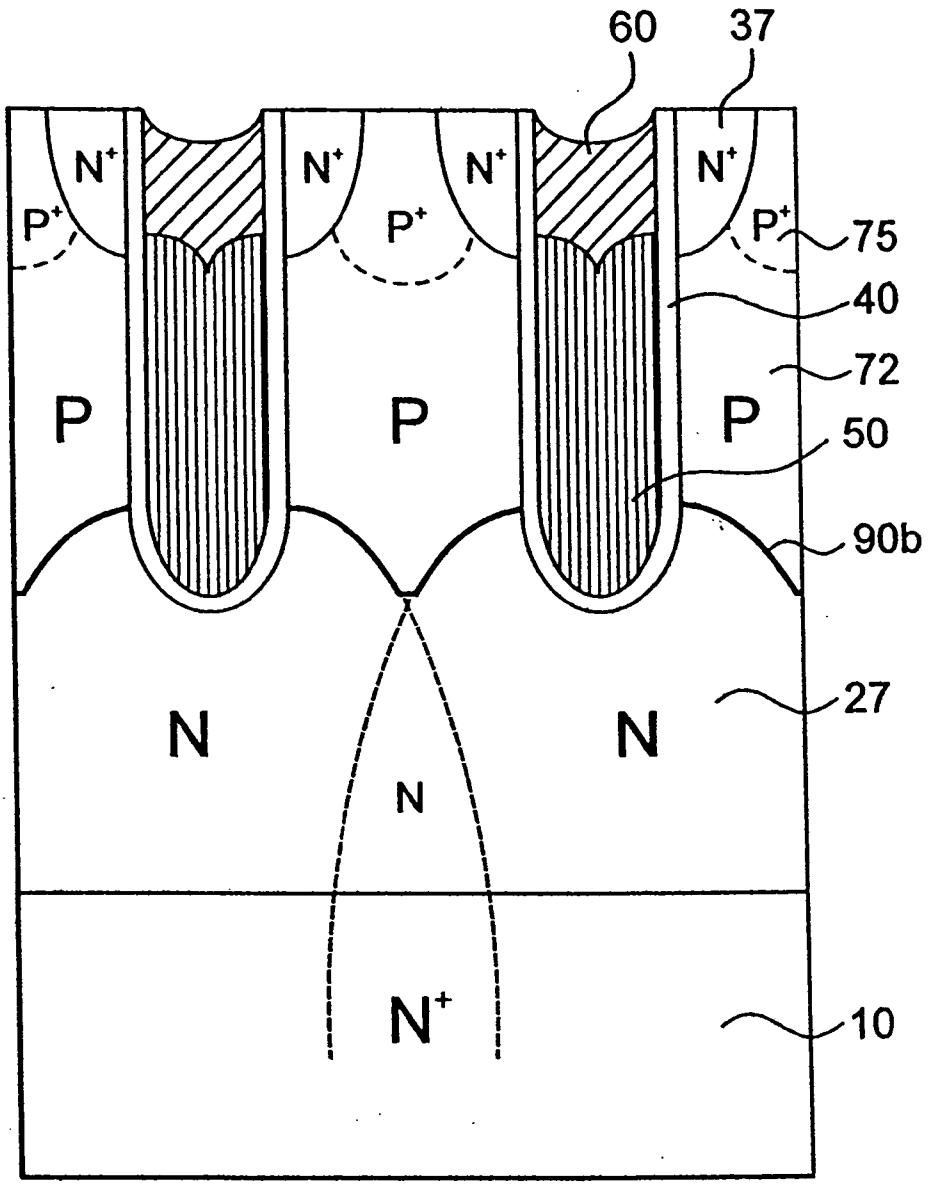


Fig. 4

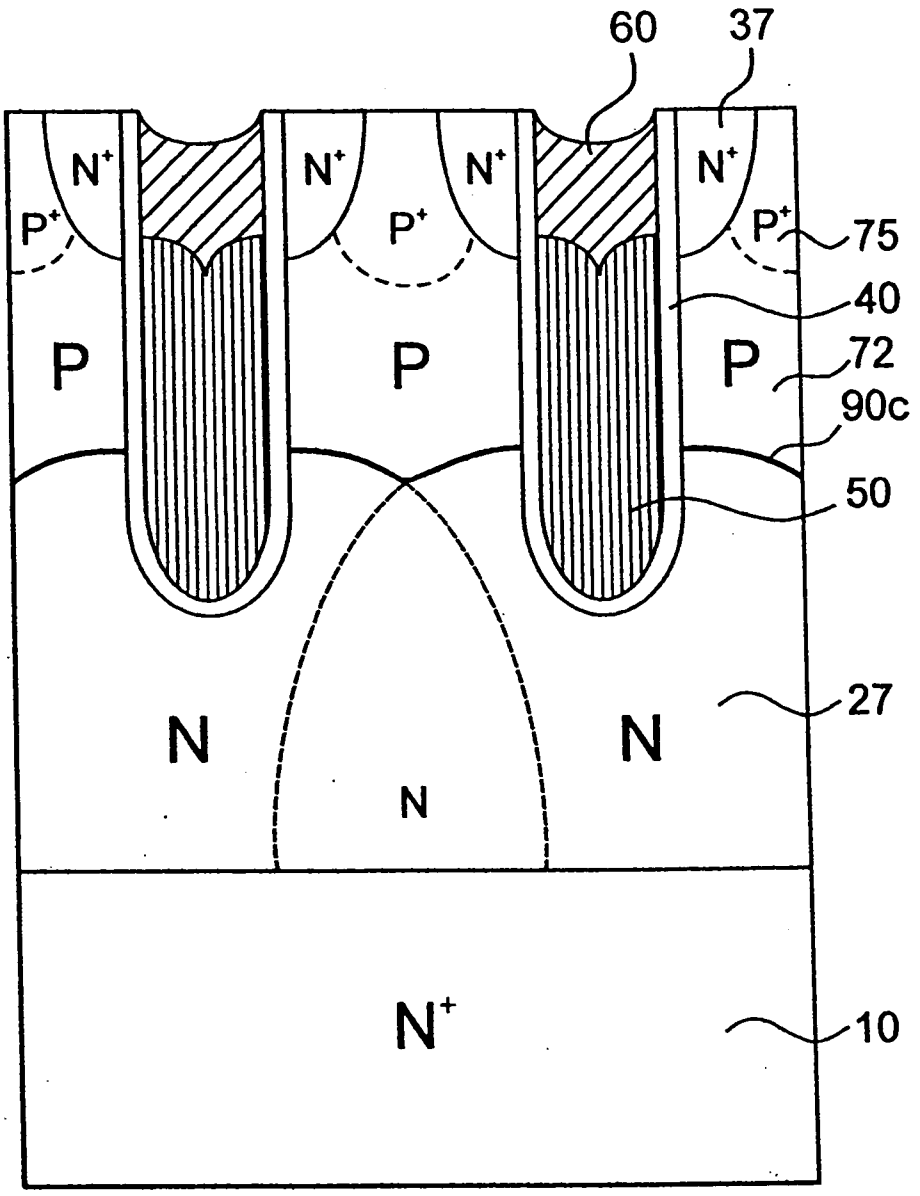


Fig. 5

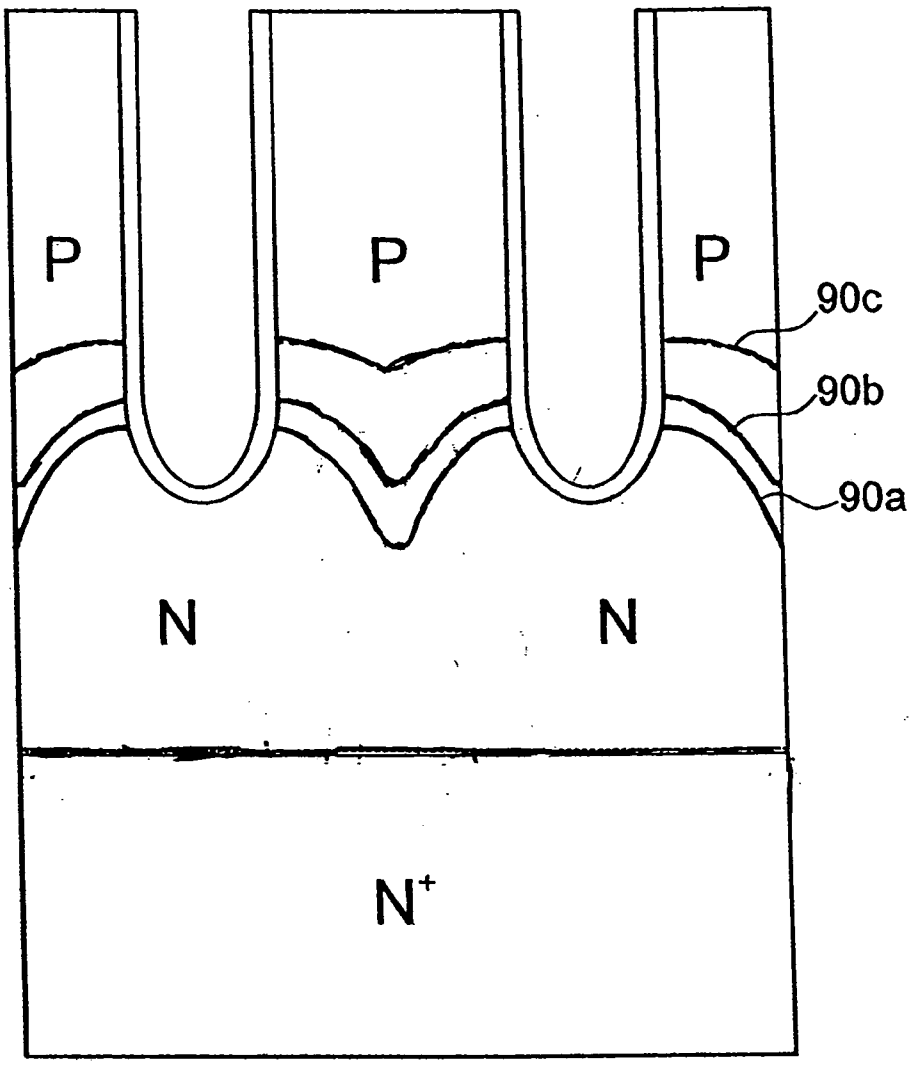


Fig. 5a

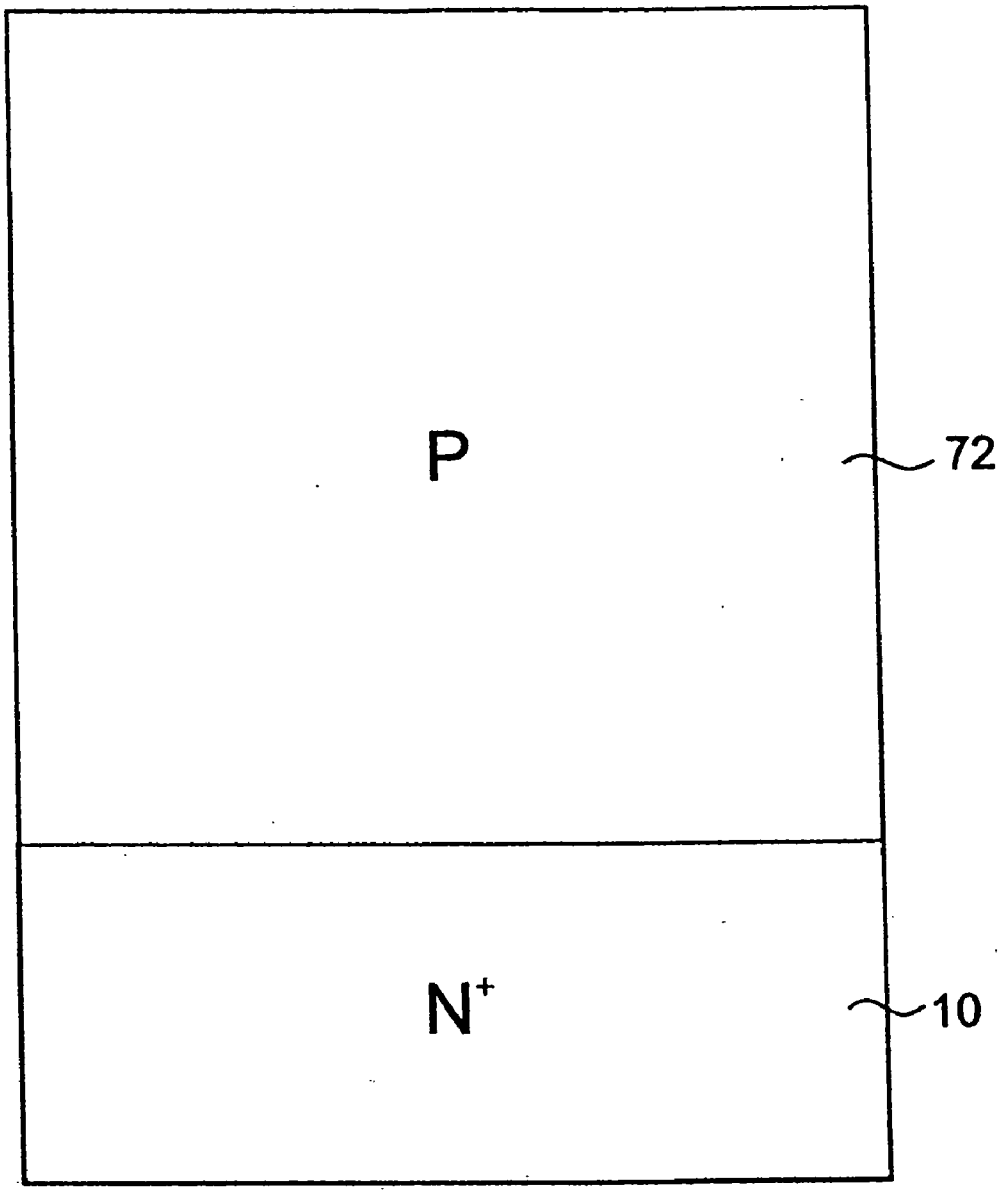


Fig. 6

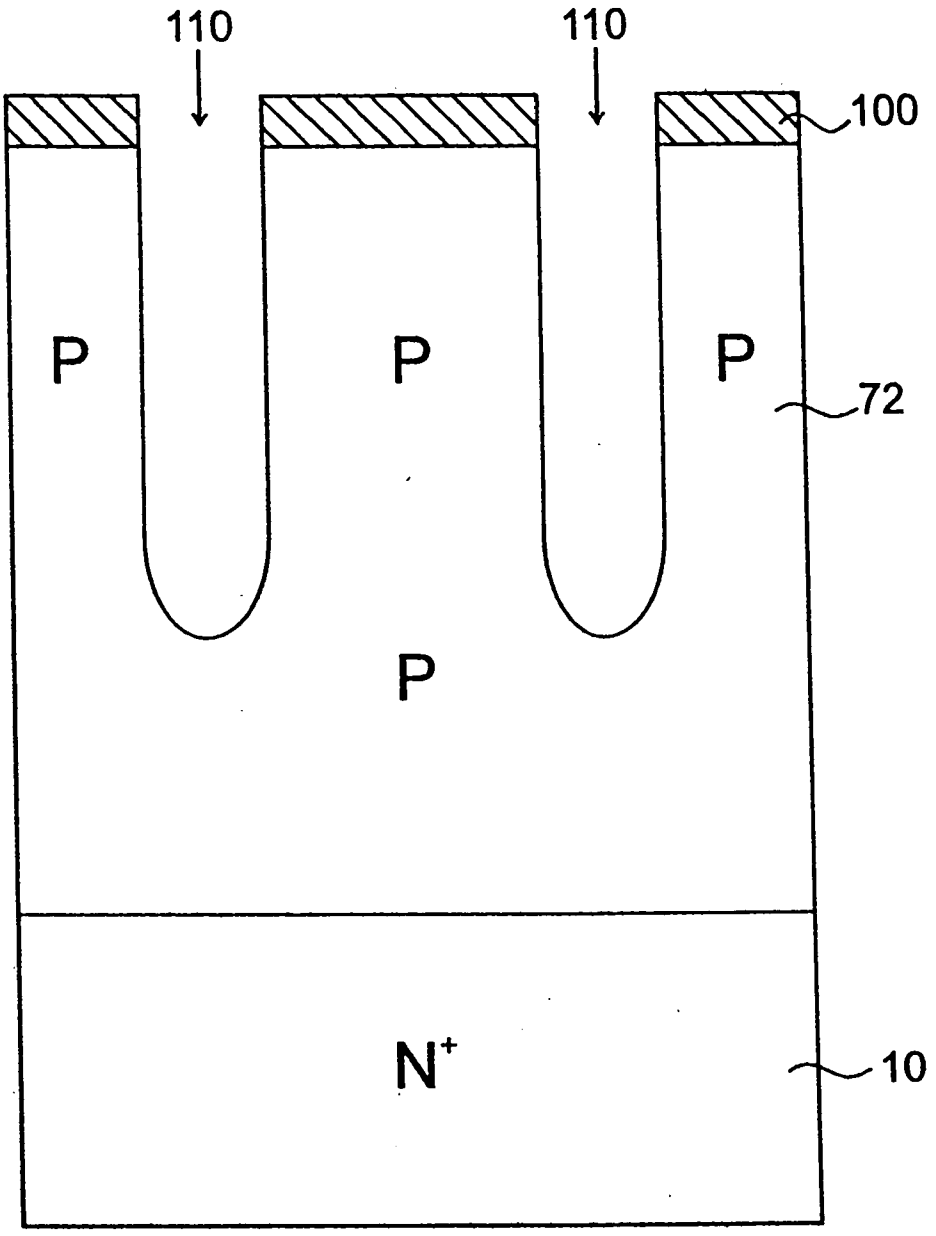


Fig. 7

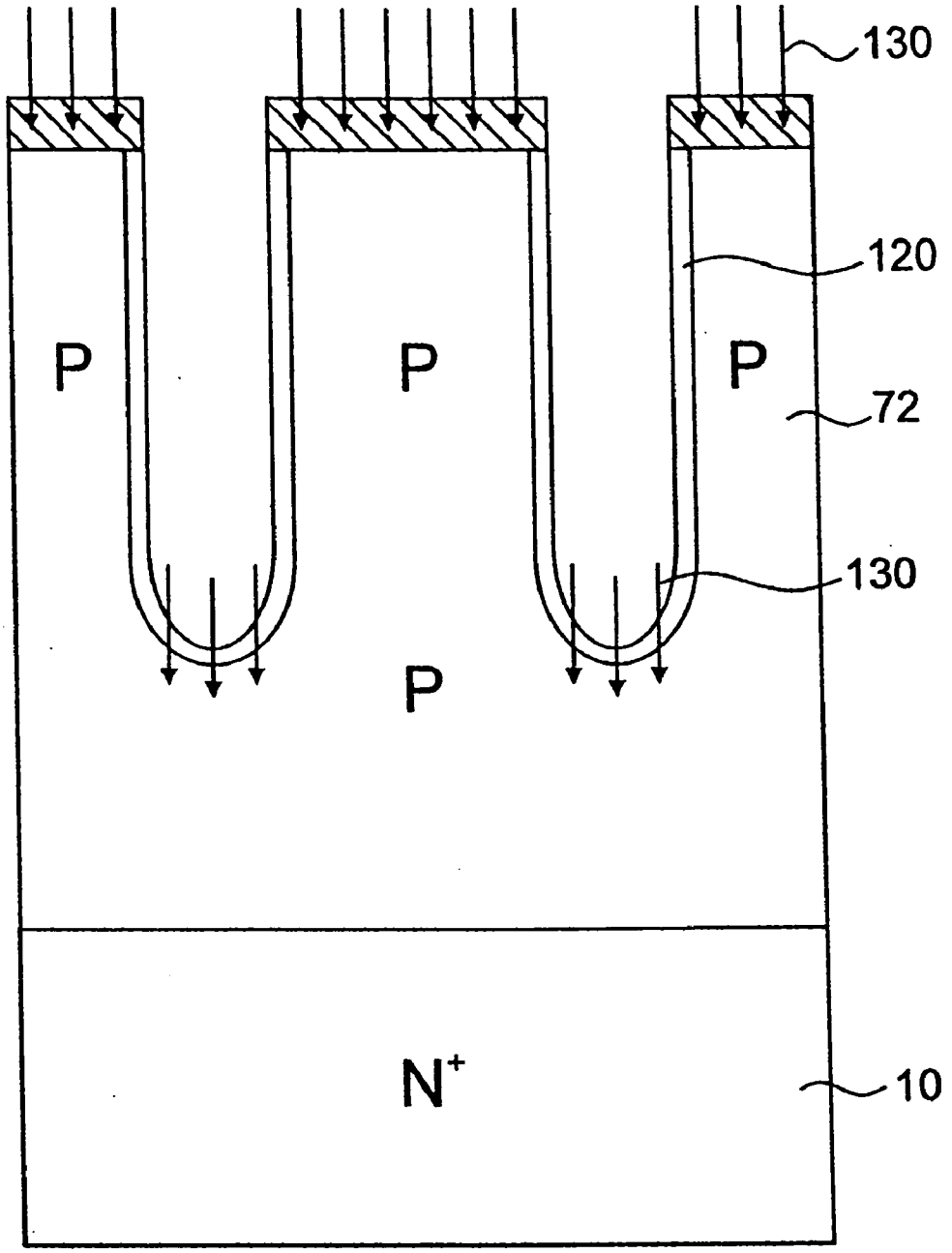


Fig. 8

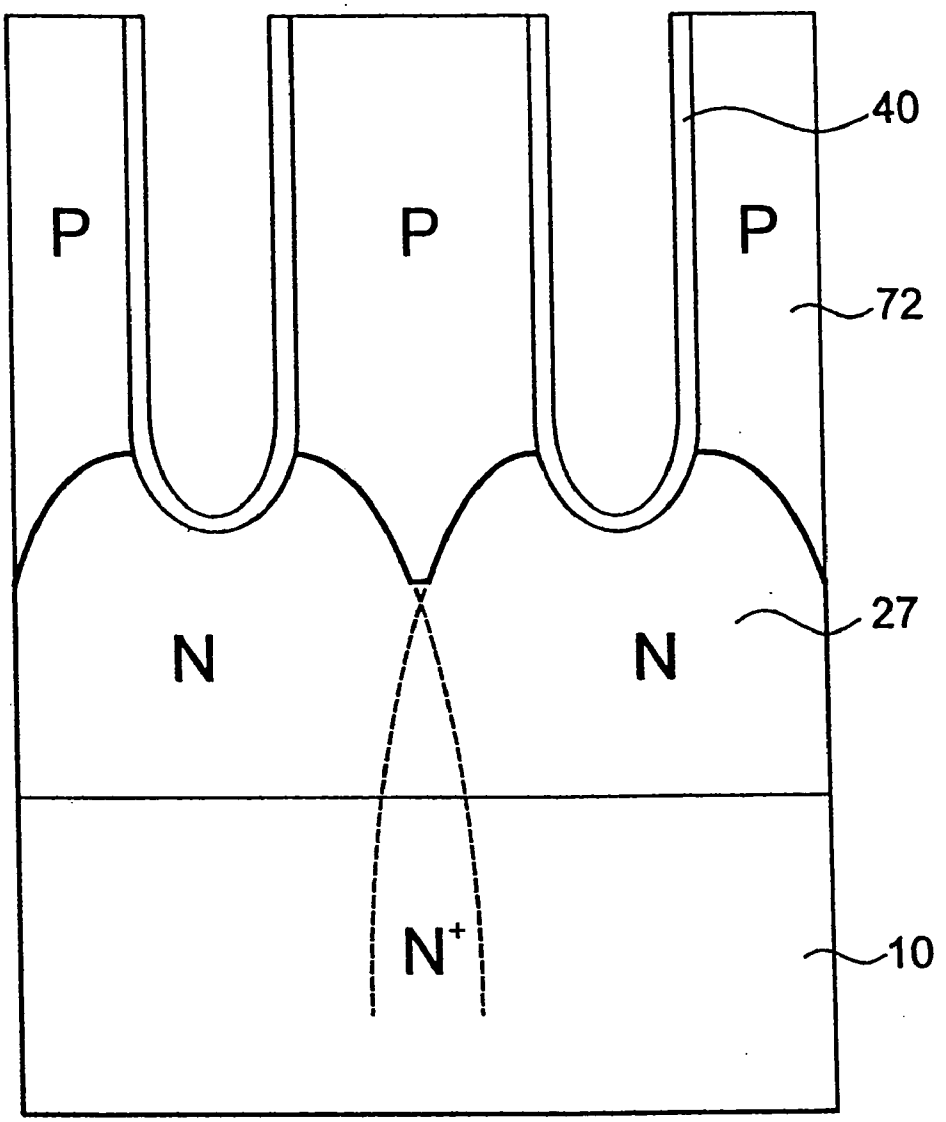


Fig. 9

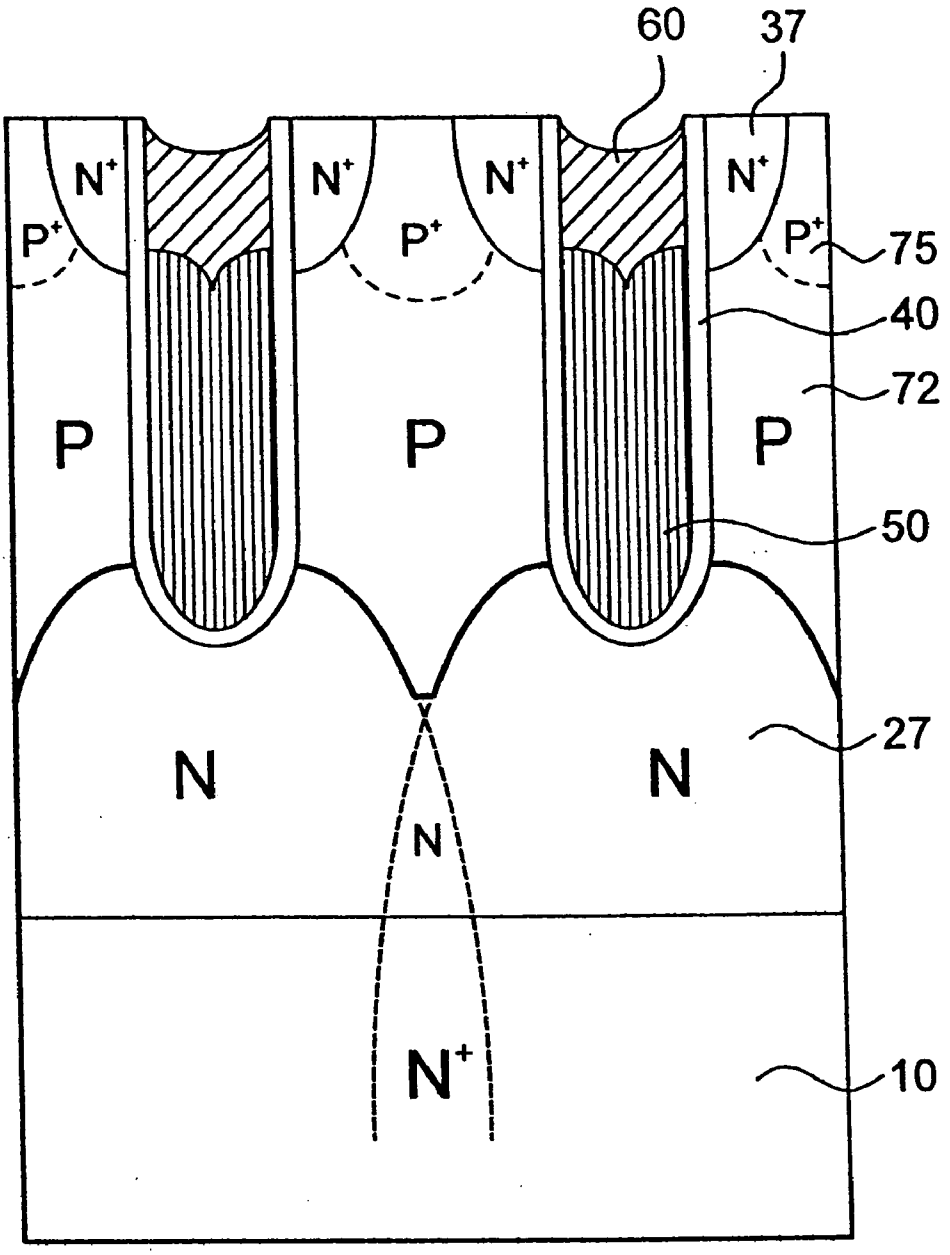


Fig. 10

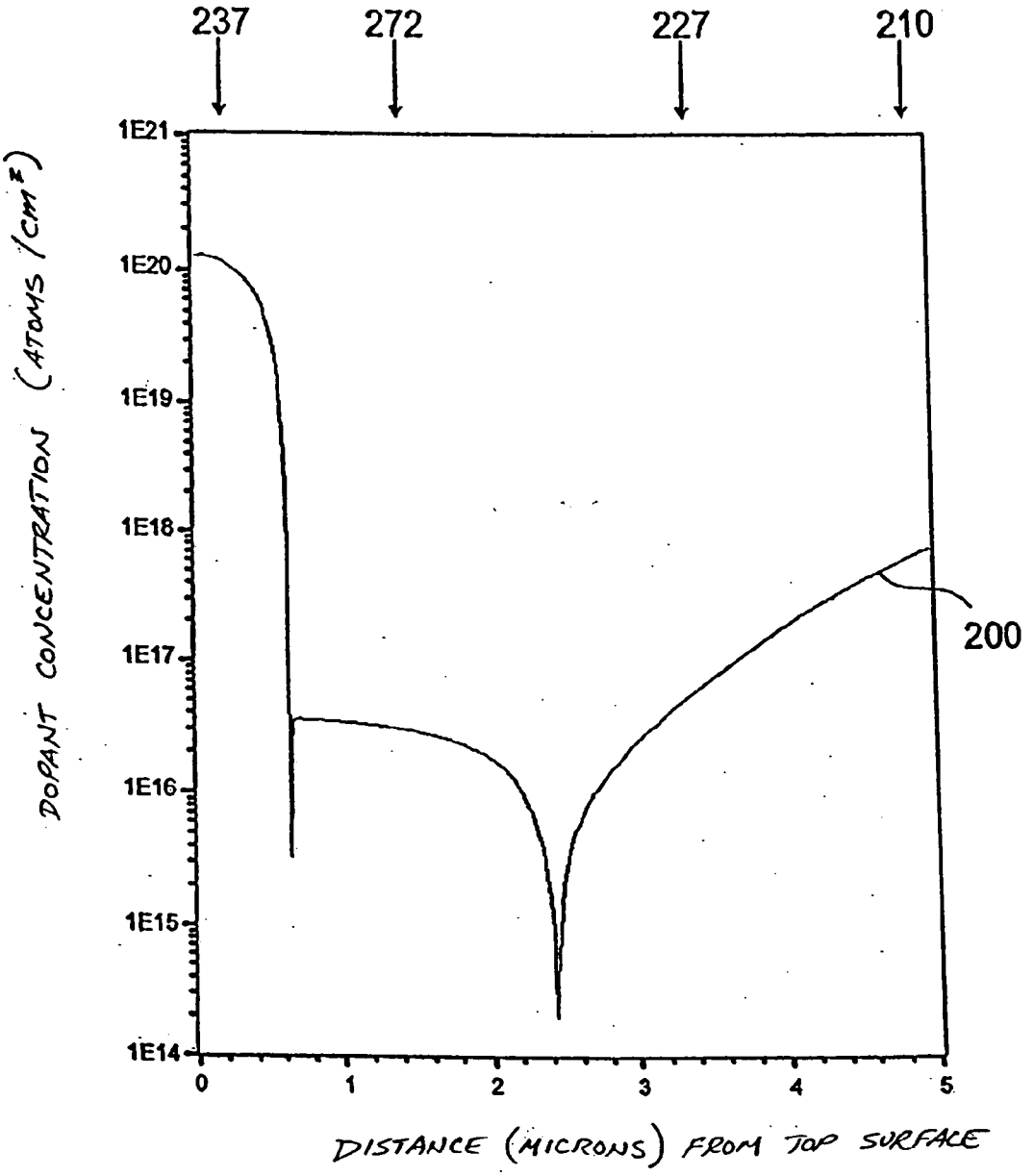

237
272
227
210
1E21
1E20
1E19
1E18
1E17
1E16
1E15
1E14
0
1
2
3
4
5
200
DOPANT CONCENTRATION (ATOMS/CM³)
DISTANCE (MICRONS) FROM TOP SURFACE

Fig. 11

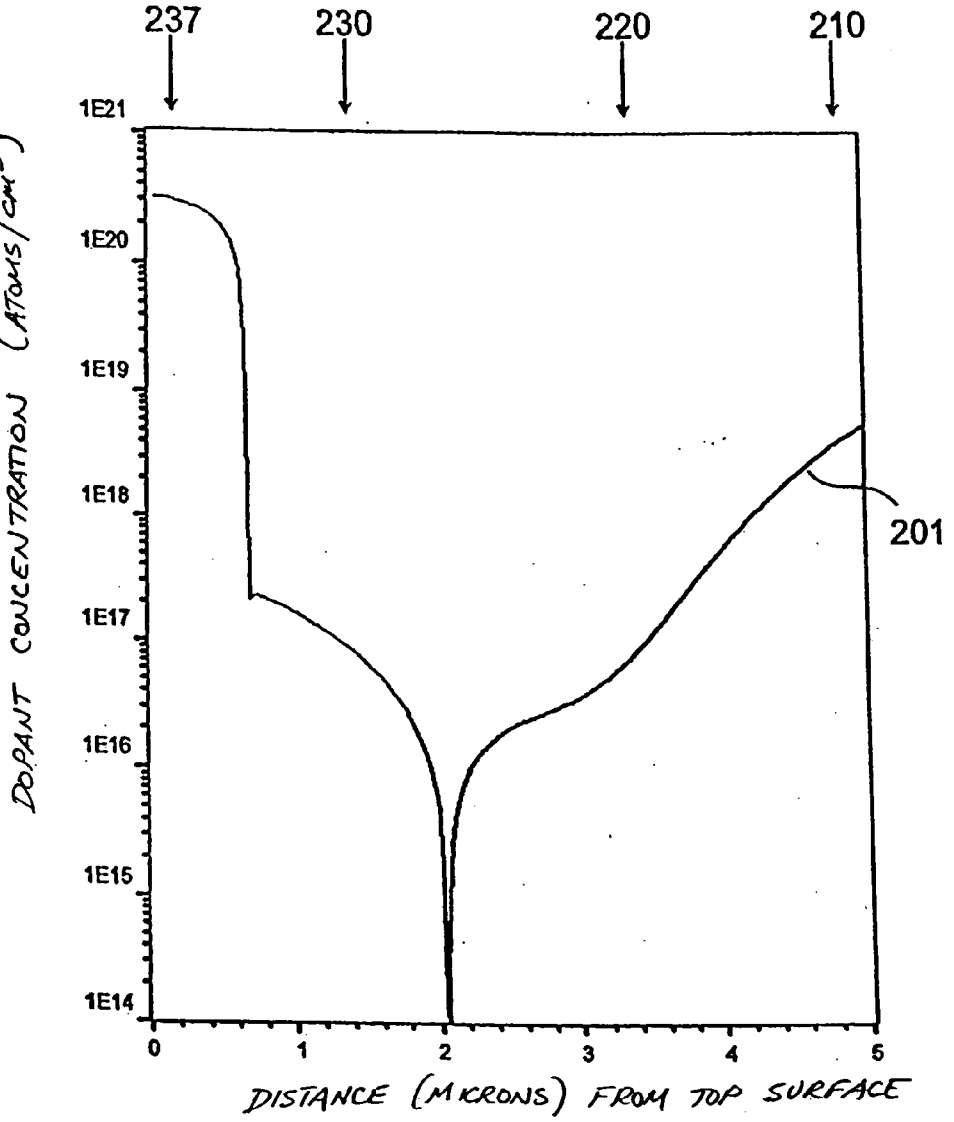


Fig. 12

(PRIOR ART)

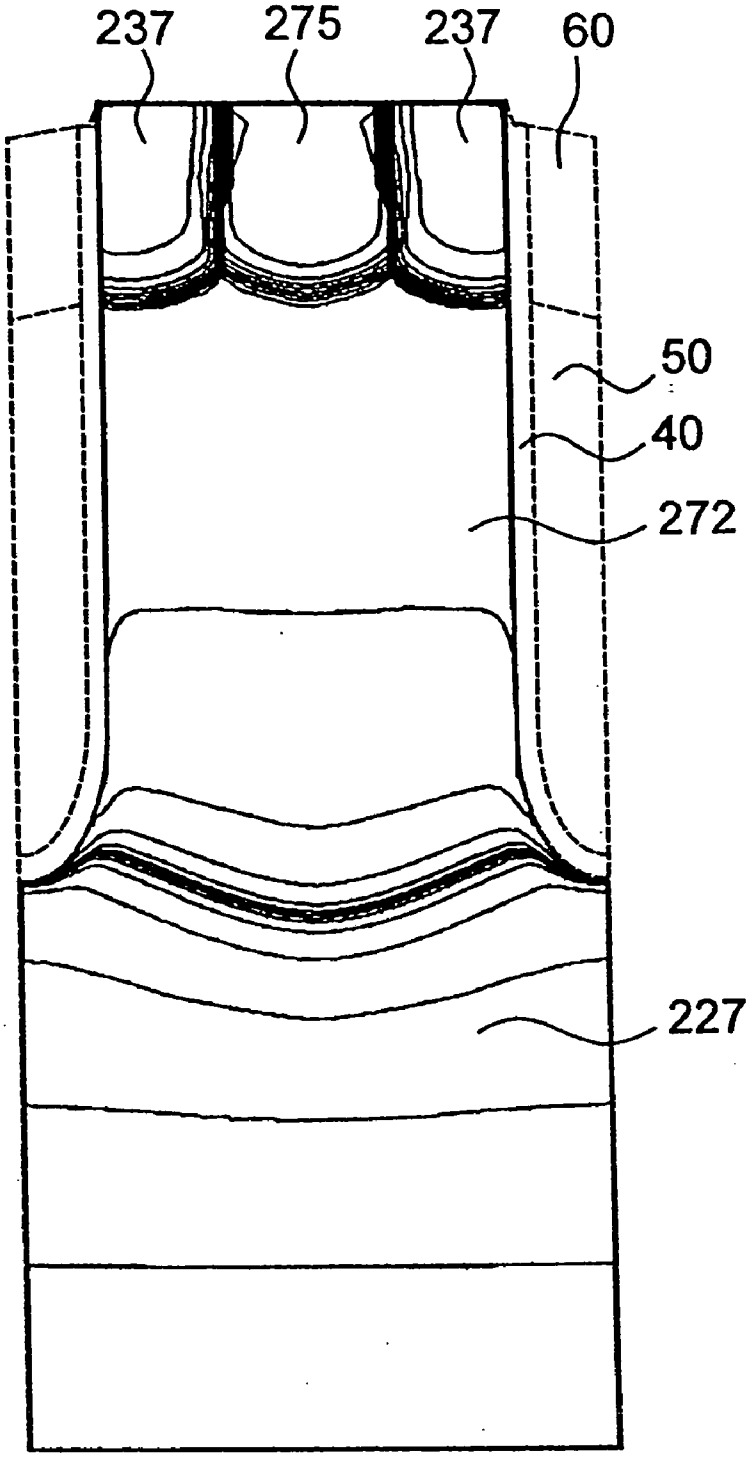


Fig. 13

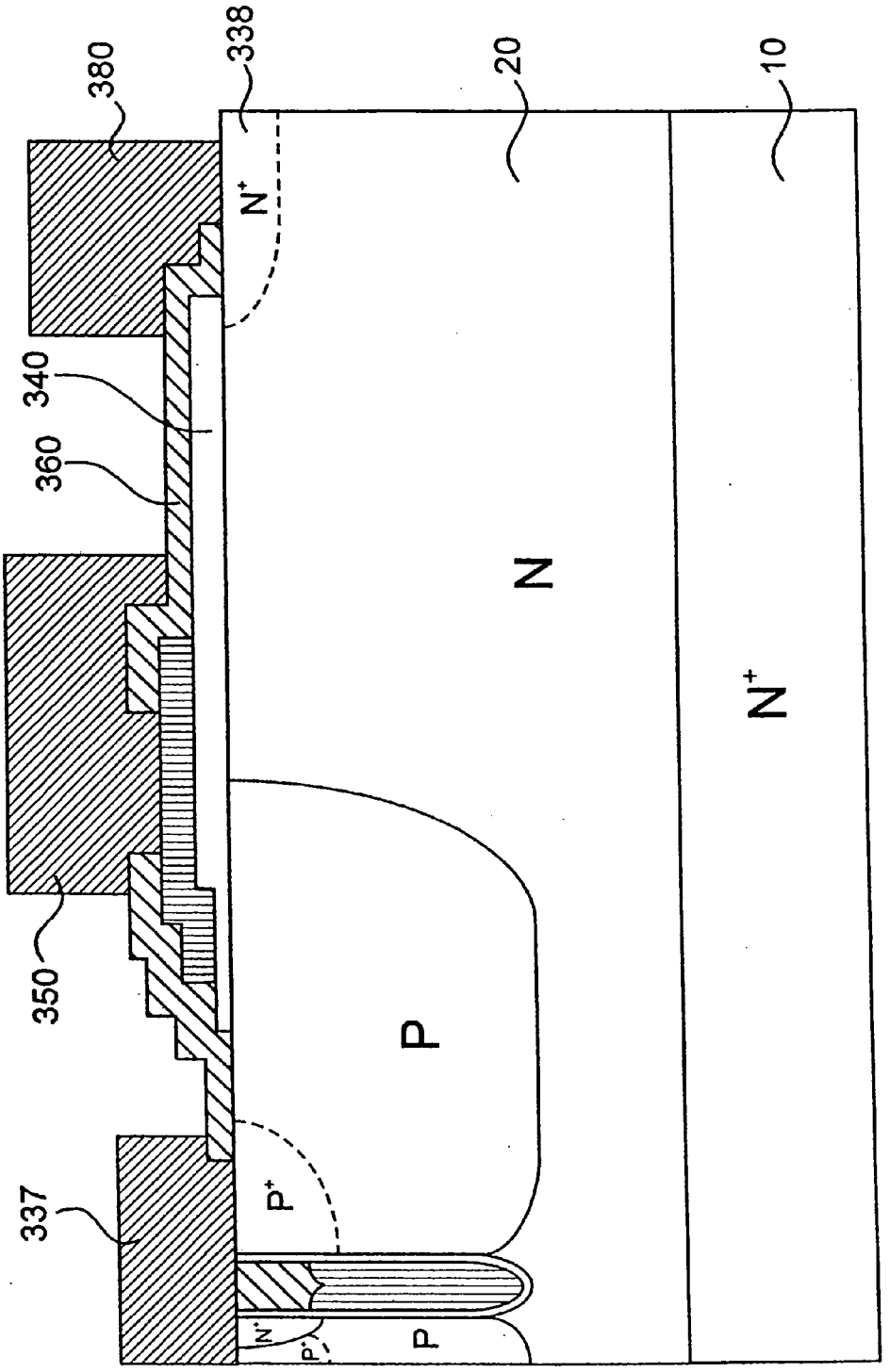


Fig. 14 (PRIOR ART)

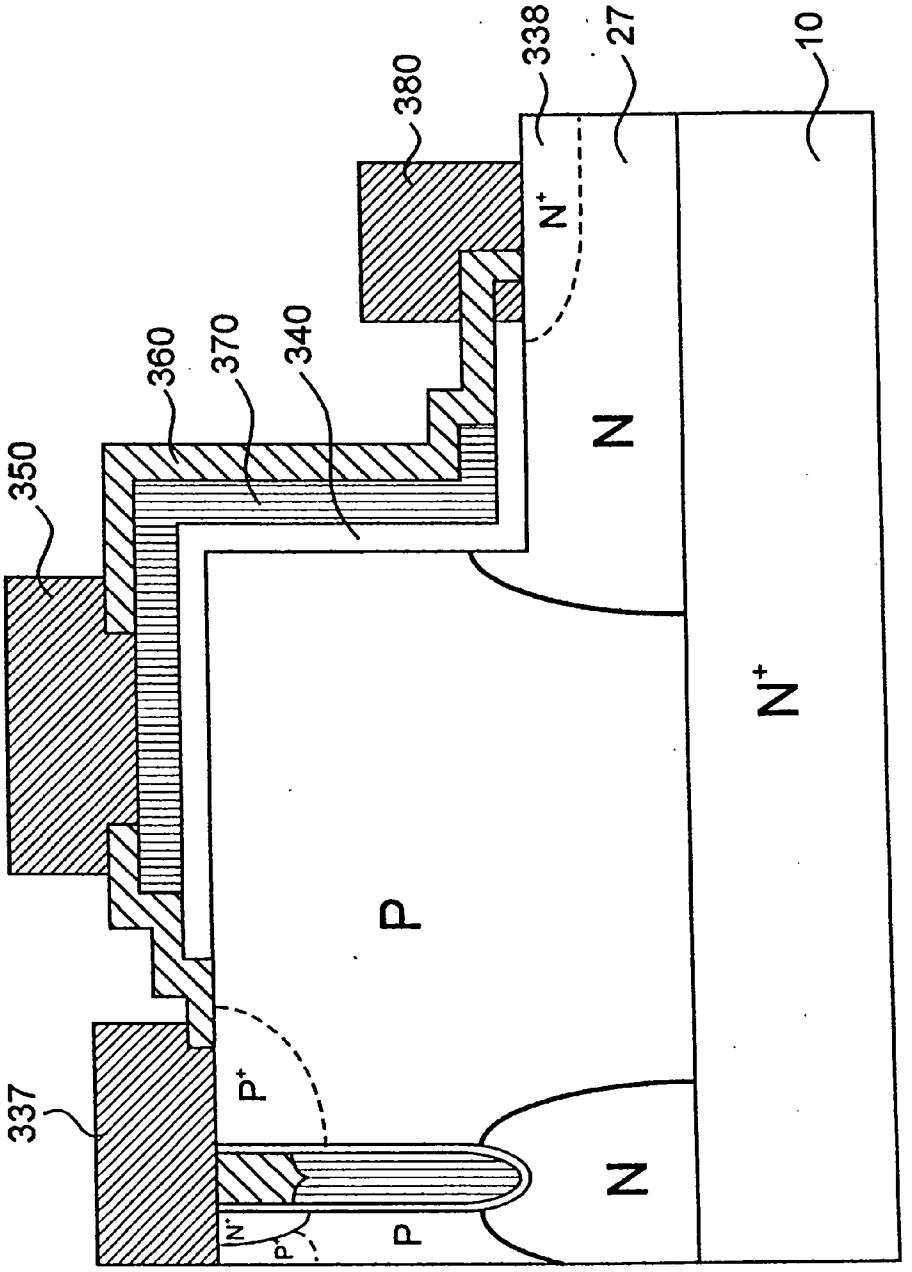


Fig. 15

LOW VOLTAGE HIGH DENSITY TRENCH-GATED POWER DEVICE WITH UNIFORMLY DOPED CHANNEL AND ITS EDGE TERMINATION TECHNIQUE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This is a continuation of U.S. patent application Ser. No. 10/795,723 filed Mar. 5, 2004 which is a divisional application of U.S. patent application Ser. No. 10/138,913 filed May 3, 2005.

FIELD OF INVENTION

[0002] This invention relates to semiconductor power devices and their fabrication, and more specifically to low-voltage vertical MOSFET power devices.

DISCUSSION OF PRIOR ART

[0003] Recently, the personal portable electronics field, including such devices as cellular phones and notebook computers, has experienced explosive growth. The systematic reduction of supply voltage, accompanied by a corresponding decrease in device feature size and high system performance, has become a primary focus for the development of more advanced power devices. The voltage scaling of the total system requires that the power MOSFETs used in power management circuitry can be efficiently turned on and off at a low gate drive voltage. In order to meet this requirement, the power semiconductor switches should have a low level threshold voltage (less than 1.0 volts). See **FIG. 1**. To lower the threshold voltage, the prior art uses a low implant dose in P-well **30** plus a thinner gate oxide **40**. This approach achieves a low gate rating, but it may result in a high channel leakage current and a poor high-temperature performance. Due to the low total net charges of the well, this approach also makes the device susceptible to punch-through breakdown. In addition, the doping in the channel is non-uniform.

[0004] Another recently-disclosed prior-art technique (shown in **FIG. 2**) employs the P-type epi-layer **70** forming the channel region of the device. The drift region **25** of the device is formed by implanting the opposite-type dopant into the trench bottom **55**, followed by a thermal annealing step. Consequently, the doping concentration of the channel region is determined by the doping concentration of the epi-layer **70**, and the doping profile along the device channel is uniform. This yields a higher total net charge located in the well for a given threshold voltage. Thus, the device's performance and off-state breakdown characteristics are expected to be improved. In this prior art, adjacent drift regions **25** clearly are not allowed to merge. The regions are kept separated to provide so-called "bulk resurf", so that the on-resistance of the device drift region **25** can be dramatically reduced [1]-[3].

[0005] As is well-known in the art, for low voltage power devices (for example, 30 volts or less) the on-resistance contribution from the drift region **25** is a very small portion of the total on-resistance. The most significant component of the device on-resistance is the resistance of the device channel region. In order to lower the channel resistance, the most efficient approach is to reduce the device unit cell pitch and increase the channel density. Unfortunately, the non-merging condition imposed on the drift regions **25** as taught in the prior art limits the minimum cell pitch and maximum channel density that the device can employ. As the result, the on-resistance of the prior art is high when used for a low voltage application. In addition, it is clear from **FIG. 2** that the prior art creates more PN junction area of the device's body-diode, resulting in a high output capacitance. Also, the parasitic BJT of the body-diode has a significantly non-uniform base width. This will degrade the body-diode forward conduction and reverse recovery characteristics. [4]

SUMMARY

[0006] The invention merges together the drift regions in a low-power trench MOSFET device via a dopant implant through the bottom of the trench. The merged drift regions permit use of a very small cell pitch, resulting in a very high channel density and a consequent significant reduction in the channel resistance. By properly choosing the implant dose and the annealing parameters of the drift region, the channel length of the device can be closely controlled, and the channel doping may be made highly uniform. In comparison with a conventional device, the invention's threshold voltage is reduced, its channel resistance is lowered, and its drift region on-resistance is also lowered. To implement the merged drift regions, the invention incorporates a new edge termination design, so that the PN junction formed by the P epi-layer and the N^+ substrate can be terminated at the edge of the die.

[0007] When compared to the prior art devices of **FIG. 1**, the more heavily P-type epitaxial layer of **FIG. 2** reduces on resistance. In addition, the separated drift regions of **FIG. 2** provide depletion regions to sustain a higher reverse voltage across the device. However, the requirement of the separated drift regions inherently reduces the density of the cells in a device. The invention provides low on resistance by using a more highly doped P-type epitaxial layer and has a higher cell density by allowing the drift regions to merge. Even with merged drift regions there is still adequate depletion to support high reverse biases. With the invention, the P-doping in the channel is more constant than the doping in prior art channels with epitaxial layers and separated drift zones. The invention provides devices with greater cell density and lower junction capacitance than devices made with separated resurf regions.

DESCRIPTION OF DRAWINGS

[0008] **FIG. 1** shows a typical prior art device using a low implant dose and a thinner gate oxide.

[0009] **FIG. 2** shows a typical prior art device using an epi-layer forming the channel region of the device.

[0010] **FIG. 3** shows the invention in a first embodiment with significant reduction of channel resistance.

[0011] **FIG. 4** shows the invention in a second embodiment with further significant reduction of channel resistance.

[0012] **FIG. 5** shows the invention in a third embodiment with still further significant reduction of channel resistance.

[0013] **FIG. 5*a*** shows a comparison of the three embodiments shown in **FIGS. 3, 4**, and **5**.

[0014] **FIGS. 6 through 10** show the important steps in fabrication of the invention.

[0015] **FIG. 11** shows the invention's doping profile along the trench sidewall.

[0016] **FIG. 12** shows the doping profile along the trench sidewall for a prior art device.

[0017] **FIG. 13** shows the contours of doping concentration in the invention.

[0018] **FIG. 14** shows the most commonly used edge termination in prior art devices.

[0019] **FIG. 15** shows the edge termination used in the invention.

DETAILED DESCRIPTION OF INVENTION

[0020] This invention addresses and resolves the problems of the prior art devices described above. See **FIG. 3**. The invention's device comprises an N^+-type substrate **10**, N-type drift regions **27**, a P-type epi-layer **72**, trenches **80**, gate oxide **40**, polysilicon **50**, BPSG **60**, N^+-type source regions **37**, and P^+-type body regions **75**. The illustrated conductivity types may of course be reversed as needed. By contrast with the prior art, the invention merges together the implanted drift regions **27**. The prior art of **FIG. 2** keeps the regions separated to provide a bulk resurf effect that lowers the on resistance and increases the depletion of the drift region during reverse votage conditions to raise the limits of the sustaining reverse voltage. Instead of the long, slanted boundary **90** between P-type epi-layer **70** and drift region **25** as shown in **FIG. 2**, the invention produces a shorter, more-level boundary **90***a* between P-type epi-layer **72** and drift region **27** as shown in **FIG. 3**. In effect, the invention reduces significantly the surface area between the epi-layer and the drift region, and separates the epi-layer completely from the substrate. Merging the drift regions permits use of a very small cell pitch and results in a very high channel density. Thus, the invention achieves a significant reduction in the channel resistance. Furthermore, the channel length of the device can be controlled by preferably choosing one or more parameters, including and not limited to the implant dose and implant as well as the temperature and time of the annealing step for driving in the implanted dopants.

[0021] As an example, a shorter channel can be achieved by increasing the driven time after the drift region implant. The shorter channel length produces a significant decrease in the channel resistance. This is depicted in **FIGS. 3, 4**, and **5**, in which the driven time changes from 10 min (**FIG. 3**), to 20 min (**FIG. 4**), and to 30 min (**FIG. 5**). Note the progressive increase in thickness of the drift region **27**, and the flattening of the boundary **90***a*, **90***b*, **90***c* between the drift region and the overlying epi-layer **72**. In addition, the device forward current spreading inside the drift region is progressively more efficient as the driven time increases (see **FIG. 3** to **FIG. 5** in order) due to a wider spreading area. Consequently, the on-resistance of the drift region is also lowered. To help make clear the differences, **FIG. 5***a* shows the three different cases in one illustration.

[0022] The forward conduction characteristics of the devices in **FIG. 3**, **FIG. 4** and **FIG. 5** have been simulated by using the finite element method. The modeled device on-resistance was extracted from the simulation results. The on-resistance per unit area of devices of **FIGS. 3, 4**, and **5** are 0.22 $m\Omega/cm^2$, 0.18 $m\Omega/cm^2$ and 0.15 $m\Omega/cm^2$ respectively. The cell pitch of all the devices is 2.0 microns. Additionally, when compared to the prior art shown in **FIG. 2**, the body-diode of the new device proposed in this invention as illustrated in **FIGS. 3, 4, 5**, and **5***a* has significantly less PN junction area. Also, the base width of the parasitic BJT of the new device's body-diode becomes more even. The body-diode of the inventive device provides improved forward conduction and reverse recovery characteristics.

[0023] In the fabrication process described in the following paragraphs, a 30V N-Channel trench-gated power MOSFET is used as an example to demonstrate the realization of the concept disclosed in this invention. Only the important process steps are illustrated.

[0024] Devices including the invention are made with the inventive process illustrated in **FIGS. 6-10**. The process begins with an N+ substrate **10** of silicon or other suitable semiconductor material. A p-type epitaxial layer **72** is grown on the substrate **10** in a manner well known in the art. Trenches **110** for holding gate structures are opened by covering the epitaxial layer **72** with a suitable mask. In one embodiment a hard mask **100** of silicon dioxide is either deposited or thermally grown on the top of the epitaxial layer **72**. A layer of photoresist is deposited on the oxide **100** and then patterned to exposed portions of the oxide. The exposed portions of the oxide **100** are removed by a suitable etch to expose portions of the epitaxial layer **72** where the trenches **100** will be formed. The substrate **10** is then etched to remove epitaxial material from the substrate and form the trenches **110**.

[0025] Next, a relatively thin gate oxide layer **120** is thermally grown on the exposed sidewall and floor surfaces of the trenches. Then the substrate is implanted with N-typed dopants **130**, such as phosphorous or arsenic. The residual oxide mask **100** on the epitaxial layer **72** blocks the N-type dopants from entering the upper surface of that layer. The thinner oxide layer **120** on the sidewalls and floors of the trenches allow the implanted N-type ions **130** to enter the epitaxial layer **72** in regions proximate the floors of the trenches.

[0026] Turing to **FIG. 9**, the hard mask **100** is removed from the surface and the implanted ions **130** are driven in by an annealing operation. The drive-in step diffuses the N-type ions in a vertical direction enough to reach the N+ substrate and in a lateral direction to extend across the lower portion of the epitaxial layer **72** and form an unbroken N-type drift region **27** along the bottom of the epitaxial layer **72**. Those skilled in the art will understand that the height of the N-type region **27** depends upon a number of factors, including and not limited to, the type of dopant used the implant energy, the concentration, and the annealing or drive-in time. One or more of the factors are adjusted to achieve the desired net concentration and height of the region **27**.

[0027] See **FIG. 10**. The remaining process steps are standard, including filling the trenches with doped polysilicon, followed by etching a recess in the polysilicon, deposition of an inter-level r-dielectric layer (such as BPSG) fill **60** and etch back to form the self-isolated buried polysilicon gate. Standard procedures may be used to create the P+ body **75** and the N+ source **37**, followed by front-side and back-side metallizations.

[0028] The detailed process described in the previous paragraphs has been simulated and verified. The prior art

shown in **FIG. 1** was also simulated for comparison. **FIG. 11** gives the doping profile **200** along the trench sidewall of the device disclosed in this invention, showing the profile through N^+ source region **237**, P-type epi-layer **272** (channel), N-type drift region **227**, and N^+ substrate **210**. **FIG. 12** gives the doping profile **201** along the same location of the prior art device, showing the profile through N^+ source region **237**, P-well **230** (channel), epi-layer **220**, and N^+ substrate **210**. The channel length and the channel doping concentration have been properly designed so that both devices exhibit non-punch-through breakdown characteristics. The drain-source breakdown voltages are 35 volts and 34 volts respectively for the new device of **FIG. 11** and the standard device of **FIG. 12**. However, the threshold voltage of the new device is about 0.7 volts, but 2.0 volts for the standard device. **FIG. 13** shows the contours of doping concentration inside the new device, through N^+ source regions **237**, P^+ body regions **275**, P-type epi-layer **272** (channel), and N-type drift region **227**. Gate oxide **40**, polysilicon **50**, and BPSG **60** are shown for clarity. It is evident that the doping concentration is almost constant in the channel region **272**.

[**0029**] Finally, it is important to point out that in the new device the PN junction formed by the P epi-layer and the N^+ substrate does not terminate at the silicon surface. As a consequence, the edge termination used for the conventional device of **FIG. 1** can not be applied to the new device disclosed in this invention or the prior art of **FIG. 2**. Currently, the most frequently used edge termination in conventional low voltage MOSFET is depicted in **FIG. 14**, with source metal **337**, gate runner metal **350**, BPSG **360**, field oxide **340**, channel stopper metal **380**, N+ channel stop **338**, epi-layer **20**, and substrate **10**. In order to address this issue, this invention provides a new edge termination as shown in **FIG. 15**. The edge of the die is etched away and a field oxide **340** is grown over the etched edge. A layer of doped polysilicon **370** is formed on the field oxide followed by insulating BPSG layer **360**. Openings are made in that layer for the metal gate runner **350** to contact the polysilicon plate layer **370**. An N+ drift contact region **338** is formed on the lower outer edge of the die for contacting the edge drift region **27**. A channel stopper metal layer **380** contacts the region **338** through suitable openings in the field oxide **340**, polysilicon layer **370** and BPSG layer **360**. This new edge termination is produced by using the same process flow as the active device. The new edge termination has a more efficient utilization of silicon area, due to the fact that the partials of the polysilicon field plate **370** and the metal gap between metal strips **350** and **380** are located along the trench sidewall. In addition, because of lower doping concentration of the P epilayer compared to the concentration of the P well in the standard device of **FIG. 1**, the electric field spreads more into the P epilayer. Consequently, for a given breakdown voltage, the new edge termination presents a smaller lateral dimension than the conventional one.

REFERENCES

[**0030**] [1] Coe, U.S. Pat. No. 4,754,310, 1988.

[**0031**] [2] Chen, U.S. Pat. No. 5,216,275, 1993.

[**0032**] [3] Tihanyi, U.S. Pat. No. 5,438,215, 1995.

[**0033**] [4] Jun Zeng, C. Frank Wheatley, Rick Stokes, Chris Kocon, and Stan Benczkowski, "Optimization of the body-diode of power MOSFETs for high efficient synchronous rectification," ISPSD '2000, pp. 145-148.

CONCLUSION, RAMIFICATIONS, AND SCOPE OF INVENTION

[**0034**] From the above descriptions, figures and narratives, the invention's advantages in providing a low-voltage high-density trench-gated power MOSFET device should be clear.

[**0035**] Although the description, operation and illustrative material above contain much specificity, these specificities should not be construed as limiting the scope of the invention but as merely providing illustrations and examples of some of the preferred embodiments of this invention.

[**0036**] Thus the scope of the invention should be determined by the appended claims and their legal equivalents, rather than by the examples given above.

1. A method for manufacturing a power mosfet comprising the steps of:

forming a gate trench mask with open and closed regions on the surface of a semiconductor substrate;

removing semiconductor material from areas exposed by the open regions of the trench mask to form a plurality of gate trenches;

forming a sacrificial gate oxide layer on the sidewalls of the trenches;

implanting the substrate with a drift region implant that penetrates the oxide on the floors of the trenches and is stopped on the surface of the substrate by the residual trench mask;

diffusing the drift region implant to form a continuous drift layer and define the length of the gate and to form a continuous lightly doped drift region extending between sidewalls of the trenches and from the drain layer toward the source region and along a lower portion of the trench sidewalls to provide a variable, lightly doped concentration that gradually decreases in density from the sidewalls of the trenches toward a plane about midway between the trenches;

removing the trench mask and the sacrificial oxide and forming a gate oxide on the surface of the trench;

depositing a layer of polysilicon on the surface of the substrate and in the trenches;

removing the polysilicon from the surface of the semiconductor substrate and leaving enough polysilicon in the gate trenches to form gates in the trenches;

implanting the substrate with a source dopant to form source regions in the surface of the semiconductor substrate and to increase the conductivity of the polysilicon in the trenches to form gate regions in the trenches;

depositing a layer of BPSG on the substrate;

removing at least apart of the BPSG layer to expose portions of the surface having the source implant;

depositing and patterning a conductive layer over the surface of the substrate to form electrical contacts to the source regions.

2. The method of claim 1 further comprising the steps of:

etching a step having a vertical face and a horizontal ledge on the edge of the die while etching the trenches;

forming a gate runner on an upper surface proximate the vertical face;

forming a heavily doped channel stop region in the horizontal ledge at the edged of the die with dopants of the same polarity as the source region; and

forming a metal contact layer over and in contact with the channel stop region.

* * * * *