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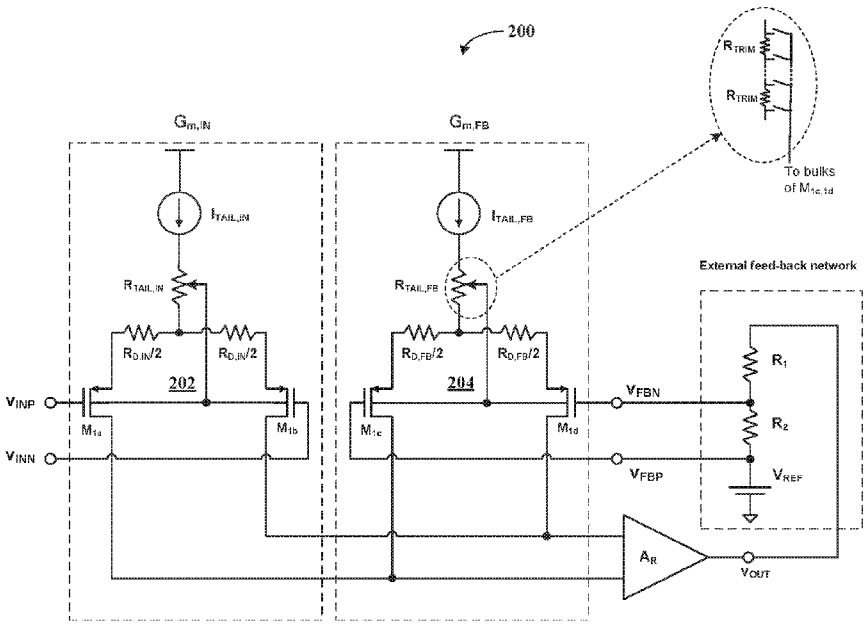


Figure 2

(57) **Abstract:** A current feed-back instrumentation amplifier (CFIA) comprises a differential pair (M_{1a}, M_{1b}) with degeneration for amplifying small differential voltages in the presence of large common-mode voltages. The CFIA includes input and feedback transconductors and a trimming circuit ($R_{TAIL,IN}$, $R_{TAIL,FB}$) that trims the back-bias voltages of the transistors in each transconductor. The trimming circuit ($R_{TAIL,IN}$, $R_{TAIL,FB}$) includes a plurality of selectable resistors disposed in the signal path of the tail current in each transconductor. Each of the plurality of selectable resistors has a switch coupled to it. When a switch is closed, only the resistors up to the respective switch are in the signal path of the bulk-to-source voltage of the differentially paired transistors. The resistor trimming circuit ($R_{TAIL,IN}$, $R_{TAIL,FB}$) reduces the mismatch between transconductances of the respective differential pair transistors, and thereby reducing the CFIA's gain error.

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METHODS OF ADJUSTING GAIN ERROR IN INSTRUMENTATION AMPLIFIERS

RELATED PATENT APPLICATION

This application claims priority to commonly owned United States Provisional Patent Application No. 62/500,448; filed May 2, 2017; which is hereby incorporated by reference herein for all purposes.

TECHNICAL FIELD

In accordance with some embodiments of the disclosed subject matter, systems and methods are provided for dynamically correcting the gain error of an instrumentation amplifier that uses a current-feedback circuit architecture.

BACKGROUND

The gain error, *e.g.*, the difference between the actual transfer function and an ideal transfer function of a current feed-back instrumentation amplifier (CFIA) depends on the accuracy of matching between the CFIA's input transconductor and feedback transconductor. Some existing CFIAs try to address the gain error using an architecture in which each transconductor includes pre-amplifiers to create a transfer function proportional to the ratio between the degeneration resistors of the input and feedback transconductors, see Figure 1. The advantage of this circuit architecture is that it provides a gain error that depends almost exclusively on matching of resistors which is superior to the matching of transistors. While the preamplifiers provide an overall low gain error, their noise adds to the total noise of the instrumentation amplifier, making this architecture less suitable for low noise designs. Another disadvantage is the presence of feedback loops around each pre-amplifier, which makes frequency compensation rather complex and difficult.

In another approach, the CFIA's transconductors are each based on a differential pair of transistors with degeneration. The noise is significantly lower than the solution that uses preamplifiers, and there will be no extra feedback loops. However, the gain error will also change: it will now be affected not only by the mismatch between the input and feedback degeneration resistors, but also by any mismatch between the degenerated differential paired transistors of each transconductor, and by any mismatch between the respective tail currents being fed into each transconductor. As noted above, resistors match much better than transistors do, so mismatches other than the mismatch between the degeneration resistors dominate the gain error.

SUMMARY

Therefore, what is needed is a CFIA having an architecture that minimizes the mismatch between other elements of the input and feedback transconductors, such as the transistors or the tail currents.

According to an embodiment, a method for gain error correction in a current-feedback instrumentation amplifier may comprise the steps of: providing an input transconductor comprising a first differential pair of transistors, a first tail current source, and a first trimming circuit coupled between the first tail current source and the first differential pair of transistors, and to a bulk of the first differential pair of transistors, wherein the first trimming circuit may vary a first back-bias voltage on the bulk of the first differential pair of transistors; providing a feedback transconductor comprising a second differential pair of transistors, a second tail current source, and a second trimming circuit coupled between the second tail current source and the second differential pair of transistors, and to a bulk of the second differential pair of transistors; wherein the second trimming circuit may vary a second back-bias voltage on the bulk of the second differential pair of transistors; and adjusting the first or second trimming circuits to reduce gain error between the input transconductor and feedback transconductor.

According to a further embodiment of the method, may comprise the steps of: providing first degeneration resistors coupled between the first differential pair of transistors and the first trimming circuit; and providing second degeneration resistors coupled between the second differential pair of transistors and the second trimming circuit. According to a further embodiment of the method, the first and second trimming circuits may comprise a plurality of series connected resistors and a plurality of switches coupled to the plurality of series connected resistors, whereby the first and second back-bias voltages may be varied. According to a further embodiment of the method, may comprise the step of storing open and closed states of the plurality of switches in a non-volatile memory. According to a further embodiment of the method, may comprise the step of coupling the input and feedback transconductors to an amplifier.

According to a further embodiment of the method, may comprise the steps of: coupling a feedback network between an output of the amplifier and inputs of the feedback transconductor; and determining the current-feedback instrumentation amplifier gain with the feedback network. According to a further embodiment of the method, may comprise

the steps of: providing a modulator circuit between the first and second tail current sources, and the first and second trimming circuits; controlling the modulator circuit by alternating first and second phase states; wherein during the first phase state the modulator circuit couples the first tail current source to the first trimming circuit and the second tail current source to the second trimming circuit, and during the second phase state the modulator circuit couples the first tail current source to the second trimming circuit, and the second tail current source to the first trimming circuit.

According to another embodiment, a current-feedback instrumentation amplifier having gain error correction may comprise: an input transconductor that may comprise a first differential pair of transistors, a first tail current source, and a first trimming circuit that may be coupled between the first tail current source and the first differential pair of transistors, and to a bulk of the first differential pair of transistors; wherein the first trimming circuit may be configured to vary a first back-bias voltage on the bulk of the first differential pair of transistors; a feedback transconductor that may comprise a second differential pair of transistors, a second tail current source, and a second trimming circuit that may be coupled between the second tail current source and the second differential pair of transistors, and to a bulk of the second differential pair of transistors; wherein the second trimming circuit may be configured to vary a second back-bias voltage on the bulk of the second differential pair of transistors; and the first or second trimming circuits may be adapted to be adjusted to reduce gain error between the input transconductor and feedback transconductor.

According to a further embodiment, the first degeneration resistors may be coupled between the first differential pair of transistors and the first trimming circuit; and second degeneration resistors may be coupled between the second differential pair of transistors and the second trimming circuit. According to a further embodiment, the first and second trimming circuits may comprise a plurality of series connected resistors and a plurality of switches coupled to the plurality of series connected resistors, wherein the plurality of resistors and switches may be adapted to vary the first and second back-bias voltages. According to a further embodiment, a non-volatile memory may be adapted for storing open and closed states of the plurality of switches According to a further embodiment, an amplifier may have inputs thereof coupled to outputs from the input and feedback

transconductors. According to a further embodiment, a feedback network may be coupled between an output of the amplifier and inputs of the feedback transconductor.

According to a further embodiment, the feedback network may comprise: a first feedback resistor; a second feedback resistor; and a voltage reference; wherein the first and second feedback resistors and the voltage reference may be connected in series, a first input of the feedback transconductor may be coupled to a node between the second feedback resistor and the voltage reference, a second input of the feedback transconductor may be coupled to a node between the first feedback resistor and the second feedback resistor, and the output of the amplifier may be coupled to the first feedback resistor; wherein gain may be determined by a ratio of resistance values of the first and second feedback resistors.

According to a further embodiment, a modulator circuit may be coupled between the first and second tail current sources, and the first and second trimming circuits, wherein the modulator circuit may be adapted to alternate between first and second phase states; wherein during the first phase state the modulator circuit may be adapted to couple the first tail current source to the first trimming circuit and the second tail current source to the second trimming circuit; and wherein during the second phase state the modulator circuit may be adapted to couple the first tail current source to the second trimming circuit, and the second tail current source to the first trimming circuit.

According to a further embodiment, the modulator circuit may comprise: a first switch coupled between the first tail current source and the first degeneration resistors; a second switch coupled between the first tail current source and the second degeneration resistors; a third switch coupled between the second tail current source and the first degeneration resistors; and a fourth switch coupled between the second tail current source and the second degeneration resistors; wherein the first and fourth switches may be configured to close and the second and third switches may be configured to open on a first phase state control signal; and the second and third switches may be configured to close and the first and fourth switches may be configured to open on a second phase state control signal.

According to a further embodiment, the first and second phase state control signals may be from a clock generator, wherein the first phase state control signal may be at a first logic level and the second phase state control signal may be at a second logic level. According to a further embodiment, the first, second, third and fourth switches may be

metal oxide semiconductor field effect transistors (MOSFETs). According to a further embodiment, the input and feedback transconductors may be fabricated on an integrated circuit die.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present disclosure may be acquired by referring to the following description taken in conjunction with the accompanying drawings wherein:

Figure 1 illustrates a schematic diagram of a prior art current-feedback instrumentation amplifier that uses preamplifiers;

Figure 1A illustrates a schematic diagram of a prior art current-feedback instrumentation amplifier;

Figure 2 illustrates a schematic diagram of a current-feedback instrumentation amplifier with a back-bias voltage trimming circuit, according to a specific example embodiment of the present disclosure;

Figures 2A and 2B illustrate schematic diagrams of trim resistor and switching arrangements for current-feedback instrumentation amplifier shown in Figure 2, according to specific example embodiments of the present disclosure;

Figure 2C illustrates a schematic diagram of a current-feedback instrumentation amplifier without degeneration resistors and comprising a back-bias voltage trimming circuit, according to another specific example embodiment of this disclosure;

Figure 3 illustrates a schematic diagram of a current-feedback instrumentation amplifier according to the circuit architecture of Figure 2 and further comprising a tail current source modulator circuit, according to yet another specific example embodiment of the present disclosure;

Figure 3A illustrates a schematic diagram of the current-feedback instrumentation amplifier shown in Figure 3 in a first phase state;

Figure 3B illustrates a schematic diagram of the current-feedback instrumentation amplifier shown in Figure 3 in a second phase state;

Figure 4 illustrates a schematic diagram of a current-feedback instrumentation amplifier with a back-bias voltage trimming circuit, according to still another specific example embodiment of the present disclosure.

While the present disclosure is susceptible to various modifications and alternative forms, specific example embodiments thereof have been shown in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific example embodiments is not intended to limit the disclosure to the particular forms disclosed herein.

DETAILED DESCRIPTION

In accordance with some embodiments of the disclosed subject matter, the present disclosure provides a Current Feed-back Instrumentation Amplifier (CFIA) fabricated on an integrated circuit die and comprising a circuit architecture that is based on a differential pair with degeneration. The present CFIA includes a trimming circuit that trims the back-bias voltages of the transistors in each transconductor. The trimming circuit may include a plurality of selectable resistors disposed in the signal path of the tail current in each transconductor. Each of the plurality of selectable resistors has a switch coupled to it. The switches in each transconductor are controlled in such a way that only one switch is closed at a time, the rest remaining open. When a switch is closed, only the resistors up to the respective switch are in the signal path of the bulk-to-source voltage of the differentially paired transistors. The closed resistance of the switch is much less than the input resistance value into the bulk terminals of the differentially paired transistors and does not affect the signal path from the selectable resistors to the bulks.

A non-volatile memory (not shown) may be used to remember the open and closed switch configurations. The resistor trimming circuit reduces the mismatch between transconductances of the respective differential pair transistors, in turn reducing mismatch of the overall transconductances of the transconductors, and thereby reducing the CFIA's gain error. The resistor trimming circuit may also be used in conjunction with a tail current modulator circuit architecture designed to eliminate the contribution of tail current mismatch to the overall gain error, and further reduce the gain error.

The present disclosure is directed toward an architecture for a CFIA comprising differential transistor pairs with degeneration for amplifying small differential voltages in the presence of large common-mode voltages. The present CFIA circuit architecture employs trimming of a target voltage, specifically the back-bias voltage, V_{BS}, that is inherent in any metal oxide semiconductor (MOS) transistor operating in a sub-threshold region. It is contemplated and within the scope of this disclosure that this invention is not

limited to just the sub-threshold region, *e.g.*, it is equally valid for transistors operating in the saturation region. The back-bias voltage is a contributor to one of the factors that affects the transconductance g_m of a particular transistor; as shown below, trimming the back-bias voltage of each MOS transistor, *e.g.*, P-channel or N-channel MOS field effect transistor (MOSFET), in the respective transconductors reduces mismatch between the transconductances of the respective MOS transistors. In various embodiments, the back-bias voltage is trimmed using a signal voltage fed from a variable resistor comprising a selectable plurality of resistors of a switched resistor network and disposed in the tail current signal path of each transconductor.

Referring now to the drawings, the details of example embodiments are schematically illustrated. Like elements in the drawings will be represented by like numbers, and similar elements will be represented by like numbers with a different lower-case letter suffix.

Referring now to Figure 1A, depicted is a schematic diagram of a prior art current-feedback instrumentation amplifier. An example current-feedback instrumentation amplifier (CFIA), generally represented by the numeral 100A, may use a differential pair with degeneration architecture. The CFIA 100 includes an input transconductor $G_{m,IN}$ that operates on differential input voltages V_{INP} and V_{INN}, and a feedback transconductor $G_{m,FB}$ that operates on feedback voltages V_{FBN} and V_{FBP}. Each transconductor ($G_{m,IN}$ and $G_{m,FB}$) has a respective tail current I_{TAIL} source. Each transconductor ($G_{m,IN}$ and $G_{m,FB}$) includes degeneration resistors R_D, a first pair of transistors M_{1a} and M_{1b} (for $G_{m,IN}$), and a second pair of transistors M_{1c} and M_{1d} (for $G_{m,FB}$). Both transconductors ($G_{m,IN}$ and $G_{m,FB}$) are coupled together and output a signal to an amplifier A_R as shown in Figure 1A.

Generally, the gain error is given by the ratio between $G_{m,IN}$ and $G_{m,FB}$. Gain error = $G_{m,IN}$ / $G_{m,FB}$ -1, where it is assumed the matching between the external resistors R_1 and R_2 is much better than the match between $G_{m,IN}$ and $G_{m,FB}$. For the CFIA 200, $G_{m,IN} = \frac{g_{m1ab}}{2+g_{m1ab}R_{D,IN}}$ and $G_{m,FB} = \frac{g_{m1cd}}{2+g_{m1cd}R_{D,FB}}$, where g_{m1ab} is the transconductance of transistors M_{1a} and M_{1b}, and g_{m1cd} is the transconductance of transistors M_{1b} and M_{1d}, and $R_{D,IN}$ and $R_{D,FB}$ have already been defined above. For simplicity, it is assumed there is no mismatch between M_{1a} and M_{1b} and they have the same transconductance, g_{m1ab}. Likewise, it is assumed there is no mismatch between M_{1c} and M_{1d} and they have the same

transconductance g_{m1cd}. For convenience, one usually choses $g_{m1ab} = g_{m1cd}$, and $R_{D,IN}=R_{D,FB}$, such that the ratio $G_{m,IN}/G_{m,FB}$ may be unity. For transistors operating in the sub-threshold region $g_{m1ab} = \frac{I_{TAIL,IN}}{2n_{ab}V_{T,ab}}$ and $g_{m1ab} = \frac{I_{TAIL,FB}}{2n_{cd}V_{T,cd}}$, where $I_{TAIL,IN}$ and $I_{TAIL,FB}$ are the tail currents of $G_{m,IN}$ and $G_{m,FB}$, respectively; n_{ab} and n_{cd} are the sub-threshold constants of transistors M_{1a} and M_{1b}, and M_{1c} and M_{1d}, respectively; and $V_{T,ab}$ and $V_{T,cd}$ the thermal voltages of M_{1a} and M_{1b}, and M_{1c} and M_{1d}, respectively. The gain error will therefore depend on the matching between $R_{D,IN}$ and $R_{D,FB}$, $I_{TAIL,IN}$ and $I_{TAIL,FB}$, n_{ab} and n_{cd}, and $V_{T,ab}$ and $V_{T,cd}$. In the ideal case, $R_{D,IN} = R_{D,FB}$, $I_{TAIL,IN} = I_{TAIL,FB}$, $n_{ab} = n_{cd}$, $V_{T,ab} = V_{T,cd}$, and the gain error is zero. This disclosure particularly addresses the contribution of the mismatch between n_{ab} and n_{cd} to the overall gain error.

It can be shown that the sub-threshold factor, n, for a MOS transistor depends on the back-bias (bulk-to-source) voltage of the transistor. The factor n is a function of the capacitances of the transistor: $n = 1 + (C_{bulk}/C_{ox})$, where C_{ox} is the gate oxide capacitance and C_{bulk} is the capacitance of the depletion region around a constant source diffusion. C_{bulk} is inversely proportional to the depletion region width, w_d, where $C_{bulk} = \varepsilon_{Si}/w_d$. The depletion region width, w_d, is, in turn, proportional to the back-bias (also known as "body bias") voltage V_{BS} present at the back gate of the transistor:

$$w_d = depletion\ region\ width = \sqrt{\frac{2\varepsilon_{Si}(2\Psi_B + V_{BS})}{qN_A}}$$

where ε_{Si} is the permittivity of silicon, Ψ_B is the Fermi potential, and N_A is the bulk concentration in the transistor material. Thus, the sub-threshold factor n is inversely proportional to the back-bias voltage V_{BS}, which means g_{m1ab} is directly proportional to V_{BSab} (of transistors M_{1a} and M_{1b}), and g_{m1cd} is directly proportional to V_{BScd} (of transistors M_{1c} and M_{1d}). Furthermore, it can be assumed that the other parameters that make up the factor n are relatively constant between transistors, such that matching V_{BS} across transistors will cause the transistors' transconductances, g_{m1ab} and g_{m1cd}, to match as well.

Referring now to Figure 2, depicted is a schematic diagram of a current-feedback instrumentation amplifier with a back-bias voltage trimming circuit, according to a specific example embodiment of the present disclosure. A CFIA, generally represented by the numeral 200, may use back-bias voltage trimming circuits to minimize or substantially eliminate the contribution of mismatched transistor transconductances to the gain error of

the CFIA 200. In some embodiments, the CFIA 200 may comprise the CFIA 100 architecture shown in Figure 1 and a trimming circuit 202, 204 in each transconductor $G_{m,IN}$, $G_{m,FB}$, respectively. The trimming circuits 202, 204 connect the bulks or "bodies" of the transistors (M_{1a}, M_{1b}) and (M_{1c}, M_{1d}) in each differential pair (*e.g.*, through the bulk or "body" terminal of the transistor) to variable resistors $R_{TAIL,IN}$ and $R_{TAIL,FB}$, respectively, that are disposed in the signal paths of the tail currents $I_{TAIL,IN}$ and $I_{TAIL,FB}$, respectively. The variable resistors $R_{TAIL,IN}$ and $R_{TAIL,FB}$ thereby serve as bias networks to which the transistor bodies M_{1a} and M_{1b}, and M_{1c} and M_{1d}, respectively, are connected, rather than being connected to power or ground. In some embodiments, the variable resistor R_{TAIL} may be a plurality of series-connected resistors R_{TRIM} that are connected to the tail current source. The trimming circuits 202, 204 are thus one way to obtain a variable bulk-to-source voltage: the bulks of transistors M_{1a} and M_{1b}, and M_{1c} and M_{1d}; are connected to the 'center tap' (represented by an arrow) of the variable resistors $R_{TAIL,IN}$ and $R_{TAIL,FB}$, respectively, placed in series with the tail currents of the input and feedback transconductors. In the architecture shown in Figure 2, $V_{BSab} = I_{TAIL,IN} * R_{TAIL,IN} + (I_{TAIL,IN} * R_{D,IN}/4)$ and $V_{BScd} = I_{TAIL,FB} * R_{TAIL,FB} + (I_{TAIL,FB} * R_{D,FB}/4)$.

Referring to Figures 2A and 2B, depicted are schematic diagrams of trim resistor and switching arrangements for current-feedback instrumentation amplifier shown in Figure 2, according to specific example embodiments of the present disclosure. The variable resistor R_{TAIL} may comprise a plurality of series coupled R_{TRIM} resistors and corresponding switches. The R_{TRIM} resistors may be series coupled between the tail current source and the bulks of the transistors. A corresponding switch when closed will connect the associated R_{TRIM} resistor to the bulks of the differentially paired transistors, altering their back-bias voltage. When the corresponding switch is open the associated R_{TRIM} resistor will no longer be part of the variable resistor R_{TAIL}. The switches may comprise MOS transistors as shown in Figure 2B.

An open and close pattern for the switches may be stored in a memory module (not shown), such as, for example but is not limited to, an 8-bit memory module. The memory module may comprise a non-volatile memory cell. Thus, the position (resistance) of the center tap may be set by means of the switches controlled by a digital code and stored in a non-volatile memory.

For instance, if due to random mismatch $G_{m,IN} < G_{m,FB}$, the gain error is measured lower than 0; increasing the V_{BS} of transistors M_{1a} and M_{1b} will lead to an increase in their g_m, and consequently in $G_{m,IN}$. This is obtained by moving the tap of the input transconductor's R_{TAIL} upwards, in other words switching on a switch of a higher code. If on the other hand, the gain error is measured higher than 0 (the case where $G_{m,IN} > G_{m,FB}$), V_{BS} of M_{1c} and M_{1d} needs to be increased until $G_{m,FB}$ becomes equal to $G_{m,IN}$ (and the gain error is 0). The center tap of the feedback transconductor's R_{TAIL} will need to move upwards. In the example shown here the trimming code has 4 bits, and the value of each resistor R_{TRIM} can only be adjusted upwards; if MSB = 0 the resistor of $G_{m,IN}$ is increased until $G_{m,IN} = G_{m,FB}$; if MSB = 1 the resistor of $G_{m,FB}$ is increased until $G_{m,FB} = G_{m,IN}$. One advantage of this method is the fact the MOS switches are arranged in such a way that when a switch is ON, its channel resistance (non-linear and process-variable) is negligible because it's in series with a high impedance node, the bulks of the differentially connected transistors.

Referring to Figure 2C, depicted is a schematic diagram of a current-feedback instrumentation amplifier without degeneration resistors and comprising a back-bias voltage trimming circuit, according to still another specific example embodiment of this disclosure. A back-bias voltage trimming circuit may be effectively used to minimize or substantially eliminate the contribution of mismatched transistor transconductances to the gain error of the CFIA 200C even without the degeneration resistors used in the CFIAs 200, 300 and 400. The CFIA 200C shown in Figure 2C operates in substantially the same fashion as the CFIA 200 described hereinabove, but is configured without degeneration resistors R_D (Figure 2).

Referring now to Figure 3, depicted is a schematic diagram of a current-feedback instrumentation amplifier according to the circuit architecture of Figure 2 and further comprising a tail current source modulator circuit, according to another specific example embodiment of the present disclosure. The circuit architecture shown in Figure 2 may be combined with an additional error-reducing circuit architecture that employs dynamic correction (*e.g.*, "chopping") of the tail current sources for each transconductor to average out the tail current values in each transconductor, thereby reducing mismatch and improving overall gain error and linearity. A CFIA, generally represented by the numeral 300, may comprise the CFIA 200 circuit architecture shown in Figure 2 and a modulator circuit 302

disposed between the tail current sources $I_{TAIL,IN}$ and $I_{TAIL,FB}$ and the R_{TAIL} resistors. The modulator circuit 302 implements dynamic correction of the tail current mismatch by periodically swapping tail current sources $I_{TAIL,IN}$ and $I_{TAIL,FB}$ to minimize or eliminate the contribution of mismatched currents to the CFIA gain error. This is in addition to the reduction of gain error by trimming the back-bias voltages, as disclosed hereinabove. In some embodiments, the modulator circuit 302 may operate based on input received as one or more regulated signals phi1 and phi2, *e.g.*, provided by a clock or another regulating circuit. In an example implementation, the regulated signals phi1 and phi2 alternately switch between low and high logic levels every half clock cycle, swapping the tail current sources between transconductors $G_{m,IN}$ and $G_{m,FB}$ twice every clock cycle.

The modulator circuit 302 implements dynamic correction of the tail current mismatch by periodically swapping tail currents: during one period the tail current $I_{TAIL,IN}$ flows into the input transconductor and the tail current $I_{TAIL,FB}$ flows into the feedback transconductor, then the modulator circuit 302 switches the tail currents, and during the next period the current $I_{TAIL,IN}$ flows into the feedback transconductor and the tail current $I_{TAIL,FB}$ flows into the input transconductor. In some embodiments, the modulator circuit 302 may operate based on input received as one or more regulated signals phi1, phi2 provided by a clock or another regulating circuit. In an example implementation, the regulated signals phi1, phi2 switch between high and low logic levels every half clock cycle, swapping the tail currents between transconductors twice every clock cycle. Over a complete clock cycle the tail current that flows into the input transconductor is on average equal to the tail current that flows into the feedback transconductor. This approach allows the portion of the gain error contributed by mismatched tail currents to be continuously corrected during operation of the CFIA 300.

Referring to Figures 3A and 3B, depicted are schematic diagrams of the current-feedback instrumentation amplifier shown in Figure 3 in first and second phase states, respectively. The modulator circuit 302 of Figure 3, may include four switches 302A-302D that may be adapted to alternately connect each tail current, $I_{TAIL,IN}$ and $I_{TAIL,FB}$, in the transconductors $G_{m,IN}$ and $G_{m,FB}$. The regulated signals phi1 and phi2 may be provided from a clock signal and are shown to be in opposite phase, such that phi1 is low when phi2 is high, and vice-versa. As shown in Figure 3A, when phi1 is low and phi2 is high, the "outer" switches 302A and 302D are closed, and the "inner" switches 302B and 302C are open. As

shown in Figure 3B, when the desired period (*e.g.*, a clock cycle, clock half-cycle, *etc.*) elapses the values of the regulated signals phi1, phi2 flip; whereby phi1 is high and phi2 is low, the "outer" switches 302A and 302D are open, and the "inner" switches 302B and 302C are closed.

To illustrate how the current invention corrects the effect of tail current mismatch to gain error, it may be assumed that the tail current of $G_{m,IN}$, $I_{TAIL,IN}$ has a nominal value of I_{TAIL}, while the tail current of transconductor $G_{m,FB}$ suffers from a random mismatch denoted by δ such that its value is $I_{TAIL,FB} = I_{TAIL} + \delta * I_{TAIL}$. During a first phase (phi1 low and phi2 high – see Figure 3A) the "baseline" current I_{TAIL} flows into the input transconductor $G_{m,IN}$ and the mismatched tail current $(1+\delta)*I_{TAIL}$ flows into the feedback transconductor $G_{m,FB}$. The transconductance of transistors M_{1a} and M_{1b}, g_{m1ab} will have a nominal value equal to g_m, while the transconductance of M_{1c} and M_{1d} will suffer from an equal mismatch, δ, $g_{m1cd} = g_m + \delta * g_m$; $G_{m,IN}$ will be equal to a nominal value Gm, while $G_{m,FB}$ will be approximately equal to $G_m(1+\delta)$. Therefore, during this phase, the gain error will be approximately $-\delta$. Then in the second phase (phi1 high and phi2 low – see figure 3B) the modulator circuit 302 switches the tail current sources, and the baseline current I_{TAIL} flows into the feedback transconductor $G_{m,FB}$ and the mismatched tail current $(1+\delta)*I_{TAIL}$ flows into the input transconductor $G_{m,IN}$. During this cycle, $G_{m,IN}$ will be $G_m(1+\delta)$, $G_{m,FB}$ will be equal to G_m, and the gain error will be approximately $+\delta$. If during one half clock cycle, the gain error is $-\delta$, and during the other half clock cycle $+\delta$, over a complete clock cycle the gain error will be on average zero. Thus, the modulator circuit 302 provides a continuous correction of the gain error during CFIA 300 operation.

Additionally, various embodiments of the present CFIA architecture are suitable for high-voltage designs, even when the difference between common-mode voltages V_{INP}, V_{INN}, V_{FBP}, V_{FBN} on the respective transconductors is large (*e.g.*, over five (5) volts).

Referring to Figure 4, depicted is a schematic diagram of a current-feedback instrumentation amplifier with a back-bias voltage trimming circuit, according to yet another specific example embodiment of the present disclosure. The CFIA 400 shown in Figure 4 is configured and operates in substantially the same fashion as the CFIA 200 described hereinabove, but its architecture comprises N-channel MOSFETS instead of P-channel MOSFETS (Figure 2).

The present invention has been described in terms of one or more preferred embodiments, and it should be appreciated that many equivalents, alternatives, variations, and modifications, aside from those expressly stated (*e.g.*, methods of manufacturing, product by process, and so forth), are possible and within the scope of the invention.

5

CLAIMS

What is claimed is:

1. A method for gain error correction in a current-feedback instrumentation amplifier, said method comprising the steps of:

providing an input transconductor, the input transconductor comprising:

a first differential pair of transistors;

a first tail current source; and

a first trimming circuit:

coupled between the first tail current source and the first differential pair of transistors, and to a bulk of the first differential pair of transistors; and

varying a first back-bias voltage on the bulk of the first differential pair of transistors;

providing a feedback transconductor, the feedback transconductor comprising:

a second differential pair of transistors;

a second tail current source; and

a second trimming circuit:

coupled between the second tail current source and the second differential pair of transistors, and to a bulk of the second differential pair of transistors; and

varying a second back-bias voltage on the bulk of the second differential pair of transistors; and

adjusting the first or second trimming circuits to reduce gain error between the input transconductor and feedback transconductor.

2. The method according to Claim 1, further comprising the steps of:

providing first degeneration resistors coupled between the first differential pair of transistors and the first trimming circuit; and

providing second degeneration resistors coupled between the second differential pair of transistors and the second trimming circuit.

3. The method according to any of Claims 1-2, wherein the first and second trimming circuits comprise a plurality of series connected resistors and a plurality of switches

coupled to the plurality of series connected resistors, whereby the first and second back-bias voltages are varied.

4. The method according to Claim 3, further comprising the step of storing open and closed states of the plurality of switches in a non-volatile memory.

5. The method according to any of Claims 1-4, further comprising the step of coupling the input and feedback transconductors to an amplifier.

6. The method according to Claim 5, further comprising the steps of:

coupling a feedback network between an output of the amplifier and inputs of the feedback transconductor; and

determining the current-feedback instrumentation amplifier gain with the feedback network.

7. The method according to any of Claims 1-6, further comprising the steps of:

providing a modulator circuit between the first and second tail current sources, and the first and second trimming circuits; and

controlling the modulator circuit by alternating first and second phase states;

wherein:

during the first phase state the modulator circuit couples the first tail current source to the first trimming circuit and the second tail current source to the second trimming circuit; and

during the second phase state the modulator circuit couples the first tail current source to the second trimming circuit, and the second tail current source to the first trimming circuit.

8. A current-feedback instrumentation amplifier having gain error correction, comprising:

an input transconductor, comprising:

a first differential pair of transistors;

a first tail current source; and

a first trimming circuit:

coupled between the first tail current source and the first differential pair of transistors, and to a bulk of the first differential pair of transistors; and

configured to vary a first back-bias voltage on the bulk of the first differential pair of transistors;

a feedback transconductor, comprising:

a second differential pair of transistors;

a second tail current source; and

a second trimming circuit:

coupled between the second tail current source and the second differential pair of transistors, and to a bulk of the second differential pair of transistors; and

configured to vary a second back-bias voltage on the bulk of the second differential pair of transistors;

wherein the first or second trimming circuits are adapted to be adjusted to reduce gain error between the input transconductor and feedback transconductor.

9. The current-feedback instrumentation amplifier according to Claim 8, further comprising:

first degeneration resistors coupled between the first differential pair of transistors and the first trimming circuit; and

second degeneration resistors coupled between the second differential pair of transistors and the second trimming circuit.

10. The current-feedback instrumentation amplifier according to any of Claims 8-9, wherein the first and second trimming circuits comprise:

a plurality of series connected resistors; and

a plurality of switches coupled to the plurality of series connected resistors;

wherein the plurality of resistors and switches are adapted to vary the first and second back-bias voltages.

11. The current-feedback instrumentation amplifier according to Claim 10, further comprising a non-volatile memory adapted for storing open and closed states of the plurality of switches.

12. The current-feedback instrumentation amplifier according to any of Claims 8-11, further comprising an amplifier having inputs coupled to outputs from the input and feedback transconductors.

13. The current-feedback instrumentation amplifier according to Claim 12, further comprising a feedback network coupled between an output of the amplifier and inputs of the feedback transconductor.

14. The current-feedback instrumentation amplifier according to Claim 13, wherein the feedback network comprises:

a first feedback resistor;

a second feedback resistor; and

a voltage reference;

wherein:

the first and second feedback resistors and the voltage reference are connected in series;

a first input of the feedback transconductor is coupled to a node between the second feedback resistor and the voltage reference;

a second input of the feedback transconductor is coupled to a node between the first feedback resistor and the second feedback resistor;

the output of the amplifier is coupled to the first feedback resistor; and

gain is determined by a ratio of resistance values of the first and second feedback resistors.

15. The current-feedback instrumentation amplifier according to any of Claims 8-14, further comprising a modulator circuit coupled between the first and second tail current sources, and the first and second trimming circuits, wherein:

the modulator circuit is adapted to alternate between first and second phase states;

during the first phase state the modulator circuit is adapted to couple the first tail current source to the first trimming circuit and the second tail current source to the second trimming circuit; and

during the second phase state the modulator circuit is adapted to couple the first tail current source to the second trimming circuit, and the second tail current source to the first trimming circuit.

16. The current-feedback instrumentation amplifier according to Claim 15, wherein the modulator circuit comprises:

a first switch coupled between the first tail current source and the first degeneration resistors;

a second switch coupled between the first tail current source and the second degeneration resistors;

a third switch coupled between the second tail current source and the first degeneration resistors; and

a fourth switch coupled between the second tail current source and the second degeneration resistors;

wherein:

the first and fourth switches are configured to close and the second and third switches are configured to open on a first phase state control signal; and

the second and third switches are configured to close and the first and fourth switches are configured to open on a second phase state control signal.

17. The current-feedback instrumentation amplifier according to Claim 16, wherein:

the first and second phase state control signals are from a clock generator; and

the first phase state control signal is at a first logic level and the second phase state control signal is at a second logic level.

18. The current-feedback instrumentation amplifier according to any of Claims 16-17, wherein the first, second, third and fourth switches are metal oxide semiconductor field effect transistors (MOSFETs).

19. The current-feedback instrumentation amplifier according to any of Claims 8-18, wherein the input and feedback transconductors are fabricated on an integrated circuit die.

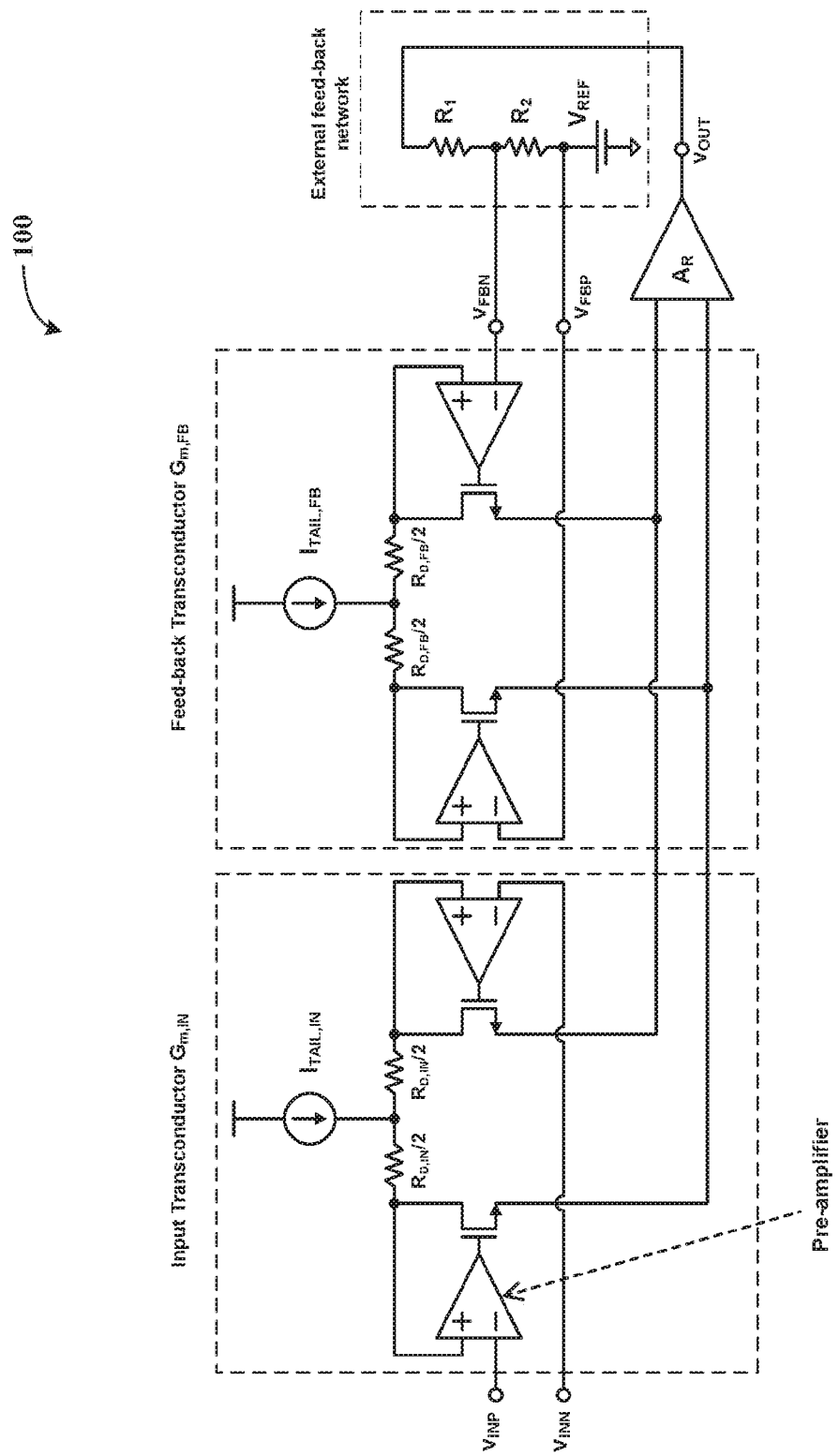


Figure 1 (Prior Art)

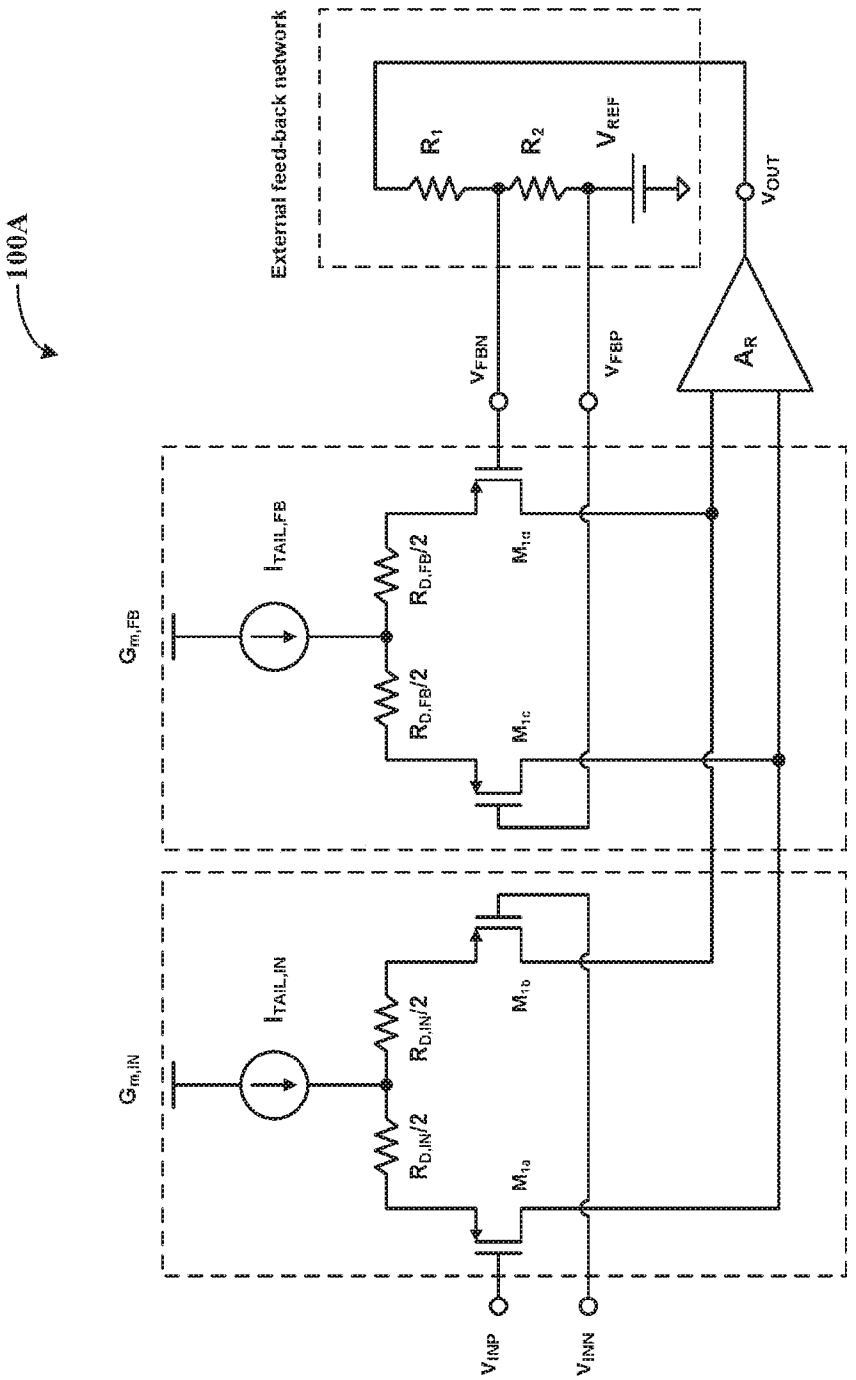


Figure 1A (Prior Art)

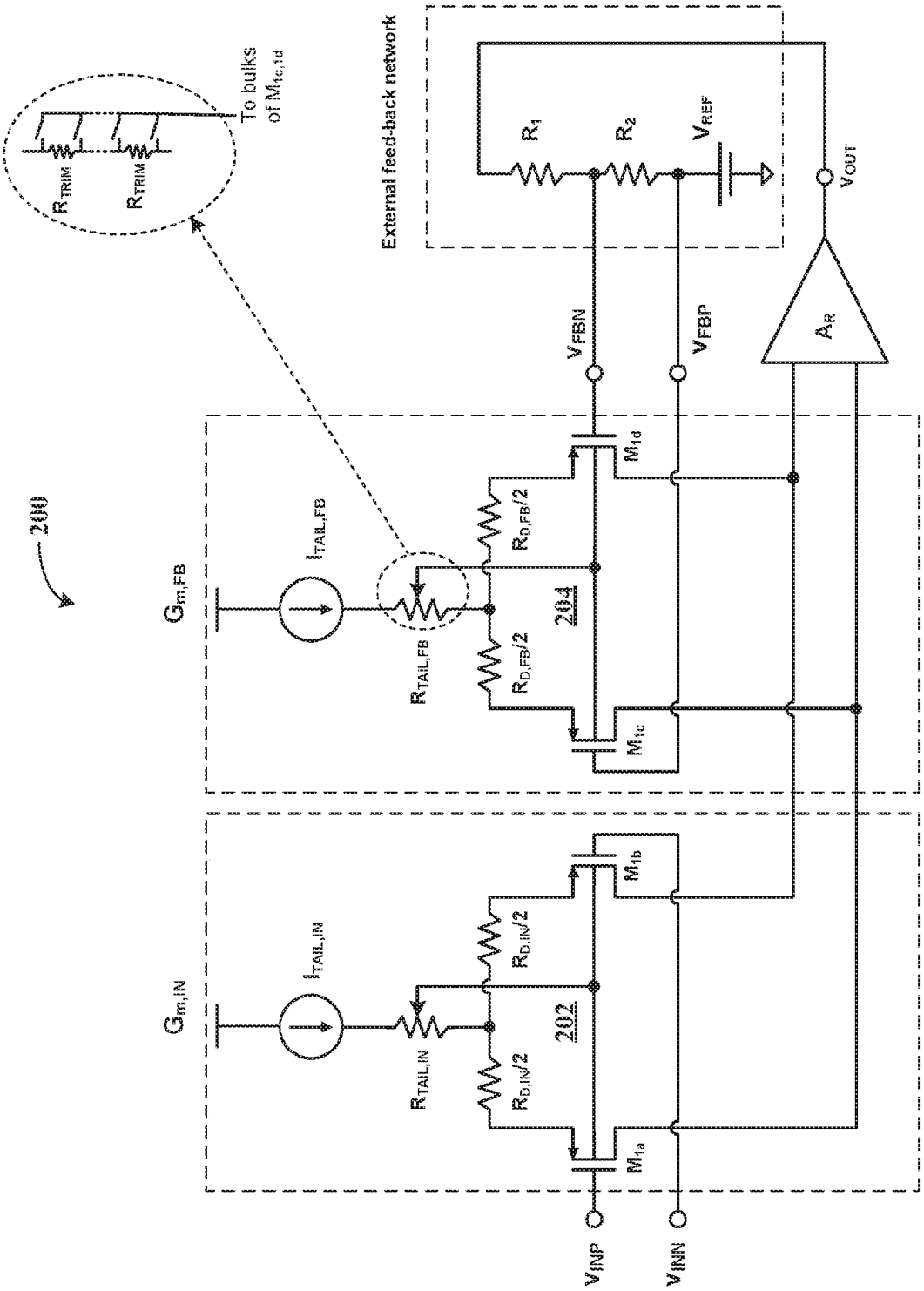

200
To bulks of $M_{1c,1d}$
R_{TRIM}
R_{TRIM}
External feed-back network
R_1
R_2
V_{REF}
V_{OUT}
A_R
V_{FBN}
V_{FBP}
$G_{m,FB}$
$I_{TAIL,FB}$
$R_{TAIL,FB}$
$R_{D,FB}/2$
$R_{D,FB}/2$
204
M_{1d}
M_{1c}
$G_{m,IN}$
$I_{TAIL,IN}$
$R_{TAIL,IN}$
$R_{D,IN}/2$
$R_{D,IN}/2$
202
M_{1b}
M_{1a}
V_{INP}
V_{INN}

Figure 2

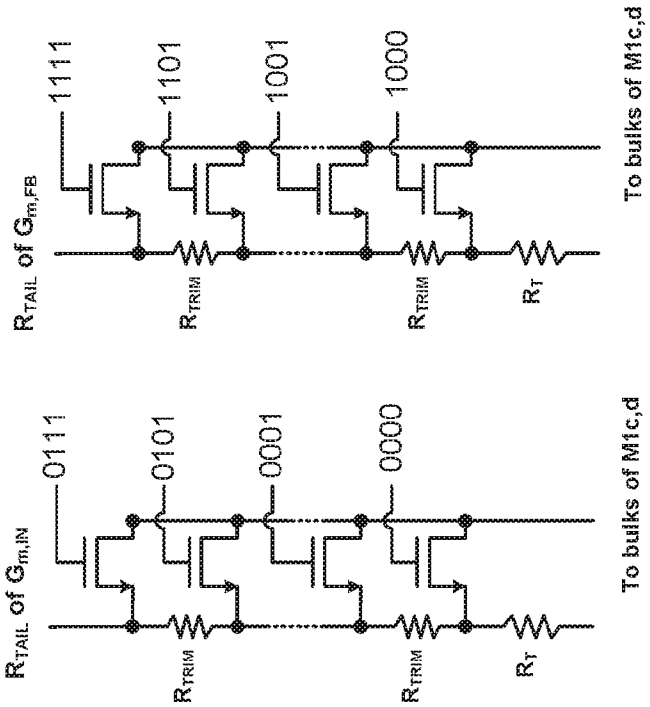


Figure 2B

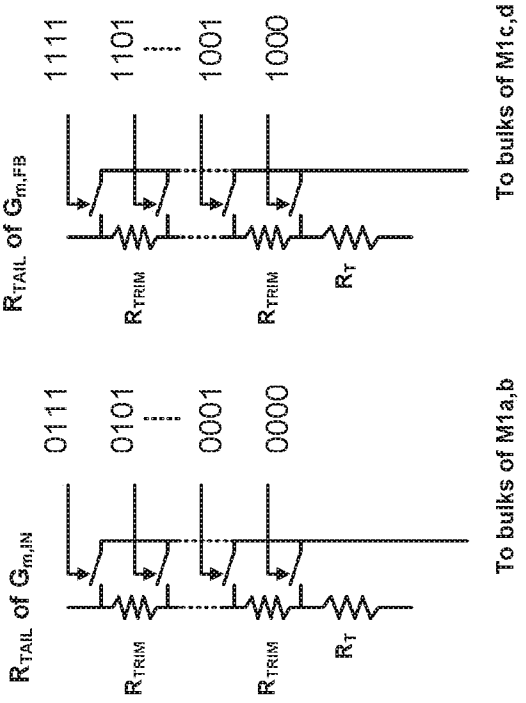


Figure 2A

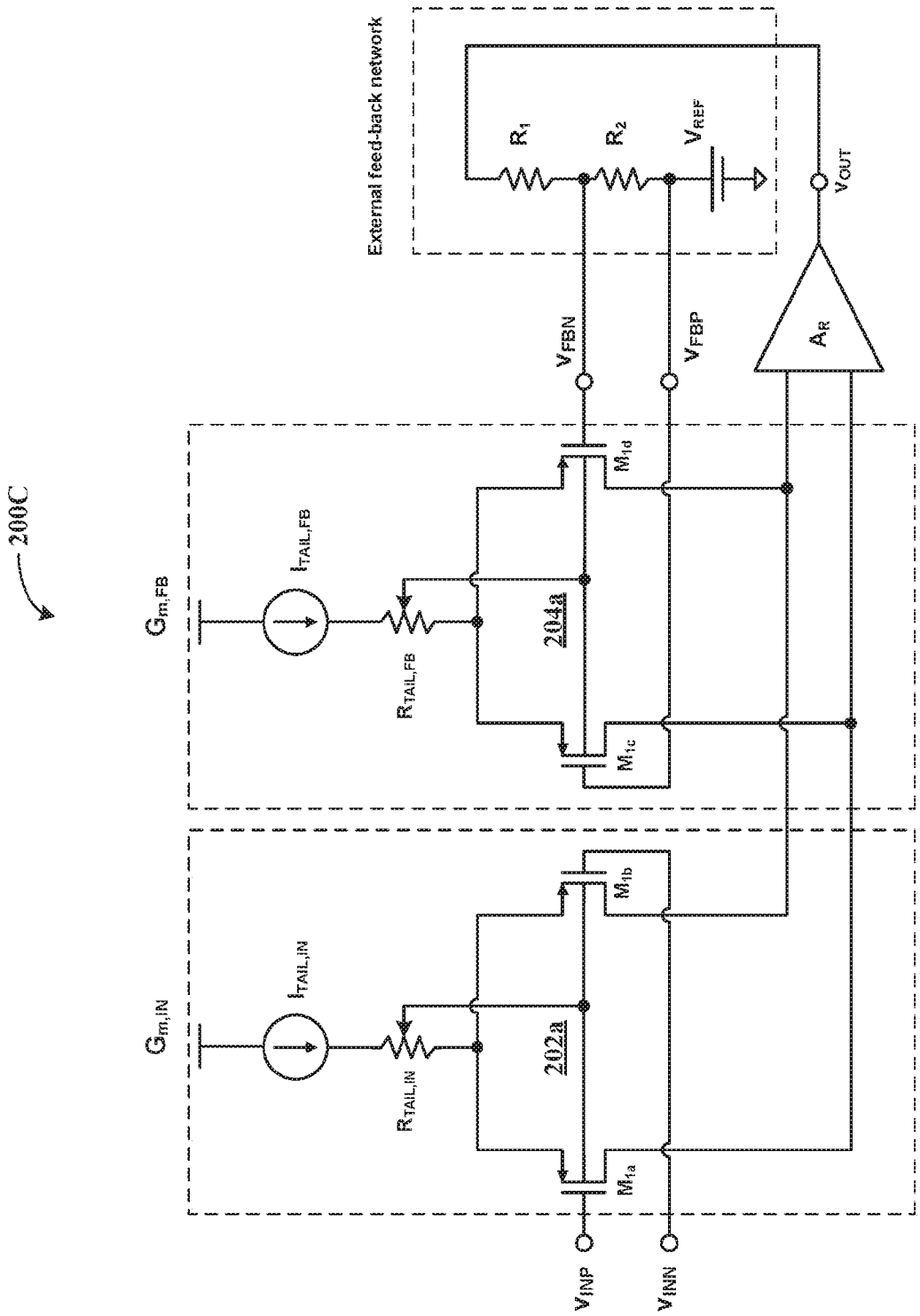

200C
External feed-back network
R1
R2
VREF
VOUT
AR
VFBN
VFBP
Gm,FB
ITAIL,FB
RTAIL,FB
204a
M1d
M1c
Gm,iN
ITAIL,iN
RTAIL,iN
202a
M1b
M1a
VINP
VINN

Figure 2C

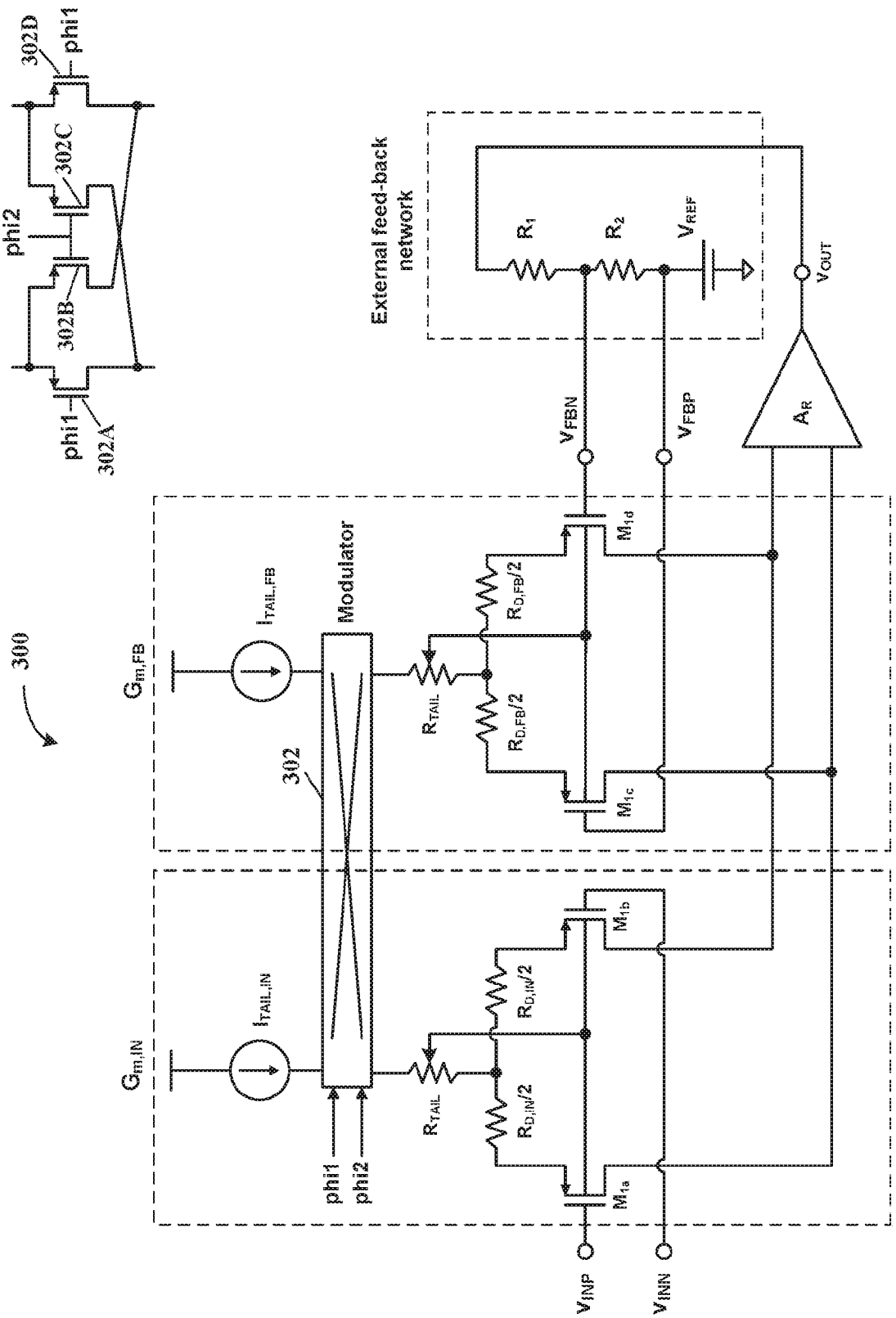

300
302
Modulator
$G_{m,FB}$
$G_{m,IN}$
$I_{TAIL,FB}$
$I_{TAIL,IN}$
R_{TAIL}
$R_{D,FB}/2$
$R_{D,IN}/2$
M_{1a}
M_{1b}
M_{1c}
M_{1d}
phi1
phi2
V_{INP}
V_{INN}
V_{FBN}
V_{FBP}
A_R
V_{OUT}
External feed-back network
R_1
R_2
V_{REF}
302A
302B
302C
302D

Figure 3

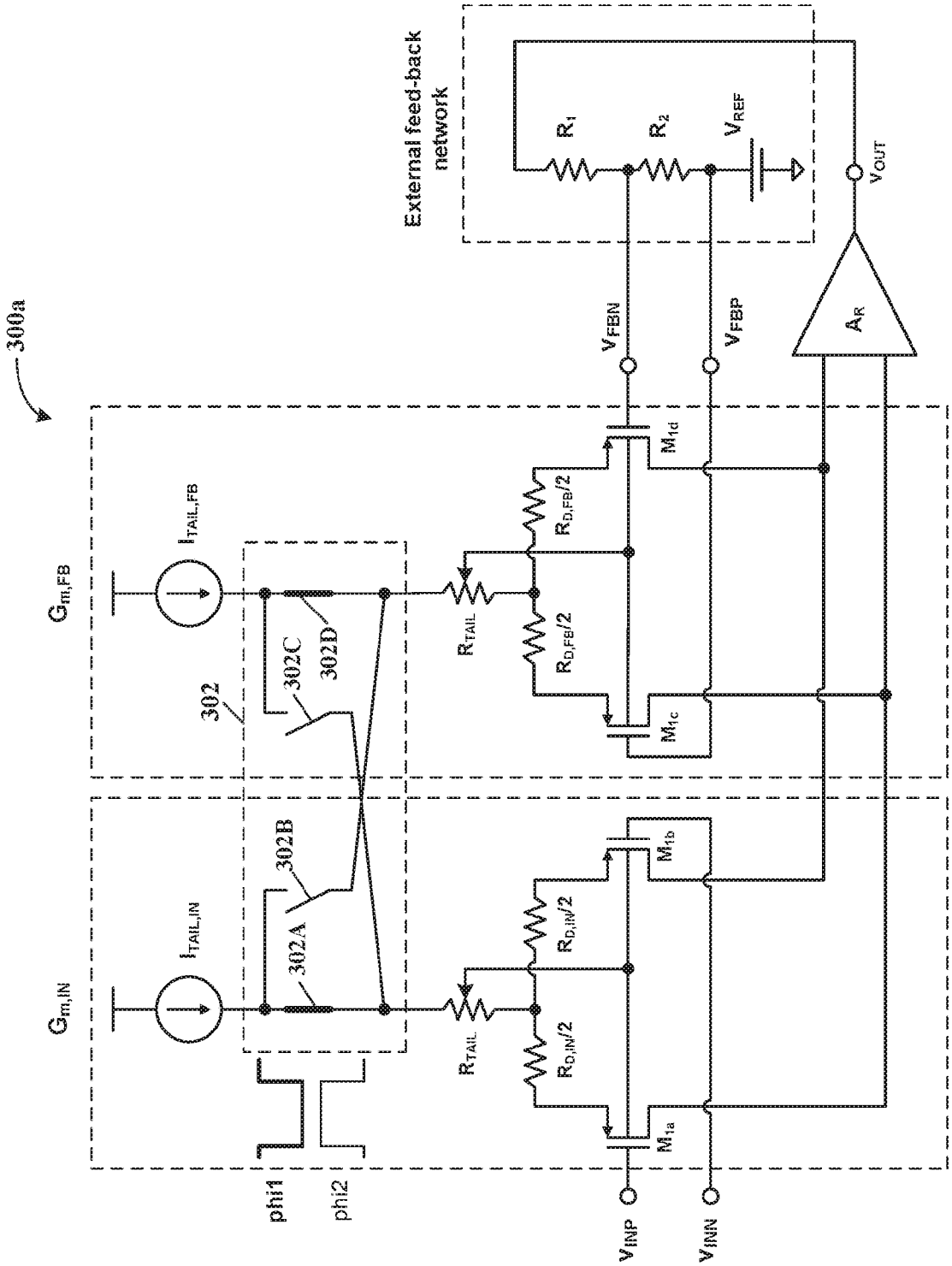

300a
External feed-back network
R1
R2
VREF
VOUT
AR
VFBN
VFBP
Gm,FB
ITAIL,FB
302
302C
302D
RTAIL
RD,FB/2
RD,FB/2
M1d
M1c
Gm,IN
ITAIL,IN
302B
302A
RD,IN/2
RD,IN/2
M1b
M1a
phi1
phi2
VINP
VINN

Figure 3A

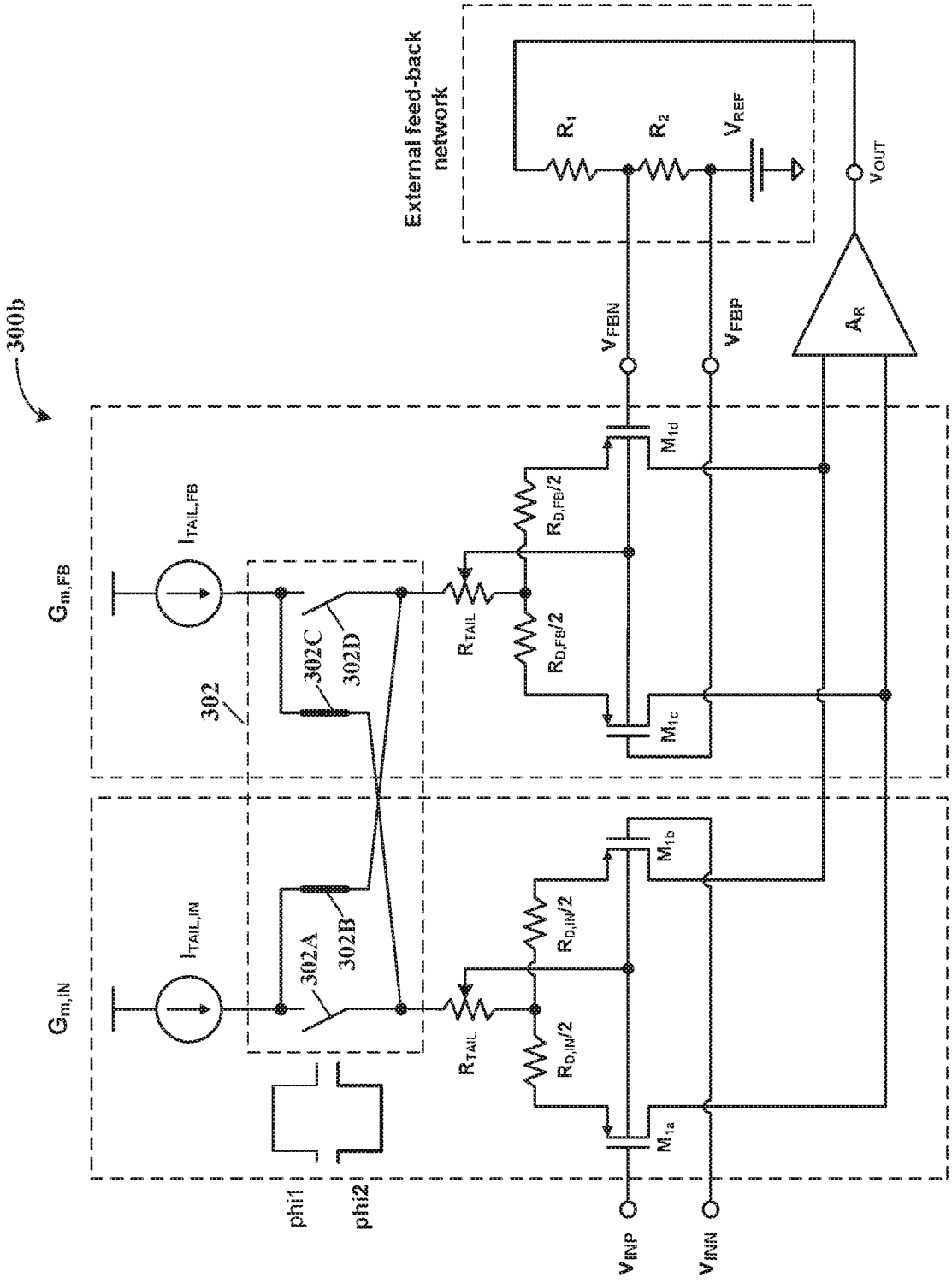

300b
External feed-back network
R1
R2
VREF
VOUT
AR
VFBN
VFBP
Gm,FB
ITAIL,FB
302
302C
302D
RTAIL
RD,FB/2
RD,FB/2
M1d
M1c
Gm,IN
ITAIL,IN
302A
302B
RTAIL
RD,IN/2
RD,IN/2
M1b
M1a
phi1
phi2
VINP
VINN

Figure 3B

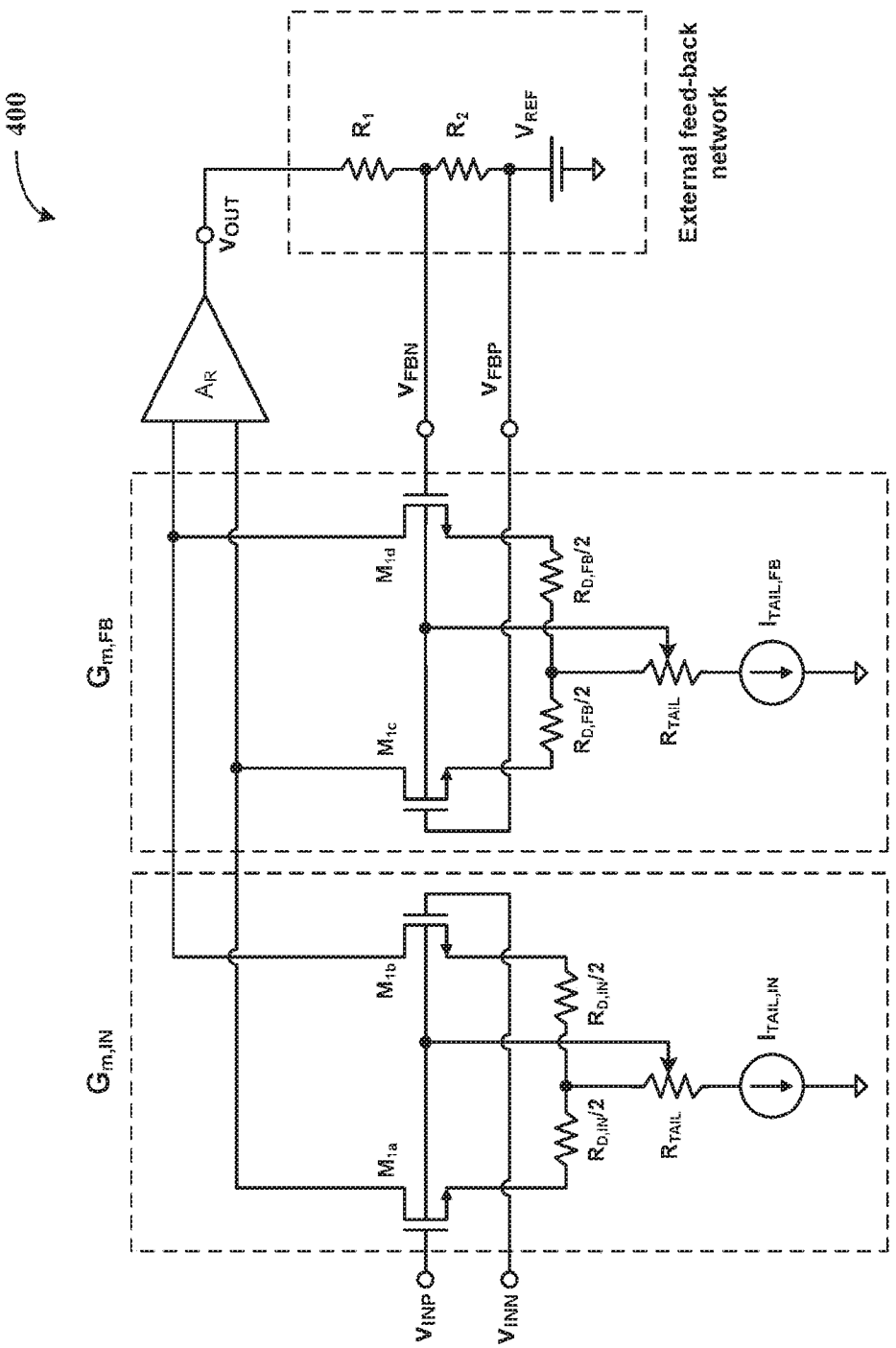

400
External feed-back network
R1
R2
VREF
VOUT
AR
VFBN
VFBP
Gm,FB
M1d
M1c
RD,FB/2
RD,FB/2
RTAIL
ITAIL,FB
Gm,IN
M1b
M1a
RD,IN/2
RD,IN/2
RTAIL
ITAIL,IN
VINP
VINN

Figure 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/029715

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F3/45 H03G1/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JAWORSKI ZBIGNIEW ED - SZCZEPANSKI PAWEL ET AL: "A fully differential OTA with dynamic offset cancellation in 28nm FD-SOI process", PROCEEDINGS OF THE SPIE - SMART STRUCTURES AND MATERIALS 2005: SMART ELECTRONICS, MEMS, BIOMEMS, AND NANOTECHNOLOGYPROCEEDINGS OF THE SPIE, THE INTERNATIONAL SOCIETY FOR OPTICAL ENGINEERING SPIE-INT. SOC. OPT. ENG. USA, 1000 20TH ST. BELLINGHAM WA 98, vol. 10175, 22 December 2016 (2016-12-22), pages 10175091-10175099, XP060080252, ISSN: 0277-786X, DOI: 10.1117/12.2261891 ISBN: 978-1-5106-1533-5 page 10175091, line 9 - page 10175098, line 6; figures 1-11 ----- -/--	1-19

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 July 2018	16/07/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Fedi, Giulio

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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/029715

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 859 095 B2 (ST MICROELECTRONICS PVT LTD [IN]) 22 February 2005 (2005-02-22) column 1, line 7 - column 6, line 13; figures 1-4	1-19
A	US 6 509 795 B1 (IVANOV VADIM V [US]) 21 January 2003 (2003-01-21) column 1, line 5 - column 9, line 12; figures 2-4	1-19
A	US 2010/329157 A1 (XING NIANWEI [US] ET AL) 30 December 2010 (2010-12-30) paragraphs [0002] - [0089]; figures 1-8	1-19

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2018/029715

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6859095 B2	22-02-2005	NONE	
US 6509795 B1	21-01-2003	NONE	
US 2010329157 A1	30-12-2010	US 2010329157 A1	30-12-2010
		WO 2010151270 A1	29-12-2010