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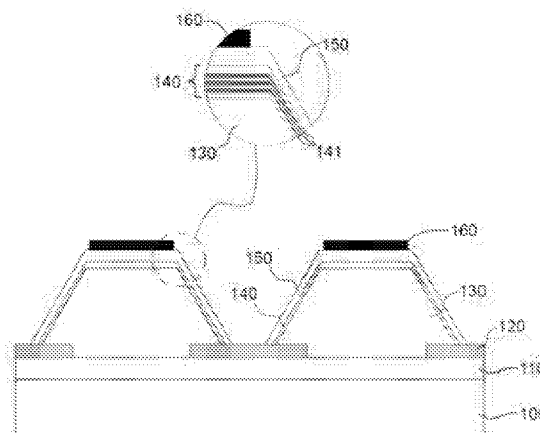


Figure 1b

(57) Abstract: The present invention provides a monolithic LED array precursor comprising: a plurality of LED structures sharing a first semiconductor layer, wherein the first semiconductor layer defines a plane of the LED array precursor, each LED structure comprising: (i) a second semiconductor layer on the first semiconductor layer, having an upper surface portion parallel to the plane of the LED array precursor, the second semiconductor layer having a regular trapezoidal cross-section normal to the upper surface portion, such that the second semiconductor layer has sloped sides; (ii) a third semiconductor layer on the second semiconductor layer, having an upper surface portion parallel to the plane of the LED array precursor, the third semiconductor layer having a regular trapezoidal cross-section normal to the upper surface portion, such that the third semiconductor layer has sloped sides parallel to the sloped sides of the second semiconductor layer; (iii) a fourth semiconductor layer on the third semiconductor layer, having an upper surface portion parallel to the plane of the LED array precursor, the fourth semiconductor layer having a regular trapezoidal cross-section normal to the upper surface portion, such that the fourth semiconductor layer has sloped sides parallel to the sloped sides of the third semiconductor layer; and (iv) a primary electrical contact on the fourth semiconductor layer, wherein the contact is only on the upper surface portion of the fourth semiconductor layer which is parallel to the plane of the LED array precursor; wherein the third semiconductor layer

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comprises a plurality of quantum well sub-layers, the quantum well sub-layers having a greater thickness on a portion parallel to the plane of the LED array precursor and a reduced thickness on a portion which is not parallel to the plane of the LED array precursor.

Monolithic LED array and a precursor thereto

The present disclosure relates to a monolithic LED array, an LED device comprising the monolithic LED array and a method of manufacture thereof. In particular, the present disclosure provides a monolithic LED array having improved light emission.

Micro light emitting diode (LED) arrays may be defined as arrays of LEDs with a size of $100 \times 100 \mu\text{m}^2$ or less. Micro LED arrays are being developed for a number of commercial as well as military applications, such as self-emitting micro-displays and projectors, which may be incorporated into a variety of devices such as wearable displays, head-up displays, camcorders, viewfinders, multisite excitation sources, and pico-projectors.

Group III-nitride-based micro LEDs are inorganic semiconductor LEDs containing GaN and its alloys with InN and AlN in the active light-emitting region. Group III-nitride based micro LEDs are popular as they can be driven at significantly higher current density and emit a higher optical power density than conventional large-area LEDs, especially organic light emitting diode (OLED) in which the light-emitting layer is an organic compound. As a result, higher luminance (brightness), defined as the amount of light emitted per unit area of the light source in a given direction, also measured in candela per square meter (cd/m^2) and commonly referred to as a Nit (nt), makes micro LEDs suitable for applications requiring, or benefiting from, high brightness, e.g., displays in high brightness environments or projection.

Additionally, high luminous efficacy expressed in lumens per watt (lm/W) in group III-nitride micro LEDs, allows lower power usage compared with other light sources and makes micro LEDs particularly suitable for portable devices. Furthermore, owing to the intrinsic material properties of group III-nitrides, micro LEDs can be operated at extreme conditions such as high or low temperatures and humidity thereby providing a performance and reliability advantage in wearable and outdoor applications.

Two main approaches currently exist for the production of inorganic micro LED arrays. In the first approach, individual micro LED devices are produced with techniques similar to those for conventional sized LEDs, these are then assembled as an array by pick and place technique onto a substrate, which may be an active matrix backplane which includes the driving circuitry for individual micro LED addressing. This first approach allows LEDs with different properties, such as different emission wavelengths, that have been fabricated on different growth substrates to be transferred onto the product substrate for the purpose of achieving full colour displays. Additionally, it allows discarding faulty devices before they become part of an array potentially improving the final yield of the array. On the other hand, the resolution (small pitch) and array size (large number of micro LEDs) that are required in a variety of applications pose severe challenges to this approach in terms of pick and place accuracy and transfer time, affecting the reliability of the process and its throughput, respectively.

The second approach uses monolithic integration to fabricate the micro LED array on a single growth substrate, thus allowing a higher integration density, smaller LEDs and smaller pitch (i.e. higher array resolution). This second approach relies on colourisation techniques to achieve full colour displays. The colourisation technology used for micro LEDs depends on the micro LED array pitch.

Conventional phosphor materials for lighting applications are currently only suitable for large pitch and low resolution arrays, and quantum dot-based wavelength converting materials are required for higher resolution applications. Regardless of the used approach, the perimeter of the active region of individual micro LEDs within an array is generally formed by an etching process that removes a portion of the light-emitting active region, thereby electrically isolating individual micro LEDs for the purpose of allowing independent current injection in each micro LED and tuning of the amount of radiative recombination within each micro LED in the array.

A less commonly employed manufacturing process uses selective area growth (SAG) to achieve an electrically isolated portion of active region that can be independently injected with a current without using an etching step as disclosed in

US 7,087,932. In the selective area growth technique, a mask is patterned on a buffer layer. The material in the mask is such that at the growth conditions, no additional material is grown directly on the mask but only inside apertures exposing portions of the surface of the underlying buffer layer.

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Luminance in III-nitride LEDs increases with increasing operating current, yet the luminous efficacy is dependent on the current density (A/cm^2), increasing initially as current density increases, reaching a maximum and then decreasing due to a phenomenon known as “efficiency droop.” Many factors contribute to the luminous efficacy of a LED device, including the ability to internally generate photons, known as internal quantum efficiency (IQE). External quantum efficiency (EQE) is defined as the number of photons emitted in the active region divided by the number of electrons injected. EQE is a function of IQE as well as the light extraction efficiency (LEE) of the LED device. At low current density the efficiency is low due to the strong effect of defects or other processes by which electrons and holes recombine without the generation of light, called non-radiative recombination. As those defects become saturated radiative recombination dominates and efficiency increases. An “efficiency droop” or gradual decrease in efficiency begins as the injection-current density surpasses a characteristic value for the LED device.

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Surface recombination is believed to be a major contributor to non-radiative recombination in micro LEDs. Defects and dangling bonds at the perimeter of the micro LED active region interrupt the atomic lattice and introduce electronic energy levels inside the normally forbidden semiconductor bandgap. This may enhance non radiative recombination by acting as stepping stones for charge carrier transitions between the conduction and valence bands.

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Surface recombination is particularly important in inorganic micro LEDs owing to the large perimeter over surface ratio and the dry etching techniques commonly used to define the perimeter around the active region. A variety of techniques are known to those skilled in the art including surface treatment with wet etchant or high temperature treatments or perimeter coverage with suitable “passivation layers” as

disclosed in US 9,601,659 which aim at mitigating damage and reducing dangling bonds at the perimeter of the active light-emitting area.

However, there remains a need for micro LED arrays and LED array precursors
5 having high integration density, smaller LEDs and smaller pitch whilst avoiding problems associated with non-radiative recombination, particularly surface recombination and a method of producing the same.

It is an object of the present invention to provide an improved LED array precursor
10 which tackles at least one of the problems associated with prior art arrays or, at least, provide a commercially useful alternative thereto.

According to a first aspect the present disclosure provides a method of forming a monolithic LED array precursor, the method comprising:

- 15 (i) providing a substrate having a surface;
(ii) forming a continuous first semiconductor layer on the surface of the substrate;
(iii) selectively masking the first semiconductor layer, by depositing a masking layer, which comprises a plurality of apertures, on the first semiconductor
20 layer;
(iv) growing a second semiconductor layer on unmasked portions of the first semiconductor layer, through the apertures of the masking layer to form a plurality of columns each having a regular trapezoidal cross-section normal to the substrate and a substantially flat upper surface portion;
25 (v) forming a third semiconductor layer covering the second semiconductor layer, wherein the third semiconductor layer comprises one or more quantum well sub-layers and has a substantially flat upper surface portion;
(vi) forming a fourth semiconductor layer covering the third semiconductor layer, whereby the fourth semiconductor layer has a substantially flat upper surface
30 portion;
(vii) forming primary electrical contacts on the substantially flat upper surface portion of the fourth semiconductor layer; and

wherein the first to fourth semiconductor layers comprise Group III-nitrides.

The present invention will now be further described. In the following passages different aspects of the invention are defined in more detail. Each aspect so defined
5 may be combined with any other aspect or aspects unless clearly indicated to the contrary. In particular, any feature indicated as being preferred or advantageous may be combined with any other feature or features indicated as being preferred or advantageous.

10 The present disclosure provides a method for forming monolithic LED array precursors in such a way that electronically isolated LED structures may be produced showing improved light emission properties and reduced non-radiative recombination. The inventors have found that by growth of the specific structures disclosed and the provision of an electrical contact only on a specific area of the
15 LED structures LED array precursors can be formed that provide LED devices having improved properties.

The present invention relates to a method of forming a monolithic LED array precursor. LEDs are well known in the art and refer to light emitting diodes.

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A monolithic array refers to the provision of multiple LED structures formed as a single piece. The array means that the LEDs are intentionally spaced across the monolithic structure and typically form a regular array, such as hexagonally close-packed array or a square packed array of LEDs.

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By the term "precursor" it is noted that the LED array described does not have the necessary opposing electrical contacts for each LED such as to allow the emission of light, nor the associated circuitry. Accordingly, the array described is a precursor to a monolithic LED array which would be formed once the necessary further steps
30 are conducted, such as including a counter electrode and any light-extraction surface, such as may be achieved by removing the substrate.

The method involves a number of numbered steps. It will be appreciated that where possible these steps may be performed simultaneously or concurrently.

5 The first step involves the provision of a substrate having a surface. Suitable substrates include sapphire, SiC and silicon. Other suitable substrates are well known in the art.

The second step involves forming a continuous first semiconductor layer on the surface of the substrate. The first semiconductor layer may act as a buffer layer.
10 The first semiconductor layer and, indeed, the further semiconductor layers, comprise Group III-nitrides. Preferably the Group III-nitrides comprise one of more of AlInGa_N, AlGa_N, InGa_N and Ga_N.

As used herein, any reference to a species by its constituent components includes
15 all available stoichiometries thereof. Thus, for example, AlGa_N includes all alloys thereof, such as Al_xGa_{1-x}N wherein x does not equal 1 or 0. Preferred stoichiometries will vary depending on the function of the specific layer.

The third step involves selectively masking the first semiconductor layer, by
20 depositing a masking layer, which comprises a plurality of apertures, on the first semiconductor layer. Preferably, the masking layer comprises SiO₂ and/or SiN_x. The SiO₂ and/or SiN_x masking layer may be deposited ex-situ with standard deposition techniques such as plasma-enhanced chemical vapour deposition. Alternatively, an in-situ SiN_x masking layer may be deposited in the reaction
25 chamber, suitable reaction chambers, such as MOCVD reactors, are well-known in the art.

Optionally the plurality of apertures form a regularly spaced array. This may resemble any configuration for the close-packing of circles, such as square packing
30 or hexagonal packing.

A preferred way of achieving the third step is by:

(a) depositing a continuous masking layer, and

(b) selectively removing a plurality of portions of said mask layer to provide a plurality of apertures.

5 Optionally selectively removing a plurality of portions of said masking layer includes selectively removing a plurality of corresponding portions of the first semiconductor layer. This means that the second optionally discontinuous layer is then formed within wells of the first semiconductor layer.

10 The fourth step involves growing an optionally discontinuous second semiconductor layer on unmasked portions of the first semiconductor layer, through the apertures of the masking layer to form a plurality of columns each having a regular trapezoidal cross-section normal to the substrate and a substantially flat upper surface portion. The flat upper portion is in a plane parallel to the plane of the substrate surface on
15 which the layers are formed.

By “regular trapezoidal cross-section” it is meant that the columns are narrower at the top than the bottom and that they have a substantially flat upper and lower parallel surfaces, with sloped linear sides. This may result in a frustroconical shape,
20 or more likely a frustropyramidal shaped having 3 or more sides, typically 6 sides. The description of “regular trapezoidal cross-section” refers to the portion of the second semiconductor layer extending above the first semiconductor layer. The very bottom portion of the second semiconductor layer is within apertures defined by the first semiconductor layer, so the bottom portion will typically have a constant
25 cross-section, rather than a tapering one. The tapering sides of the column are referred to herein as sides or facets. Where the second layer is continuous, the trapezoidal cross-section is the discontinuous portion of the second semiconductor layer extending above the continuous planar portion of the second semiconductor layer.

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Preferably the sides of the columns have a substantially consistent angle (α) to a plane parallel to the first semiconductor layer. That is, the angle between the side of

the columns and a plane parallel to the first semiconductor does not change significantly. Preferably the angle α is between 50° and 70°, more preferably it is between 58° and 64°, most preferably about 62°.

- 5 Preferably each of the plurality of columns in the second semiconductor layer are truncated hexagonal pyramids.

The fifth step involves forming an optionally discontinuous third semiconductor layer covering the optionally discontinuous second semiconductor layer, wherein the third
10 semiconductor layer comprises one or more quantum well sub-layers and has a substantially flat upper surface portion.

By “substantially flat upper surface portion” it should be understood to mean the upper portion of the particular semiconductor layers is generally parallel to the first
15 semiconductor layer (i.e. provides a plane parallel to the plane of the substrate).

The inventors have found that the deposition of the material of the third semiconductor layer on the second semiconductor layer occurs with a thick uppermost surface but significantly thinner layers being deposited on the facets.
20 This arises automatically due to the speed of growth in various directions relative to the crystal structure.

The layers being deposited on the inclined planes around the mask apertures are generally thinner compared with the layers being deposited on the c-plane-oriented
25 surface portions. In particular, InGaN multiple quantum wells (MQW) that are deposited between n-type doped and the p-type doped layers in the p-n junction within a LED are thinner in the portions that are deposited in contact with inclined surfaces compared with the portions that are deposited in contact with c-plane-oriented surfaces.

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It is known to those skilled in the art that emission from inclined GaN planes may provide a means of improving efficiency of lighting devices by virtue of the reduced

polarisation field in semipolar planes. Additionally, presence of different MQW thickness at inclined planes compared with flat surface portions may also achieves phosphor-free multi-wavelength emission from a single device for the purpose of colour tuning.

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In contrast to this, one objective of the present invention is to confine light generation to the substantially flat surface region preventing carrier injection and/or diffusion into the inclined planes and potential non-radiative recombination at the perimeter of the active region where the periodic arrangement of atoms in the crystal terminates. The carrier confinement in the top flat region is to be achieved by restricting the formation of an electrical contact region to a portion of the top flat surface away from the inclined planes.

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The thickness of a MQW should be understood to mean the average shortest distance between the upper and lower surfaces of the quantum well sub-layers. The thickness of each of the quantum well sub-layers in a specific portion (such as the c-plane or the inclined facet) are preferably substantially the same. The thickness of the MQW is preferably substantially constant across the specific portion that it is deposited on and therefore, the upper and lower surfaces are substantially parallel.

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Preferably, the thickness of the portions of the MQW oriented along the c-plane are greater than 1nm, greater than 1.5nm, greater than 2nm, greater than 2.5nm. Preferably the thickness of the portion of the MQW oriented along the c-plane are less than 15nm, less than 12nm, less than 8nm, less than 5nm. In a preferred embodiment, the thickness of the portion of the MQW oriented along the c-plane are between 1nm and 15nm, more preferably between 2nm and 12nm, most preferably between 2.5nm and 8nm.

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Preferably, the thickness of the portions of the MQW on inclined facets are greater than 0.05nm, greater than 0.1nm, greater than 0.15nm greater than 0.2nm. Preferably the thickness of the portion of the MQW on inclined facets are less than 5nm, less than 2nm, less than 1nm, less than 0.8nm. In a preferred embodiment,

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the thickness of the portion of the MQW on inclined facets are between 0.1nm and 1nm, more preferably between 0.15nm and 0.6nm, most preferably between 0.2nm and 0.5nm.

- 5 Additionally, the difference in MQW thickness between the portions of the MQW oriented along the c-plane and the portions of the MQW on inclined facets corresponds to a bandgap difference between the two MQW portions that effectively prevents diffusion of carriers from the flat MQW portions into the inclined MQW portions. This is a similar mechanism as the one that occurs around
- 10 threading dislocations in III-nitrides LEDs where injected carriers are confined away from the threading dislocation cores preventing the possibility of non-radiative recombination. Incidentally, the MQW composition in regions being deposited on the facets may also differ from the composition of the MQW in the thick uppermost surface in such a way as carrier confinement in the thick uppermost surface still
- 15 occur. As a result, a uniform and relatively narrow wavelength emission is to be expected.

The inventors have recognised that when the band gap difference effectively prevents diffusion of carriers from the flat MQW portions into the inclined MQW

20 portions. Such confinement of carriers requires a potential barrier of a few multiples of kT (where kT is the Boltzmann constant multiplied by temperature, which is equal to approximately 25.7 meV at room temperature of 298 K). The difference required in MQW thickness between the portions of the MQW oriented along the c-plane and the portions of the MQW on inclined facets so as to achieve a potential barrier of a

25 few multiple of kT varies with the composition of the MQW and can be readily calculated by the skilled person. Preferably, the barrier to confinement of the carriers, which are electrons and/or holes, is greater than $2kT$, greater than $3kT$, greater than $4kT$ and most preferably greater than $5kT$. Preferably, the temperature is room temperature (298 K).

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In a preferred embodiment, the thickness of the portions of the MQW oriented along the c-plane are greater than 2nm, and the thickness of the portions of the MQW on

inclined facets are less than 2nm. In a more preferred embodiment, the thickness of the portions of the MQW oriented along the c-plane are greater than 2.5nm, and the thickness of the portions of the MQW on inclined facets are less than 1.5nm.

- 5 The sixth step involves forming an optionally discontinuous fourth semiconductor layer covering the optionally discontinuous third semiconductor layer, whereby the fourth semiconductor layer has a substantially flat upper surface portion. Again, the deposition of the material of the fourth semiconductor layer on the third semiconductor layer occurs with a thick uppermost surface but much thinner layers
10 being deposited on the facets.

Preferably, the fourth semiconductor layer is doped with magnesium. Optionally, the Mg doping density is higher in a thick uppermost surface but much lower in the layers being deposited on the facets such to further aid the confinement of the carrier injection to the thick uppermost surface of the third semiconductor layer.

- 15 Preferably the second, third, and fourth semiconductor layers are discontinuous. While preferably the masking method of the first aspect produces discontinuous layers, in some embodiments with particularly tight pitch the third, fourth and fifth semiconductor layers may fuse. This forms continuous or partially continuous
20 portions where these layers are shared by a number of LED structures.

The first semiconductor may have a thickness between 100nm and 8um and preferably between 3um and 5um.

- 25 The columns of the second semiconductor layer may have a thickness between 500nm and 4um and preferably between 1um and 2um.

- The substantially flat upper surface portion of the third semiconductor layer may have a thickness between 30nm and 150nm and preferably between 40nm and
30 60nm.

The substantially flat upper surface portion fourth semiconductor layer may have a thickness between 50nm and 300nm and preferably between 100nm and 150nm.

5 The portions of the semiconductor layers not aligned with the apertures in the mask have a thickness of from 0nm up to the minimum value of the respective layer discussed above. While the masked areas are relatively less favourable to growth of subsequent semiconductor layers it may not be completely prevented.

10 The seventh step involves forming primary electrical contacts on the substantially flat upper surface portion of the optionally discontinuous fourth semiconductor layer. Any conventional electrode material can be used and it may be applied by conventional techniques such as thermal evaporation or electron-beam evaporation.

15 Each of the above-described layers may be formed of one or more sub-layers. For example, the first semiconductor layer may be formed of compositionally graded layers of $\text{Al}_x\text{Ga}_{1-x}\text{N}$.

20 Optionally, the first semiconductor layer comprises a sublayer, proximal to the second semiconductor, the sublayer comprising silicon doped GaN. Preferably, the first semiconductor layer is substantially undoped with the exception of the silicon doped sublayer. In one embodiment the first semiconductor layer comprises a plurality of undoped (Al)GaN sublayers layers and a silicon doped sublayer. The silicon doped $\text{Al}_x\text{Ga}_{1-x}\text{N}$ sublayer may have a thickness between 100nm and 1µm
25 and preferably between 300nm and 500nm. Preferably, the Al composition is between $x=0$ and 0.2, more preferably between 0.05 and 0.1. Preferably the doping level is between $1 \times 10^{18} \text{at/cm}^3$ and $1 \times 10^{21} \text{at/cm}^3$, more preferably between $1 \times 10^{20} \text{at/cm}^3$ and $2 \times 10^{20} \text{at/cm}^3$.

30 Preferably, where the first semiconductor layer comprises a silicon doped sublayer, the silicon doped sublayer is partially removed when forming the plurality of apertures so that the second semiconductor layer is formed directly on an undoped

portion of the first semiconductor layer. Advantageously, this structure allows the use of a highly silicon doped layer for beneficial current spreading without reducing material quality since the (Al)GaN:Si sublayer is removed where the second semiconductor is grown.

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All of the above deposition steps can be performed using conventional semiconductor formation systems. The formation of semiconductor layers for LED production is well known in the art, such as MOCVD.

10 As will be appreciated, each of the second semiconductor layer columns provides the base for an individual LED structure formed from the associated layers in the final monolithic LED array precursor.

A further aspect of the invention provides a similar method, but with an alternative
15 approach to forming the second semiconductor layer. All aspects of the first aspect discussed above can be combined freely with this embodiment.

In this further aspect the first semiconductor layer is treated to provide a pattern of amorphous material which is less favoured for subsequent layer growth. This
20 means that the second semiconductor layer preferentially forms on the crystalline untreated regions, resulting in columns. This layer may be continuous or discontinuous, depending on the relative growth achieved in the treated and untreated regions. The trapezoidal cross-section is the discontinuous portion of the second semiconductor layer extending above the continuous planar portion of the
25 second semiconductor layer.

Specifically, this further aspect provides a method of forming a monolithic LED array precursor, the method comprising:

- (i) providing a substrate having a surface;
- 30 (ii) forming a continuous first semiconductor layer on the surface of the substrate;

(iii) selectively treating the first semiconductor layer to form an amorphous surface region, wherein the amorphous surface region defines a plurality of untreated portions of the first semiconductor layer;

5 (iv) growing a second semiconductor layer on the untreated portions of the first semiconductor layer to form a plurality of columns each having a regular trapezoidal cross-section normal to the substrate and a substantially flat upper surface portion;

10 (v) forming a third semiconductor layer covering the second semiconductor layer, wherein the third semiconductor layer comprises one or more quantum well sub-layers and has a substantially flat upper surface portion;

(vi) forming a fourth semiconductor layer covering the third semiconductor layer, whereby the fourth semiconductor layer has a substantially flat upper surface portion; and

15 (vii) forming primary electrical contacts on the substantially flat upper surface portion of the fourth semiconductor layer

wherein the first to fourth semiconductor layers comprise Group III-nitrides.

20 Optionally, the first semiconductor layer comprises a sublayer, proximal to the second semiconductor, the sublayer comprising silicon doped GaN. Preferably, the first semiconductor layer is substantially undoped with the exception of the silicon doped sublayer. That is, preferably the first semiconductor layer comprises a plurality of undoped (Al)GaN sublayers layers and a silicon doped sublayer.

25 Preferably, selectively treating the first semiconductor layer comprises amorphising a surface portion of the first semiconductor layer by ion implantation. Preferably the selective treating comprises a step of lithographic patterning and etching followed by ion implantation. Suitable ions for implantation may be selected from N^+ , H^+ and Ar^+ . Advantageously, lithographic patterning and etching an appropriate masking pattern prevents ion damage to the un-etched regions of the first semiconductor layer.

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Optionally, in the method of the second aspect step (iii) comprises:

(a) depositing a continuous masking layer comprising masking layer material on the continuous first semiconductor layer;

(b) selectively removing masking layer material to provide a plurality of masked regions of the first semiconductor layer;

5 (c) treating the first semiconductor layer with ion implantation to form amorphous material in said layer, except in the masked regions, and

(b) removing the remaining masking layer material and, optionally, removing a plurality of corresponding portions of the first semiconductor layer, to provide the plurality of untreated portions of the first semiconductor layer.

10

Preferably, where the first semiconductor layer comprises a silicon doped sublayer, the silicon doped sublayer is partially removed when forming the plurality of apertures so that the second semiconductor layer is formed directly on an undoped portion of the first semiconductor layer. Advantageously, this structure allows the use of a highly silicon doped layer for beneficial current spreading without reducing material quality since the AlGaIn:Si sublayer is removed where the second semiconductor is grown.

15

Preferably in the method of the second aspect the second, third and fourth semiconductor layers are discontinuous.

20

The following disclosure relates to preferable features which may apply equally to both of the aspects discussed above.

25 Preferably the second semiconductor layer is n-type doped. Preferably, the second semiconductor layer is n-type doped with silicon or germanium, preferably silicon.

Preferably, the third semiconductor layer is undoped.

30 Preferably the fourth semiconductor layer is p-type doped and, preferably the fourth semiconductor layer is doped with magnesium.

Advantageously, the above layer compositions provide LED active regions having good light generating and light emitting properties.

Preferably, the pixel pitch of the monolithic LED precursor is 10 nm or less, even
5 more preferably 8nm or less. The pixel pitch may be from 1nm to 10nm, more preferably from 4nm to 8nm.

Preferably, the width of each LED structure (pixel) is less than 10nm. When the pixels have a truncated hexagonal pyramidal shape, the width of each pixel is the
10 maximum length across the base of the hexagonal pyramid. That is the distance across the base of the hexagonal pyramid from one corner to the opposite corner. Where the layers are continuous, the hexagonal base is the base of the discontinuous portion of the topmost semiconductor layer extending above the continuous planar portion of the second semiconductor layer. Preferably, the width
15 is less than 9nm, less than 8nm, less than 7nm, less than 6nm, less than 5nm. Preferably, the width of each LED structure is between 2nm and 8nm, even more preferably between 3nm and 6nm.

Preferably the first semiconductor layer has a wurtzite crystal structure with a
20 (0001) plane, and the substantially flat upper surface portion of the fourth semiconductor layer is parallel to the (0001) plane of the first semiconductor layer. Equally, each of the flat upper surfaces of the second and third semiconductor layers should be parallel to the (0001) plane of the first semiconductor layer.

25 Preferably the method further comprises removing the substrate to facilitate light extraction from the bottom of the manufactured device (which is flipped in use). Alternative at least a portion of the substrate is removed corresponding to each of the individual LED structures described above, to expose a portion of the first semiconductor layer for light-extraction from the array precursor. Preferably the
30 substrate is entirely removed and optionally a roughened surface layer is adhered to the exposed first semiconductor layer. The substrate, also known as the growth substrate, provides a surface on which the LED array is grown, but generally does

not form part of the final device. Preferably the substrate is substantially completely removed in order to minimise absorption in case of a non-transparent substrate such as Si and to minimise cross talk between LED structures in the array in case of a transparent substrate such as SiC or Sapphire.

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Optionally the substrate is selectively removed to form a plurality of collimating channels, each of the collimating channels aligned with a primary contact formed on the substantially flat upper surface portion of the fourth semiconductor layer.

- 10 Optionally, the method further comprises providing a step of at least partially removing the substrate, and at least partially removing the first semiconductor layer to form a plurality of dome or lens structures corresponding to, and aligned with, each of the plurality of columns of the second semiconductor layer. Preferably, the method comprises completely removing the substrate and partially removing the
- 15 first semiconductor layer to provide a plurality on convex domes distal to the second semiconductor layer. Each of the domes being aligned with one of the plurality of LED structures of the array.

- Advantageously, the dome structures improve light extraction and collimation of the
- 20 LED structures without requiring the addition of further material. Preferably the plurality of dome structures may be coated with a dielectric coating or a clear epoxy layer in order to minimise reflection at the surface of the dome.

- Preferably the method may further comprise a step of providing one or more
- 25 transparent insulating layers followed by a reflective layer on at least the portions of the fourth semiconductor layer distal to the third semiconductor layer which are not provided with the primary electrical contacts. Preferably, the insulating layers comprise SiO₂ and/or SiN_x. Advantageously, such coating layers may improve light extraction from the LED structures by reducing light loss within the array and may
- 30 improve collimation of the extracted light.

Optionally, the method further comprises forming one or more secondary electrical contacts in electrical communication with the primary electrical contacts across the quantum well sub-layers to form a monolithic LED array. By providing the secondary electrical contacts, all features necessary for the LED array to function are provided. That is, applying a potential difference across the primary and secondary contacts will cause the LED structure(s) to produce light.

Preferably the one or more secondary electrical contacts are formed on the first semiconductor layer.

10

The monolithic LED array precursor that is formed preferably comprises at least four LED structures, each LED structure corresponding to a distinct second semiconductor layer portion, the corresponding third semiconductor layer portion formed thereon, the corresponding fourth semiconductor layer portion formed thereon and the corresponding primary electrical contact formed thereon. The LED array precursor is preferably a micro LED array.

15

Preferably the monolithic LED array precursor comprises at least first and second sub-arrays of LED structures, each sub-array capable of emitting light at a different dominant wavelength.

20

In a further aspect the present disclosure provides a monolithic LED array precursor. This is preferably obtainable by one of the methods described in the aspects above. Accordingly, all aspects described in relation to the structures formed in the above methods apply equally to the precursor described herein.

25

In a further aspect the present disclosure provide a monolithic LED array precursor comprising:

a plurality of LED structures sharing a first semiconductor layer, wherein the first semiconductor layer defines a plane of the LED array precursor, each LED structure comprising:

30

(i) a second semiconductor layer on the first semiconductor layer, having an upper surface portion parallel to the plane of the LED array precursor, the second semiconductor layer having a regular trapezoidal cross-section normal to the upper surface portion, such that the second semiconductor layer has sloped sides;

5 (ii) a third semiconductor layer on the second semiconductor layer, having an upper surface portion parallel to the plane of the LED array precursor, the third semiconductor layer having a regular trapezoidal cross-section normal to the upper surface portion, such that the third semiconductor layer has sloped sides parallel to the sloped sides of the second semiconductor layer;

10 (iii) a fourth semiconductor layer on the third semiconductor layer, having an upper surface portion parallel to the plane of the LED array precursor, the fourth semiconductor layer having a regular trapezoidal cross-section normal to the upper surface portion, such that the fourth semiconductor layer has sloped sides parallel to the sloped sides of the third semiconductor layer; and

15 (iv) a primary electrical contact on the fourth semiconductor layer, wherein the contact is only on the upper surface portion of the fourth semiconductor layer which is parallel to the plane of the LED array precursor;

wherein the third semiconductor layer comprises a plurality of quantum well sub-layers, the quantum well sub-layers having a greater thickness on a portion
20 parallel to the plane of the LED array precursor and a reduced thickness on a portion which is not parallel to the plane of the LED array precursor.

Preferably the LED array precursor comprises a mask portion at the interface between the first and second semiconductor layers. The mask portion of the LED
25 precursor may be the same as those discussed in respect to the first aspect above. Alternatively, the LED array precursor may have amorphised portions of the first semiconductor layer produced by ion implantation.

Preferably a spacing of the sloped sides of the third semiconductor layer from the
30 sloped sides of the second semiconductor layer is less than a spacing of the upper surface portion of the third semiconductor layer from the upper surface portion of the second semiconductor layer.

Preferably a spacing of the sloped sides of the fourth semiconductor layer from the sloped sides of the third semiconductor layer is less than a spacing of the upper surface portion of the fourth semiconductor layer from the upper surface portion of the third semiconductor layer.

Optionally the second, third and fourth semiconductor layers are shared between LED structures in the array. This may occur when manufacturing the precursor using the second aspect described above, which has an amorphous base pattern which discourages subsequent overlying growth.

Preferably the plurality of LED structures form a regularly spaced array. Preferably the second-fourth layers of the LED structures are truncated hexagonal pyramids.

Advantageously, the above layer compositions provide LED active regions having good light generating and light extraction properties.

Preferably the first semiconductor layer has a wurtzite crystal structure with a (0001) plane, and the substantially flat upper surface portion of the fourth semiconductor layer is parallel to the (0001) plane of the first semiconductor layer.

Preferably, the LED structures of the LED array precursor comprise a shared light-extraction layer on the first semiconductor layer on a surface distal from the second semiconductor layer. In one embodiment the shared light-extraction layer comprises a plurality of collimating channels, each of the collimating channels aligned with a primary contact. Alternatively, the first semiconductor layer forms a plurality of dome or lens structures corresponding to, and aligned with, the plurality of LED structures on the surface distal from the second semiconductor layer.

In a further aspect the present disclosure provides a monolithic LED array comprising the monolithic LED array precursor described herein and further comprises one or more secondary electrical contacts in electrical communication

with the primary electrical contacts across the quantum well sub-layers. This array is based on the precursor described above and, preferably, as obtained from the methods described herein. Accordingly, all features described in those aspects apply equally to this further aspect.

5

Preferably the monolithic LED array comprises at least four LED structures. The LED array is preferably a micro LED array. Preferably the monolithic LED array comprises at least first and second sub-arrays of LED structures, each sub-array capable of emitting light at a different dominant wave-length. Preferably the light-

10 generating layers in each sub-array emit light at a narrow wavelength bandwidth, preferably in the range between 370nm and 680nm, more preferably between 420nm and 520nm.

15

In a further aspect the present disclosure provides a display device comprising the monolithic LED array disclosed herein. Preferably the method of the present disclosure is suitable for producing the LED array precursors and LED arrays disclosed herein.

20

The invention will now be described in relation to the following non-limiting figures. Further advantages of the disclosure are apparent by reference to the detailed description when considered in conjunction with the figures, which are not to scale so as to more clearly show the details, wherein like reference numbers indicate like elements throughout the several views, and wherein:

25

Figure 1 shows an LED array precursor according to the first aspect in which:

Figure 1a shows a plan view of the LED array precursor.

Figure 1b shows a cross section of the LED array precursor.

30

Figure 2 shows a cross section of a portion of an LED array precursor according to the second aspect.

Figure 3 shows a cross section through an embodiment of an LED array precursor wherein the first semiconductor layer comprises a silicon doped surface layer.

5 Figures 4a-4e show further details of and LED structure of an LED array precursor according to the first aspect.

Figures 5a-5c show simulated light extraction efficiency values and full width at half maximum beam angles in degrees for LEDs of the present disclosure.

10

Figures 6a-6c show a scanning electron microscope (SEM) image and atomic force microscope (AFM) measurements for a micro LED of the present disclosure. In figures 6d and 6e, the light path within a micro LED according to the present invention with and without a convex dome are

15

illustrated.

Figure 7 shows an LED array of the present disclosure.

20 Figure 1a shows a plan view of a portion of an LED array precursor according to the first aspect of the present disclosure. Figure 1b shows a vertical cross section along line S1.

25 The LED array precursor 1 of Figure 1 comprises a growth substrate (100); a first semiconductor layer (110); a masking layer (120); a discontinuous second semiconductor layer comprising a plurality of columns (130); a discontinuous third semiconductor layer (140), comprising a plurality of quantum well sublayers (141); a discontinuous fourth semiconductor layer (150); and primary electrical contacts (160) on the substantially flat upper surface portions of the discontinuous fourth semiconductor layer (150).

30

The regular trapezoidal cross section of the second semiconductor layer (130) can be seen in the cross section. In the embodiment shown the inclined portions of the

third semiconductor layer (140) and fourth semiconductor layer (150) are thinner than the portions parallel to the substantially flat upper surface portions. Similarly, the inclined portions of the quantum well sublayers (141) are thinner than the portions parallel to the substantially flat upper surface portions of the second semiconductor layer (130).

In the plan view of Figure 1b, the hexagonal shape of the columns may be seen as the upper surface of the fourth semiconductor layer (150) with the primary electrical contacts (160) isolated in the middle of each column. The area between the columns is the upper surface of the mask layer (120).

The LED array precursor of Figure 2 comprises a growth substrate (100); a first semiconductor layer (110); an amorphous surface region of the first semiconductor layer (121); a second semiconductor layer comprising a plurality of columns (130); a third semiconductor layer (140), comprising a plurality of quantum well sublayers (not shown); a fourth semiconductor layer (150); and primary electrical contacts (160) on the substantially flat upper surface portions of the discontinuous fourth semiconductor layer (150).

In the embodiment of Figure 2, the second, third, and fourth semiconductor layers (130, 140, 150) are continuous.

Figure 3 shows a cross section of a single LED structure of an LED array precursor of the invention wherein the first semiconductor layer (110) comprises a silicon doped sublayer (190) at the surface proximal the second semiconductor layer (130). Additionally, in forming the mask layer (120) the first semiconductor layer has been partially removed below the aperture in the mask layer so that the second semiconductor layer (130) penetrates into the first semiconductor layer (110) through silicon doped sublayer (190).

Figure 4a shows a single LED structure of an LED array precursor of the first aspect wherein the growth substrate has been completely removed and first

semiconductor layer (110) has been shaped into the form of a dome aligned with the LED structures. In the LED structure of Figure 4b the surface of the dome has been coated with a dielectric coating or clear epoxy layer (115) in order to minimise reflection at the surface of the convex dome. In Figure 4c, the dome has been
5 coated as in Figure 4b and the surface of the columns have been coated with transparent layers of SiO₂ and/or SiN_x and a reflective layer (170). Specifically, the exposed surface of the inclined portions of the fourth semiconductor layer (150) have been coated. Advantageously these features (the dome, the dome coating and the coating of the sides of the columns) improve light extraction and
10 collimation.

The inventors have found that adding a dome-shaped region aligned with the pyramid base enhances the light extraction out of the pyramids as shown in Fig.4a-4c. Advantageously, this complements the collimation effect as obtained by total-
15 internal reflection at the pyramid sidewalls. Preferably, the dome-shaped region has a radius of curvature matching the size of the base of the pyramid. That is, the base of the dome shaped region and the base of the pyramid are preferably about the same size.

Figures 4d and 4e show illustrative light paths within a micro LED according to the present invention. Comparing Figure 4d with Figure 4e, it is clear that the addition of a convex dome aligned with the pyramid base reduces the amount of light that is reflected back inside the micro LED at the light extracting surface (the surface from which light escapes the LED) thereby further improving the light extraction
25 efficiency.

Figures 5a-5c show simulated light extraction efficiency values and full width at half maximum beam angles in degrees for three model LEDs of the present disclosure. Specifically, Figure 5a corresponds to an LED where the sides of the columns are
30 uncoated whereas in Figure 5b the sides are coated with SiO₂ and in Figure 5c the sides have been coated with Ag/Si₃N₄.

Compared with known structures aimed at improving light extraction out of conventional LEDs whereby pyramids are etched on a surface distal from an otherwise planar and unbounded light-generating region, the light generating region in the disclosed invention is completely contained within the pyramid-shaped structure, thereby substantially preventing light propagation sideways (parallel to the LED layers).

Compared to yet another class of already known similar structures where the light-generating region is completely contained within inclined surfaces which are obtained by dry etching with the aim of improving light extraction (see for example US7518149), the inclined facets as obtained with a selective area growth process are superior in view of light extraction as they are smoother compared with surfaces obtained by dry etching thereby promoting total-internal reflection at the inclined sidewalls and collimating a higher percentage of the generated light towards the light-extracting surface which is met at a near-to-normal angle.

Figures 6a shows an SEM image and figure 6b shows AFM measurements of a micro LED according to the present disclosure. Figure 6c is a cross section of the AFM measurement in Figure 6b showing in more detail the topography of the micro LED in correspondence of the sidewalls. The images demonstrate that the method disclosed in the present invention generates smooth micro LED sidewalls.

A more consistently reproducible sidewall inclination, generally with an angle at the base of the pyramid (α in Fig.4a) close to 62° is obtained by virtue of the differential growth rate on different crystallographic planes compared with anisotropic dry etching. This is shown by the AFM cross section of figure 6c.

It is understood by those skilled in the art that whereas the improvement of light extraction as obtained by the presence of inclined sidewalls surrounding the light-generating region is ascribed to the effect of total-internal reflection, the light-extraction enhancement obtained by adding a dome-shaped region arises from a reduction in the total-internal reflection at the light-extracting surface as a larger

portion of the light is already partially collimated by the inclined facets and therefore meets the internal dome surface at a near-to-normal angle. Hence, in consideration of the fact that light extraction from the dome-shaped surface does not rely on total-internal reflection, obtaining the domes by dry etching does not constitute an
5 impairment to the working principle hereby disclosed.

Figure 7 shows a cross section through an LED array of the present disclosure. The LED array of Figure 7 comprises the LED array precursor of Figure 1. The array precursor has been flipped and bonded to a backplane comprising a backplane
10 substrate (200) and backplane contact pads (202). The growth substrate of the LED array precursor has been removed and a roughening layer (112) has been laminated onto the exposed surface of the first semiconductor layer (110). Additionally, secondary electrical contacts (180) have been applied to the first semiconductor layer. The primary and secondary electrical contacts are in electrical
15 contact with each other via the LED structure.

It will be appreciated by the skilled person that the various embodiments discussed above may be combined in a single LED backlight. For example the dome, dome coating 115 and coated sides of the columns (170), as shown in Figure 4, may be
20 combined with the silicon doped sublayer (190) of Figure 3.

Although preferred embodiments of the invention have been described herein in detail, it will be understood by those skilled in the art that variations may be made thereto without departing from the scope of the invention or of the appended claims.

Claims:

1. A monolithic LED array precursor comprising:
a plurality of LED structures sharing a first semiconductor layer, wherein the first semiconductor layer defines a plane of the LED array precursor, each LED structure comprising:
 - (i) a second semiconductor layer on the first semiconductor layer, having an upper surface portion parallel to the plane of the LED array precursor, the second semiconductor layer having a regular trapezoidal cross-section normal to the upper surface portion, such that the second semiconductor layer has sloped sides;
 - (ii) a third semiconductor layer on the second semiconductor layer, having an upper surface portion parallel to the plane of the LED array precursor, the third semiconductor layer having a regular trapezoidal cross-section normal to the upper surface portion, such that the third semiconductor layer has sloped sides parallel to the sloped sides of the second semiconductor layer;
 - (iii) a fourth semiconductor layer on the third semiconductor layer, having an upper surface portion parallel to the plane of the LED array precursor, the fourth semiconductor layer having a regular trapezoidal cross-section normal to the upper surface portion, such that the fourth semiconductor layer has sloped sides parallel to the sloped sides of the third semiconductor layer; and
 - (iv) a primary electrical contact on the fourth semiconductor layer, wherein the contact is only on the upper surface portion of the fourth semiconductor layer which is parallel to the plane of the LED array precursor;wherein the third semiconductor layer comprises a plurality of quantum well sub-layers, the quantum well sub-layers having a greater thickness on a portion parallel to the plane of the LED array precursor and a reduced thickness on a portion which is not parallel to the plane of the LED array precursor.
2. The monolithic LED array precursor of claim 1, wherein a spacing of the sloped sides of the third semiconductor layer from the sloped sides of the second semiconductor layer is less than a spacing of the upper surface portion of the third

semiconductor layer from the upper surface portion of the second semiconductor layer, and/or

wherein a spacing of the sloped sides of the fourth semiconductor layer from the sloped sides of the third semiconductor layer is less than a spacing of the upper surface portion of the fourth semiconductor layer from the upper surface portion of the third semiconductor layer.

3. The monolithic LED array precursor of claim 1 or claim 2, wherein the sloped faces of each layer form a plurality of planar facets.
4. The monolithic LED array precursor of any of claims 1 to 3, wherein the second, third and fourth semiconductor layers are shared between LED structures
5. The monolithic LED array precursor of any of claims 1 to 4, wherein the first semiconductor layer has a wurtzite crystal structure with a (0001) plane, and the substantially flat upper surface portion of the fourth semiconductor layer is parallel to the (0001) plane of the first semiconductor layer
6. The monolithic LED array precursor of any of claims 1 to 5, wherein the first semiconductor layer comprises a plurality of lens structures corresponding to and aligned with the plurality of LED structures.
7. A monolithic LED array comprising the monolithic LED array precursor of any of claims 1 to 6 and further comprising one or more secondary electrical contacts in electrical communication with the primary electrical contacts across the quantum well sub-layers.
8. The monolithic LED array of claim 7, wherein the monolithic LED array comprising at least first and second sub-arrays of LED structures, each sub-array capable of emitting light at a different dominant wave-length.

9. A display device comprising the monolithic LED array according to any of claims 7 or 8.

10. A method of forming a monolithic LED array precursor, the method comprising:

- (i) providing a substrate having a surface;
 - (ii) forming a continuous first semiconductor layer on the surface of the substrate;
 - (iii) selectively masking the first semiconductor layer, by depositing a masking layer, which comprises a plurality of apertures, on the first semiconductor layer;
 - (iv) growing a second semiconductor layer on unmasked portions of the first semiconductor layer, through the apertures of the masking layer to form a plurality of columns each having a regular trapezoidal cross-section normal to the substrate and a substantially flat upper surface portion;
 - (v) forming a third semiconductor layer covering the second semiconductor layer, wherein the third semiconductor layer comprises one or more quantum well sub-layers and has a substantially flat upper surface portion;
 - (vi) forming a fourth semiconductor layer covering the third semiconductor layer, whereby the fourth semiconductor layer has a substantially flat upper surface portion;
 - (vii) forming primary electrical contacts on the substantially flat upper surface portion of the fourth semiconductor layer; and
- wherein the first to fourth semiconductor layers comprise Group III-nitrides.

11. The method according to claim 10, wherein the second, third, and fourth semiconductor layers are discontinuous.

12. The method according to claim 10 or claim 11, wherein step (iii) comprises:

- (a) depositing a continuous masking layer, and
- (b) selectively removing a plurality of portions of said mask layer to provide a plurality of apertures, optionally wherein selectively removing a plurality of portions

of said masking layer includes selectively removing a plurality of corresponding portions of the first semiconductor layer.

13. A method of forming a monolithic LED array precursor, the method comprising:

- (i) providing a substrate having a surface;
 - (ii) forming a continuous first semiconductor layer on the surface of the substrate;
 - (iii) selectively treating the first semiconductor layer to form an amorphous surface pattern, wherein the amorphous surface pattern defines a plurality of untreated portions of the first semiconductor layer;
 - (iv) growing a second semiconductor layer on the untreated portions of the first semiconductor layer to form a plurality of columns each having a regular trapezoidal cross-section normal to the substrate and a substantially flat upper surface portion;
 - (v) forming a third semiconductor layer covering the second semiconductor layer, wherein the third semiconductor layer comprises one or more quantum well sub-layers and has a substantially flat upper surface portion;
 - (vi) forming a fourth semiconductor layer covering the third semiconductor layer, whereby the fourth semiconductor layer has a substantially flat upper surface portion; and
 - (vii) forming primary electrical contacts on the substantially flat upper surface portion of the fourth semiconductor layer
- wherein the first to fourth semiconductor layers comprise Group III-nitrides.

14. A method according to any of claims 10 to 13, wherein the plurality of apertures form a regularly spaced array.

15. A method according to any of claims 10 to 14, wherein the first semiconductor layer has a wurtzite crystal structure with a (0001) plane, and the substantially flat upper surface portion of the fourth semiconductor layer is parallel to the (0001) plane of the first semiconductor layer.

16. A method according to any of claims 10 to 15, the method further comprising forming one or more secondary electrical contacts in electrical communication with the primary electrical contacts across the quantum well sub-layers to form a monolithic LED array, preferably wherein the one or more secondary electrical contacts are formed on the first semiconductor layer.
17. A method according to any of claims 10 to 16, wherein the monolithic LED array precursor comprising at least first and second sub-arrays of LED structures, each sub-array capable of emitting light at a different dominant wavelength.
18. A method according to any of claims 10 to 17, further comprising a step of at least partially removing the substrate, and at least partially removing the first semiconductor layer to form a plurality of dome or lens structures corresponding to and aligned with each of the plurality of columns of the second semiconductor layer.
19. A method according to any of claims 10 to 18, wherein the substrate is selectively removed to form a plurality of collimating channels, each of the collimating channels aligned with a primary contact formed on the substantially flat upper surface portion of the fourth semiconductor layer.
20. A monolithic LED array precursor or LED array obtainable by the method of any of claims 10 to 19.

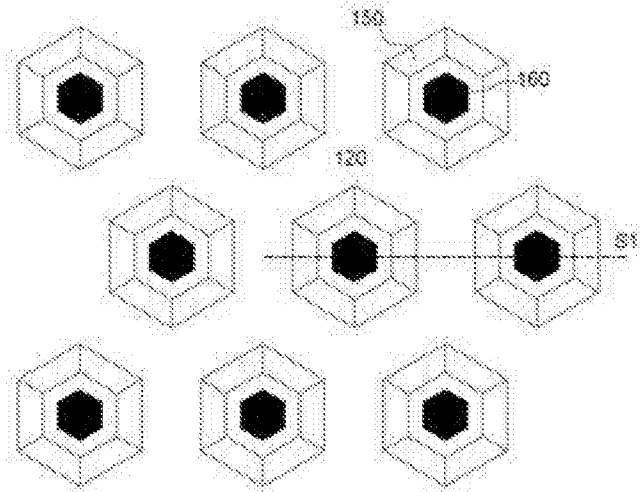


Figure 1a

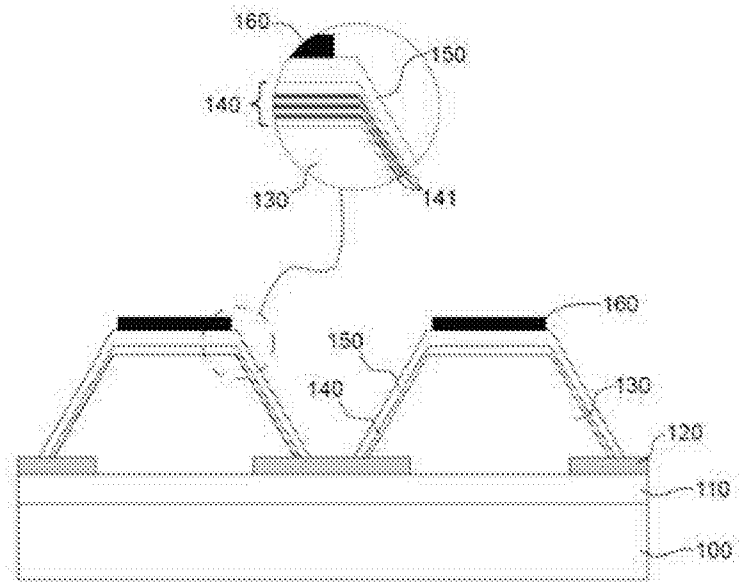


Figure 1b

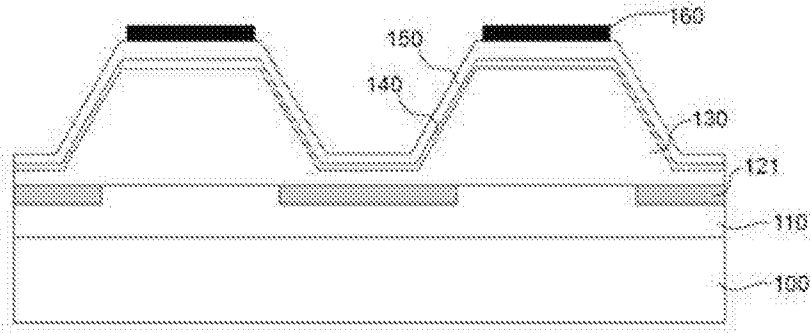


Figure 2

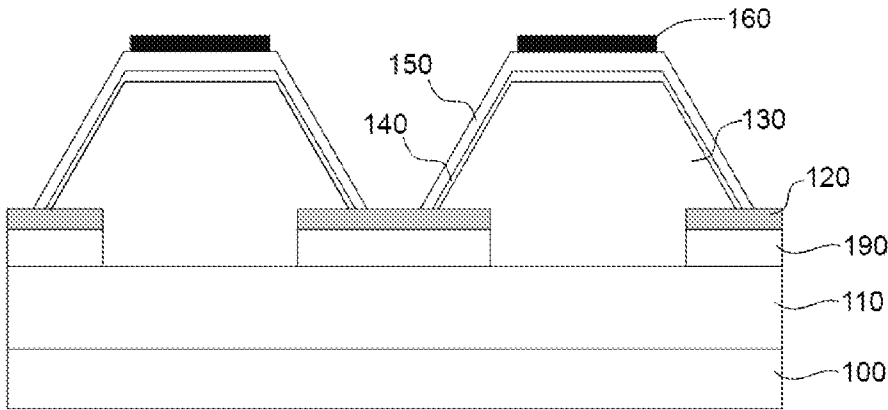


Figure 3

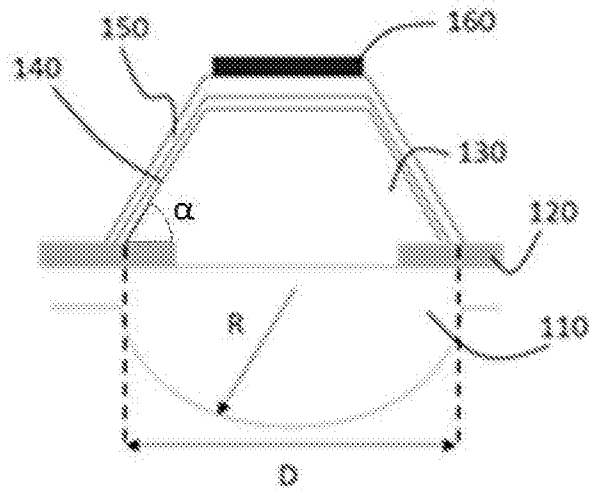


Figure 4a

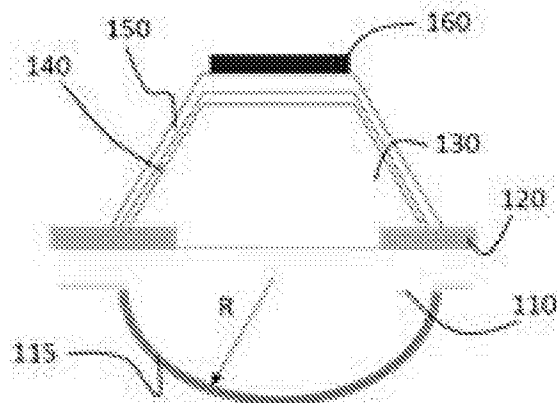


Figure 4b

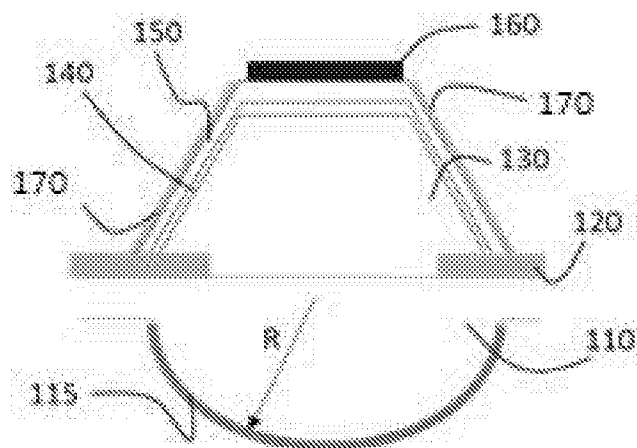


Figure 4c

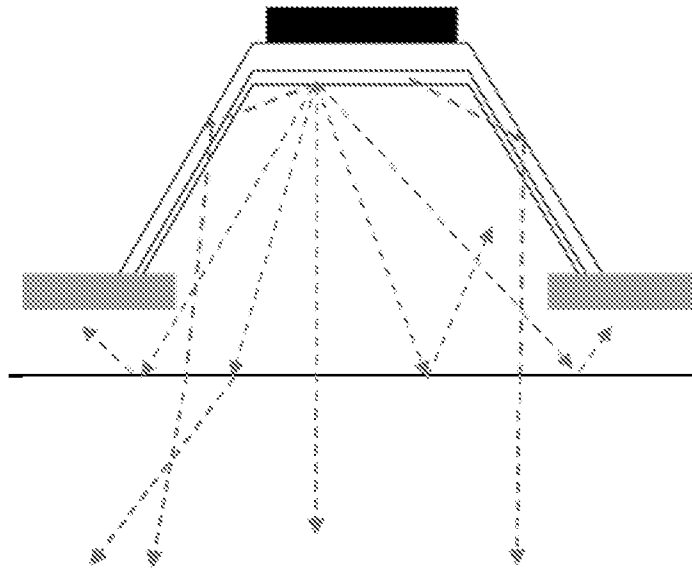


Figure 4d

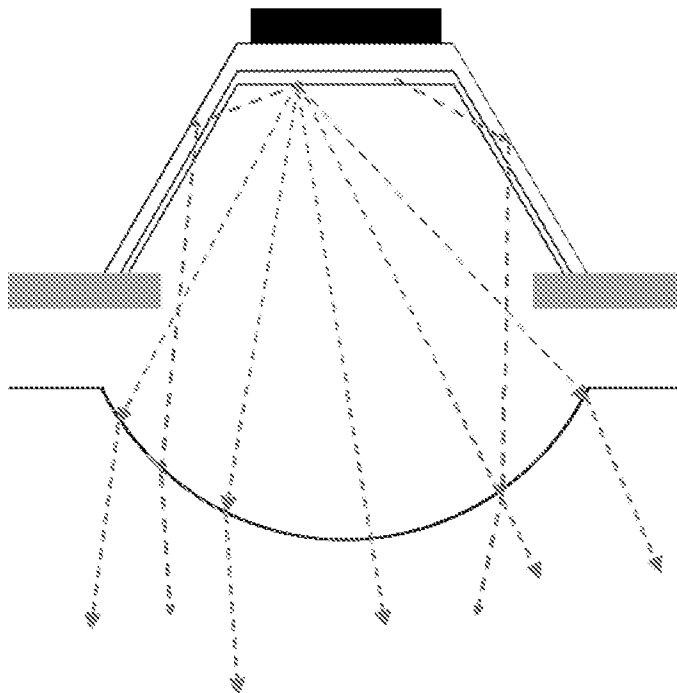


Figure 4e

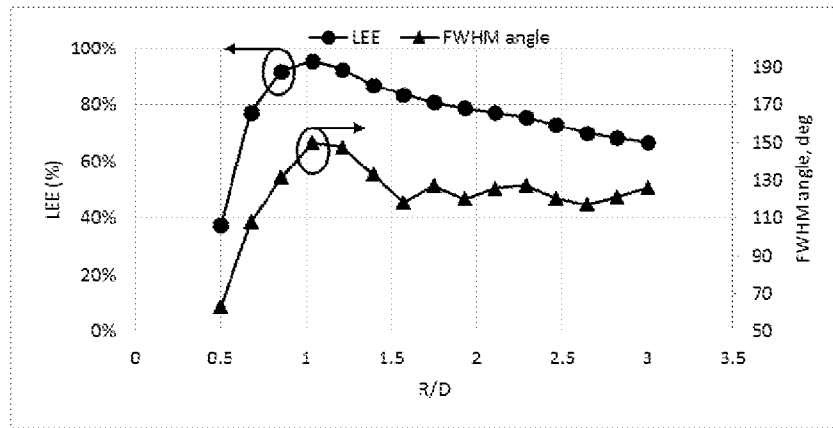


Figure 5a

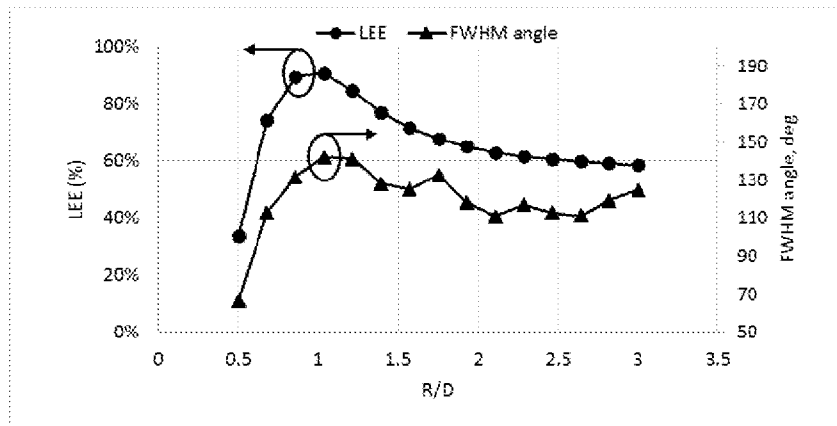


Figure 5b

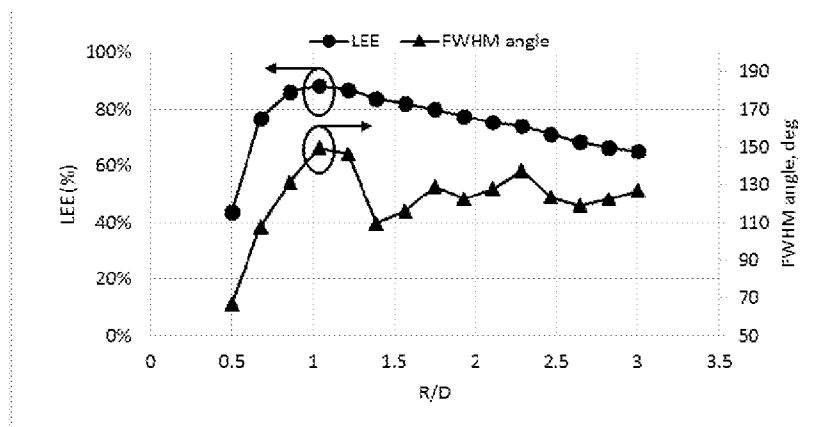


Figure 5c

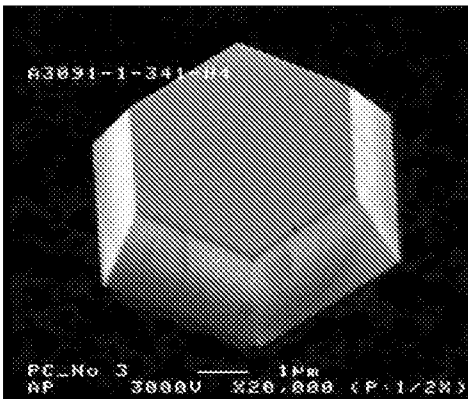


Figure 6a

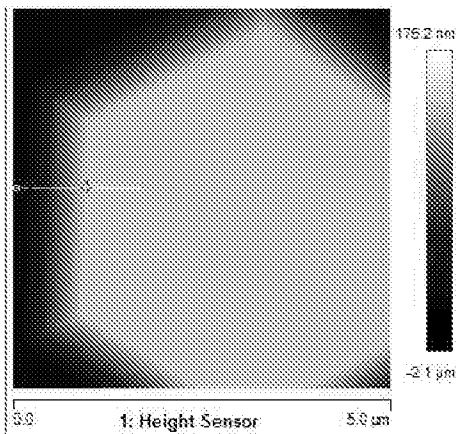


Figure 6b

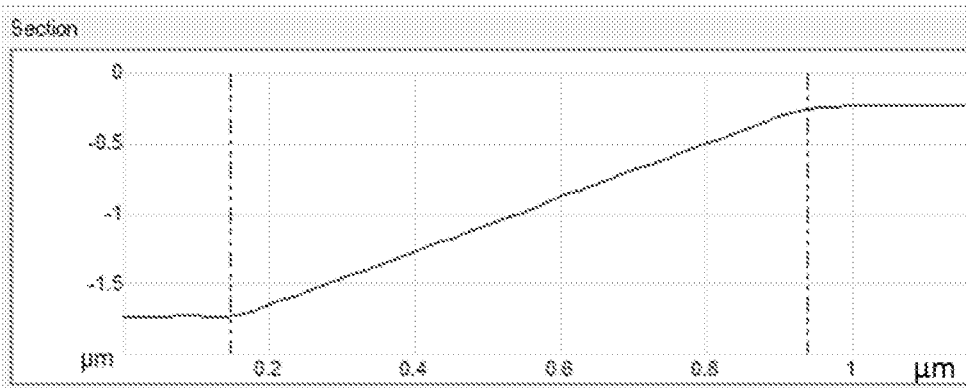


Figure 6c

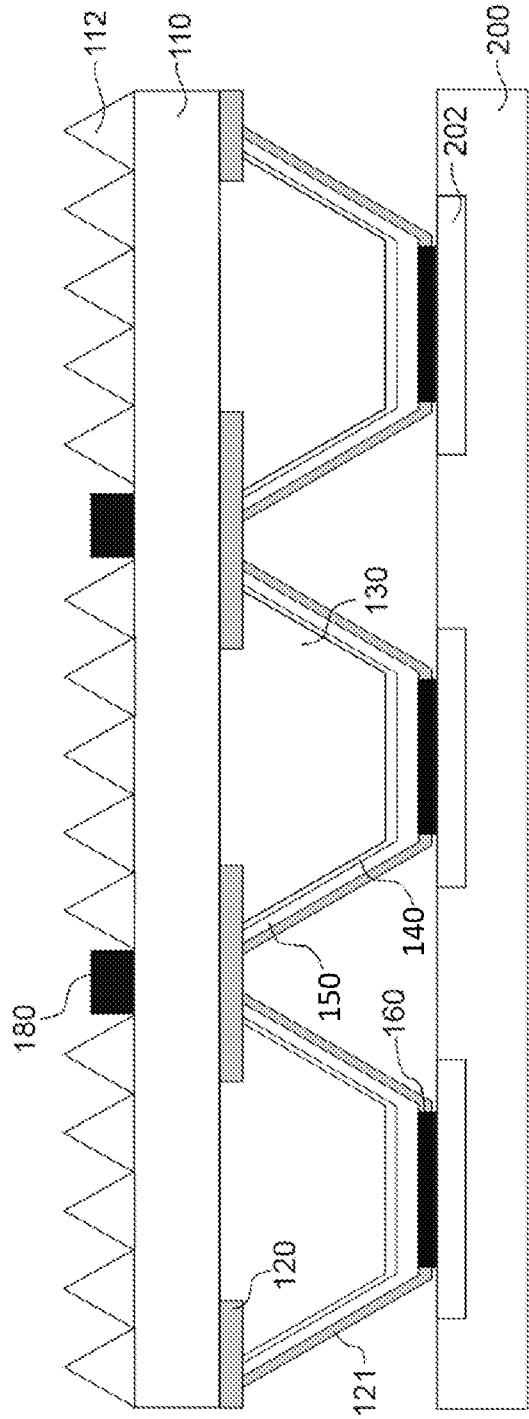


Figure 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2019/051894

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/15 H01L33/24
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MING-LUN LEE ET AL.: "White emission from non-planar InGaN/GaNMQW LEDs grown on GaN template with truncated hexagonal pyramids", OPTICS EXPRESS, vol. 23, no. 7, 233182, 30 March 2015 (2015-03-30), pages A401-A412, XP002794380, DOI: 10.1364/OE.23.00A401	1-5,7,9, 10, 13-16,20
Y	page A407; figures 1,3,5 ----- -/--	6,18,19



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

18 September 2019

Date of mailing of the international search report

30/09/2019

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
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Authorized officer

Pérennès, Frédéric

INTERNATIONAL SEARCH REPORT

International application No

PCT/GB2019/051894

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	G.F. YANG ET AL: "InGaN/GaN multiple quantum wells on selectively grown GaN microfacets and the applications for phosphor-free white light-emitting diodes", REVIEWS IN PHYSICS, vol. 1, 1 November 2016 (2016-11-01), pages 101-119, XP055537837, ISSN: 2405-4283, DOI: 10.1016/j.revip.2016.06.001 figure 14 -----	10-12, 14,15,20
X	WO 2012/059837 A1 (KONINKL PHILIPS ELECTRONICS NV [NL] ET AL.) 10 May 2012 (2012-05-10) page 11, line 29 - page 12, line 10; figures 2,3 page 7, lines 16-21 -----	1,8,10, 12,14, 17,20
Y	US 2013/048940 A1 (SILLS SCOTT E [US] ET AL) 28 February 2013 (2013-02-28) figures 4,5 -----	6,18,19

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2019/051894

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			US 2015171273 A1	18-06-2015
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