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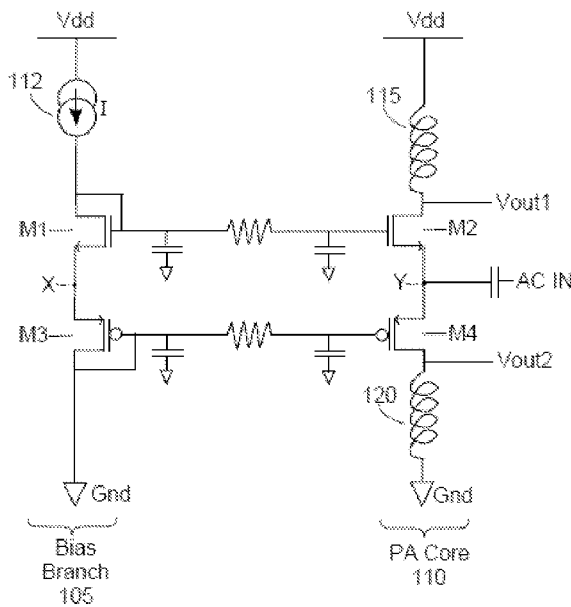
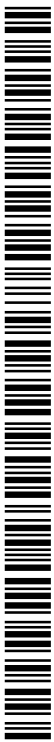


FIG. 1

(57) Abstract: A current mirror includes a bias branch, which includes first and second transistors in series between a voltage source and ground, a voltage divider coupled between the voltage source and ground, an op-amp configured to receive a divided voltage of the voltage divider and a voltage of a node between the first and second transistors, and drive a gate of the second transistor to pull the node to the divided voltage. The current mirror further includes a power amplifier core coupled to the bias branch. The power amplifier core includes first and second drive transistors configured in series between the voltage source and ground. Gates of the first transistor and the first drive transistor are coupled, and gates of the second transistor and the second drive transistor are coupled.



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ACCURATE BIAS TRACKING FOR PROCESS VARIATION AND SUPPLY MODULATION

CROSS REFERENCE TO RELATED APPLICATIONS

5 [0001] This application claims the benefit of, and priority to, U.S. Provisional App. No. 61/426,740, filed December 23, 2010, titled "Accurate Bias Tracking for Process Variation and Supply Modulation," of Leong et al., which is incorporated herein by reference in its entirety for all purposes.

10 FIELD OF USE

[0002] Embodiments of the present invention generally relate to current mirror circuits, and more particularly embodiments of the present invention relate to accurate bias tracking for process variation and supply modulation in current mirror circuits.

15 BACKGROUND

[0003] Unless otherwise indicated herein, the approaches described in this section are not prior art to the claims in this application and are not admitted to be prior art by inclusion in this section.

[0004] A current mirror is a circuit configured to copy a current in one branch of the circuit
20 by controlling the current in another branch of the circuit so that the output current of the circuit may be held constant regardless of whether the load on the circuit changes. The current being copied may be for a DC source or an AC source. Current mirrors find use in a variety of applications, such as power amplification. A amplifier might be configured to receive an RF signal and amplify the power of the RF signal. To accurately reproduce the RF
25 signal with amplified power, the power amplifier may be biased by a current mirror so that the current of the power amplifier remains constant.

[0005] FIG. 1 is a simplified schematic of a known current mirror 100. The current mirror includes a bias branch 105 and a power amplifier (PA) core 110. The bias branch 105 includes transistors M1 and M3 in series and the PA core includes transistors M2 and M4 in
30 series. The transistors of the current mirror are MOSFETs. For convenience, transistors M1, M2, M3, and M4 are sometimes referred to herein as M1, M2, M3, and M4, respectively, without the prefix term "transistor." M1 and M2 are source connected to a power source Vdd with M1 connected to Vdd via a controlled current source 112 and with M2 source connected to Vdd via an inductor 115. The source and gate of M1 are connected to define a gate-source

node, which is connected to the gate of M2 to bias M2. A first Vout1 node is disposed between inductor 115 and the source of M2.

[0006] M3 and M4 are drain connected to ground with M4 drain connected to ground via an inductor 120. The drain and gate of M3 are connected to define a gate-drain node, which is connected to the gate of M4 to bias M4. A second Vout2 node is disposed between inductor 120 and the drain of M4. M1 and M3 act as a voltage divider for Vdd where the node X between M1 and M3 should be $V_{dd}/2$. Similarly M2 and M4 act as a voltage divider where the voltage at node Y should also be $V_{dd}/2$. Node Y is the input node for an AC input into the PA core.

[0007] For accurate current mapping by current mirror 100, the voltage of node X between M1 and M3 should track the voltage of node Y between M2 and M4. However, the voltage of node X can be indeterminate. The indeterminate nature of the voltage at node X makes node Y to be either more or less than $V_{dd}/2$, which effects the current mirroring and thereby effects the linearity range of the PA core.

SUMMARY

[0008] Embodiments of the present invention generally relate to current mirror circuits, and more particularly embodiments of the present invention relate to accurate bias tracking for process variation and supply modulation in current mirror circuits.

[0009] According to one embodiment of the present invention, a current mirror includes a bias branch coupled to a power amplifier core. The bias branch includes first and second transistors configured in series between a voltage source and a ground, and a voltage divider coupled between the voltage source and the ground. The bias branch further includes an op-amp configured to receive as input a divided voltage of the voltage divider and a voltage of a node between the first and second transistors. The op-amp is configured to drive a gate of the second transistor to pull the node to the divided voltage if the voltage at the node raises above the divided voltage or drops below the divided voltage. The power amplifier core includes third and fourth transistors configured in series between the voltage source and the ground. A gate of the first transistor and a gate of the third transistor are coupled. The gate of the second transistor and a gate of the fourth transistor are coupled.

[0010] According to a specific embodiment, the first and second transistors are complimentary to the third and fourth transistors.

[0011] According to another specific embodiment, the divided voltage is a voltage of the voltage source divided by two.

[0012] According to another specific embodiment, the voltage divider includes first, second, and third resistors in series with the first resistor coupled to the voltage source, the third resistor coupled to ground, and the second resistors coupled between the first and the third resistors. First and second source-drain regions of the first transistor are coupled, respectively, to the voltage source and the first source-drain region of the second transistor. A second source-drain region of the second transistor is coupled to ground. The bias branch further includes a second op-amp having a first input coupled to the first source-drain region of the first transistor, a second input coupled to the voltage divider between the first resistor and the second resistor and configured to receive a second divided voltage of the voltage source. The second op-amp further includes output configured to drive a gate of the first transistor to pull the second node to the second divided voltage if a second voltage at the second node raises above the second divided voltage or drops below the second divided voltage.

[0013] According to another specific embodiment, the bias branch further includes a coupling capacitor disposed between the first source-drain region and the gate of the first transistor.

[0014] According to another specific embodiment, the current mirror of further includes a first bias resistor coupled between the gate of the first transistor and the gate of the third transistor, and a second bias resistor coupled between the gate of the second transistor and the gate of the fourth transistor.

[0015] According to another specific embodiment, the current mirror further includes first and second capacitors coupled to opposite ends of the first bias resistors; and third and fourth capacitors coupled to opposite ends of the second bias resistor.

[0016] According to another specific embodiment, the first, second, third, and fourth capacitors are configured to decouple an input node of the current mirror from an output node of the current mirror.

[0017] According to another specific embodiment, a node between the third and fourth transistors is an input node configured to receive an AC signal. A node between the first inductor and the third transistor is a first output node. A node between the second inductor and the fourth transistor is a second output node.

[0018] According to another specific embodiment, the bias branch further includes a controlled-current source coupled between the voltage source and a first source-drain region of the first transistor, and the power core is configured to mirror a current from the controlled-current source provided to the bias branch.

- [0019] According to another specific embodiment, the bias branch further includes a fifth transistor coupled between the controlled-current source and the first source-drain region of the first transistor, and a sixth transistor coupled between the ground and a first source-drain region of the second transistor. The PA core further includes a seventh transistor coupled
5 between the first inductor and a first source-drain region of the third transistor, and an eighth transistor coupled between the ground and a first source-drain region of the fourth transistor. The gates of the fifth and the seventh transistors are coupled to a first bias-voltage source, and the gates of the sixth and eighth transistors are coupled to each other and to a second bias-voltage source.
- 10 [0020] According to another specific embodiment, the fifth, sixth, seventh, and eighth transistors are configured to decouple an input of the cascade mirror from outputs of the cascade mirror.
- [0021] According to another specific embodiment, the current mirror further includes a first resistor coupled between the gate of the fifth transistor and the gate of the seventh transistor,
15 and a second resistor coupled between the gate of the second transistor and the gate of the fourth transistor.
- [0022] According to another specific embodiment, the current mirror further includes first and second capacitors coupled to opposite ends of the first resistor; and third and fourth capacitors coupled to opposite ends of the second resistor.
- 20 [0023] According to another embodiment, a circuit method for controlling node voltages of a current mirror includes comparing a reference voltage with first node voltage at a node between first and second transistors, which form a bias branch of a current mirror, and generating a voltage signal that represents a difference between the reference voltage and the first node voltage. The circuit method further includes applying the voltage signal to a gate
25 of the first transistor to drive the first node voltage to a determinate voltage.
- [0024] According to a specific embodiment, the determinate voltage is the reference voltage.
- [0025] According to another specific embodiment, the method further includes voltage dividing down a supply voltage via a set of resistors to generate the reference voltage.
- 30 [0026] According to another specific embodiment, the method further includes comparing a second reference voltage with second node voltage at a node between the second transistor and a voltage source, and generating a second voltage signal that represents a difference between the second reference voltage and the second node voltage. The method further

includes applying the second voltage signal to a gate of the second transistor to drive the second node voltage to a second determinate voltage.

[0027] According to another specific embodiment, the second determinate voltage is the second reference voltage.

5 [0028] According to another specific embodiment, the method further includes voltage dividing down the supply voltage via the set of resistors to generate the second reference voltage, wherein the first reference voltage is lower than the second reference voltage.

[0029] The following detailed description and accompanying drawings provide a more detailed understanding of the nature and advantages of the present invention.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0030] FIG. 1 is a simplified schematic of a known current mirror;

[0031] FIG. 2 is a simplified schematic of a current mirror according to one embodiment of the present invention;

15 [0032] FIG. 3 is a simplified schematic of a current mirror according to an alternative embodiment of the present invention; and

[0033] FIG. 4 is a simplified schematic of a current mirror according to another alternative embodiment of the present invention.

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DETAILED DESCRIPTION

[0034] Described herein are circuit embodiments for current mirrors and circuit operation methods for the current mirrors where the current mirrors provide substantially accurate bias tracking for process variation and supply modulation. Via accurate bias tracking, the current mirroring and hence the linearity range of the current mirrors are improved. Thereby, a

25 signal received by a current mirror according to embodiments of the present invention may be power amplified relatively accurately and predictably.

[0035] In the following description, for purposes of explanation, numerous examples and specific details are set forth in order to provide a thorough understanding of embodiments of the present invention. Particular embodiments as defined by the claims may include some or

30 all of the features in these examples alone or in combination with other features described below, and may further include modifications and equivalents of the features and concepts described herein.

[0036] Current mirrors are circuits that are configured to copy a current in one branch of the circuit by controlling the current in another branch of the circuit so that the output current

of the circuit may be held constant regardless of whether the load on the circuit changes. FIG. 2 is a simplified schematic of a current mirror 200 according to one embodiment of the present invention. The current mirror includes a bias branch 205 and a power amplifier (PA) core 210. Current mirror 200 may be configured to amplify the power of a received signal 215, such as a radio frequency (RF) signal, and output a power-amplified signal 220.

[0037] According to one embodiment, bias branch 205 includes bias transistors M1 and M3 connected in series and the PA core includes drive transistors M2 and M4 connected in series. M1, M2, M3, and M4 may be MOSFETs. M1 and M2 may be complimentary to M3 and M4. Specifically, M1 and M2 may be pMOS transistors and M3 and M4 may be nMOS transistors. M1 and M2 may be connected via the sources of M1 and M2 to a power source Vdd with the source of M1 connected to Vdd via a controlled current source 225, and with the source of M2 connected to Vdd via an inductor 230. The gates of M1 and M2 may be coupled with M1 configured to bias M2. The gates may be coupled by a bias resistor 235. It will be understood by those of skill in the art that while in one specific configuration of sources and drains is described, the sources and drains of the various transistors may be otherwise arranged according to alternative embodiments of the present invention. Further, other transistor technology may be used in the alternative embodiments. The described alternative embodiments and the equivalents of the described alternative embodiments are to be considered embodiments of the presently described invention. It is noted that specific source and drain configurations of the transistors are described as a matter of convenience to provide a full understanding of specific embodiments.

[0038] According to one embodiment, the source of M3 is coupled to the drain of M1, and the source of M4 is coupled to the drain of M2. The drains of M3 and M4 may be connected to ground. The drain of M4 may be coupled to ground via an inductor 237. The gates of M3 and M4 may be coupled with M3 configured to bias M4. The gates of M3 and M4 may be coupled via a bias resistor 240. A first Vout1 node is disposed between inductor 230 and the source of M2, and a second Vout2 node is disposed between inductor 237 and the drain of M4.

[0039] According to one embodiment, a first op-amp 245 is coupled to a node X where node X is between the drain of M1 and the source of M3. The op-amp is configured to control the voltage of node X so that the voltage at node X is not indeterminate. Providing that the voltage at node X is not indeterminate further provides that the voltage at node X tracks the voltage at a node Y, which is between the drain of M2 and the source of M4. Node

Y is the input of current mirror 200 and may be configured to receive an AC signal so that the PA core may amplify the received AC signal.

[0040] First op-amp 245 is further configured to control the source-gate voltages of M3 and M4 so that the source-gate voltages track. According to a specific embodiment, node X is coupled to a negative input 245a of the first op-amp and an output 245b of the first op-amp is coupled to the gates of M3 and M4. A node W is coupled to a positive input 245c where node W is set at a reference voltage. The reference voltage at node W is set by series resistors R1, R2, and R3, which are disposed in series from Vdd to ground. Resistor R1 may be coupled directly to Vdd and resistor R3 may be coupled directly to ground with resistor R2 coupled between resistors R1 and R3. Resistors R1, R2, and R3 are configured as voltage dividers to set node W and a node T to predetermined reference voltages. According to one embodiment, the reference voltage at node W is set by resistors R1, R2, and R3 and is the reference voltage for the first op-amp. Resistors R1, R2, and R3 may be selected so that the reference voltage at node W is $V_{dd}/2$. Node X will be driven to $V_{dd}/2$ by the first op-amp, which is configured to drive the gate of M3 higher or lower so that M3 may drive node X to the reference voltage at node W (e.g., $V_{dd}/2$) if the voltage at node X drifts above or below the reference voltage at node W. By driving node X to the reference voltage at node W, the voltage at node X will not be indeterminate and the source-gate voltages of M3 and M4 will also be made to track. Driving node X to the known reference voltage at node W results in node Y also being set to the reference voltage at node W (e.g., $V_{dd}/2$), which extends the linearity range of the PA core across the process variation and temperature (PVT) parameters.

[0041] According to another embodiment of the present invention, a second op-amp 250 is coupled to a node V, the node T, and the gates of M1 and M2. A positive input 250a of the second op-amp is coupled to node V where node V is disposed between controlled current source 225 and the source of M1. A negative input 250b of the second op-amp is coupled to node T, and an output 250c of the second op-amp is coupled to the gates of M1 and M2.

[0042] The voltage of node T is set by resistors R1, R2, and R3, which are serially coupled between Vdd and ground. R1, R2, and R3 operate as a voltage divider to set the voltage of node T. The voltage at node T is the reference voltage for the second op-amp.

[0043] Node V will be driven to the predetermined reference voltage at node T by the second op-amp, which is configured to drive the gate of M1 higher or lower so that M1 may drive node V to the predetermined reference voltage if the voltage at node V drifts above or below the reference voltage at node T. By driving node V to the reference voltage at node T, the voltage at node V will not be indeterminate and the source-gate voltages of M1 and M2

will be made to track. Also, by driving node V to the voltage at node T, the predetermined voltage at node V will be substantially close to the voltage at node S where node S is between inductor 230 and the source of M2. For example, the predetermined voltage at node V may be within approximately 3 percent of the voltage at node S where the voltage at node S is V_{dd}. The voltage at node V is set to a substantial maximum voltage via controlled-current source 225 being in the saturation region across the PVT parameters. With the voltage of node V substantially close to the voltage at node S, the current from controlled-current source 225 will be substantially accurately mirrored in the PA core.

[0044] With the voltages at node V and node X set at predetermined reference voltages, not only are the nodal voltages controlled, but the source-drain voltage drop across M1 and M3 are deterministic. Similarly, with the voltages at node S and node Y set to track the voltages at node V and node X respectively, the source-drain voltages across M2 and M4 are deterministic. Controlling the voltages at the various nodes V, S, X, and Y, and the voltage drops across the M1, M2, M3, and M4 provides that the current tracking of current mirror is substantially improved and the linearity range of the PA core is substantially improved across the PVT parameters.

[0045] According to one embodiment, the resistances of the resistors R1, R2, and R3 are substantially fixed values. It is noted that if V_{dd} shifts up or down, the voltages at node V and node X will track the rise and fall of V_{dd}. For example, the voltage of node X will remain substantially at V_{dd}/2 regardless of whether V_{dd} at the source shifts up or down.

[0046] FIG. 3 is a simplified schematic of a current mirror 300 according to an alternative embodiment of the present invention. The same numbering scheme used above with respect to current mirror 200 is used for identifying substantially similar elements of current mirror 300. Current mirror 300 is substantially similar to current mirror 200 but differs in that current mirror 300 includes a coupling capacitor 305 disposed across the source and the gate of M1. Current mirror 300 may further include capacitors 310 and 315 disposed on opposite sides of bias resistor 235. A first capacitor node of capacitor 310 is coupled to a first side of bias resistor 235 and to the gate of M1. A second capacitor node of capacitor 310 is coupled to ground. A first capacitor node of capacitor 315 is coupled to a second side of bias resistor 235 and to the gate of M2. A second capacitor node of capacitor 315 is coupled to ground. The source and gate of M1 may also be coupled by a coupling capacitor 440.

[0047] Current mirror 300 may further include capacitors 320 and 325 disposed on opposite sides of bias resistor 242. A first capacitor node of capacitor 320 is coupled to a first side of bias resistor 240 and to the gate of M3. A second capacitor node of capacitor 320

is coupled to ground. A first capacitor node of capacitor 325 is coupled to a second side of bias resistor 240 and to the gate of M4. A second capacitor node of capacitor 325 is coupled to ground. Capacitors 310, 315, 320, and 325 are configured to isolate an AC signal received at the input at node Y from coupling to the bias branch.

5 [0048] FIG. 4 is a simplified schematic of a current mirror 400 according to another alternative embodiment of the present invention. Current mirror 400 is substantially similar to current mirror 200 and current mirror 300 but differs in that current mirror 400 includes cascade transistors M1b and M2b coupled between the bias branch and the PA core. Current mirror 400 also includes cascade transistors M3b and M4b coupled between the bias branch
10 and the PA core. M1b and M2b may be pMOS transistors, and M3b and M4b may be nMOS transistors. M1b may be disposed in series with M1 and may have a source coupled to controlled-current source 225 and a drain coupled to the source of M1. M2b may be disposed in series with M2 and may have a source coupled to inductor 230 and a drain coupled to the source of M2. The gates of M1b and M2b may be coupled via a biasing resistor 405.
15 Capacitors 410 and 415 may be coupled to the gates of M1b and M2b, and to biasing resistor 405 substantially similarly to the coupling of capacitors 310 and 315 to M1, M2, and biasing resistor 235 as described above with respect to current mirror 300. As described above with respect to current mirror 100, specific configurations of drains and sources of the various transistors are described for convenience. It will be understood by those of skill in the art that
20 specific source and drain configurations may be alternatively arranged according to alternative embodiments of the present invention based, for example, on other transistor technology used.

[0049] M3b may be disposed in series with M3 and may have a drain coupled to ground and a source coupled to the drain of M3. M4b may be disposed in series with M4 and may
25 have a drain coupled to ground via inductor 235 and a source coupled to the drain of M4. The gates of M3b and M4b may be coupled via a biasing resistor 420. Capacitors 425 and 430 may be coupled to the gates of M3b and M4b, and to biasing resistor 420 substantially similarly to the coupling of capacitors 320 and 325 to M3, M4, and biasing resistor 240 as described above with respect to current mirror 300. The first output Vout1 of current mirror
30 400 is between the source of M2b and inductor 230, and the second output Vout2 of current mirror 400 is between the drain of M4b and inductor 235. The gate of M1b may be coupled to a first bias-voltage source configured to provide a first bias voltage Vbias1 to the gate of M1b, and the gate of M3b may be coupled to a second bias-voltage source configured to

provide a second bias voltage V_{bias2} to the gate of M3b. V_{bias1} and V_{bias2} provide that transistors M1b, M2b, M3b, and M4b turn on relatively strongly.

[0050] According to one embodiment, M1b and M2b arranged in the described cascade configuration are configured to isolate an AC signal received at the input (node Y) from the first output V_{out1} . M3b and M4b arranged in the described cascade configuration are configured to isolate an AC signal received at the input (node Y) from the second output V_{out2} . The cascade pair of M1b and M2b further force the source voltage of M1 and M2 to track, and the cascade pair of M3b and M4b further force the drain voltages of M3 and M4 to track by further controlling the voltages at nodes X and V. Improved tracking of voltages between the bias branch and the PA core provides further improved tracking of the current from the controlled-current to in the PA core and further improvement of the linearity range of the PA core across the PVT parameters.

[0051] The above description illustrates various embodiments of the present invention along with examples of how aspects of the present invention may be implemented. The above examples and embodiments should not be deemed to be the only embodiments, and are presented to illustrate the flexibility and advantages of the present invention as defined by the following claims. Based on the above disclosure and the following claims, other arrangements, embodiments, implementations, and equivalents may be employed without departing from the scope of the invention as defined by the claims.

WHAT IS CLAIMED IS:

- 1 1. A current mirror comprising:
2 a bias branch including:
3 first and second transistors configured in series between a voltage
4 source and a ground; and
5 a voltage divider coupled between the voltage source and the ground;
6 and
7 an op-amp configured to receive as input a divided voltage of the
8 voltage divider and a voltage of a node between the first and second
9 transistors, and drive a gate of the second transistor to pull the node to the
10 divided voltage;
11 a power amplifier core coupled to the bias branch including:
12 third and fourth transistors configured in series between the voltage source and
13 the ground, wherein:
14 a gate of the first transistor and a gate of the third transistor are coupled, and
15 the gate of the second transistor and a gate of the fourth transistor are coupled.
- 1 2. The current mirror of claim 1, wherein the first and second transistors
2 are complimentary to the third and fourth transistors.
- 1 3. The current mirror of claim 1, wherein the divided voltage is a voltage
2 of the voltage source divided by two.
- 1 4. The current mirror of claim 1, wherein:
2 the voltage divider includes first, second, and third resistors in series with the first
3 resistor coupled to the voltage source, the third resistor coupled to ground, and the second
4 resistor coupled between the first and the third resistors,
5 first and second source-drain regions of the first transistor are coupled, respectively,
6 to the voltage source and the first source-drain region of the second transistor,
7 a second source-drain regions of the second transistor is coupled to ground, and
8 the branch further includes:
9 a second op-amp having a first input coupled to the first source-drain region of
10 the first transistor, a second input coupled to the voltage divider between the first resistor and
11 the second resistor and configured to receive a second divided voltage of the voltage source,
12 and an output configured to drive a gate of the first transistor to pull the second node to the
13 second divided voltage.

1 5. The current mirror of claim 5, wherein the bias branch further includes
2 a coupling capacitor disposed between the first source-drain region and the gate of the first
3 transistor.

1 6. The current mirror of claim 5 further comprising:
2 a first resistor coupled between the gate of the first transistor and the gate of the third
3 transistor, and
4 a second resistor coupled between the gate of the second transistor and the gate of the
5 fourth transistor.

1 7. The current mirror of claim 7, further comprising:
2 first and second capacitors coupled to opposite ends of the first resistors; and
3 third and fourth capacitors coupled to opposite ends of the second resistor.

1 8. The current mirror of claim 8, wherein the first, second, third, and
2 fourth capacitors are configured to decouple an input node of the current mirror from an
3 output node of the current mirror.

1 9. The current mirror of claim 1, wherein:
2 a node between the third and fourth transistors is an input node configured to
3 receive an AC signal,
4 a node between the first inductor and the third transistor is a first output node,
5 and
6 a node between the second inductor and the fourth transistor is a second output
7 node.

1 10. The current mirror of claim 1, wherein the bias branch further includes
2 a controlled-current source coupled between the voltage source and a first source-drain region
3 of the first transistor, and the power core is configured to mirror a current from the
4 controlled-current source provided to the bias branch.

1 11. The current mirror of claim 10, wherein:
2 the bias branch further includes:
3 a fifth transistor coupled between the controlled-current source and the first
4 source-drain region of the first transistor, and
5 a sixth transistor coupled between the ground and a first source-drain region of
6 the second transistor; and
7 the PA core further includes:
8 a seventh transistor coupled between the first inductor and a first source-drain
9 region of the third transistor, and

10 a eighth transistor coupled between the ground and a first source-drain region
11 of the fourth transistor, and wherein
12 gates of the fifth and seventh transistors are coupled to a first bias-voltage
13 source, and
14 gates of the sixth and eighth transistors are coupled to each other and to a
15 second bias-voltage source.

1 12. The current mirror of claim 11, wherein the fifth, sixth, seventh, and
2 eighth transistors are configured to decouple an input of the cascade mirror from outputs of
3 the cascade mirror.

1 13. The current mirror of claim 11, further comprising:
2 a first resistor coupled between the gate of the first cascade transistor and the gate of
3 the seventh transistor, and
4 a second resistor coupled between the gate of the second transistor and the gate of the
5 fourth transistor.

1 14. The current mirror of claim 13, further comprising
2 first and second capacitors coupled to opposite ends of the first resistor; and
3 third and fourth capacitors coupled to opposite ends of the second resistor.

1 15. A circuit method for controlling node voltages of a current mirror
2 comprising:
3 comparing a reference voltage with first node voltage at a node between first
4 and second transistors, which form a bias branch of a current mirror;
5 generating a voltage signal that represents a difference between the reference
6 voltage and the first node voltage; and
7 applying the voltage signal to a gate of the first transistor to drive the first
8 node voltage to a determinate voltage.

1 16. The circuit method of claim 15, wherein the determinate voltage is the
2 reference voltage.

1 17. The circuit method of claim 16, further comprising voltage dividing
2 down a supply voltage via a set of resistors to generate the reference voltage.

1 18. The circuit method of claim 17, further comprising:
2 comparing a second reference voltage with second node voltage at a node
3 between the second transistor and a voltage source;
4 generating a second voltage signal that represents a difference between the
5 second reference voltage and the second node voltage; and

6 applying the second voltage signal to a gate of the second transistor to drive
7 the second node voltage to a second determinate voltage.

1 19. The circuit method of claim 18, wherein the second determinate
2 voltage is the second reference voltage.

1 20. The circuit method of claim 16, further comprising voltage dividing
2 down the supply voltage via the set of resistors to generate the second reference voltage,
3 wherein the first reference voltage is lower than the second reference voltage.

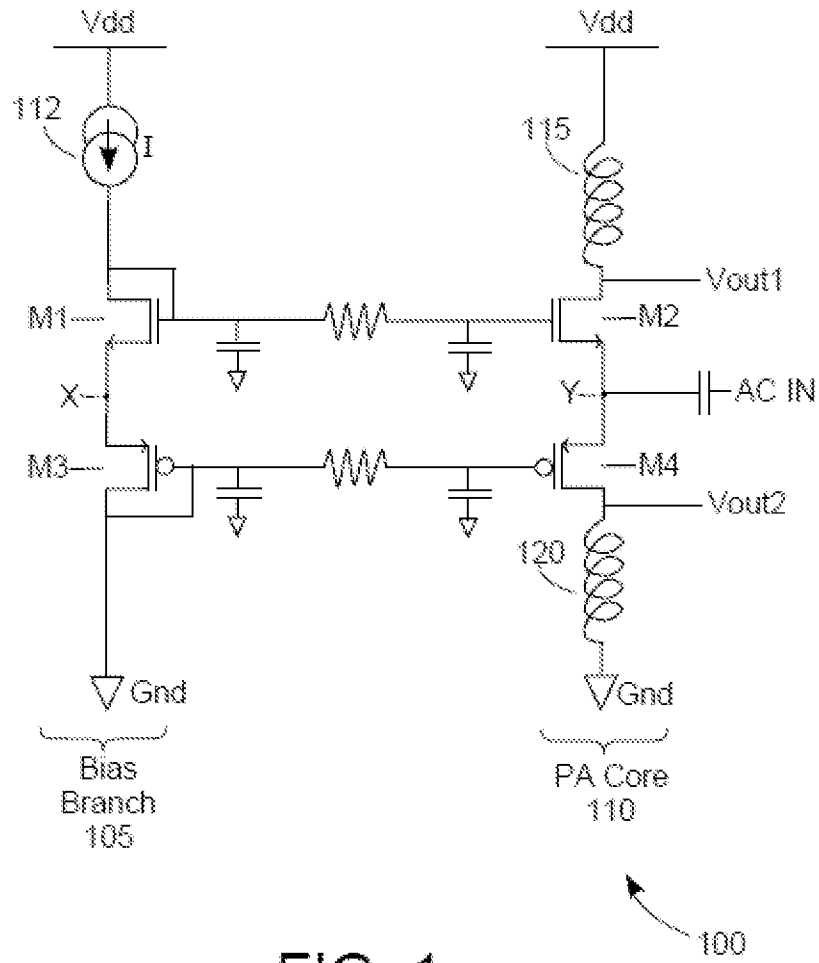


FIG. 1

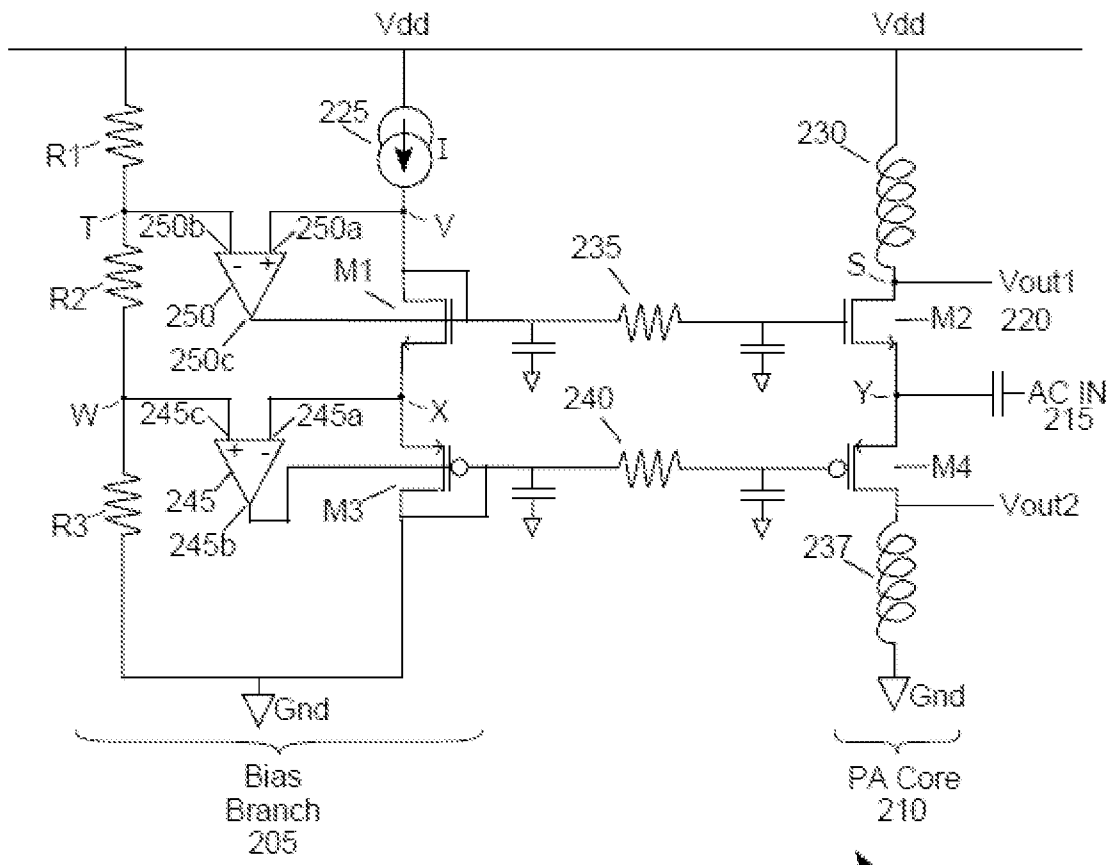


FIG. 2

200

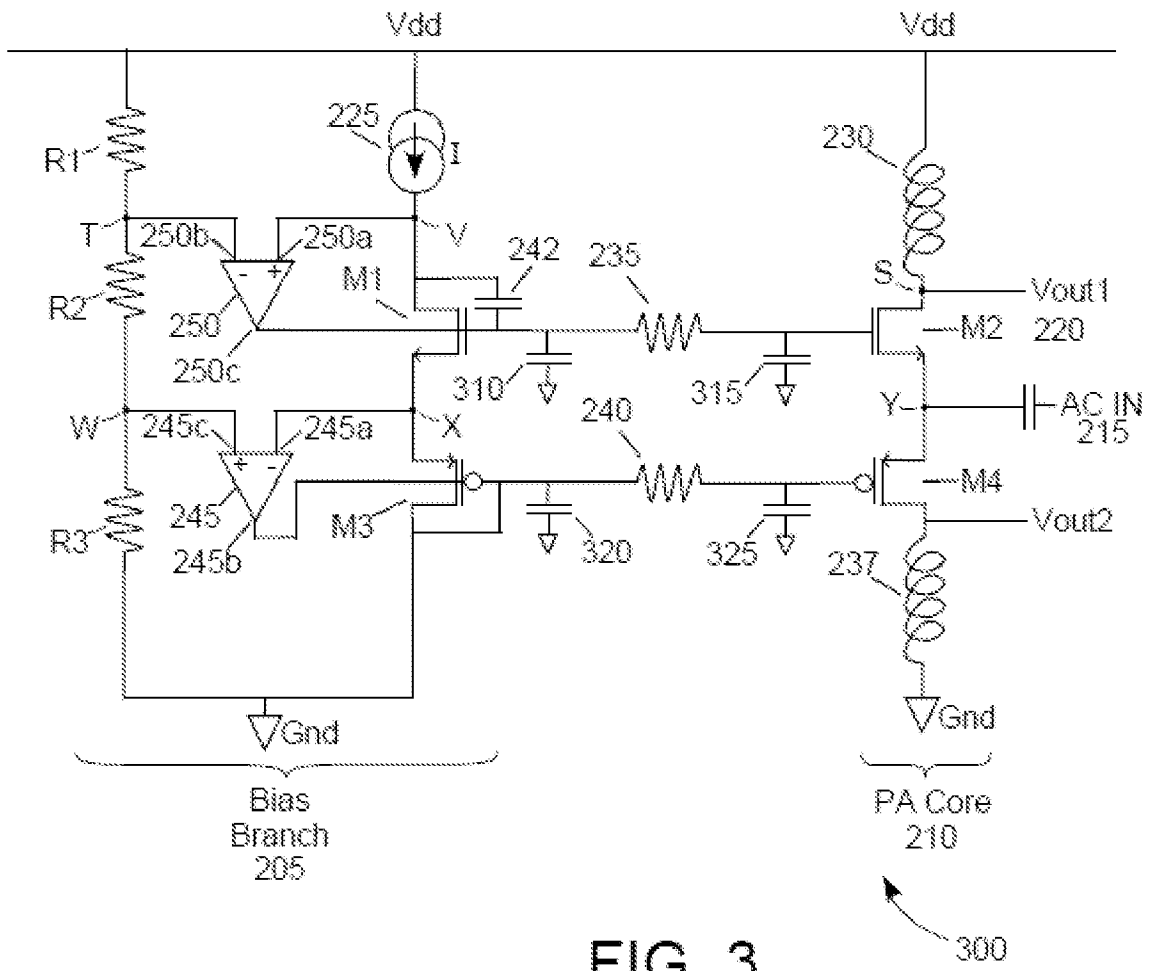


FIG. 3

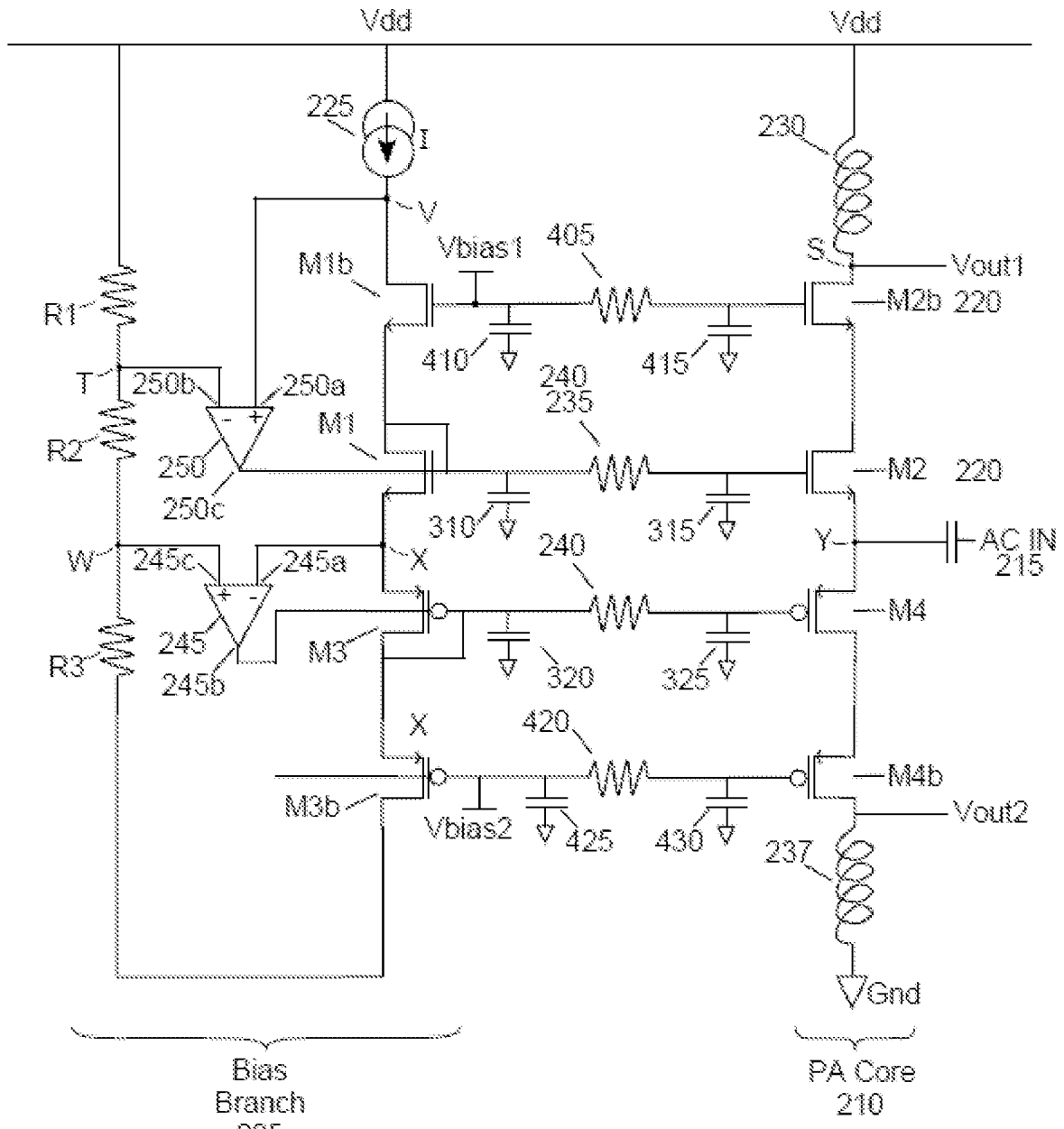


FIG. 4

400