(19) World Intellectual Property **Organization**

International Bureau





(43) International Publication Date 4 November 2004 (04.11.2004)

PCT

(10) International Publication Number WO 2004/095212 A3

(51) International Patent Classification⁷:

G06F 12/10

(21) International Application Number:

PCT/US2004/005736

(22) International Filing Date: 26 February 2004 (26.02.2004)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

10/396,675

25 March 2003 (25.03.2003) US

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- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM,ZW.

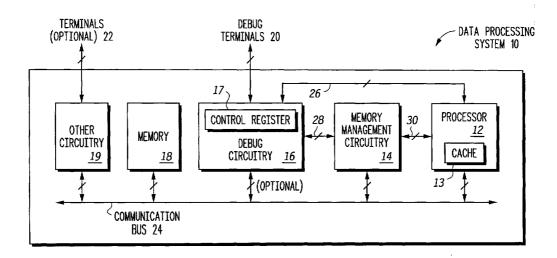
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments
- (88) Date of publication of the international search report: 24 February 2005

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: MEMORY MANAGEMENT IN A DATA PROCESSING SYSTEM



(57) Abstract: A data processing (10) includes memory management circuitry (14) which allows additional control over the physical address (83) and over the address attributes (84) which are provided for use by data processing system (10). One use of this additional control over the physical address (83) and over the address attributes (84) is to avoid address translation failure and unintended modification of cache (13) and memory (18) system state during debugging.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US04/05736

A. CLASSIFICATION OF SUBJECT MATTER IPC(7) : G06F 12/10						
	US CL: 711/202 According to International Patent Classification (IPC) or to both national classification and IPC					
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B. FIELI	OS SEARCHED					
Minimum documentation searched (classification system followed by classification symbols) U.S.: 711/202 711/118,125,138,163,201,203-209;714/24,29-34,38-39,46,718,724,734						
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched						
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) Please See Continuation Sheet						
C. DOC	C. DOCUMENTS CONSIDERED TO BE RELEVANT					
Category *	Citation of document, with indication, where ap	propriate, of the relevant passages	Relevant to claim No.			
X 	US 6,499,123 B1 (McFarland et al.) 24 December 20	02, see entire document.	1-5, 8-12, 14-28, 30 and 32-36			
Y			12 21 27 20 and 42			
Y,E	US 6,748,558 B1 (Gonzales et al.) 08 June 2004, see	13,31,37-29 and 43 13,31,37-39 and 43				
A	US 5,900,014 A (Bennett) 04 May 1999.		1-45			
A	US 6,446,221 B1 (Jaggar et al.) 03 September 2002.		1-45			
A	US 5,530,804 A (Edgington et al.) 25 June 1996.		1-45			
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Date of the actual completion of the international search 21 September 2004 (21.09.2004)		Date of mailing of the international search report 14 DEC 2004				
	ailing address of the ISA/US		- 11 1			
Mail Stop PCT, Attn: ISA/US Commissioner for Patents		Authorized officer VINCENT TRANS Janua R. Matthews				
Ale	D. Box 1450 exandria, Virginia 22313-1450 o. (703) 305-3230	Telephone No. (571) 272-3613				

Form PCT/ISA/210 (second sheet) (January 2004)

	INTERNATIONAL SEARCH REPORT	International application No. PCT/US04/05736	
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