(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 May 2003 (01.05.2003)

PCT

(10) International Publication Number
WO 03/036702 A2

(51) International Patent Classification[7]: H01L 21/285

(21) International Application Number: PCT/US02/30337

(22) International Filing Date:
27 September 2002 (27.09.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/986,232 22 October 2001 (22.10.2001) US

(71) Applicant: **MOTOROLA, INC.** [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(72) Inventor: **REBER, Douglas, M.**; 13114 Troops Trail, Austin, TX 78727 (US).

(74) Agents: **KOCH, William, E.** et al.; Corporate Law Department, Intellectual Property Section, 7700 West Parmer Lane, MD: TX32/PL02, Austin, TX 78729 (US).

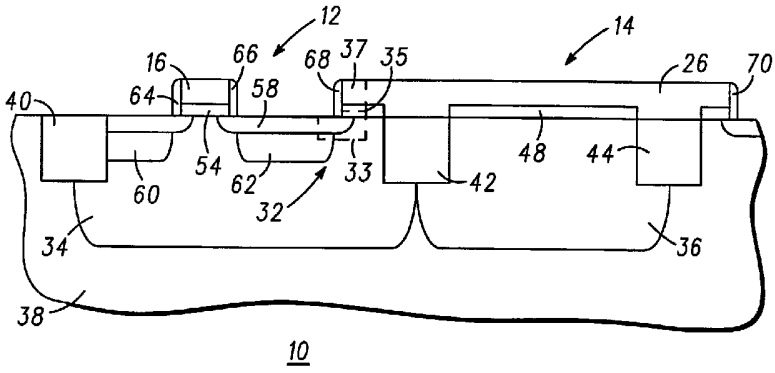
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** INTEGRATED CIRCUIT HAVING INTERCONNECT TO A SUBSTRATE AND METHOD THEREFOR



(57) **Abstract:** A contact (32) between a source/drain (20) and a gate (26) is made by making a selected portion (35) of the gate dielectric (46) conductive by an implant into that selected portion (35) of the gate dielectric (46). The gate material is in a layer over the entire integrated circuit (10). Areas (32) where gates (26) are to connect to source/drains (20) are identified and the gate dielectric (46) at those identified locations (35) is implanted to make it conductive. The source/drains (20) are formed so that they extend under these areas of conductive gate dielectric (35) so that at these locations the implanted gate dielectric (35) shorts the gate (26) to the source/drain (20). This saves area on the integrated circuit (10), reduces the need for interconnect layers, and avoids the problems associated with depositing and etching polysilicon on an exposed silicon substrate.

WO 03/036702 A2

INTEGRATED CIRCUIT HAVING INTERCONNECT TO A SUBSTRATE AND METHOD THEREFOR

Background of the Invention

Field of the Invention

This invention relates to integrated circuits and more particularly to making contact between interconnect and substrate.

Related Art

Integrated circuits comprise transistors formed in active regions that are interconnected by interconnect layers. Typically, these interconnect layers are polysilicon or metal that are made in layers above the substrate. Active regions are formed in the substrate itself. A relatively simple connection that is commonly required in the integrated circuit is a source/drain of one transistor connected to a gate of another transistor. Typically, this occurs by providing an interconnect layer for making the connection from a layer that is above the gate. This requires area on the integrated circuit and thus is a factor in the overall size of the integrated circuit. Another type of contact that has been utilized is known as a buried contact in which polysilicon, which is the typical gate material, is in direct contact with the substrate for making contact between a source/drain and gate.

One of the difficulties and problems associated with buried contacts is that the substrate tends to be excessively etched in the area immediately adjacent to or at the edge of the polysilicon that was making contact to the substrate. This occurs because the opening to the substrate, and thus to the source/drain, must be made before the

polysilicon is deposited. Thus the etch of the polysilicon that is used for the contact can create a substrate overetch problem.

Thus there is a need for contacts that do not require as much space as those of upper level interconnect and do not have the problems associated with buried contacts.

Brief Description of the Drawings

FIG. 1 is a circuit diagram of a circuit known in the prior art;

FIG. 2 is a top view of the circuit of FIG. 1 made according to an embodiment of the present invention;

FIGs. 3-6 are sequential cross-sections in processing of a portion of the circuit of FIG. 2; and

FIGs. 7-9 are sequential cross-sections in processing of another portion of the circuit of FIG. 2.

Description of the Invention

A standard connection of a drain to a gate is achieved by an implant into gate dielectric material to achieve a connection between a source/drain formed in a substrate and a gate of another transistor. The connection between the gate material and the substrate, and thus source/drain, is achieved by implanting into the gate material in that area so that the gate dielectric becomes conductive in that location. This is better understood by reference to the figures and the following description.

Shown in FIG. 1 is a circuit 10 that is known in the prior art and is very common in integrated circuits but which is made differently than that of the prior art and configured differently than that of the prior art. Circuit 10 comprises a transistor 12 and a transistor 14. Transistor 12

has a gate 16, a source/drain 18, and a source/drain 20. As used herein a source/drain is the doped region adjacent to a gate that can be a source or a drain, depending how it is used in a given circuit. Transistor 14 has a source/drain 22 and a source/drain 24. Source/drains 18, 22 and 24 are shown as not being connected but in a completed circuit would have connections to either other circuitry or to power supply terminals. Similarly, gate 16 would be connected to other circuitry or a reference or signal. Source/drain 20 is connected to gate 26 of transistor 14. A source/drain to gate connection is very common in integrated circuits.

Shown in FIG. 2 is circuit 10 in a layout according to an embodiment of the invention. Circuit 10 comprises an active region 28 and an active region 30. Active region 28 is for forming transistor 12 and active region 30 is for forming transistor 14. Gate 26 overlies active region 30 and is connected to source/drain region 20 of transistor 14 at a contact 32. Active region 28 has gate 16 overlying it and contains source/drain regions 18 and 20. Active region 30 contains source/drain regions 22 and 24. Contact 32 is achieved by having at least a portion of that region implanted so that gate dielectric material becomes conductive in that area. Thus, gate 26, which extends over active region 18, makes contact with drain 20 through contact 32.

Shown in FIG. 3 is a cross-section showing transistors 12 and 14 at a relatively early stage in processing. This stage in processing is conventional. Circuit 10 comprises a substrate 38, which is P-, having a P-well 34 and an N-well 36. Substrate 38 is shown as having conductive material 50 over P-well 34 and N-well 36 and overlying gate dielectric material 46 and 48. P-well 34 is between isolation regions 40 and 42. N-well 36 is between isolation regions 42 and 44 as shown in FIG. 3. Overlying FIG. 3 between isolation regions 40 and 42 is gate

dielectric material 46 and between isolation regions 42 and 44 is gate dielectric material 48. Overlying gate dielectric material 46 and 48 is polysilicon layer 50. Substrate 38 may also be silicon on insulator (SOI) in which case there would be a semiconductor layer over an in insulator. Wells 34 and 36 would be in the semiconductor layer and isolation regions 40, 42, and 44 would extend to the insulator.

Shown in FIG. 4 is circuit 10 after photoresist 52 has been deposited and patterned so that there is an opening at a location for contact 32 in active region 28. This shows an implant that has its center depth at dielectric material 46 in contact area 32. The result is a doped region 33 in P-well 34, an implanted gate dielectric 35, and an implanted polysilicon region 37. An effective dopant material is boron for the purpose of causing dielectric material 46 at contact 32 to be highly conductive. Gate dielectric material may be other materials and instead of polysilicon the gate electrode may be formed of other materials as well. In such cases it may be desirable to provide a different dopant than boron to form the needed conduction and short circuit between the gate dielectric material and the overlying gate material. One such dopant may be aluminum, and another may be phosphorus. It may be advantageous to use phosphorus, which causes N-type conductivity, when implanting into the P-well. A gate dielectric material other than silicon oxide may be hafnium oxide. Other materials may be chosen as well. Thus, a short circuit is formed to the polysilicon without the polysilicon having to have been etched prior to forming the short circuit. In conventional buried contacts it is necessary to open the well or area to be contacted followed by a polysilicon deposition. The subsequent etching is not only cumbersome in terms of the sequence but also can

form the etched out areas of the substrate adjacent to the area where the polysilicon is etched after the substrate has been exposed.

Shown in FIG. 5 is polysilicon 50 and gate materials 46 after a patterned etch to leave gate 16 over gate dielectric 54 formed of gate dielectric material 46. Also, a source/drain extension 56 and a source/drain extension 58 are formed using gate 16 as a mask. Source/drain extensions 56 and 58 are N-type formed by implanting a combination of arsenic and phosphorus. The particular species and combination of species for implanting may vary as needed. Also left is gate 26 that extends to contact area 32. Thus, gate 26 overlaps the region of gate dielectric material that was implanted. The portion of the gate dielectric that was implanted is the portion that ultimately forms the contact between gate 26 and drain 20 so some of this implanted gate material must remain after the etch of polysilicon 50. It may be desirable to have a combination boron and indium halo implant before extensions 56 and 58. This halo implant is not shown because halo implants are well understood in the art and for not unnecessarily complicating the drawings.

Shown in FIG. 6 is a circuit 10 after sidewall formation and a combination arsenic and phosphorus implant to form heavily doped source/drain regions 60 and 62. Gate 16 has sidewall spacers 64 and 66. Gate 26 has sidewall spacers 68 and 70. This shows a completed transistor 12 of the N-channel type and completed transistor 14 of the P-channel type. Gate 26 is connected to drain 20 at contact 32. Drain 20 is made up of heavily doped region 62 and extension region 58. If contact area 32 is implanted with phosphorus, the contact area may extend past source/drain extension 58 as shown in FIG. 6. If, however, contact area 32 is doped with boron, which forms P-type regions, then

contact area 32 should not extend laterally past source/drain extension 58. The doped region of the gate dielectric material is conductive and thus will make contact with the doped region under it. If this doped gate dielectric is only in contact with the source/drain, then it will only short gate 26 to drain 20 and not to well 34. If the doped portion of the gate dielectric extends laterally past drain 20, then it should be in contact with a doped region of a conductivity type opposite to that of well 34 and thus the implant of the gate dielectric as shown in FIG. 6 should form N-type regions.

Shown in FIG. 7 is transistor 14 at the same stage in processing as that shown in FIG. 3. In this cross section, FIG. 7 shows N-well 36 and isolation regions 70 and 72 as well as gate dielectric material 48.

Shown in FIG. 8 is transistor 14 after polysilicon 50 has been etched to form gate 74 and source/drain extensions 76 and 78. These extensions are formed in a manner analogous to that shown in FIG. 5 but at a different process step because the doping type is different for transistor 12 than for transistor 14. These source/drain extensions are formed by implanting a combination of arsenic and boron. The steps required for FIG. 8 may be either before or after those for FIG. 5.

Shown in FIG. 9 is a completed transistor 14 after formation of sidewall spacers 80 and 82 that provide a mask for formation of heavily doped source/drain regions 84 and 86 to complete formation of source/drain region 22 and source/drain region 24 formed by implants using a combination of boron.

Thus is it seen that a completed circuit 10, as shown in cross-sections 3-6 and cross-sections 7-9, show a completed transistor 12 and a completed transistor 14 having a drain of transistor 12 connected to the gate of transistor 14 without having to apply a conductive material over

a source/drain in order to make that contact. This avoids the problems associated with buried contacts and provides very compact interconnect between the drain of one transistor and the gate of another. This has the effect of reducing the need for higher level interconnect thus reducing complexity of processing and opportunities for defects. Thus, by having the reduced area, the chip area is reduced overall providing an opportunity to provide a lower cost without significant process complications.

Also a similar benefit may be achieved by a circuit feature other than a transistor such as a resistor. Another circuit feature may have an electrode, such as polysilicon gate 26, extending over a source/drain and making electrical contact thereto by way of a conductive implanted dielectric such as region 35 shown in FIGs. 4, 5, and 6.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS

1. A method for forming an electrical contact comprising:

providing a semiconductor substrate;

forming a dielectric layer over the semiconductor substrate;

forming a conductive layer over the dielectric layer;

implanting a first species into a first portion of the dielectric layer to form a conductive doped dielectric;

patterning the dielectric layer to form a patterned dielectric layer, wherein the patterned dielectric layer comprises the conductive doped dielectric; and

patterning the conductive layer to form a patterned conductive layer, wherein a portion of the patterned conductive layer electrically contacts the conductive doped dielectric.

2. The method of claim 1, wherein implanting a first species into a first portion of the dielectric layer comprises:

forming a patterned photoresist layer over the conductive layer; and

implanting through the conductive layer.

3. The method of claim 1 further comprising:

implanting an area of the semiconductor substrate under the conductive doped dielectric with the first species to form a doped substrate region while implanting the first species into the first portion;

forming a first gate electrode when patterning the conductive layer;

forming a first conductive region adjacent the first gate electrode and within the semiconductor substrate; and

forming a second conductive region adjacent the first gate electrode and within the semiconductor substrate, wherein a portion of the second conductive region overlaps a portion of the doped substrate region.

4. The method of claim 3, wherein forming the second conductive region further comprises implanting the first species into the second conductive region.

5. The method of claim 3, wherein forming the second conductive region further comprises implanting a second species into the second conductive region, wherein the second species is a different conductivity than the first species.

6. A semiconductor device comprising:

a first transistor comprising:

a first gate electrode formed over the first gate dielectric;

a first conductive region formed within a substrate and adjacent the first gate dielectric;

a second conductive region formed within the substrate and adjacent the first gate dielectric; and

a first gate dielectric formed over the substrate; and

a second transistor comprising:

a second gate electrode formed over the first gate dielectric;

a third conductive region formed within the substrate and adjacent the second gate dielectric;

a fourth conductive region formed within the substrate and adjacent the second gate dielectric; and

a second gate dielectric formed over the substrate;

and wherein:

the second gate electrode is part of a conductive layer;

the conductive layer electrically contacts a conductive doped dielectric; and

the conductive doped dielectric is electrically connected to the first conductive region.

7. The device of claim 6, wherein a portion of the conductive layer overlies the conductive doped dielectric.

8. The device of claim 6, wherein the first conductive region is electrically isolated from the third and fourth conductive regions.

9. The device of claim 6, wherein the conductive doped dielectric is a heavily doped oxide layer.

10. The device of claim 9, wherein the conductive doped dielectric is silicon dioxide and is doped with an element selected from the group consisting of: phosphorus, boron, aluminum, gallium, germanium, indium, arsenic, tungsten, and silicon.

11. The device of claim 6, wherein the first transistor is in an n-type well and the second transistor are in a p-type well.

12. The device of claim 6, further comprising:

a doped area of the semiconductor substrate under the conductive doped dielectric, wherein the conductive doped dielectric and the doped area are doped with a species with a first conductivity and the doped area overlaps the first conductive area.

13. The device of claim 12, wherein the first conductive area is doped to a conductivity different than the doped area.

14. The device of claim 12, wherein the first conductivity is p-type.

15. The device of claim 12, wherein the first conductivity is n-type.

16. The method of claim 12, wherein the first conductive area is more heavily doped than the doped area.

17. A semiconductor device comprising:

a first active area;

a second active area;

a first dielectric layer over a first portion of the active area;

a first conductive layer over the first dielectric layer;

a second dielectric layer over the second active area;

a first portion of a second conductive layer over the second dielectric layer;

a conductive doped dielectric over a second portion of the first active area; and

a second portion of the second conductive layer over the conductive doped dielectric and the first active area.

18. The device of claim 17, wherein the third dielectric layer is electrically connected to a conductive area adjacent the first dielectric layer and the first conductive layer.

19. The device of claim 17, wherein the conductive area is a source/drain region.

20. The device of claim 17, wherein the conductive doped dielectric is silicon dioxide and the dopant is selected from the group consisting of: phosphorus, boron, aluminum, gallium, germanium, indium, arsenic, tungsten, and silicon.

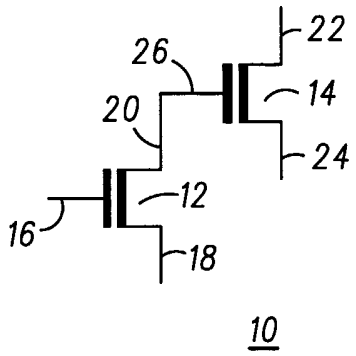
21. The device of claim 17, wherein a salicide is formed over the first and second conductive layers.

22. An integrated circuit, comprising:

a substrate having a first well region;

a transistor formed in the first well region having a first source/drain region in the first well region and a second source/drain region;

a circuit feature having a conductive electrode extending over the first source/drain region and physically separated from the first source/drain by a conductive implanted dielectric, wherein the conductive implanted dielectric electrically shorts the conductive electrode to the first source/drain region.



-PRIOR ART-

FIG. 1

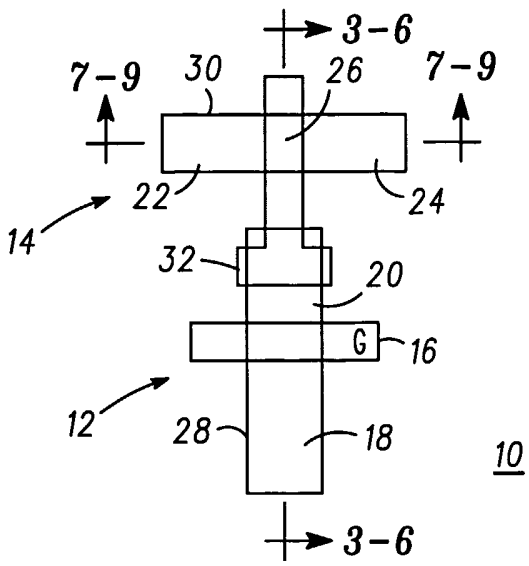
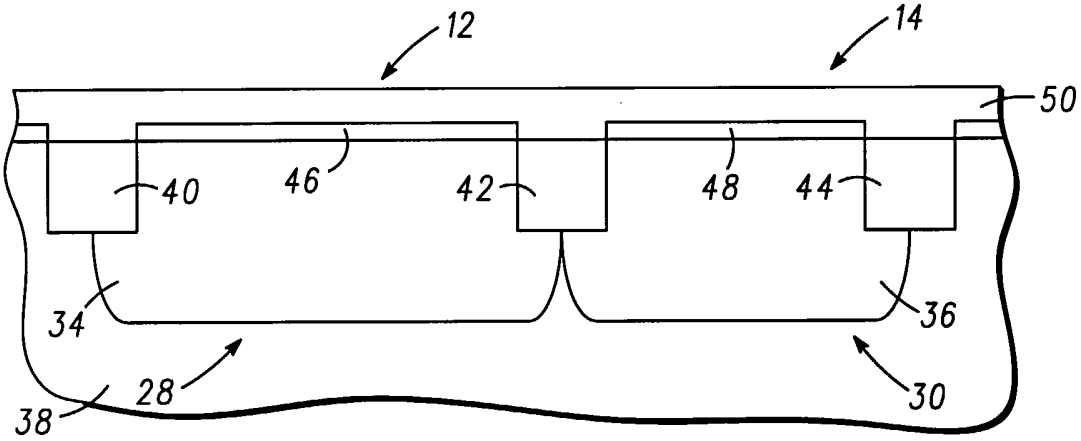
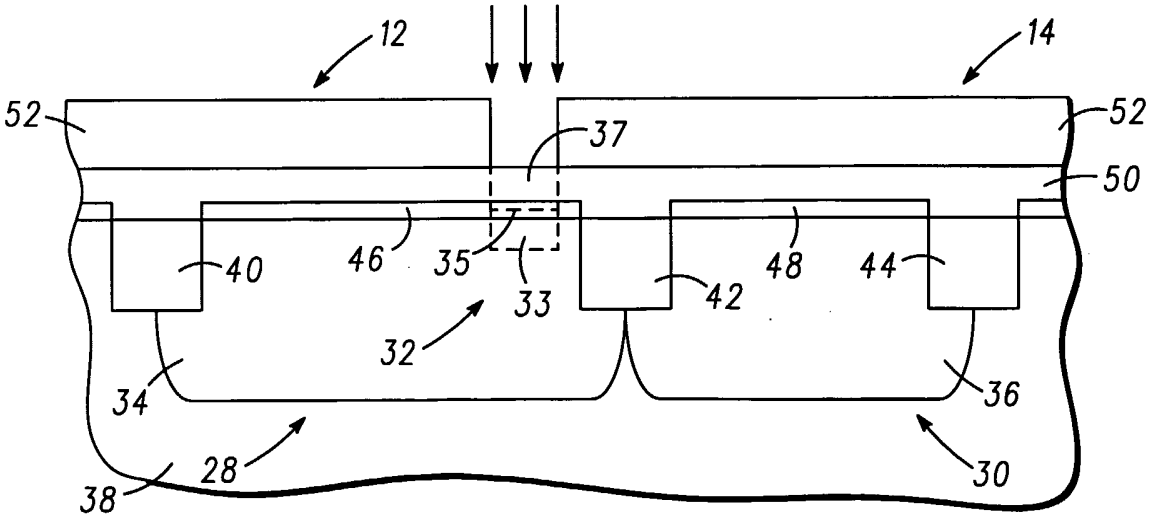


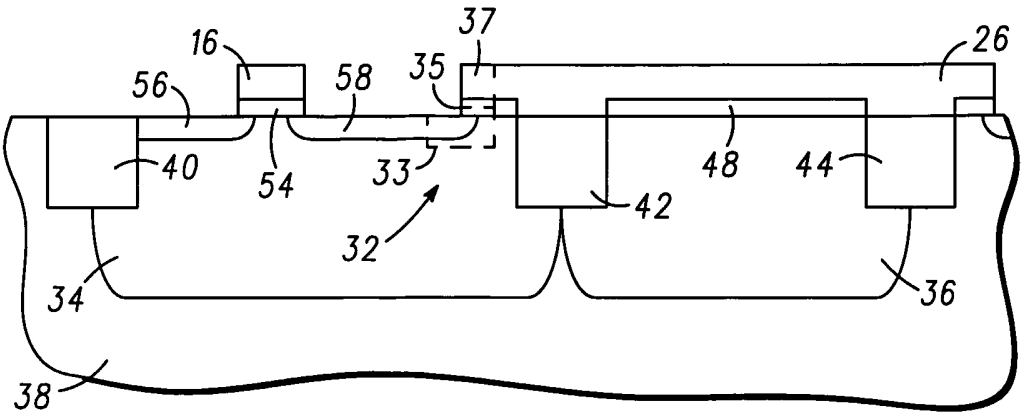
FIG. 2



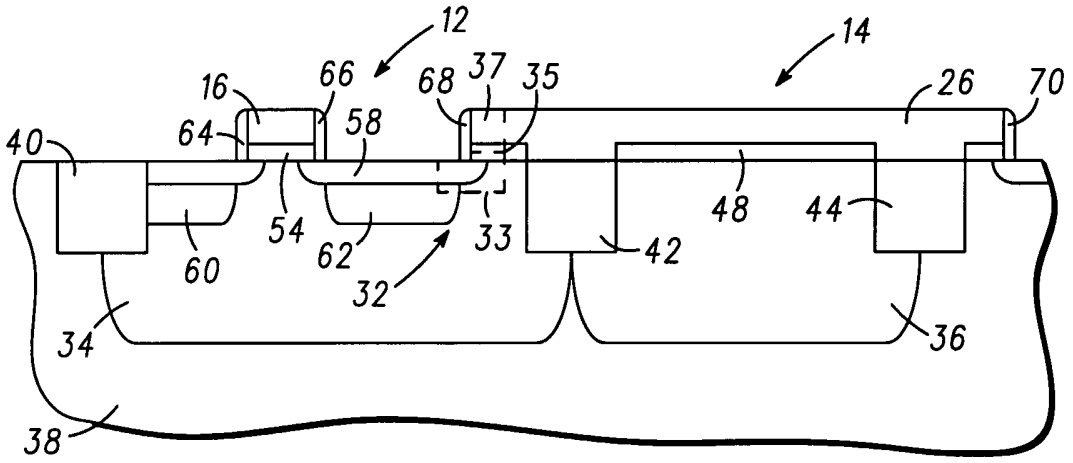
10 FIG. 3



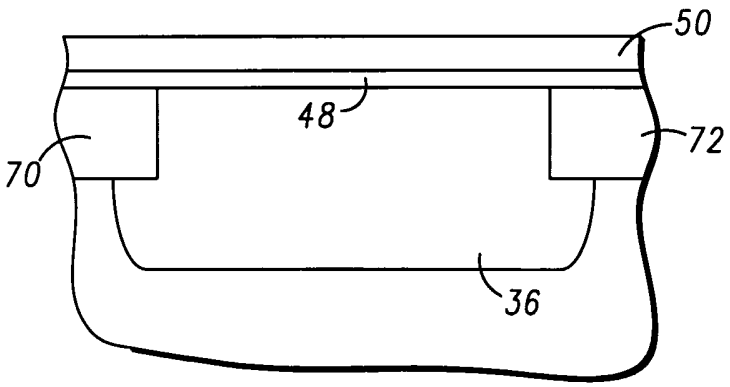
10 FIG. 4



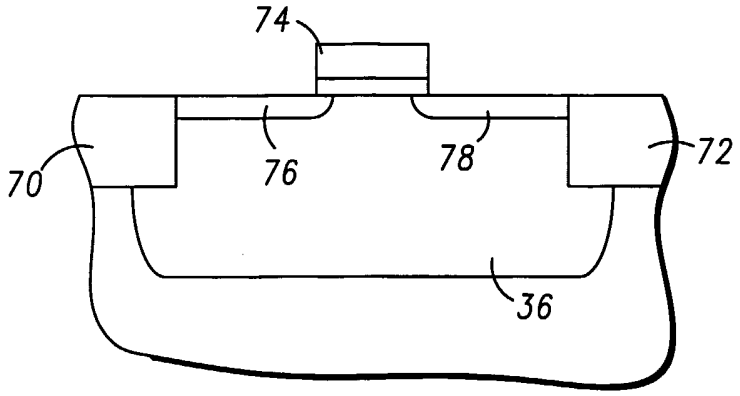
10 FIG. 5



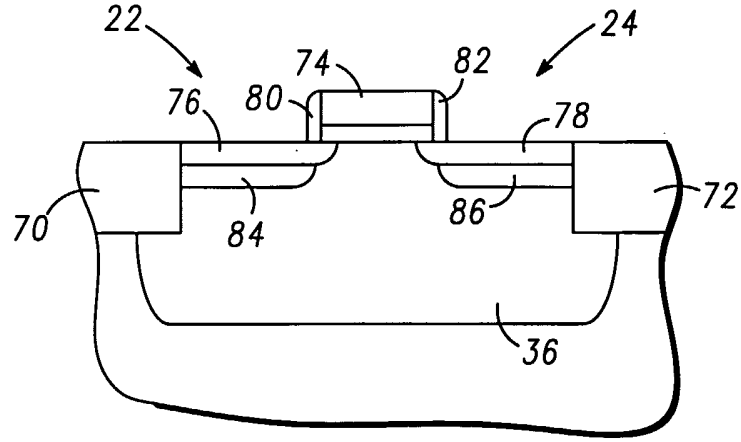
10 FIG. 6



14 FIG. 7



14 FIG. 8



14 FIG. 9