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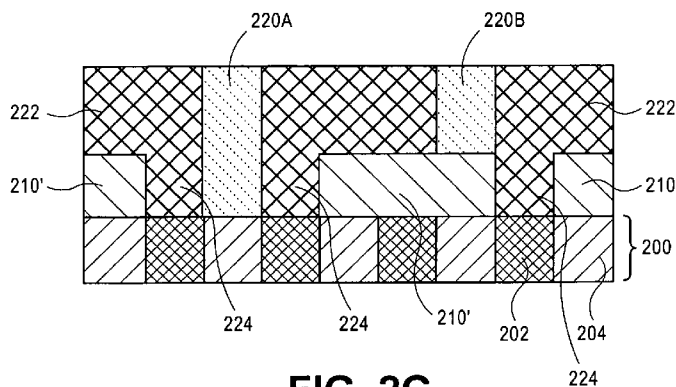
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(54) Title: APPROACHES FOR PATTERNING METAL LINE ENDS FOR BACK END OF LINE (BEOL) INTERCONNECTS

**FIG. 2G**

(57) Abstract: Approaches for patterning metal line ends for back end of line (BEOL) interconnects, and the resulting structures, are described. In an example, a metallization layer of an interconnect structure for a semiconductor die includes a metal line disposed in a trench of an interlayer dielectric (ILD) material layer. The ILD material layer is composed of a first dielectric material. A conductive via is disposed in the ILD material layer, below and electrically connected to the metal line. A dielectric plug is directly adjacent to the metal line and the conductive via. The dielectric plug is composed of a second dielectric material different from the first dielectric material.



**APPROACHES FOR PATTERNING METAL LINE ENDS FOR BACK END OF LINE (BEOL)
INTERCONNECTS**

TECHNICAL FIELD

5 **[0001]** Embodiments of the invention are in the field of semiconductor structures and processing and, in particular, approaches for patterning metal line ends for back end of line (BEOL) interconnects.

BACKGROUND

10 **[0002]** For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products
15 with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.

[0003] Integrated circuits commonly include electrically conductive microelectronic structures, which are known in the arts as vias, to electrically connect metal lines or other interconnects above the vias to metal lines or other interconnects below the vias. Vias are
20 typically formed by a lithographic process. Representatively, a photoresist layer may be spin coated over a dielectric layer, the photoresist layer may be exposed to patterned actinic radiation through a patterned mask, and then the exposed layer may be developed in order to form an opening in the photoresist layer. Next, an opening for the via may be etched in the dielectric layer by using the opening in the photoresist layer as an etch mask. This opening is referred to
25 as a via opening. Finally, the via opening may be filled with one or more metals or other conductive materials to form the via.

[0004] In the past, the sizes and the spacing of vias has progressively decreased, and it is expected that in the future the sizes and the spacing of the vias will continue to progressively decrease, for at least some types of integrated circuits (e.g., advanced microprocessors, chipset
30 components, graphics chips, etc.). One measure of the size of the vias is the critical dimension of the via opening. One measure of the spacing of the vias is the via pitch. Via pitch represents the center-to-center distance between the closest adjacent vias. It is to be appreciated that with scaling to smaller vias, scaling to smaller non-conductive spaces or interruptions between metals lines (referred to as “line ends,” “plugs” or “cuts”) connected by vias may also need to be
35 performed.

[0005] When patterning extremely small line ends (plugs or cuts) with extremely small pitches by such lithographic processes, several challenges present themselves, especially when the pitches are around 70 nanometers (nm) or less and/or when the critical dimensions of the line ends are around 35nm or less. Also, as line end pitches scale ever smaller over time, the overlay tolerances tend to scale with them at an even greater rate than lithographic equipment is able to keep up.

[0006] Another such challenge is that the critical dimensions of the line ends generally tend to scale faster than the resolution capabilities of the lithographic scanners. Shrink technologies exist to shrink the critical dimensions of the line ends. However, the shrink amount tends to be limited by the minimum line end pitch, as well as by the ability of the shrink process to be sufficiently optical proximity correction (OPC) neutral, and to not significantly compromise line width roughness (LWR) and/or critical dimension uniformity (CDU).

[0007] Yet another such challenge is that the LWR and/or CDU characteristics of photoresists generally need to improve as the critical dimensions of the line ends decrease in order to maintain the same overall fraction of the critical dimension budget. However, currently the LWR and/or CDU characteristics of most photoresists are not improving as rapidly as the critical dimensions of the line ends are decreasing.

[0008] A further such challenge is that the extremely small via pitches generally tend to be below the resolution capabilities of even extreme ultraviolet (EUV) lithographic scanners. As a result, commonly two, three, or more different lithographic masks may be used, which tend to increase the costs. At some point, if pitches continue to decrease, it may not be possible, even with multiple masks, to print line ends for these extremely small pitches using EUV scanners.

[0009] Thus, improvements are needed in the area of line end manufacturing technologies.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1A illustrates a plan view and corresponding cross-sectional view taken along the a-a' axis of the plan view of a metallization layer of a state-of-the-art semiconductor device.

[0011] Figure 1B illustrates a cross-sectional view of a line end or plug fabricated using a state-of-the-art processing scheme.

[0012] Figure 1C illustrates another cross-sectional view of a line end or plug fabricated using a state-of-the-art processing scheme.

[0013] Figures 2A-2G illustrate cross-sectional views representing various operations in a process for patterning metal line ends for back end of line (BEOL) interconnects, in accordance with an embodiment of the present invention, wherein:

[0014] Figure 2A illustrates a starting structure having a line trench formed in an upper portion of an interlayer dielectric (ILD) material layer formed above an underlying metallization layer;

[0015] Figure 2B illustrates the structure of Figure 2A following formation of via trenches in the lower portion of the ILD material layer;

[0016] Figure 2C illustrates the structure of Figure 2B following formation of a sacrificial material above the ILD material layer and in the line trench and the via trenches;

[0017] Figure 2D illustrates the structure of Figure 2C following patterning of the sacrificial material to form an opening exposing a portion of the lower metallization layer between two metal lines of the underlying metallization layer;

[0018] Figure 2E illustrates the structure of Figure 2D following filling of the openings of the sacrificial material with a dielectric material;

[0019] Figure 2F illustrates the structure of Figure 2E following removal of the sacrificial material to provide dielectric plugs; and

[0020] Figure 2G illustrates the structure of Figure 2F following filling of the line trenches and the via trenches with a conductive material.

[0021] Figure 3A illustrates a cross-sectional view of a metallization layer of an interconnect structure for a semiconductor die that includes dielectric line ends or plugs having a seam therein, in accordance with an embodiment of the present invention.

[0022] Figure 3B illustrates a cross-sectional view of a metallization layer of an interconnect structure for a semiconductor die that includes a dielectric line end or plug that is not immediately adjacent a conductive via, in accordance with an embodiment of the present invention.

[0023] Figure 4 illustrates a computing device in accordance with one implementation of an embodiment of the invention.

[0024] Figure 5 is an interposer implementing one or more embodiments of the invention.

DESCRIPTION OF THE EMBODIMENTS

[0025] Approaches for patterning metal line ends for back end of line (BEOL) interconnects, and the resulting structures, are described. In the following description, numerous specific details are set forth, such as specific integration and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the

present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

[0026] One or more embodiments described herein are directed to techniques for patterning metal line ends. Embodiments may include aspects of one or more of contact
5 fabrication, damascene processing, dual damascene processing, interconnect fabrications, and metal line trench patterning.

[0027] To provide context, in the advanced nodes of semiconductor manufacturing, the low level interconnects are created by separate patterning processes of the line grating, line ends, and vias. The fidelity of the composite pattern tends to degrade as the vias encroach upon the
10 line ends and vice-versa. Embodiments described herein provide for a line end process also known as a plug process that eliminates associated proximity rules. Embodiments may allow for a via to be placed at the line end and a large via to strap across a line end.

[0028] To provide further context, Figure 1A illustrates a plan view and corresponding cross-sectional view taken along the a-a' axis of the plan view of a metallization layer of a state-
15 of-the-art semiconductor device. Figure 1B illustrates a cross-sectional view of a line end or plug fabricated using a state-of-the-art processing scheme. Figure 1C illustrates another cross-sectional view of a line end or plug fabricated using a state-of-the-art processing scheme.

[0029] Referring to Figure 1A, a metallization layer 100 includes metal lines 102 formed in a dielectric layer 104. The metal lines 102 may be coupled to underlying vias 103. The
20 dielectric layer 104 may include line end or plug regions 105. Referring to Figure 1B, a state-of-the-art line end or plug region 105 of a dielectric layer 104 may be fabricated by patterning a hardmask layer 110 on the dielectric layer 104 and then etching exposed portions of the dielectric layer 104. The exposed portions of the dielectric layer 104 may be etched to a depth suitable to form a line trench 106 or further etched to a depth suitable to form a via trench 108.
25 Referring to Figure 1C, two vias adjacent opposing sidewalls of the line end or plug 105 may be fabricated in a single large exposure 116 to ultimately form line trenches 112 and via trenches 114.

[0030] However, referring again to Figures 1A-1C, fidelity issues and/or hardmask erosion issues may lead to imperfect patterning regimes. By contrast, one or more embodiments
30 described herein include implementation of a process flow involving construction of a line end dielectric (plug) after a trench and via patterning process.

[0031] In an aspect, then, one or more embodiments described herein are directed to approaches for building non-conductive spaces or interruptions between metals lines (referred to as "line ends," "plugs" or "cuts") and, in some embodiments, associated conductive vias.
35 Conductive vias, by definition, are used to land on a previous layer metal pattern. In this vein, embodiments described herein enable a more robust interconnect fabrication scheme since

alignment by lithography equipment is relied on to a lesser extent. Such an interconnect fabrication scheme can be used to relax constraints on alignment/exposures, can be used to improve electrical contact (e.g., by reducing via resistance), and can be used to reduce total process operations and processing time otherwise required for patterning such features using conventional approaches.

[0032] In an exemplary processing scheme, Figures 2A-2G illustrate cross-sectional views representing various operations in a process for patterning metal line ends for back end of line (BEOL) interconnects, in accordance with an embodiment of the present invention.

[0033] Referring to Figure 2A, a method of fabricating a metallization layer of an interconnect structure for a semiconductor die includes forming a line trench 208 in an upper portion (above a lower portion 210) of an interlayer dielectric (ILD) material layer 206 formed above an underlying metallization layer 200. The underlying metallization layer 200 includes metal lines 202 disposed in a dielectric layer 204.

[0034] Referring to Figure 2B, via trenches 212A and 212B are formed in the lower portion 210 of the ILD material layer 206 to form a patterned lower portion 210' of the ILD material layer 206. As an exemplary embodiment, the via trench 212A exposes two metal lines 202 of the underlying metallization layer 200, while the via trench 212B exposes one metal line 202 of the underlying metallization layer 200.

[0035] Referring to Figure 2C, a sacrificial material 214, such as a matrix material, is formed above the ILD material layer (portions 210' shown in Figure 2C) and in the line trench 208 and the via trenches 212A and 212B. In an embodiment, a patterned hardmask layer 216 is formed on the sacrificial material 214, as is depicted in Figure 2C.

[0036] Referring to Figure 2D, the sacrificial material 214 is patterned to form an opening (left-hand side opening of Figure 2D) exposing a portion of the lower metallization layer 200 between the two metal lines 202 of the underlying metallization layer 200 associated with via trench 212A of Figure 2B. In the exemplary embodiment shown, the sacrificial material 214 is further patterned to form an opening (right-hand side opening of Figure 2D) exposing a portion of the patterned lower portion 210' of the ILD material layer adjacent via trench 212B of Figure 2B. In an embodiment, the sacrificial material 214 is patterned by transferring the pattern of patterned hardmask 216 to the sacrificial material 214 by an etch process.

[0037] Referring to Figure 2E, the openings of the sacrificial material 214 (now shown as patterned and filled sacrificial material 214') are filled with a dielectric material 218. In one embodiment, the openings of the sacrificial material 214 are filled with the dielectric material 218 using a deposition process selected from the group consisting of atomic layer deposition (ALD) and chemical vapor deposition (CVD). In one embodiment, the openings of the sacrificial material 214 are filled with the dielectric material 218 of a first dielectric material

composition. In one such embodiment, the ILD material layer 206 includes a second dielectric material composed of a different material than the first dielectric material composition. In another such embodiment, however, the ILD material layer 206 is composed of the first dielectric material.

5 [0038] Referring to Figure 2F, the filled sacrificial material 214' is removed to provide dielectric plugs 220A and 220B. In the exemplary embodiment shown, dielectric plug 220A is disposed on the portion of the lower metallization layer 200 between the two metal lines 202 of the underlying metallization layer 200. Dielectric plug 220A is adjacent a via trench 212A and line trench 208' and, in the case shown in Figure 2F, is between essentially symmetric via
10 trenches 212A and line trenches 208'. Dielectric plug 220B is disposed on a portion of the patterned lower portion 210' of the ILD material layer 206. Dielectric plug 220B neighbors a via trench 212B and corresponding line trench (right-hand side of dielectric plug 220B). In an embodiment, the structure of Figure 2E is subjected to a planarization process used to remove overburden regions of the dielectric material 218, to remove the patterned hardmask 216, and to
15 reduce a height of the sacrificial material 214' and the portions of the dielectric material 218 therein. The sacrificial material 214' is then removed by using a selective wet or dry processing etch technique.

[0039] Referring to Figure 2G, the line trenches 208' and the via trenches 212A and 212B are filled with a conductive material. In one embodiment, filling the line trenches 208' and
20 the via trenches 212A and 212B with the conductive material forms metal lines 222 and conductive vias 224 in a patterned dielectric layer 210'. In an exemplary embodiment, referring to plug 220A, a first metal line 222 and a first conductive via 224 are directly adjacent to the left-hand sidewall of dielectric plug 220A. A second metal line 222 and a second conductive via 224 are directly adjacent to the right-hand sidewall of dielectric plug 220A. Referring to plug
25 220B, a first metal line 222 is directly adjacent to the right-hand sidewall of dielectric plug 220B and an underlying portion of the patterned lower portion 210' of the ILD layer is directly adjacent a first conductive via 224. On the left-hand side of dielectric plug 220B, however, only a metal line 22 and not an associated conductive via are associated with the dielectric plug 220B. In an embodiment, the metal fill process is performed by depositing and then planarizing one or
30 more metal layers over the structure of Figure 2F.

[0040] Referring again to Figure 2G several different embodiments can be demonstrated using the illustration. For example, in an embodiment, the structure of Figure 2G represents a final metallization layer structure. In another embodiment, the dielectric plugs 220A and 22B are removed to provide an air gap structure. In another embodiment, the dielectric plugs 220A
35 and 22B are replaced with another dielectric material. In another embodiment, the dielectric

plugs 220A and 22B may be a sacrificial pattern that is ultimately transferred to another underlying interlayer dielectric material layer.

[0041] In an exemplary embodiment, referring again to Figure 2G (and previous processing operations), a metallization layer of an interconnect structure for a semiconductor die includes a metal line 222 disposed in a trench 208' of an interlayer dielectric (ILD) material layer 206. The ILD material layer 206 is composed of a first dielectric material. A conductive via 224 is disposed in the ILD 206 material layer, below and electrically connected to the metal line 222. A dielectric plug 220A (or 220B) is directly adjacent to the metal line 222 and the conductive via 224. A second metal line 222 and conductive via 224 may also be directly adjacent to the dielectric plug (e.g., dielectric plug 220A). In one embodiment, the dielectric plug 220A (or 220B) is composed of a second dielectric material different from the first dielectric material.

[0042] It is to be appreciated that filling the openings of the sacrificial material 214 with the dielectric material may lead to formation of a seam in the dielectric material approximately in the center of the resulting dielectric plug. For example, Figure 3A illustrates a cross-sectional view of a metallization layer of an interconnect structure for a semiconductor die that includes dielectric line ends or plugs having a seam therein, in accordance with an embodiment of the present invention.

[0043] Referring to Figure 3A, a metallization layer of an interconnect structure for a semiconductor die includes metal lines 220 disposed in trenches of an interlayer dielectric (ILD) material layer (lower portion 210' shown). Conductive vias 224 are disposed in the ILD material layer 210', below and electrically connected to the metal lines 222. Dielectric plugs 320A and 320B are directly adjacent to the metal lines 222 and the conductive vias 224. The dielectric plugs 320A and 320B each include a seam 300 approximately in the center of the dielectric plug, e.g., attributable to deposition formation of the dielectric plug by chemical vapor deposition (CVD) or atomic layer deposition (ALD).

[0044] It is to be appreciated that a line end or plug may be associated with metal lines that do not have underlying vias immediately adjacent the dielectric plug. For example, Figure 3B illustrates a cross-sectional view of a metallization layer of an interconnect structure for a semiconductor die that includes a dielectric line end or plug that is not immediately adjacent a conductive via, in accordance with an embodiment of the present invention. Referring to Figure 3B, dielectric plug 320 is associated with metal lines 222 that do not have underlying vias (such as vias 224) immediately adjacent the dielectric plug 320.

[0045] A resulting structure such as described in association with Figure 2G, Figure 3A or Figure 3B may subsequently be used as a foundation for forming subsequent metal line/via and ILD layers. Alternatively, the structure of Figure 2G, Figure 3A or Figure 3B may represent

the final metal interconnect layer in an integrated circuit. It is to be appreciated that the above process operations may be practiced in alternative sequences, not every operation need be performed and/or additional process operations may be performed. In an embodiment, offset due to conventional lithograph/dual damascene patterning that must otherwise be tolerated, is a mitigated factor for the resulting structures described herein. It is also to be appreciated that, in subsequent fabrication operations, the dielectric layer(s) may be removed to provide air gaps between the resulting metal lines.

[0046] In an embodiment, as used throughout the present description, interlayer dielectric (ILD) material is composed of or includes a layer of a dielectric or insulating material.

Examples of suitable dielectric materials include, but are not limited to, oxides of silicon (e.g., silicon dioxide (SiO_2)), nitrides of silicon (e.g., silicon nitride (Si_3N_4)), doped oxides of silicon, fluorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof. The interlayer dielectric material may be formed by conventional techniques, such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or by other deposition methods.

[0047] In an embodiment, as is also used throughout the present description, interconnect material is composed of one or more metal or other conductive structures. A common example is the use of copper lines and structures that may or may not include barrier layers between the copper and surrounding ILD material. As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. For example, the metal interconnect lines may include barrier layers, stacks of different metals or alloys, etc. The interconnect lines are also sometimes referred to in the arts as traces, wires, lines, metal, or simply interconnect.

[0048] In an embodiment, as is also used throughout the present description, hardmask materials are composed of dielectric materials different from the interlayer dielectric material. In one embodiment, different hardmask materials may be used in different regions so as to provide different growth or etch selectivity to each other and to the underlying dielectric and metal layers. In some embodiments, a hardmask layer includes a layer of a nitride of silicon (e.g., silicon nitride) or a layer of an oxide of silicon, or both, or a combination thereof. Other suitable materials may include carbon-based materials, such as silicon carbide. In another embodiment, a hardmask material includes a metal species. For example, a hardmask or other overlying material may include a layer of a nitride of titanium (e.g., titanium nitride) or another metal. Potentially lesser amounts of other materials, such as oxygen, may be included in one or more of these layers. Alternatively, other hardmask layers known in the art may be used depending upon the particular implementation. The hardmask layers maybe formed by CVD, PVD, or by other deposition methods.

[0049] It is to be appreciated that the layers and materials described in association with Figures 2A-2G, 3A and 3B are typically formed on or above an underlying semiconductor substrate or structure, such as underlying device layer(s) of an integrated circuit. In an embodiment, an underlying semiconductor substrate represents a general workpiece object used to manufacture integrated circuits. The semiconductor substrate often includes a wafer or other piece of silicon or another semiconductor material. Suitable semiconductor substrates include, but are not limited to, single crystal silicon, polycrystalline silicon and silicon on insulator (SOI), as well as similar substrates formed of other semiconductor materials. The semiconductor substrate, depending on the stage of manufacture, often includes transistors, integrated circuitry, and the like. The substrate may also include semiconductor materials, metals, dielectrics, dopants, and other materials commonly found in semiconductor substrates. Furthermore, the structure depicted in Figure 1G or 3F may be fabricated on underlying lower level interconnect layers.

[0050] As described above, patterned features may be patterned in a grating-like pattern with lines, holes or trenches spaced at a constant pitch and having a constant width. The pattern, for example, may be fabricated by a pitch halving or pitch quartering approach. In an example, a blanket film (such as a polycrystalline silicon film) is patterned using lithography and etch processing which may involve, e.g., spacer-based-quadruple-patterning (SBQP) or pitch quartering. It is to be appreciated that a grating pattern of lines can be fabricated by numerous methods, including 193nm immersion litho (193i), EUV and/or EBDW lithography, directed self-assembly, etc.

[0051] In an embodiment, lithographic operations are performed using 193nm immersion litho (193i), EUV and/or EBDW lithography, or the like. A positive tone or a negative tone resist may be used. In one embodiment, a lithographic mask is a trilayer mask composed of a topographic masking portion, an anti-reflective coating (ARC) layer, and a photoresist layer. In a particular such embodiment, the topographic masking portion is a carbon hardmask (CHM) layer and the anti-reflective coating layer is a silicon ARC layer.

[0052] To provide further context for the above described embodiments, patterning and aligning of features at less than approximately 50 nanometer pitch requires many reticles and critical alignment strategies that are extremely expensive for a semiconductor manufacturing process. Generally, embodiments described herein involve the fabrication of metal and line end patterns based on the positions of overlying orthogonal grating structures which may be in alignment with an underlying layer. Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits and/or microelectronic devices. Examples of such integrated circuits include, but are not limited to, processors, chipset components, graphics processors, digital signal processors, micro-controllers, and the like. In other

embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the arts. For example, in computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The integrated circuits may be coupled with a bus and other

5 components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.

[0053] Figure 4 illustrates a computing device 400 in accordance with one implementation of the invention. The computing device 400 houses a board 402. The board 402
10 may include a number of components, including but not limited to a processor 404 and at least one communication chip 406. The processor 404 is physically and electrically coupled to the board 402. In some implementations the at least one communication chip 406 is also physically and electrically coupled to the board 402. In further implementations, the communication chip 406 is part of the processor 404.

[0054] Depending on its applications, computing device 400 may include other
15 components that may or may not be physically and electrically coupled to the board 402. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a
20 battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0055] The communication chip 406 enables wireless communications for the transfer of data to and from the computing device 400. The term “wireless” and its derivatives may be used
25 to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 406 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE
30 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 400 may include a plurality of communication chips 406. For instance, a first communication chip 406 may be dedicated to shorter range wireless
35 communications such as Wi-Fi and Bluetooth and a second communication chip 406 may be

dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0056] The processor 404 of the computing device 400 includes an integrated circuit die packaged within the processor 404. In some implementations of embodiments of the invention, the integrated circuit die of the processor includes one or more structures, such as metal interconnect layers having metal line ends (plugs or cuts) built in accordance with implementations of embodiments of the invention. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0057] The communication chip 406 also includes an integrated circuit die packaged within the communication chip 406. In accordance with another implementation of embodiments of the invention, the integrated circuit die of the communication chip includes one or more structures, such as metal interconnect layers having metal line ends (plugs or cuts) built in accordance with implementations of embodiments of the invention.

[0058] In further implementations, another component housed within the computing device 400 may contain an integrated circuit die that includes one or more structures, such as metal interconnect layers having metal line ends (plugs or cuts) built in accordance with implementations of embodiments of the invention.

[0059] In various implementations, the computing device 400 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 400 may be any other electronic device that processes data.

[0060] Figure 5 illustrates an interposer 500 that includes one or more embodiments of the invention. The interposer 500 is an intervening substrate used to bridge a first substrate 502 to a second substrate 504. The first substrate 502 may be, for instance, an integrated circuit die. The second substrate 504 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 500 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 500 may couple an integrated circuit die to a ball grid array (BGA) 506 that can subsequently be coupled to the second substrate 504. In some embodiments, the first and second substrates 502/504 are attached to opposing sides of the interposer 500. In other embodiments, the first and second substrates 502/504 are attached to the same side of the interposer 500. And

in further embodiments, three or more substrates are interconnected by way of the interposer 500.

[0061] The interposer 500 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further
5 implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[0062] The interposer may include metal interconnects 508 and vias 510, including but not limited to through-silicon vias (TSVs) 512. The interposer 500 may further include
10 embedded devices 514, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 500. In accordance with embodiments
15 of the invention, apparatuses or processes disclosed herein may be used in the fabrication of interposer 500.

[0063] Thus, embodiments of the present invention include approaches for patterning metal line ends for back end of line (BEOL) interconnects, and the resulting structures.

[0064] In an embodiment, a metallization layer of an interconnect structure for a
20 semiconductor die includes a metal line disposed in a trench of an interlayer dielectric (ILD) material layer. The ILD material layer is composed of a first dielectric material. A conductive via is disposed in the ILD material layer, below and electrically connected to the metal line. A dielectric plug is directly adjacent to the metal line and the conductive via. The dielectric plug is composed of a second dielectric material different from the first dielectric material.

[0065] In one embodiment, the metal line and the conductive via are adjacent a first
25 sidewall of the dielectric plug. The metallization layer further includes a second metal line disposed in a second trench of the ILD material layer, directly adjacent a second, opposite, sidewall of the dielectric plug.

[0066] In one embodiment, the metallization layer further includes a second conductive
30 via disposed in the ILD material layer, below and electrically connected to the second metal line, and directly adjacent to the second sidewall of the dielectric plug.

[0067] In one embodiment, a portion of the ILD material layer is directly below the second metal line directly adjacent to the second sidewall of the dielectric plug.

[0068] In one embodiment, the dielectric plug includes a seam approximately in the
35 center of the dielectric plug.

[0069] In an embodiment, a metallization layer of an interconnect structure for a semiconductor die includes a metal line disposed in a trench of an interlayer dielectric (ILD) material layer. A conductive via is disposed in the ILD material layer, below and electrically connected to the metal line. A dielectric plug is directly adjacent to the metal line and the
5 conductive via. The dielectric plug includes a seam approximately in the center of the dielectric plug.

[0070] In one embodiment, the metal line and the conductive via are adjacent a first sidewall of the dielectric plug. The metallization layer further includes a second metal line disposed in a second trench of the ILD material layer, directly adjacent a second, opposite,
10 sidewall of the dielectric plug.

[0071] In one embodiment, the metallization layer further includes a second conductive via disposed in the ILD material layer, below and electrically connected to the second metal line, and directly adjacent to the second sidewall of the dielectric plug.

[0072] In one embodiment, a portion of the ILD material layer is directly below the
15 second metal line directly adjacent to the second sidewall of the dielectric plug.

[0073] In an embodiment, a method of fabricating a metallization layer of an interconnect structure for a semiconductor die includes forming a line trench in an upper portion of an interlayer dielectric (ILD) material layer formed above an underlying metallization layer. The method also includes forming a via trench in a lower portion of the ILD material layer, the
20 via trench exposing two metal lines of the underlying metallization layer. The method also includes forming a sacrificial material above the ILD material layer and in the line trench and the via trench. The method also includes patterning the sacrificial material to form an opening exposing a portion of the lower metallization layer between the two metal lines of the underlying metallization layer. The method also includes filling the opening of the sacrificial material with
25 a dielectric material. The method also includes removing the sacrificial material to provide a dielectric plug on the portion of the lower metallization layer between the two metal lines of the underlying metallization layer. The method also includes filling the line trench and the via trench with a conductive material.

[0074] In one embodiment, filling the line trench and the via trench with the conductive
30 material includes forming a first metal line in the line trench and a first conductive via in the via trench, the first metal line and the first conductive via directly adjacent to a first sidewall of the dielectric plug.

[0075] In one embodiment, filling the line trench and the via trench with the conductive material further includes forming a second metal line in the line trench and a second conductive
35 via in the via trench, the second metal line and the second conductive via directly adjacent to a second sidewall of the dielectric plug opposite the first sidewall.

[0076] In one embodiment, filling the opening of the sacrificial material with the dielectric material includes using a deposition process selected from the group consisting of atomic layer deposition (ALD) and chemical vapor deposition (CVD).

5 [0077] In one embodiment, filling the opening of the sacrificial material with the dielectric material includes forming a seam in the dielectric material approximately in the center of the dielectric plug.

[0078] In one embodiment, filling the opening of the sacrificial material with the dielectric material includes filling with a first dielectric material composition.

10 [0079] In one embodiment, the ILD material layer includes a second dielectric material composition different from the first dielectric material composition.

[0080] In one embodiment, the ILD material layer includes the first dielectric material composition.

15 [0081] In one embodiment, patterning the sacrificial material includes forming a patterned hardmask on the sacrificial material and transferring a pattern of patterned hardmask to the sacrificial material by an etch process.

[0082] In one embodiment, removing the sacrificial material includes planarizing the sacrificial material and the dielectric material and then selectively etching away remaining portions of the sacrificial material.

20 [0083] In an embodiment, a method of fabricating a metallization layer of an interconnect structure for a semiconductor die includes forming a line trench in an upper portion of an interlayer dielectric (ILD) material layer formed above an underlying metallization layer. The method also includes forming a sacrificial material above the ILD material layer and in the line trench. The method also includes patterning the sacrificial material to form an opening exposing a portion of a lower portion of the ILD material layer. The method also includes filling
25 the opening of the sacrificial material with a dielectric material. The method also includes removing the sacrificial material to provide a dielectric plug on the portion of the lower portion of the ILD material layer. The method also includes filling the line trench with a conductive material.

30 [0084] In one embodiment, filling the line trench with the conductive material includes forming a first metal line in the line directly adjacent to a first sidewall of the dielectric plug and forming a second metal line in the line trench directly adjacent to a second sidewall of the dielectric plug opposite the first sidewall.

35 [0085] In one embodiment, filling the opening of the sacrificial material with the dielectric material includes using a deposition process selected from the group consisting of atomic layer deposition (ALD) and chemical vapor deposition (CVD).

[0086] In one embodiment, filling the opening of the sacrificial material with the dielectric material includes forming a seam in the dielectric material approximately in the center of the dielectric plug.

5 [0087] In one embodiment, filling the opening of the sacrificial material with the dielectric material includes filling with a first dielectric material composition, and the ILD material layer includes a second dielectric material composition different from the first dielectric material composition.

10 [0088] In one embodiment, filling the opening of the sacrificial material with the dielectric material includes filling with a first dielectric material composition, and the ILD material layer includes the first dielectric material composition.

CLAIMS

What is claimed is:

1. A metallization layer of an interconnect structure for a semiconductor die, the metallization
5 layer comprising:
 - a metal line disposed in a trench of an interlayer dielectric (ILD) material layer, the ILD material layer comprising a first dielectric material;
 - a conductive via disposed in the ILD material layer, below and electrically connected to the metal line; and
 - 10 a dielectric plug directly adjacent to the metal line and the conductive via, the dielectric plug comprising a second dielectric material different from the first dielectric material.
2. The metallization layer of claim 1, wherein the metal line and the conductive via are adjacent a first sidewall of the dielectric plug, the metallization layer further comprising:
15 a second metal line disposed in a second trench of the ILD material layer, directly adjacent a second, opposite, sidewall of the dielectric plug.
3. The metallization layer of claim 1, further comprising:
 - a second conductive via disposed in the ILD material layer, below and electrically connected
20 to the second metal line, and directly adjacent to the second sidewall of the dielectric plug.
4. The metallization layer of claim 1, wherein a portion of the ILD material layer is directly below the second metal line directly adjacent to the second sidewall of the dielectric plug.
25
5. The metallization layer of claim 1, wherein the dielectric plug comprises a seam approximately in the center of the dielectric plug.
6. A metallization layer of an interconnect structure for a semiconductor die, the metallization
30 layer comprising:
 - a metal line disposed in a trench of an interlayer dielectric (ILD) material layer;
 - a conductive via disposed in the ILD material layer, below and electrically connected to the metal line; and
 - a dielectric plug directly adjacent to the metal line and the conductive via, the dielectric plug
35 comprising a seam approximately in the center of the dielectric plug.

7. The metallization layer of claim 6, wherein the metal line and the conductive via are adjacent a first sidewall of the dielectric plug, the metallization layer further comprising:

a second metal line disposed in a second trench of the ILD material layer, directly adjacent a second, opposite, sidewall of the dielectric plug.

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8. The metallization layer of claim 6, further comprising:

a second conductive via disposed in the ILD material layer, below and electrically connected to the second metal line, and directly adjacent to the second sidewall of the dielectric plug.

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9. The metallization layer of claim 6, wherein a portion of the ILD material layer is directly below the second metal line directly adjacent to the second sidewall of the dielectric plug.

10. A method of fabricating a metallization layer of an interconnect structure for a

15 semiconductor die, the method comprising:

forming a line trench in an upper portion of an interlayer dielectric (ILD) material layer formed above an underlying metallization layer;

forming a via trench in a lower portion of the ILD material layer, the via trench exposing two metal lines of the underlying metallization layer;

20 forming a sacrificial material above the ILD material layer and in the line trench and the via trench;

patterning the sacrificial material to form an opening exposing a portion of the lower metallization layer between the two metal lines of the underlying metallization layer;

filling the opening of the sacrificial material with a dielectric material;

25 removing the sacrificial material to provide a dielectric plug on the portion of the lower metallization layer between the two metal lines of the underlying metallization layer; and filling the line trench and the via trench with a conductive material.

11. The method of claim 10, wherein filling the line trench and the via trench with the

30 conductive material comprises forming a first metal line in the line trench and a first conductive via in the via trench, the first metal line and the first conductive via directly adjacent to a first sidewall of the dielectric plug.

12. The method of claim 11, wherein filling the line trench and the via trench with the

35 conductive material further comprises forming a second metal line in the line trench and a

second conductive via in the via trench, the second metal line and the second conductive via directly adjacent to a second sidewall of the dielectric plug opposite the first sidewall.

13. The method of claim 10, wherein filling the opening of the sacrificial material with the dielectric material comprises using a deposition process selected from the group consisting of atomic layer deposition (ALD) and chemical vapor deposition (CVD).

14. The method of claim 13, wherein filling the opening of the sacrificial material with the dielectric material comprises forming a seam in the dielectric material approximately in the center of the dielectric plug.

15. The method of claim 10, wherein filling the opening of the sacrificial material with the dielectric material comprises filling with a first dielectric material composition.

16. The method of claim 15, wherein the ILD material layer comprises a second dielectric material composition different from the first dielectric material composition.

17. The method of claim 15, wherein the ILD material layer comprises the first dielectric material composition.

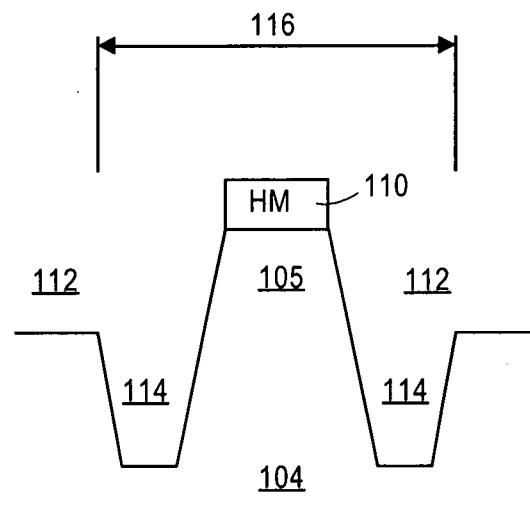
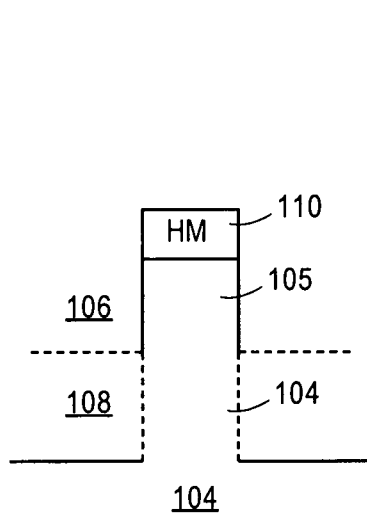
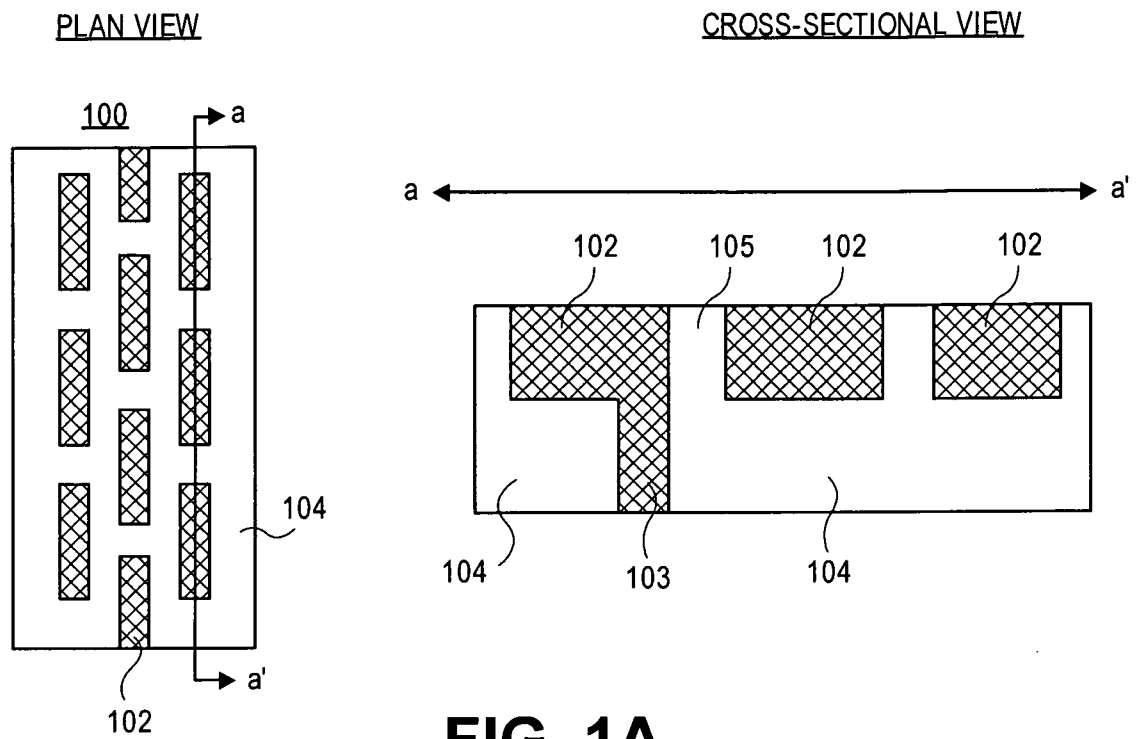
18. The method of claim 10, wherein patterning the sacrificial material comprises forming a patterned hardmask on the sacrificial material and transferring a pattern of patterned hardmask to the sacrificial material by an etch process.

19. The method of claim 10, wherein removing the sacrificial material comprises planarizing the sacrificial material and the dielectric material and then selectively etching away remaining portions of the sacrificial material.

20. A method of fabricating a metallization layer of an interconnect structure for a semiconductor die, the method comprising:
forming a line trench in an upper portion of an interlayer dielectric (ILD) material layer formed above an underlying metallization layer;
forming a sacrificial material above the ILD material layer and in the line trench;
patterning the sacrificial material to form an opening exposing a portion of a lower portion of the ILD material layer;
filling the opening of the sacrificial material with a dielectric material;

removing the sacrificial material to provide a dielectric plug on the portion of the lower portion of the ILD material layer; and
filling the line trench with a conductive material.

- 5 21. The method of claim 20, wherein filling the line trench with the conductive material comprises forming a first metal line in the line directly adjacent to a first sidewall of the dielectric plug and forming a second metal line in the line trench directly adjacent to a second sidewall of the dielectric plug opposite the first sidewall.
- 10 22. The method of claim 20, wherein filling the opening of the sacrificial material with the dielectric material comprises using a deposition process selected from the group consisting of atomic layer deposition (ALD) and chemical vapor deposition (CVD).
- 15 23. The method of claim 22, wherein filling the opening of the sacrificial material with the dielectric material comprises forming a seam in the dielectric material approximately in the center of the dielectric plug.
- 20 24. The method of claim 20, wherein filling the opening of the sacrificial material with the dielectric material comprises filling with a first dielectric material composition, and the ILD material layer comprises a second dielectric material composition different from the first dielectric material composition.
- 25 25. The method of claim 20, wherein filling the opening of the sacrificial material with the dielectric material comprises filling with a first dielectric material composition, and the ILD material layer comprises the first dielectric material composition.



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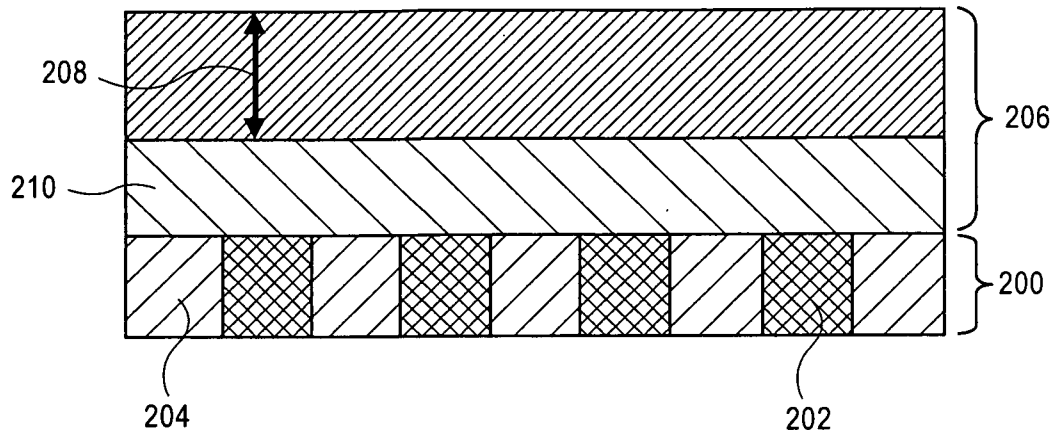


FIG. 2A

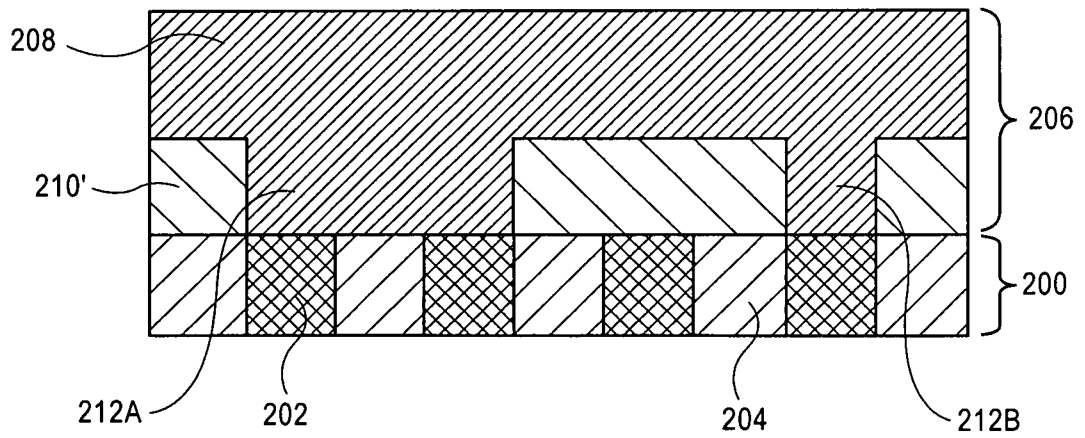
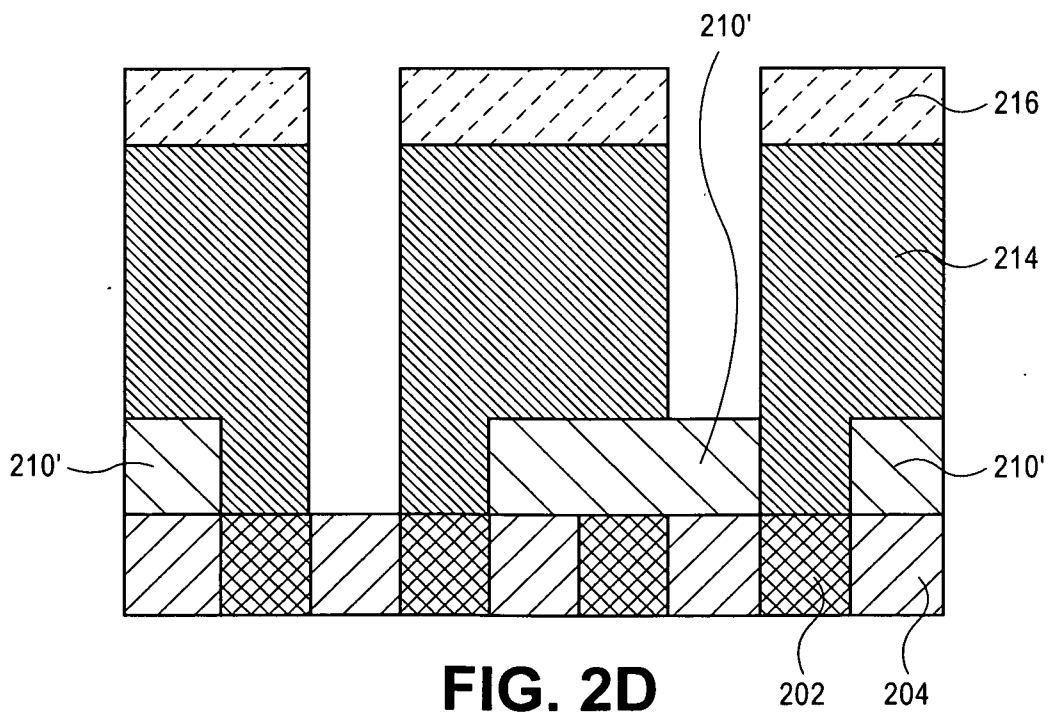
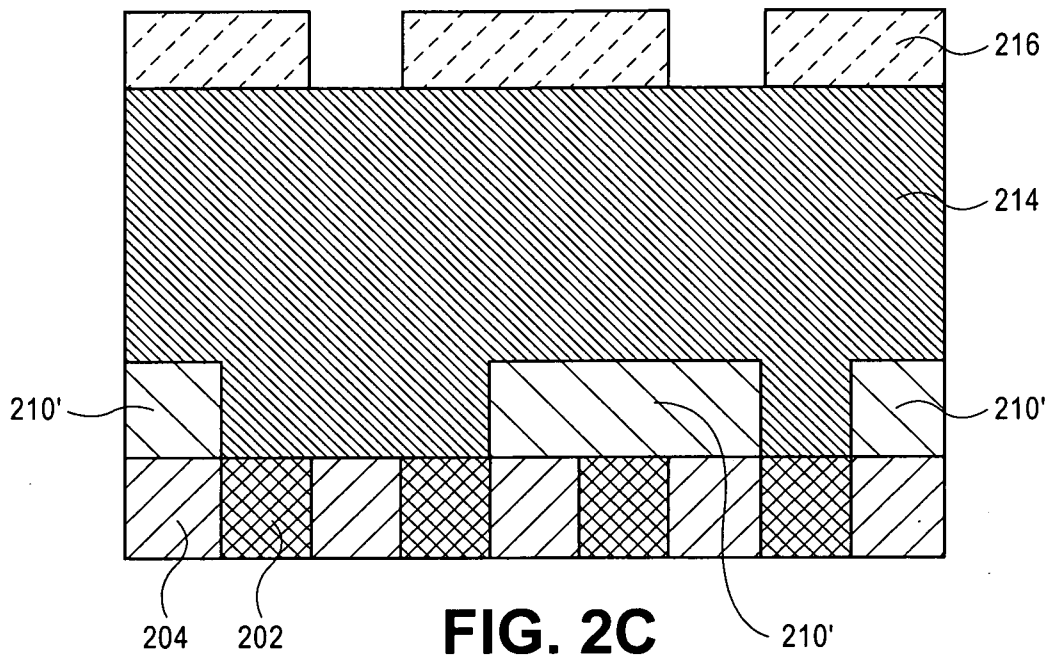


FIG. 2B

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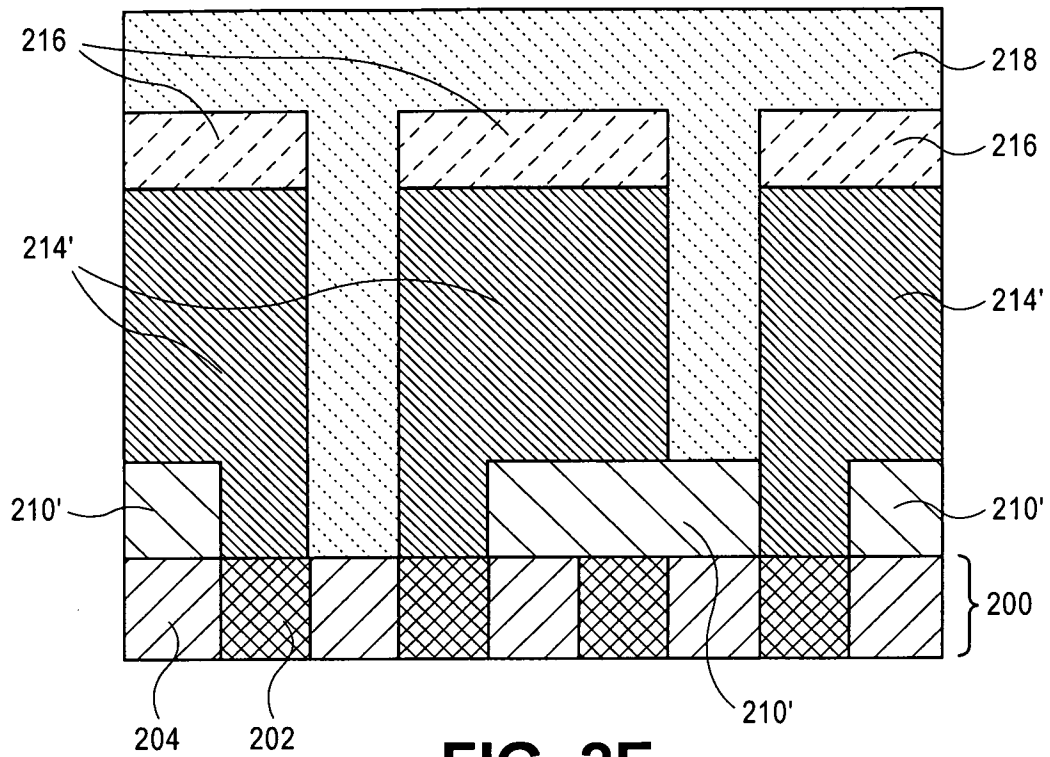


FIG. 2E

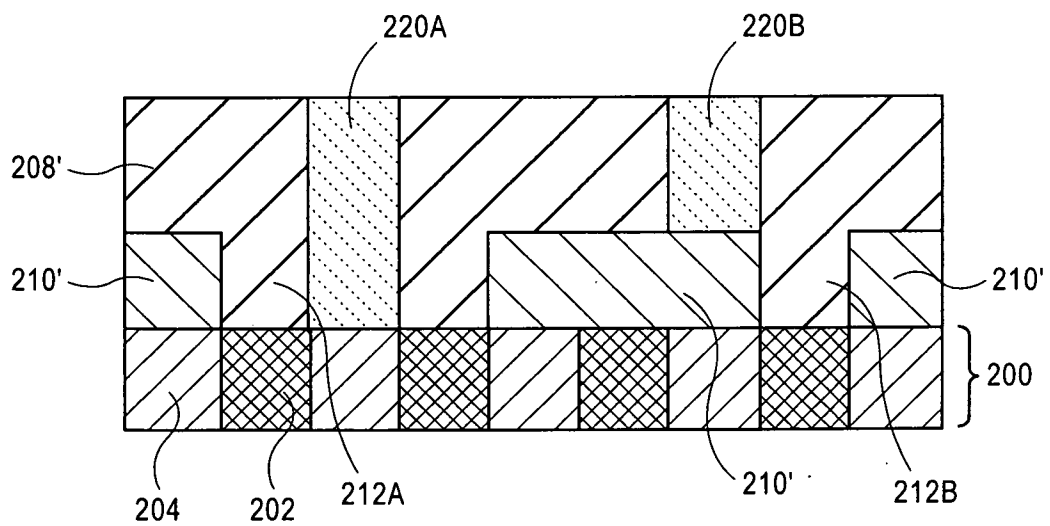
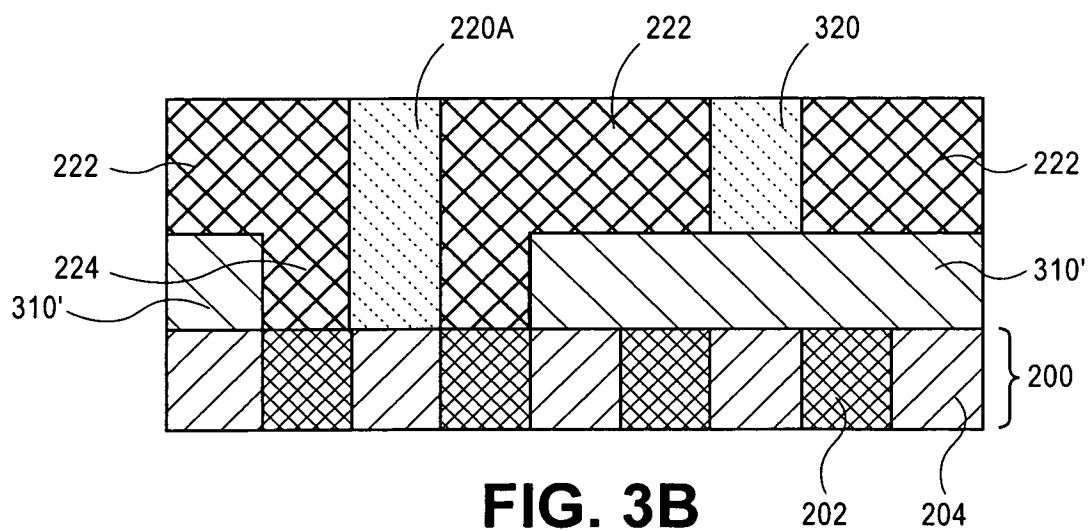
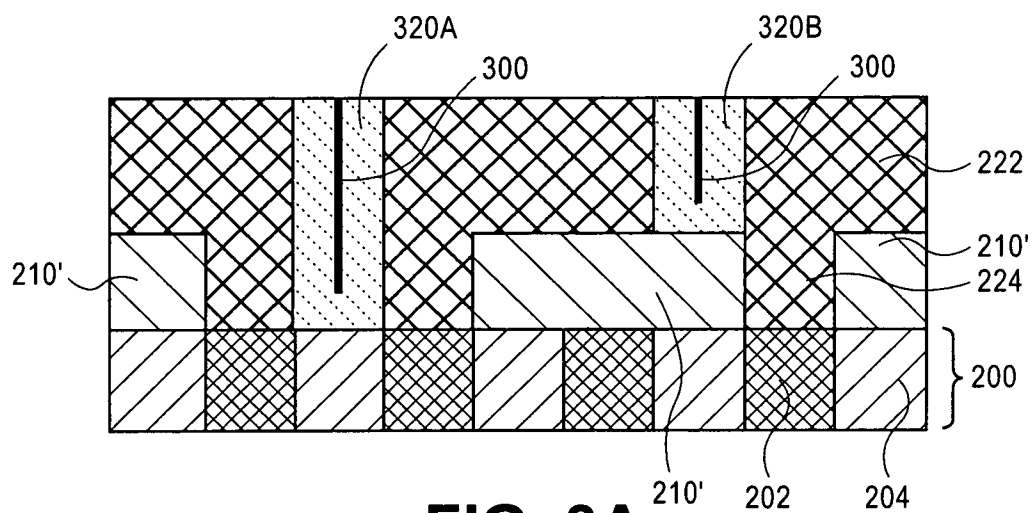
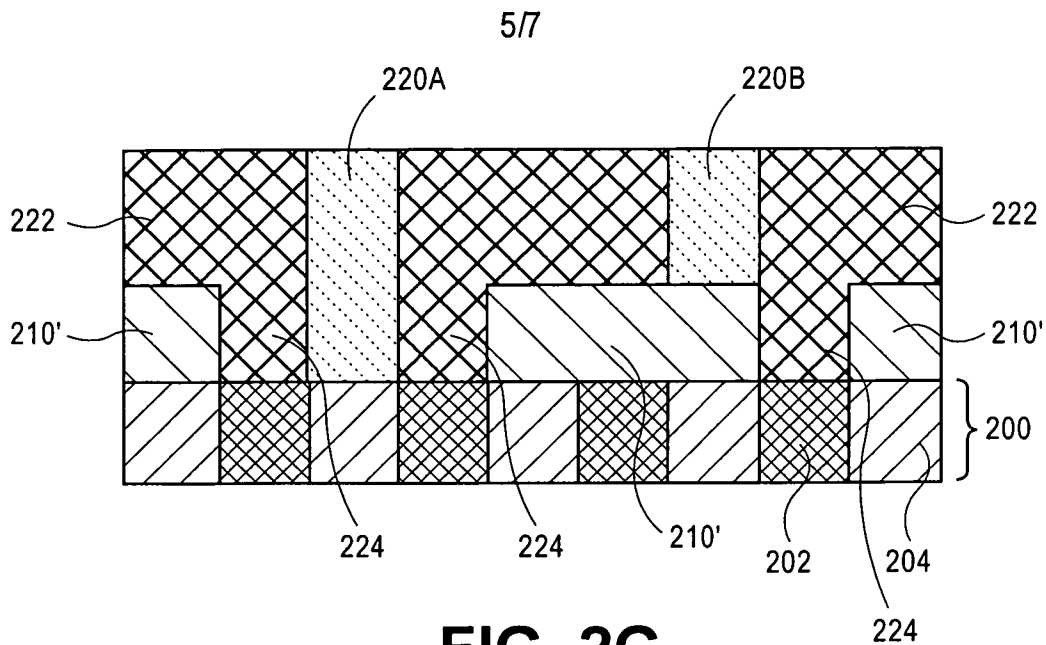


FIG. 2F



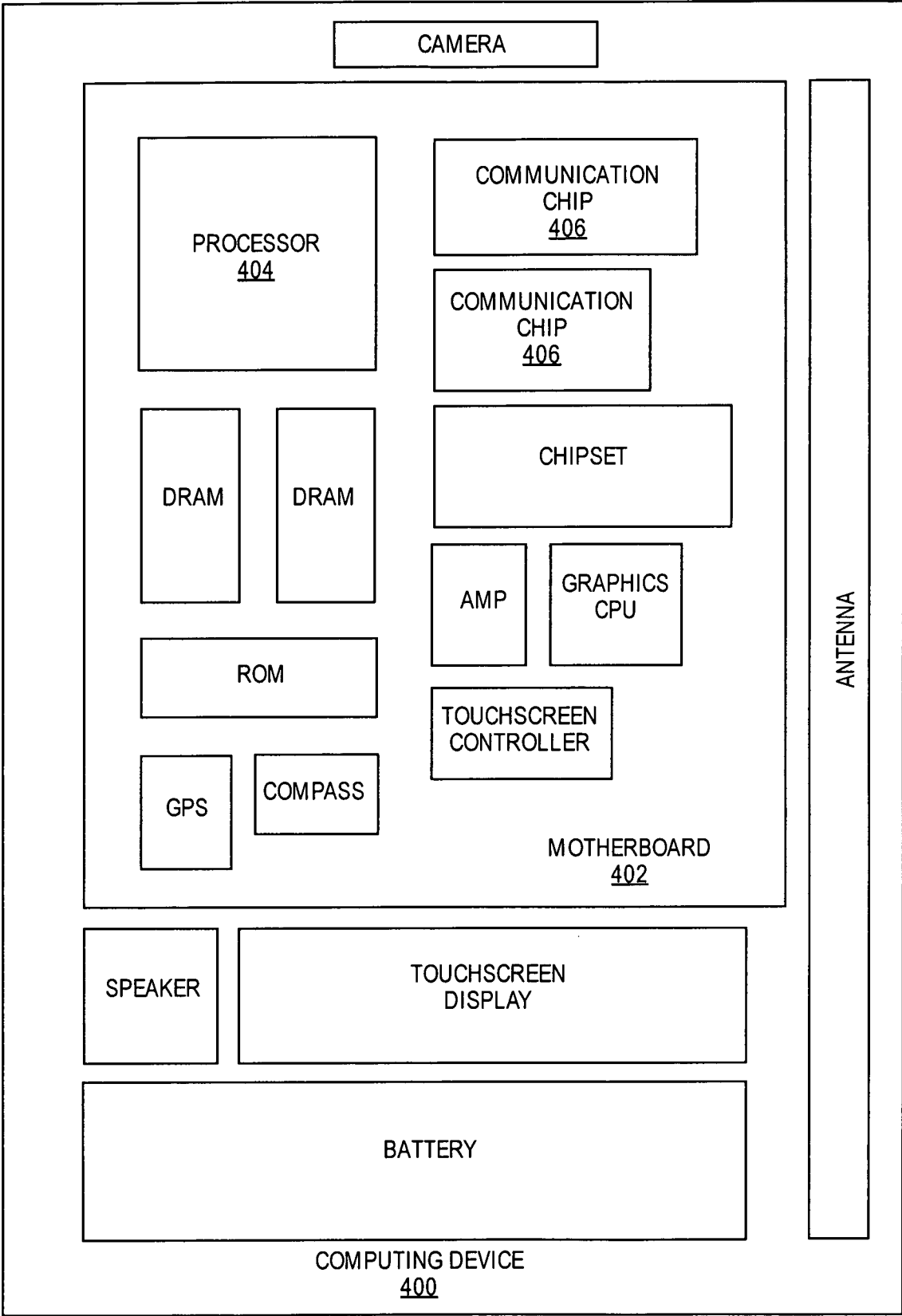
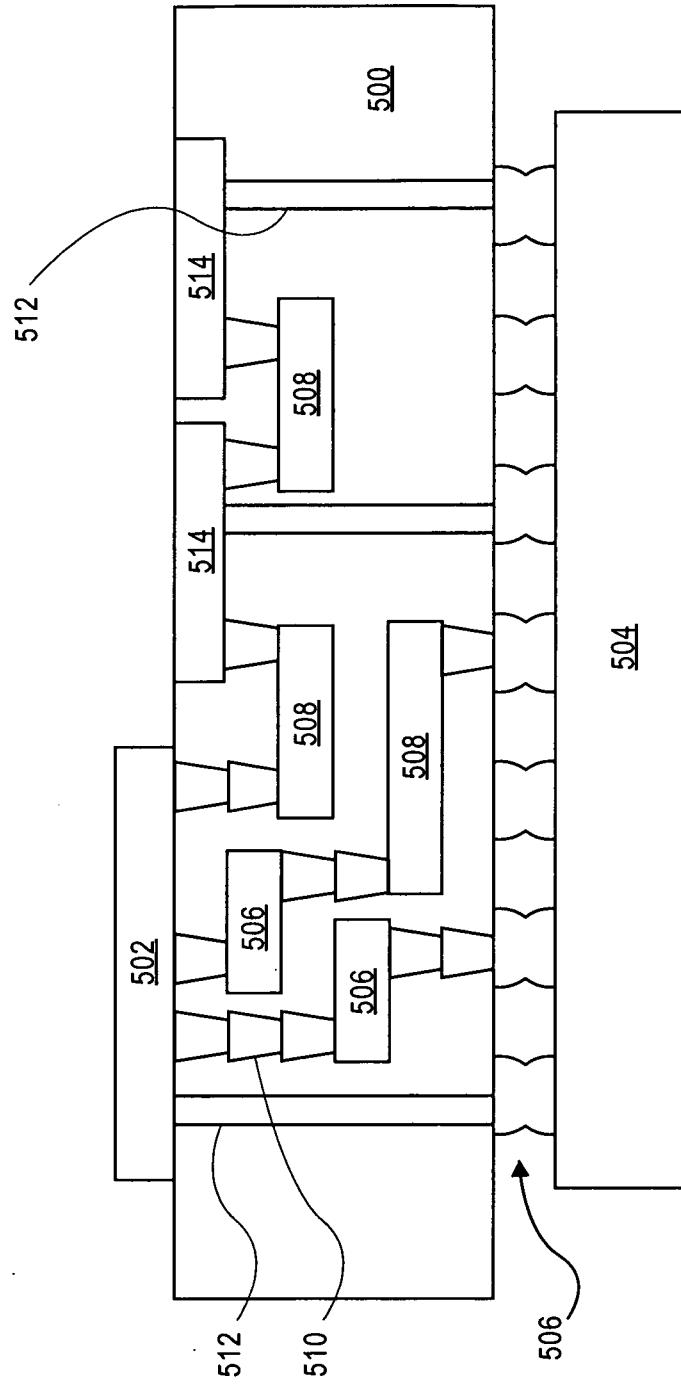


FIG. 4

**FIG. 5**

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/768(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/768; H01L 23/48; H01L 29/40; H01L 23/498; H01L 23/522; H01L 23/532

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: dielectric, contact, metal, interconnect, etch, seam

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015-0102496 A1 (STMICROELECTRONICS, INC.) 16 April 2015 See abstract, paragraphs [0029]-[0071] and figures 2-14.	1-19
A		20-25
A	US 2005-0263896 A1 (WATER LUR et al.) 01 December 2005 See abstract, paragraphs [0040]-[0047] and figures 4-8.	1-25
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A	US 2002-0130416 A1 (SHI-QING WANG et al.) 19 September 2002 See abstract, paragraphs [0099]-[0115] and figures 3-10.	1-25
A	US 2010-0133694 A1 (KARL W. BARTH et al.) 03 June 2010 See abstract, paragraphs [0019]-[0026] and figures 1-6.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

22 September 2016 (22.09.2016)

Date of mailing of the international search report

22 September 2016 (22.09.2016)

Name and mailing address of the ISA/KR

International Application Division

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189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/000492

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