Method for driving a three-electrode plasma display panel with application of DC voltage to address electrodes during the sustain period

The present invention relates to a plasma display panel, and more particularly, to a method for driving a plasma display panel. The driving method of the plasma display panel according to the present invention comprises the steps of: supplying alternately a sustain pulse to a scanning electrode and a sustain electrode during a sustain period; and supplying a DC voltage of positive polarity to an address electrode during a part of the sustain period. According to the driving method of the plasma display panel of the present invention, it is possible to achieve a stable address discharge and to prevent the damage of the circuit components and the erroneous discharge owing to excessive voltage fluctuation.

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<td>Priority:</td>
<td>05.06.2003 KR 2003036300</td>
</tr>
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**Fig. 6**

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<table>
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<tr>
<td>Y</td>
<td></td>
<td></td>
<td>A</td>
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<tr>
<td>Z</td>
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subfield
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Description


BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a plasma display panel, and more particularly, to a method for driving a plasma display panel.

Description of the Background Art

[0003] A plasma display panel (hereinafter, referred to as a "PDP") is adapted to display an image by light-emitting phosphors with ultraviolet rays generated during the discharge of an inert mixed gas such as He+Xe, Ne+Xe or He+Ne+Xe, or the like. This PDP can be easily made thin and large, and it can provide greatly increased image quality with the recent development of the relevant technology.

[0004] Referring now to FIG. 1, a discharge cell of a three-electrode AC surface discharge type PDP includes a scan electrode 30Y and a sustain electrode 30Z which are formed on the bottom surface of an upper substrate 10, and an address electrode 20X formed on a lower substrate 18. Each of the scan electrode 30Y and the sustain electrode 30Z include transparent electrodes 1 Y and 12Z, and metal bus electrodes 13Y and 13Z which have a line width smaller than that of the transparent electrodes 12Y and 12Z and are respectively disposed at one side edges of the transparent electrodes. The transparent electrodes 12Y and 12Z, which are generally made of ITO (indium tin oxide), are formed on the bottom surface of the upper substrate 10. The metal bus electrodes 13Y and 13Z, which are generally made of metal such as chromium (Cr), are formed on the transparent electrodes 12Y and 12Z, and serves to reduce a voltage drop caused by the transparent electrodes 12Y and 12Z having high resistance.

[0005] On the bottom surface of the upper substrate 10 in which the scan electrode 30Y and the sustain electrode 30Z are placed parallel to each other, is laminated an upper dielectric layer 14 and a protective layer 16. The upper dielectric layer 14 is accumulated with a wall charge generated during plasma discharging. The protective layer 16 is adapted to prevent damages of the upper dielectric layer 14 due to sputtering caused during plasma discharging, and improve efficiency of secondary electron emission. As the protective layer 16, magnesium oxide (MgO) is generally used.

[0006] A lower dielectric layer 22 and a barrier rib 24 are formed on the lower substrate 18 in which the address electrode 20X is formed. A phosphor layer 26 is applied to the surfaces of both the lower dielectric layer 22 and the barrier rib 24. The address electrode 20X is formed in the direction of crossing the scan electrode 30Y and the sustain electrode 30Z. The barrier rib 24 is disposed in parallel with the address electrode 20X and prevents ultraviolet rays and visible lights to be caused during plasma discharging from getting leaked to an adjacent discharge cells. The phosphor layer 26 is excited with an ultraviolet ray generated during the plasma discharging to generate any one visible light of red, green and blue lights. An inert mixed gas is injected into the discharge spaces defined between the upper substrate 10 and the barrier ribs 24 and between the lower substrate 18 and the barrier ribs 24.

[0007] In this PDP, one frame is divided into a plurality of sub-fields which having different luminance frequencies and is driven with time division, thereby implementing the gradation of image. Each of sub-fields are divided into an initialization period for initializing an entire screen, an address period for selecting an address line, and a sustain period for implementing gradation of image in response to the luminance frequency. Herein, the initialization period consists of a setup period which provided with a rising ramp waveform and a setdown period which provided with a falling ramp waveform.

[0008] For example, when displaying an image with 256-level gray scale, a period (16.67ms) of one frame that corresponds to 1/60 second is divided into eight sub-fields (SF1 to SF8), as shown in FIG. 2. Each of the eight sub-fields (SF1 to SF8) consists of the initialization period, the address period, and the sustain period, as mentioned above. The initialization periods and the address periods of each of the sub-fields have equal intervals. But the sustain periods of each of the sub-fields have increasing intervals in the ratio of $2^n (n = 0, 1 , 2, 3, 4, 5, 6, 7)$.

[0009] FIG. 3 shows a driving waveform of PDP which provided to two sub-fields.

[0010] In FIG. 3, Y indicates a scanning electrode and Z indicates a sustain electrode, and X indicates an address electrode.

[0011] Referring to FIG. 3, a PDP is driven with a reset period for initializing an entire screen and an address period for selecting a cell, and a sustain period for maintaining the discharge of the selected cell.

[0012] In the reset period, a rising ramp waveform (Ramp-up) is applied to all scanning electrodes Y during a setup period. This rising ramp waveform (Ramp-up) makes the cells of the entire screen to generate a weak discharge, thereby forming a wall charge in the cells. In the setdown period, after being provided with the rising ramp waveform (Ramp-up), a falling ramp waveform (Ramp-down) which is falling in the positive polarity lower than a peak voltage of the rising ramp waveform (Ramp-up) is applied to the scanning electrodes Y, simultaneously. The falling ramp waveform (Ramp-down)
makes the cells to generate a weak discharge, so that an unnecessary charge of wall charge and space charge generated by the setup discharge may be removed and a wall charge which is necessary for address discharge in the cells of the entire screen may be remained uniformly.

In the address period, scan pulses (scan) of a negative polarity are sequentially applied to the scanning electrodes Y, and in the same time, data pulses (data) of positive polarity are applied to the address electrodes X. A voltage difference between the scan pulses (scan) and the data pulses (data) is added to the wall charge generated during the initialization period, so that an address discharge may be generated in the cells to which the data pulses (data) are applied. Therefore, a wall charge generates in the cells selected by the address discharge.

On the other hand, during the setdown period and the address period, the sustain electrodes Z is provided with a DC voltage of positive polarity having a sustain voltage level Vs.

In the sustain period, sustain pulses (sus) are alternatively applied to the scanning electrodes Y and the sustain electrodes Z. Then, the cells selected by the address discharge are added with the wall voltage and sustain pulses (sus) in the cells, so that a sustain discharge may be generated in the form of surface discharge between the scanning electrode Y and the sustain electrode Z whenever the application of the sustain pulses (sus). Finally, after completion of the sustain discharge, the sustain electrode Z is supplied with an erasing ramp waveform (erase) having small pulse width, and the wall charge in the cells is erased the erasing ramp waveform.

However, the conventional PDPs have problems in that a discharge efficiency become lower by the wall charge to be formed in the address electrode X. More specifically, the address electrodes X maintains a base potential during the sustain period that the sustain pulses is alternatively supplied to the scanning electrodes Y and the sustain electrodes Z.

Herein, the address electrodes X maintaining the base potential are accumulated with predetermined wall charges generated from the sustain discharge. This wall charges causes the sustain discharge having a low luminance efficiency. In practical, the wall charges formed in the address electrodes X have a wall voltage that is equal to around half voltage of the sustain pulses.

In order to solve this problem, it has proposed that the address electrodes X are supplied with a DC voltage of positive polarity having an address voltage level Va during a sustain period, as shown in FIG. 4. When the address electrodes X are supplied with the DC voltage of positive polarity during the sustain period, the Wall charges generated in the address electrodes X become minimized, the driving efficiency becomes higher, accordingly. In other words, a stable sustain discharge is achieved by lowering the wall voltage of the wall charges formed in the address electrodes X. Practically, it has experimentally proved that the driving efficiency of PDP is improved when the address electrodes X had been supplied with the DC voltage of positive polarity during the sustain period.

However, a driving method shown in FIG. 4 has a problem that an erroneous discharge is generated when there are both a selective write subfield and a selective erase sub-field. Referring to FIG. 5, the selective erase sub-fields are consisted of the address period and the sustain period, thus the address discharge of the address period is followed immediately after completion of the sustain period. Herein, in order to higher the driving efficiency, if the address electrodes X is supplied with the DC voltage of positive polarity having the address voltage level during the sustain period in the sub-fields before beginning of the selective erase sub-fields, a discharge condition is changed. Therefore, an amount of the wall charges of positive polarity which is accumulated in the address electrodes X may be decreased accordingly, and in the subsequent address period, the amount of the wall voltage in the address electrodes X becomes insufficient, thereby generating an erroneous discharge.

**SUMMARY OF THE INVENTION**

Accordingly, an object of the present invention is to solve at least the problems and disadvantages of the background art.

An object of the present invention is to provide a method for driving a plasma display panel which can improve a driving efficiency and prevent an erroneous discharge.

According to an embodiment of the present invention, a method for driving a plasma display panel comprises the steps of: supplying alternately a sustain pulse to a scanning electrode and a sustain electrode during a sustain period; and supplying a DC voltage of positive polarity to an address electrode during a part of the sustain period.

**BRIEF DESCRIPTION OF THE DRAWINGS**

The invention will be described in detail with reference to the following drawings in which like numerals refer to like elements.

FIG. 1 is a perspective view showing the configuration of a discharge cell of a conventional three-electrode AC surface discharge type plasma display panel.

FIG. 2 is a diagram showing a frame of a plasma display panel shown in FIG. 1.

FIG. 3 is a waveform diagram showing an driving waveform applied to a plasma display panel shown in FIG. 1.

FIG. 4 is a waveform diagram showing another driving waveform applied to a plasma display panel.
A method for driving a plasma display panel according to an embodiment of the present invention comprises the steps of supplying alternately a sustain pulse to a scanning electrode and a sustain electrode during a sustain period; and supplying a DC voltage of positive polarity to an address electrode during a part of the sustain period.

In the method for driving a display panel, the DC voltage of positive polarity is supplied during a period with the exception of a latter part of the sustain period.

In the method for driving a plasma display panel, the latter part of the sustain period is a period including at least one sustain pulse.

On the other hand, during the setdown period and the address period, the sustain electrodes Z are provided with a DC voltage of positive polarity having a sustain voltage level Vs.

In the sustain period, sustain pulses (sus) are alternatively applied to the scanning electrodes Y and the sustain electrodes Z. And, the address electrodes X are applied with a DC voltage of positive polarity having the address voltage level Va before supplying of at least one sustain pulse, for example the last sustain pulse pair, during the sustain discharge. Then, the cells selected by the address discharge are added with the wall voltage and sustain pulses (sus) in the cells, so that a sustain discharge may be generated in the form of surface discharge between the scanning electrode Y and the sustain electrode Z whenever the application of the sustain pulses (sus). The address electrodes X are applied with the DC voltage of positive polarity having the address voltage level Va, and the wall charges are not accumulated in the address electrodes X, so the sustain discharge is more efficiently generated. Furthermore, even though the address electrodes X are applied with a base potential and the process is directly advanced from the address period to the selective erase sub-fields in at least one sustain pulse, for example the last sustain pulse pair, during the sustain discharge as shown in (A) of FIG. 6, the address discharge become implemented.
because the amount of wall voltage of the address electrodes X is sufficient.

[0046] More specifically, when the selective erase sub-fields follows the selective write sub-fields as shown in FIG. 7, the sustain period of the last selective write sub-fields may be regarded as a reset period for the first selective erase sub-fields subsequent following the last selective write sub-fields.

[0047] During this sustain period, a driving efficiency is improved by application the DC voltage of positive polarity having the address voltage level Va to the address electrodes X in order not to accumulate the wall charges to the address electrodes X. However, when the DC voltage of positive polarity having the address voltage level Va is applied to the address electrodes X, an amount of the wall charges which is accumulated in the address electrodes X may be decreased, accordingly, and then in the address discharge of the subsequent selective erase sub-fields, the amount of the wall voltage in the address electrodes X becomes insufficient, thereby generating an erroneous discharge. Therefore, as shown in FIG. 7, in at least one sustain pulse, for example the last sustain pulse pair, before completion of the sustain discharge of the last selective write sub-field immediately before proceeding to the selective erase sub-field, the address electrodes X is applied with a base potential as shown in (B) of FIG. 7. Consequently, since the address electrodes X are sufficiently accumulated with the wall charges, even though the process is directly advanced to the selective erase sub-fields in which the address period immediately begin, the stable address discharge can be achieved because the amount of wall voltage of the address electrodes X is sufficient.

[0048] On the other hand, the sustain pulses are normally supplied to the scanning electrodes Y and the sustain electrodes Z with alternation. The interval of two sustain pulses which are supplied alternatively is successively operated with the sustain operation without interruption. If any interruption time is obtained from the interval of two sustain pulses which are supplied alternatively, only very short time interval (around maximum few hundreds ns) will be possible. In the actual driving, it is very difficult to maintain a stable voltage owing to a discharge current and a rising phenomenon. Thus, in the operation period of the sustain pulse without interruption, if the DC voltage of positive polarity having the address voltage level Va applied to the address electrodes X is removed as in the first embodiment of the present invention, there may occur damage of the circuit components and erroneous discharge owing to excessive voltage fluctuation. Accordingly, a driving method as shown in FIG. 8 is proposed.

[0049] FIG. 8 is a diagram showing a method for driving a plasma display panel according to a second embodiment of the present invention.

[0050] Referring to FIG. 8, a PDP according to the second embodiment of the present invention is driven with a reset period for initializing an entire screen, an address period for selecting a cell, and a sustain period for maintaining discharge of the selected cells.

[0051] In the reset period, a rising ramp waveform (Ramp-up) is simultaneously applied to all scanning electrodes Y during a setup period. This rising ramp waveform (Ramp-up) causes a weak discharge within the cells of the entire screen, thereby forming a wall charge in the cells. In the setdown period, after being provided with the rising ramp waveform (Ramp-up), a falling ramp waveform (Ramp-down) which is falling in the positive polarity lower than a peak voltage of the rising ramp waveform (Ramp-up) is applied to the scanning electrodes Y, simultaneously. The falling ramp waveform (Ramp-down) causes a weak erase discharge within the cells, so that an unnecessary charge of wall charge and space charge generated by the setup discharge may be removed and a wall charge which is necessary for address discharge in the cells of the entire screen may be remained uniformly.

[0052] In the address period, scan pulses (scan) of a negative polarity are sequentially applied to the scanning electrodes Y, and in the same time, data pulses (data) of positive polarity are applied to the address electrodes X. A voltage difference between the scan pulses (scan) and the data pulses (data) is added to the wall charge generated during the initialization period, so that an address discharge may be generated in the cells to which the data pulses (data) are applied. Therefore, a wall charge generates in the cells selected by the address discharge.

[0053] On the other hand, during the setdown period and the address period, the sustain electrodes Z is provided with a DC voltage of positive polarity having a sustain voltage level Vs.

[0054] In the sustain period, a sustain pulses (sus) are alternatively applied to the scanning electrodes Y and the sustain electrodes Z. And, the address electrodes X are applied with a DC voltage of positive polarity having the address voltage level Va before supplying of at least one sustain pulse, for example the last sustain pulse pair, during the sustain discharge. In this time, during a predetermined interval (Δt) before and after the time when the DC voltage of positive polarity having the address voltage level Va applied to the address electrodes X is dropped to the base potential, a base potential is applied to the scanning electrodes Y and the sustain electrodes Z. Then, the cells selected by the address discharge are added with the wall voltage and sustain pulses (sus) in the cells, so that a sustain discharge may be generated in the form of surface discharge between the scanning electrode Y and the sustain electrode Z whenever the application of the sustain pulses (sus). The address electrodes X are applied with the DC voltage of positive polarity having the address voltage level Va, and the wall charges are not accumulated in the address electrodes X, so the sustain discharge is more efficiently generated. Furthermore, even though the process is directly advanced to the selective erase sub-fields.
in which the address period immediately begin by application of the base potential to the address electrodes X in at least one sustain pulse, for example the last sustain pulse pair, before completion of the sustain discharge as shown in (A) of FIG. 8, and by application the base potential to the scanning electrodes Y and the sustain electrodes Z during a predetermined interval (\(\Delta t\)) before and after the time when the DC voltage of positive polarity having the address voltage level \(Va\) applied to the address electrodes X is dropped to the base potential, not only it is possible to achieve the stable address discharge, but also it is possible to prevent the damage of the circuit components and the erroneous discharge owing to excessive voltage fluctuation, because the amount of wall voltage of the address electrodes X is sufficient.

More specifically, when the selective erase sub-fields follows the selective write sub-fields as shown in FIG. 9, the sustain period of the last selective write sub-fields may be regarded as a reset period for the first selective erase sub-fields following the last selective write sub-fields. During this sustain period, a driving efficiency is improved by application the DC voltage of positive polarity having the address voltage level \(Va\) to the address electrodes X in order not to accumulate the wall charges to the address electrodes X. However, when the DC voltage of positive polarity having the address voltage level \(Va\) is applied to the address electrodes X, an amount of the wall charges which is accumulated in the address electrodes X may be decreased accordingly, and when in the address discharge of the subsequent selective erase sub-fields, the amount of the wall voltage in the address electrodes X becomes insufficient, therefore the erroneous discharge may be caused. Furthermore, in the operation period of the sustain pulse without interruption, if the DC voltage of positive polarity having the address voltage level \(Va\) applied to the address electrodes X is removed, there may occur damage of the circuit components and the erroneous discharge owing to excessive voltage fluctuation. Therefore, as shown in FIG. 9, even though the process is directly advanced: to the selective erase sub-fields in which the address period immediately begin by application of the base potential to the address electrodes X in at least one sustain pulse, for example the last sustain pulse pair, before completion of the sustain discharge as shown in (D) of FIG. 9, and by application the base potential to the scanning electrodes Y and the sustain electrodes Z during a predetermined interval (\(\Delta t\)) before and after the time when the DC voltage of positive polarity having the address voltage level \(Va\) applied to the address electrodes X is dropped to the base potential, not only it is possible to achieve the stable address discharge, but it is also possible to prevent the damage of the circuit components and the erroneous discharge owing to excessive voltage fluctuation, because the amount of wall voltage of the address electrodes X is sufficient.

As described above, according to the driving method of the plasma display panel according to the present invention, in order to improve the driving efficiency, the base potential is applied in the period corresponding to the at least one sustain pulse before completion of the sustain discharge when the DC voltage of positive polarity having the address voltage level is supplied to the address electrodes during the sustain period, thereby stabilizing the subsequent address discharge.

Further, during a predetermined interval (\(\Delta t\)) before and after the time when the DC voltage of positive polarity having the address voltage level \(Va\) applied to the address electrodes X is dropped to the base potential, a base potential is applied to the scanning electrodes Y and the sustain electrodes Z, thereby preventing the damage of the circuit components and the erroneous discharge owing to excessive voltage fluctuation.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

The claims refer to examples of preferred embodiments of the invention. However, the invention also refers to combinations of any claim or claims with any other claim or claims and/or with any feature or combination of features which is or are disclosed in the description and/or in the drawings.

**Claims**

1. A method for driving a plasma display panel, comprising the steps of:
   - supplying alternately a sustain pulse to a scanning electrode and a sustain electrode during a sustain period; and
   - supplying a DC voltage of positive polarity to an address electrode during a part of the sustain period.

2. The method of claim 1, wherein the DC voltage of positive polarity is supplied during a period with the exception of a latter part of the sustain period.

3. The method of claim 2, wherein the latter part of the sustain period is a period including at least one sustain pulse.

4. The method of claim 3, wherein the latter part of the sustain period is supplied with a base potential of the address electrode.

5. The method of claim 4, wherein the base potential
is supplied to the scanning electrode and the sustain electrode when a voltage applied to the address electrode is changed from the DC voltage of positive polarity to the base potential.
Fig. 3

[Diagram showing a timeline for a process with labels such as Ramp-up, Ramp-down, Scan, Sus, erase, data, setup, address, sustain, reset, subfield 1, and subfield 2]
Fig. 4

Ramp-up

Ramp-down

Scan

Sus

data

set up

set down

address

sustain

reset

subfield
Fig. 6

Ramp-up

Ramp-down

Scan

Sus

Y

Z

X

setup

data

reset

address

sustain

subfield
Fig. 7

- Ramp-up
- Ramp-down
- Scan
- Sus
- B
- Va
- Setup
- Setdown
- Address
- Sustain
- Address
- Sustain
- Selective writing subfield
- Selective erasing subfield
Fig. 9