

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
16 March 2006 (16.03.2006)

PCT

(10) International Publication Number
WO 2006/028477 A1

(51) International Patent Classification: ⁷ G02F 1/035, G02B 6/13

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(21) International Application Number:
PCT/US2004/039419

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(22) International Filing Date:
24 November 2004 (24.11.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/607,691 7 September 2004 (07.09.2004) US

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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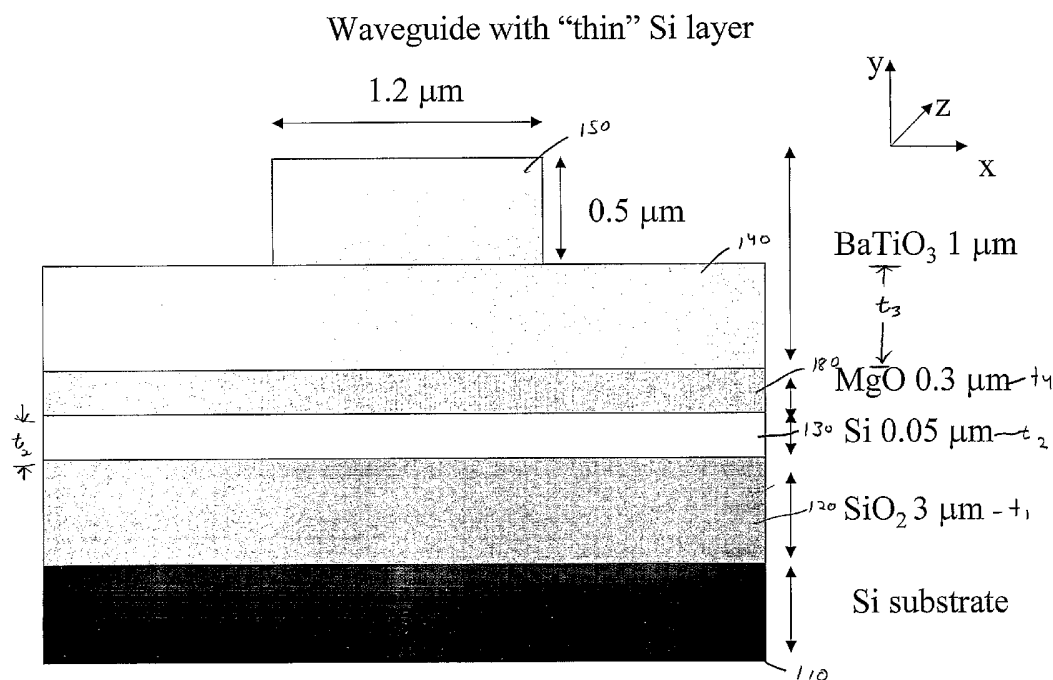
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Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: FABRICATION OF ELECTRO-OPTICAL STRUCTURES



(57) Abstract: Optical waveguide structures are formed over insulator layers. An electro-optical layer may be formed over a thin crystalline semiconductor layer.

FABRICATION OF ELECTRO-OPTICAL STRUCTURES

Related applications

This application claims the benefit of U.S. Provisional Application 60/607,691, filed September 7, 2004, the entire disclosure of which is hereby incorporated by reference.

Background

5 High quality electro-optical layers are needed for fabrication of optical waveguides. Such layers may include crystalline material formed over semiconductor substrates. Barium titanate (BaTiO_3 or, hereafter, BT), in particular, has attracted a great deal of attention in recent years for its electro-optic (E-O) and piezo-electric properties. Its large E-O coefficient, for example, may enable the fabrication of highly miniaturized optical modulators for fiber optic-
10 based data transmission systems.

To exploit the advantage of miniaturization, the integration of electro-optical layers onto semiconductor substrates, such as silicon (Si) substrates, is desirable. Silicon, in particular, represents an especially useful substrate material in that it can take the form of a high-quality single crystal and provides the basis for most microelectronics. The formation of electro-optical
15 layers directly on a bulk silicon substrate or on a thick silicon layer, however, may result in difficulties in confining light to the electro-optical layer due to possible losses to the underlying silicon material. The higher refractive index of silicon can draw light from an electro-optical waveguide, for example.

Summary

20 The present invention facilitates formation of electro-optical layers on semiconductor-on-insulator (SOI) substrates having thin crystalline top layers, with or without buffer layers. For example, highly oriented BaTiO_3 -based thin films, suitable for microphotonic application, may be grown and integrated onto Si wafers by utilization of silicon-on-insulator substrates. Such substrates generally include a relatively thin layer of crystalline semiconductor material,
25 such as silicon, over an insulator, which itself resides above a semiconductor, e.g., silicon, substrate. SOI structures have gained importance in the semiconductor industry because of their ability to limit transistor gate capacitance, thereby enabling faster switching speeds.

Preferably, several criteria should be satisfied when integrating electro-optical thin films onto semiconductor substrates. First, the electro-optical layer should be grown in an epitaxial

fashion, highly oriented along a crystalline direction, to provide a relatively high E-O effect. Preferably, the electro-optical layer is grown with a (001) orientation. Second, the electro-optical layer should be sufficiently spatially separated from the semiconductor substrate to optically decouple a device formed in the electro-optical film from the higher refractive index semiconductor substrate. This separation may be achieved by the formation of one or more layers between the substrate and the electro-optical layer. Lastly, the layer(s) separating the electro-optical layer from the underlying semiconductor substrate should have an index of refraction lower than that of the electro-optical layer to insure confinement of light within the subsequently formed waveguides, and should be chemically stable in contact with the electro-optical layer.

These criteria may be satisfied by the use of commercially available SOI wafers with a sufficiently thick insulator layer, e.g., an oxide layer, to optically decouple the E-O waveguide structures from the semiconductor substrate, and a thin, high-quality, single-crystalline semiconductor top layer, capable of initiating the growth of high quality epitaxial films thereover. A typical thickness of the insulator layer is from 1 to 3 micrometers (μm), although, for some applications, the required insulator thickness may be as high as 10 μm . However, if the top crystalline semiconductor layer of an SOI wafer is too thick, e.g., > 100 nanometers (nm), light leakage may result from the electro-optical layer into the crystalline semiconductor top layer. One solution to this problem is to insert another buffer layer between the electro-optical and the crystalline semiconductor top layer sufficiently thick to optically decouple these layers. This solution, however, may introduce additional complexity into the waveguide design and fabrication process. Moreover, because the thick intermediate oxide of the SOI wafer already serves to decouple the electro-optical layer from the underlying semiconductor substrate, the buffer layer(s) are not needed for decoupling the electro-optical layer from the underlying semiconductor substrate.

On the other hand, it has been found that a crystalline semiconductor layer having a thickness no greater than 100 nm may prevent light leakage between the electro-optical layer and the top crystalline semiconductor layer. In some embodiments, the original crystalline semiconductor layer is no thicker than 100 nm, while in other embodiments, the layer is thinned to a suitable thickness (e.g., less than or equal to about 50 nm). In still other embodiments, the crystalline semiconductor layer is oxidized completely during or subsequent to the process of depositing buffer or electro-optical layers.

In accordance with the invention, a semiconductor crystalline layer no thicker than about

100 nm placed over an insulating layer provides a suitable basis for growing an electro-optical crystalline layer and at the same time has no significant optical effects on the optical radiation propagating in the electro-optical crystalline layer.

In one aspect, therefore, the invention features an optical waveguide structure that
5 includes a semiconductor substrate, an insulator layer disposed over the semiconductor substrate, a crystalline semiconductor layer disposed over the insulator layer, and an electro-optical layer disposed over the crystalline semiconductor layer. The crystalline semiconductor layer desirably has a thickness less than or equal to approximately 100 nm.

The electro-optical layer may include at least one of BaTiO₃, PbTiO₃, (Pb,La)TiO₃,
10 (Pb,Zr)TiO₃, (Pb,La)(Zr,Ti)O₃, ZrTiO₃, LaZrTiO₃, LiNbO₃, LiTaO₃, Sr_xBa_{1-x}Nb₂O₆ (SBN:x), Ba_{1-x}Ca_xTiO₃ with x selected from a range of about 0.2 to about 0.5, KNbO₃, and KNbTaO₃, and may have a thickness ranging from about 500 nm to about 1000 nm. The electro-optical layer may also be thicker or thinner depending on the specific waveguide. For a ridge waveguide, a thickness ranging from 300 nm to about 2 μm is preferred; for an indiffused waveguide, a higher
15 thickness may be needed, i.e., 10 μm. The crystalline semiconductor layer includes a semiconductor material, such as silicon, and its thickness may be less than approximately 100 nm and, more desirably, no greater than 50 nm.

A first buffer layer may be disposed between the electro-optical layer and the crystalline semiconductor layer. The first buffer layer may include at least one of MgO, MgAl₂O₄, Al₂O₃,
20 LaAlO₃, LSAT (LaAlO₃)_{0.3}(Sr₂AlTaO₆)_{0.7}, CeO₂, Y₂O₃, YSZ, BaO, SrO, Ba_{1-x}Sr_xO, SrTiO₃, Pb_xBa_{1-x}TiO₃, BaTiO₃, and Ba_{1-x}Sr_xTiO₃. The thickness of the first buffer layer may be selected from a range of approximately 30 nm to approximately 3000 nm. A first buffer layer thickness below 500 nm helps to achieve a high quality, highly oriented electro-optical layer. Moreover, in contrast to a thicker film, less process time is necessary to grow a thin layer, the thickness may
25 be more uniform, and the thin layer is more likely to be dislocation-free.

A second buffer layer may be disposed over the first buffer layer. The second buffer layer may include at least one of MgO, MgAl₂O₄, Al₂O₃, LaAlO₃, LSAT
(LaAlO₃)_{0.3}(Sr₂AlTaO₆)_{0.7}, CeO₂, Y₂O₃, YSZ, BaO, SrO, Ba_{1-x}Sr_xO, SrTiO₃, Pb_xBa_{1-x}TiO₃, BaTiO₃, and Ba_{1-x}Sr_xTiO₃. The second buffer layer may have a thickness selected from a range
30 of about 10 nm to about 3000 nm.

A ridge layer may be disposed over the electro-optical layer. The ridge layer may include a dielectric material, such as at least one of Si₃N₄, silicon-rich nitride (SiN), hydrogensilsesquioxanes (HSQ), SiO₂, yttrium-stabilized zirconia (YSZ), CeO₂, MgO, BaO,

SrO, $\text{Ba}_{1-x}\text{Sr}_x\text{O}$, MgAl_2O_4 , LaAlO_3 , LSAT (LaAlO_3)_{0.3}($\text{Sr}_2\text{AlTaO}_6$)_{0.7}, Al_2O_3 , Y_2O_3 , BaTiO_3 , PbTiO_3 , $(\text{Pb},\text{La})\text{TiO}_3$, $(\text{Pb},\text{Zr})\text{TiO}_3$, $(\text{Pb},\text{La})(\text{Zr},\text{Ti})\text{O}_3$, ZrTiO_3 , LaZrTiO_3 , LiNbO_3 , LiTaO_3 , $\text{Sr}_x\text{Ba}_{1-x}\text{Nb}_2\text{O}_6$ (SBN:x), $\text{Ba}_{1-x}\text{Ca}_x\text{TiO}_3$ with x selected from a range of about 0.2 to about 0.5, KNbO_3 , and KNbTaO_3 .

5 A ridge may be defined by a lift-off technique, an etch step, and/or transforming a portion of an HSQ layer into silicon dioxide. The ridge material and method of ridge formation may be selected to define a ridge with relatively smooth sidewalls, thereby enhancing light confinement. The ridge-material may include a material with an index of refraction similar to that of the electro-optical layer.

10 A cladding layer may be disposed over the electro-optical layer and the ridge layer. The cladding layer should have an index of refraction lower than that of the electro-optical layer, and may include at least one of silicon dioxide, Si_3N_4 , SiN, HSQ, a polymer, MgO, and Al_2O_3 .

 In typical applications, one or more electrodes are disposed in electrical communication with the electro-optical layer.

15 The insulator layer may be amorphous. The insulator layer may include silicon dioxide, silicon nitride, aluminum oxide, and/or magnesium oxide.

 In another aspect, an optical waveguide structure includes an amorphous insulator layer, and an electro-optical layer in contact with the amorphous insulator layer.

 In another aspect, the invention features a method for forming an optical waveguide
20 structure, including the steps of (i) providing an insulator layer, and a crystalline semiconductor layer disposed over the insulator layer; (ii) forming an electro-optical layer over the crystalline semiconductor layer; and (iii) controlling the thickness of the crystalline semiconductor layer to be no greater than about 100 nm.

 Forming the electro-optical layer may include selecting a crystallographic orientation of
25 the electro-optical layer, such as by growing the electro-optical layer in the preferred crystallographic orientation, or by poling and/or cleaving. The crystallographic direction may be determined by a crystallographic orientation of the crystalline semiconductor layer. The electro-optical layer may be formed using at least one of physical vapor deposition, chemical vapor deposition, atomic layer deposition, molecular beam epitaxy, a sol-gel technique, screen printing,
30 and layer transfer.

 The step of controlling the thickness of the crystalline semiconductor layer may be performed prior to forming the electro-optical layer. The thickness of the crystalline semiconductor layer may be controlled to be no greater than 50 nm. The crystalline

semiconductor layer may include or consist of a semiconductor, such as silicon.

A first buffer layer may be formed over the crystalline semiconductor layer, such as by at least one of physical vapor deposition (e.g. sputtering or pulsed laser deposition), chemical vapor deposition, atomic layer deposition, molecular beam epitaxy, and a sol-gel technique.

5 Using any or a combination of these techniques, a second buffer layer may be formed over the first buffer layer, and a ridge may be formed over the electro-optical layer. Forming the ridge layer may include forming an HSQ layer, and a portion of the HSQ layer may be transformed, e.g., by exposure by an electron beam, into silicon dioxide to define a ridge.

10 Finally, a cladding layer may be formed over the electro-optical layer. An electrode in electrical communication with the electro-optical layer may be formed.

In another aspect, the invention includes a method for forming an optical waveguide structure, including the steps of (i) providing an insulator layer, and a crystalline semiconductor layer disposed over the insulator layer, (ii) forming an electro-optical layer over the crystalline semiconductor layer, and (iii) essentially completely oxidizing the crystalline semiconductor
15 layer.

Oxidizing the crystalline semiconductor layer may involve a high temperature anneal. Oxidizing the crystalline semiconductor layer may involve oxygen diffusion through the electro-optical layer. A first and possibly additional buffer layer(s) may be formed over the crystalline semiconductor layer, and oxidizing the crystalline semiconductor layer may involve oxygen
20 diffusion through the first buffer and/or additional buffer layers.

Brief Description of Drawings

Figures 1A–1H are schematic cross-sectional and perspective views illustrating a method for fabricating a structure including an electro-optical layer in accordance with the invention;

25 Figures 2A–2B are schematic cross-sectional views illustrating alternative embodiments including buffer layers;

Figures 3A–3D are schematic cross-sectional views illustrating an alternative method for fabricating a structure including an electro-optical layer in accordance with the invention;

30 Figures 4A–4D are schematic cross-sectional views illustrating another alternative method for fabricating a structure including an electro-optical layer in accordance with the invention;

Figures 5A–5D are schematic cross-sectional views illustrating yet another alternative method for fabricating a structure including an electro-optical layer in accordance with the

invention; and

Figures 6A–6D are schematic cross-sectional views and graphs illustrating the light propagation characteristics of a waveguide made in accordance with the invention.

Like-referenced features represent common features in corresponding drawings.

5

Detailed Description

In accordance with the present invention, high-quality electro-optical materials, such as BT, are formed on crystalline materials such as silicon. In particular, an electro-optical layer is formed over a thin crystalline semiconductor layer, such as silicon, that enables the epitaxial formation thereover of a high-quality layer. An insulating layer may keep the electro-optical layer optically decoupled from an underlying semiconductor substrate. This approach results in structures with reduced light losses to underlying material during operation of optical devices, and can utilize conventional, readily available SOI wafers for the fabrication of waveguides. It is to be understood that the presence of an underlying semiconductor substrate is not essential to the invention. The insulating layer may also act as an underlying substrate.

15

Referring to Figure 1A, an SOI wafer 100 may include a semiconductor substrate 110 formed of a semiconductor material, such as a group IV material, a III-V material, or a II-VI material, and may include or consist of Si, Ge, SiGe, SiC, GaAs, InP, or GaN; a preferred substrate 110 includes or consists of Si. An insulator layer 120 may be disposed over the semiconductor substrate 110. Insulator layer 120 may include or consist of, for example, silicon dioxide (SiO₂), silicon nitride (Si₃N₄ or other compositions), aluminum oxide, magnesium oxide, and/or other dielectric materials, or may be a multilayer structure including one or more different materials. The insulator layer 120 may have a thickness t_1 ranging from approximately 2 to 10 or more (e.g., up to approximately 100) μm , although the preferred thickness t_1 range is approximately 3 to 10 μm . The economics of fabrication may favor relatively thin insulator layers, while the need to optically couple to large-diameter fibers may require relatively thick layers.

25

A crystalline semiconductor layer 130 may be disposed over the insulator layer 120. The crystalline semiconductor layer 130 may include or consist of a semiconductor material, such as a group IV material, a III-V material, or a II-VI material (e.g., Si, Ge, SiGe, SiC, GaAs, InP, and/or GaN). In a preferred embodiment, the crystalline semiconductor layer 130 includes or consists of Si. The crystalline semiconductor layer 130 preferably has a thickness t_2 greater than 0 Å, i.e., sufficient to enable epitaxial growth of electro-optical or other crystalline layers over the crystalline semiconductor layer 130; this may involve as few as one or several atomic

30

layers. To prevent any significant optical loss from a waveguide fabricated over the crystalline semiconductor layer 130 to the crystalline semiconductor layer 130, the crystalline semiconductor layer 130 should be thinner than ~100 nm, and ideally is no thicker than ~50 nm. Commercially available SOI wafers generally include a top crystalline silicon layer having a thickness greater than or equal to 300 nm, typically up to 1000 nm. Managing this excess thickness is discussed below.

Referring to Figure 1B, an electro-optical layer 140 may be disposed over the crystalline semiconductor layer 130. The electro-optical layer 140 may include a material having a relatively high E-O effect, e.g., higher than 20 pm/V, such as BaTiO₃, PbTiO₃, (Pb,La)TiO₃, (Pb,Zr)TiO₃, (Pb,La)(Zr,Ti)O₃, ZrTiO₃, LaZrTiO₃, LiNbO₃, LiTaO₃, Sr_xBa_{1-x}Nb₂O₆ (SBN:x), Ba_{1-x}Ca_xTiO₃ with x selected from a range of about 0.2 to about 0.5, KNbO₃, and KNbTaO₃. The electro-optical layer 140 generally has a thickness t_3 suitable for use as a waveguide. Preferably, thickness t_3 ranges from about 500 nm to about 1000 nm, although the electro-optical layer 140 may be thicker or thinner depending on the specific waveguide for which it will be used. For example, for a ridge waveguide, a thickness t_3 ranging from 300 nm to about 2 μ m may be preferred; for an indiffused waveguide, a higher thickness t_3 may be needed, e.g., 10 μ m.

The electro-optical layer 140 may be formed by a suitable deposition process, such as physical vapor deposition (e.g., sputtering by use of, e.g., a sputtering deposition tool manufactured by Kurt J. Lesker or pulsed laser deposition by use of, e.g., a LPX325i system manufactured by Lambda Physics); chemical vapor deposition; atomic layer deposition; molecular beam epitaxy; a sol-gel technique; screen printing; or electro-optical layer transfer from a single crystal substrate using ion slicing and wafer bonding techniques.

The electro-optical layer 140 may be formed with a particular crystallographic orientation. The crystallographic orientation of the electro-optical layer 140 may be determined by growing the electro-optical layer 140 in a particular crystallographic orientation, which itself may be determined by a crystallographic orientation of the underlying crystalline layer 130. Alternatively, the crystallographic direction of the electro-optical layer 140 may be selected by poling or cleaving the layer. For example, the electro-optical layer 140 may have a highly (110)/(101) orientation when it is grown on a YSZ, CeO₂, or SrTiO₃ buffer layer on an SOI wafer 100. The orientation of such polycrystalline electro-optical layer 140 may be modified by poling and cleaving to obtain, e.g., (001) crystallographic orientation.

The insulator layer 120 may ultimately serve to optically decouple, i.e., optically isolate the electro-optical layer 140 from the semiconductor substrate 110 (which typically has a higher

refractive index).

Referring to Figure 1C, a ridge 150 may be defined by patterning the electro-optical layer 140. The ridge 150 may serve as a waveguide in a finished device, in which case it will have dimensions suitable for use as a waveguide, e.g., a height h_1 of about 50 nm to about 400 nm and a width w_1 of about 300 nm to about 3000 nm. The ridge 150 may be defined by patterning the electro-optical layer 140 by, e.g., the definition of a photoresist mask (not shown) and an etch step, e.g., an anisotropic etch.

Referring to Figures 1D and 1E, an alternative method for defining the ridge 150 may include the use of a lift-off technique, which permits use of different materials for ridge 150 and electro-optical layer 140. Here, a photoresist layer (not shown) is defined over the electro-optical layer 140 and exposed, such that substantially no photoresist remains on the regions of the electro-optical layer 140 over which the ridge 150 will be defined. A ridge layer (not shown) may be formed over the photoresist layer. The photoresist layer and portions of the ridge layer disposed over the photoresist layer are then lifted off by developing the photoresist layer, leaving behind ridge 150.

Referring to Figures 1F-1G, in another alternative embodiment, the ridge 150 may be defined by the use of HSQ. A ridge layer 155 including or consisting of HSQ is spun onto a top surface of the electro-optical layer 140. The ridge layer 155 may have a thickness t_{10} selected from a range of about 400 nm to 5000 nm. A region 155a of the HSQ ridge layer 155 may be exposed with an electron beam 157 to define the ridge 150. Upon exposure to the electron beam, HSQ is transformed to SiO_2 . After the exposure of the region 155a, unexposed regions 155b are developed and washed away. Ridge 150 including or consisting of silicon dioxide disposed over the electro-optical layer is thereby defined. A suitable anneal may be performed to complete the SiO_2 transformation and to reduce possible optical losses. It is to be understood that the method of defining a ridge waveguide by the use of HSQ described above is a method of fabrication of silicon dioxide waveguides that may find applications in a more general context than the one of the present invention. It may be used for forming a silicon dioxide ridge waveguide over a dielectric layer having a refractive index higher than, or equal to, that of silicon dioxide. In an embodiment, the dielectric layer may comprise SIN or SiO_2 .

The ridge 150 may include a dielectric material, such as Si_3N_4 , silicon-rich nitride (SIN), HSQ, SiO_2 , YSZ, CeO_2 , MgO , BaO , SrO , $\text{Ba}_{1-x}\text{Sr}_x\text{O}$, MgAl_2O_4 , LaAlO_3 , LSAT $(\text{LaAlO}_3)_{0.3}(\text{Sr}_2\text{AlTaO}_6)_{0.7}$, Al_2O_3 , Y_2O_3 , BaTiO_3 , PbTiO_3 , $(\text{Pb,L a})\text{TiO}_3$, $(\text{Pb,Zr})\text{TiO}_3$, $(\text{Pb,L a})(\text{Zr,Ti})\text{O}_3$, ZrTiO_3 , LaZrTiO_3 , LiNbO_3 , LiTaO_3 , $\text{Sr}_x\text{Ba}_{1-x}\text{Nb}_2\text{O}_6$ (SBN:x), $\text{Ba}_{1-x}\text{Ca}_x\text{TiO}_3$

with x selected from a range of about 0.2 to about 0.5, KNbO_3 , and/or KNbTaO_3 . The ridge material and method of ridge formation may be selected to define a ridge with relatively smooth sidewalls, thereby enhancing light confinement. The ridge material may include a material with an index of refraction similar to that of the electro-optical layer.

5 In an exemplary embodiment, ridge 150 is formed from Si_3N_4 and the electro-optical layer 140 consists of BaTiO_3 . The use of Si_3N_4 enables the formation of a ridge 150 with smoother sidewalls than may be achieved with a ridge formed from BaTiO_3 , thereby enhancing light confinement.

10 The material of the ridge 150 may be selected to have an index of refraction similar to that of the electro-optical layer 140. For example, ridge 150 may be formed from SIN with an index of refraction of 2.2, and the electro-optical layer 140 may be formed from BaTiO_3 with an index of refraction of 2.25.

Referring to Figure 1H, a first electrode 160a and a second electrode 160b may be formed to enable electrical communication with the electro-optical layer 140. The electrodes 160a, 160b may be formed, for example, above the electro-optical layer 140. The first and second electrodes 160a, 160b may be formed from a conductive material, such as Au, Au/Ti, Pt, Cr, Ag, Ir, Ru, and/or Ni. For example, the electrodes 160a, 160b may be defined by the formation of a conductive layer by, e.g., deposition, followed by patterning the conductive layer by, e.g., photoresist definition and an anisotropic etch.

20 A cladding layer 170 may be formed over the electro-optical layer 140 and ridge 150. The cladding layer 170 may include a material having a refractive index less than that of the electro-optical layer 140 and ridge 150. Suitable materials include, e.g., silicon dioxide, Si_3N_4 , SIN, SiON, HSQ, a polymer such as polymethyl methacrylate (PMMA), MgO, and Al_2O_3 .

Referring to Figures 2A and 2B, in an embodiment, buffer layers (e.g., a first buffer layer 180 and, optionally, a second buffer layer 190) may be grown between the crystalline semiconductor layer 130 and the electro-optical layer 140 to prevent chemical reaction between the layers 130, 140, and to control the orientation and quality of the electro-optical layer 140. These first and second buffer layers 180, 190 may include or consist of, e.g., MgO, MgAl_2O_4 , Al_2O_3 , LaAlO_3 , LSAT ($(\text{LaAlO}_3)_{0.3}(\text{Sr}_2\text{AlTaO}_6)_{0.7}$), CeO_2 , Y_2O_3 , YSZ, BaO, SrO, $\text{Ba}_{1-x}\text{Sr}_x\text{O}$ ($\sim 0.3 \leq x \leq \sim 1$), SrTiO_3 , $\text{Pb}_x\text{Ba}_{1-x}\text{TiO}_3$, BaTiO_3 , $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$ ($\sim 0.3 \leq x \leq \sim 1$) or some combination of these materials. The first buffer layer 180 may have a thickness t_4 and the second buffer layer 190 may have a thickness t_5 , with each thickness t_4 , t_5 selected from a range of about 10 nm to about 3000 nm, preferably about 200 nm to about 500 nm. The use of a relatively thick

first buffer layer 180 and/or second buffer layer 190 may enhance optical decoupling, as well as enable the formation of relatively crack-free electro-optical layer 140. Buffer layers that are too thick, however, may crack or peel off.

In an exemplary embodiment, the electro-optical layer 140 consists of BaTiO_3 having a thickness t_3 selected from a range of approximately 500 nm to approximately 1000 nm. The first buffer layer 180 consists of MgO with a thickness t_4 of about 200 nm. In an alternative exemplary embodiment, the electro-optical layer 140 consists of BaTiO_3 having a thickness t_3 selected from a range of approximately 500 nm to approximately 1000 nm. The electro-optical layer 140 is disposed over second buffer layer 190, which consists of $(\text{Pb,Ba})\text{TiO}_3$ and has a thickness t_5 of equal to or less than 50 nm. The second buffer layer 190 is disposed over the first buffer layer 180 consisting of MgO with a thickness t_4 of about 200 nm. In both exemplary embodiments, the electro-optical layer 140 and the first buffer layer 180 may be disposed over an SOI wafer.

The electro-optical layer 140 may include BT. Then, in an embodiment with only one buffer layer, the first buffer layer 180 may include a very thin $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$ ($\sim 0.3 \leq x \leq \sim 1$) seed layer (with thickness t_4 equal to or less than 50 nm) that may be used to control the BaTiO_3 orientation.

Electro-optical layer 140 may include material having a selected crystalline orientation. In an exemplary structure, SOI wafer 100 may include a crystalline semiconductor layer 130 having a thickness t_2 of 100 nm or less, preferably 50 nm or less, and an insulator layer 120 including SiO_2 and having thickness t_1 of about 3000 nm. A first buffer layer 180 including MgO and having a thickness t_4 of 200 nm is disposed over the crystalline semiconductor layer 130. Electro-optical layer 140 may include BaTiO_3 having a strong (001) crystallographic orientation, with a thickness t_3 selected from a range of about 500 nm to 1000 nm.

In another exemplary embodiment, as above, SOI wafer 100 may include crystalline layer 130 with a thickness t_2 of 100 nm or less, preferably 50 nm or less, and insulator layer 120 including SiO_2 and having thickness t_1 of about 3000 nm. A first buffer layer 180 consisting of MgO and having a thickness t_4 of about 200 nm is disposed over the crystalline semiconductor layer 130. A second buffer layer 190 including $\text{Pb}_{1-x}\text{Ba}_x\text{TiO}_3$ with $x = 0.9$ may be disposed over the first buffer layer 180. The thickness t_5 of the second buffer layer 190 is less than 100 nm. Electro-optical layer 140 consists of BaTiO_3 having a strong (001) crystallographic orientation, with a thickness t_3 selected from a range of about 500 nm to 1000 nm.

In an embodiment, prior to the formation of the electro-optical layer 140, crystalline

semiconductor layer 130 may be thinned to the desired thickness t_2 (generally less than 100 nm) if, for example, a conventional SOI wafer is employed. The thickness of the crystalline semiconductor layer may be controlled to be no greater than 100 nm. For example, if the starting SOI wafer has a semiconductor top layer (e.g., crystalline semiconductor layer 130) with an initial thickness of greater than ~100 nm, the crystalline semiconductor layer 130 may be thinned by, e.g., oxidation, before or after the deposition of overlying layers, or by, e.g., polishing or etching before the deposition of overlying layers. Furthermore, thinning may involve a multi-step process beginning, for example, with oxidation followed by a chemical etch and, optionally, a dry etch, as is well-known in the art. Oxidation may be partial, i.e., so that a residual thin crystalline semiconductor layer 130 exists at the end of the fabrication process, or complete, i.e. so that the crystalline semiconductor layer 130 is essentially gone at the end of the process. In any event, complete oxidation may not take place before the deposition of the overlying layer has started. Oxidation may be initiated by diffusion of oxygen from the atmosphere through the layers deposited over the SOI structure, either after the buffer layer growth or after the electro-optical layer growth. The oxidation step may be performed even if the semiconductor top layer is less than 100 nm thick.

More specifically, referring to Figure 3A, in an embodiment, an initial thickness t_2 of crystalline semiconductor layer 130, disposed over insulator layer 120, is greater than 100 nm. First buffer layer 180 is disposed over crystalline semiconductor layer 130. A high temperature anneal is performed, e.g., at a temperature selected from a range of about 600 °C to about 900 °C for approximately 0.1 to 3 hours in an oxygen or air ambient. During this annealing step, oxygen diffuses through the first buffer layer 180 to the crystalline semiconductor layer 130. Referring to Figure 3B, the crystalline semiconductor layer 130 may be completely oxidized, resulting in a thicker insulator layer in direct contact with first buffer layer 180. Referring to Figure 3C and 3D, electro-optical layer 140 may be formed over first buffer layer 180, and ridge 150 may be defined either from or over the electro-optical layer 140.

In another embodiment, the crystalline semiconductor layer is oxidized after the formation of the electro-optical layer 140. Referring to Figure 4A, the first buffer layer 180 is disposed over the crystalline semiconductor layer 130. The electro-optical layer 140 is disposed over the first buffer layer 180. Referring to Figure 4B, a high temperature anneal is performed, e.g., at a temperature selected from a range of about 600 °C to about 900 °C for approximately 0.1 to 3 hours in an oxygen or air ambient. During this annealing step, oxygen diffuses through the electro-optical layer 140 and the first buffer layer 180 to the crystalline semiconductor layer

130.

Referring to Figure 4C, the crystalline semiconductor layer 130 may be completely oxidized, resulting in a thicker insulator layer in direct contact with first buffer layer 180.

Referring to Figure 4D, ridge 150 may be defined either from or over the electro-optical layer 140.

Referring to Figures 5A–5D, in an alternative embodiment, the electro-optical layer 140 may be disposed over and in contact with insulator layer 120 (i.e., there is no first buffer layer 180). The insulator layer 120 includes an amorphous, i.e., non-crystalline material. This structure may be obtained as follows. Referring to Figure 5A, electro-optical layer 140 is disposed directly on crystalline semiconductor layer 130, as discussed above with reference to Figures 1A and 1B.

Referring to Figure 5B, a high temperature anneal is performed, e.g., at a temperature selected from a range of about 600 °C to about 900 °C for approximately 0.1 to 3 hours in an oxygen or air ambient. During this annealing step, oxygen diffuses through the electro-optical layer 140 to the crystalline semiconductor layer 130.

Referring to Figure 5C, the crystalline semiconductor layer 130 may be completely oxidized, resulting in the electro-optical layer being disposed over and in direct contact with amorphous insulator 120. Referring to Figure 5D, ridge 150 may be defined either from or over the electro-optical layer 140.

Exemplary embodiments illustrate the effect of having a thin crystalline semiconductor layer on light confinement. Referring to Figures 6A – 6D, in an exemplary embodiment, ridge 150 has a height h_1 of 0.5 μm and a width w_1 of about 1.2 μm . Ridge 150 is made of BT and is disposed over electro-optical layer 140 that is also formed from BT and has a thickness t_3 of about 0.5 μm . First buffer layer 180 is formed from MgO and has a thickness of about 0.3 μm . The electro-optical layer and first buffer layer 180 are formed over an SOI wafer 100. The SOI wafer 100 includes Si substrate 110, insulator layer 120 formed of SiO_2 and having a thickness t_1 of 3 μm , and crystalline semiconductor layer 230 formed of Si and having a thickness t_2 thicker than about 100 nm, e.g., about 0.2 μm , i.e., 200 nm. This crystalline semiconductor layer 230 is thicker than the crystalline semiconductor layer desirably employed in connection with the invention. As illustrated in Figure 6B, the mode shape for this waveguide fabricated with a thick silicon layer is indicative of great propagation losses, e.g., 25dB/cm at a wavelength of 1.55 μm , due to the spreading of the non-confined components of the optical mode into the thick Si crystalline semiconductor layer.

Referring to Figure 6C, an exemplary waveguide formed in accordance with the invention has the same materials, thicknesses, and dimensions as the waveguide of Figure 6A. Instead of the thick Si crystalline semiconductor layer, however, the exemplary waveguide formed in accordance with the invention has a thin Si crystalline semiconductor layer 130 with a thickness t_2 that is less than 100 nm, e.g., about 0.05 μm , i.e., 50 nm. Referring to Figure 6D, light propagated through the waveguide is confined to the ridge 150 and a portion of the electro-optical layer 140. The thin Si crystalline semiconductor layer 130 does not support the propagation of non-confined light components, so that the mode propagation is substantially loss free.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The foregoing embodiments are therefore to be considered in all respects illustrative rather than limiting on the invention described herein. Scope of the invention is thus indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein.

What is claimed is:

- 1 1. An optical waveguide structure comprising:
2 an insulator layer;
3 a crystalline semiconductor layer disposed over the insulator layer; and
4 an electro-optical layer disposed over the crystalline layer,
5 wherein the crystalline semiconductor layer has a thickness less than or equal to
6 approximately 100 nm.
- 1 2. The optical waveguide structure of claim 1, wherein the electro-optical layer comprises
2 at least one material selected from the group consisting of BaTiO₃, PbTiO₃, (Pb,La)TiO₃,
3 (Pb,Zr)TiO₃, (Pb,La)(Zr,Ti)O₃, ZrTiO₃, LaZrTiO₃, LiNbO₃, LiTaO₃, Sr_xBa_{1-x}Nb₂O₆ (SBN:x),
4 Ba_{1-x}Ca_xTiO₃ with x selected from a range of about 0.2 to about 0.5, KNbO₃, and KNbTaO₃.
- 1 3. The optical waveguide structure of claim 2, wherein the electro-optical layer comprises
2 BaTiO₃.
- 1 4. The optical waveguide structure of claim 1, wherein the electro-optical layer has a
2 thickness ranging from about 300 nm to about 10 μm.
- 1 5. The optical waveguide structure of claim 1, wherein the crystalline semiconductor layer
2 comprises a material selected from the group consisting of group IV material, a III-V material,
3 and a II-VI material.
- 1 6. The optical waveguide structure of claim 4, wherein the crystalline semiconductor layer
2 comprises silicon.
- 1 7. The optical waveguide structure of claim 1, wherein the crystalline semiconductor layer
2 has a thickness no greater than approximately 50 nm.
- 1 8. The optical waveguide structure of claim 1, further comprising:
2 a semiconductor substrate,
3 wherein the insulator layer is disposed over the semiconductor substrate.
- 1 9. The optical waveguide structure of claim 8, wherein the semiconductor substrate
2 comprises a material selected from the group consisting of a group IV material, a III-V material,
3 and a II-VI material.

- 1 10. The optical waveguide structure of claim 1, further comprising:
2 a first buffer layer disposed between the electro-optical layer and the crystalline layer.
- 1 11. The optical waveguide structure of claim 10, wherein the first buffer layer comprises a
2 material selected from the group consisting of MgO, MgAl₂O₄, Al₂O₃, LaAlO₃, LSAT
3 (LaAlO₃)_{0.3} (Sr₂AlTaO₆)_{0.7}, CeO₂, Y₂O₃, YSZ, BaO, SrO, Ba_{1-x}Sr_xO, SrTiO₃, Pb_xBa_{1-x}TiO₃,
4 BaTiO₃, and Ba_{1-x}Sr_xTiO₃.
- 1 12. The optical waveguide structure of claim 10, wherein the first buffer layer has a
2 thickness selected from a range of approximately 30 nm to approximately 3000 nm.
- 1 13. The optical waveguide structure of claim 10, further comprising:
2 a second buffer layer disposed over the first buffer layer.
- 1 14. The optical waveguide structure of claim 13, wherein the second buffer layer comprises
2 a material selected from the group consisting of MgO, MgAl₂O₄, Al₂O₃, LaAlO₃, LSAT
3 (LaAlO₃)_{0.3} (Sr₂AlTaO₆)_{0.7}, CeO₂, Y₂O₃, YSZ, BaO, SrO, Ba_{1-x}Sr_xO, SrTiO₃, Pb_xBa_{1-x}TiO₃,
4 BaTiO₃, and Ba_{1-x}Sr_xTiO₃.
- 1 15. The optical waveguide structure of claim 14, wherein the second buffer layer has a
2 thickness selected from a range of about 10 nm to about 3000 nm.
- 1 16. The optical waveguide structure of claim 1, further comprising:
2 a ridge disposed over the electro-optical layer.
- 1 17. The optical waveguide structure of claim 16, wherein the ridge comprises a dielectric
2 material.
- 1 18. The optical waveguide structure of claim 17, wherein the ridge comprises a material
2 selected from the group consisting of Si₃N₄, silicon-rich nitride (SIN), HSQ, SiO₂, YSZ, CeO₂,
3 MgO, BaO, SrO, Ba_{1-x}Sr_xO, MgAl₂O₄, LaAlO₃, LSAT (LaAlO₃)_{0.3}(Sr₂AlTaO₆)_{0.7}, Al₂O₃, Y₂O₃,
4 BaTiO₃, PbTiO₃, (Pb,Li)TiO₃, (Pb,Zr)TiO₃, (Pb,Li)(Zr,Ti)O₃, ZrTiO₃, LaZrTiO₃, LiNbO₃,
5 LiTaO₃, Sr_xBa_{1-x}Nb₂O₆ (SBN:x), Ba_{1-x}Ca_xTiO₃ with x selected from a range of about 0.2 to about
6 0.5, KNbO₃, and KNbTaO₃.
- 1 19. The optical waveguide structure of claim 1, further comprising a cladding layer disposed
2 over the electro-optical layer.

- 1 20. The optical waveguide structure of claim 19, wherein the cladding layer comprises a
2 material selected from the group consisting of silicon dioxide, Si₃N₄, SiN, SiON, HSQ, a
3 polymer, MgO, and Al₂O₃.
- 1 21. The optical waveguide structure of claim 1, further comprising:
2 an electrode disposed in electrical communication with the electro-optical layer.
- 1 22. The optical waveguide structure of claim 1, wherein the insulator layer is amorphous.
- 1 23. The optical waveguide structure of claim 1, wherein the insulator layer comprises a
2 material selected from the group consisting of silicon dioxide, silicon nitride, aluminum oxide
3 and magnesium oxide.
- 1 24. The optical waveguide structure of claim 23, wherein the insulator layer comprises
2 silicon dioxide.
- 1 25. An optical waveguide structure comprising:
2 an amorphous insulator layer; and
3 an electro-optical layer in contact with the amorphous insulator layer.
- 1 26. A method for forming an optical waveguide structure, the method comprising the steps
2 of:
3 providing an insulator layer;
4 providing a crystalline semiconductor layer disposed over the insulator layer;
5 forming an electro-optical layer over the crystalline semiconductor layer; and
6 controlling the thickness of the crystalline semiconductor layer to be no greater than
7 about 100 nm.
- 1 27. The method of claim 26, wherein forming the electro-optical layer comprises selecting a
2 crystallographic orientation of the electro-optical layer.
- 1 28. The method of claim 27, wherein selecting the crystallographic orientation comprises
2 growing the electro-optical layer in the crystallographic orientation.
- 1 29. The method of claim 28, wherein the crystallographic orientation is determined by the
2 crystallographic orientation of the crystalline semiconductor layer.

- 1 30. The method of claim 27, wherein selecting the crystallographic orientation comprises at
2 least one of poling and cleaving.
- 1 31. The method of claim 26, wherein forming the electro-optical layer comprises at least one
2 method selected from the group consisting of physical vapor deposition, chemical vapor
3 deposition, atomic layer deposition, molecular beam epitaxy, a sol-gel technique, screen printing,
4 and layer transfer.
- 1 32. The method of claim 26, wherein the step of controlling the thickness of the crystalline
2 semiconductor layer is performed prior to forming the electro-optical layer.
- 1 33. The method of claim 26, wherein the thickness is controlled to be no greater than 50 nm.
- 1 34. The method of claim 26, wherein the crystalline semiconductor layer comprises silicon.
- 1 35. The method of claim 26, further comprising:
2 forming a first buffer layer over the crystalline semiconductor layer.
- 1 36. The method of claim 35, wherein forming the first buffer layer is accomplished by at
2 least one of physical vapor deposition, chemical vapor deposition, atomic layer deposition,
3 molecular beam epitaxy, and a sol-gel technique.
- 1 37. The method of claim 36, wherein physical vapor deposition comprises at least one of
2 sputtering and pulsed laser deposition.
- 1 38. The method of claim 35, further comprising:
2 forming a second buffer layer over the first buffer layer.
- 1 39. The method of claim 38, wherein forming the second buffer layer comprises at least one
2 method selected from the group consisting of physical vapor deposition, chemical vapor
3 deposition, atomic layer deposition, molecular beam epitaxy, and a sol-gel technique.
- 1 40. The method of claim 39, wherein physical vapor deposition comprises at least one of
2 sputtering and pulsed laser deposition.
- 1 41. The method of claim 26, further comprising:
2 forming a ridge layer over the electro-optical layer.

- 1 42. The method of claim 41, wherein forming the ridge layer comprises at least one method
2 selected from the group consisting of physical vapor deposition, chemical vapor deposition,
3 atomic layer deposition, molecular beam epitaxy, and a sol-gel technique.
- 1 43. The method of claim 42, wherein physical vapor deposition comprises at least one of
2 sputtering and pulsed laser deposition.
- 1 44. The method of claim 42, further comprising:
2 defining a ridge by a lift-off technique.
- 1 45. The method of claim 42, further comprising:
2 defining a ridge by an etch step.
- 1 46. The method of claim 41, wherein forming the ridge layer comprises forming an HSQ
2 layer, the method further comprising:
3 transforming a portion of the HSQ layer into silicon dioxide to define a ridge.
- 1 47. The method of 46, wherein transforming the portion of the HSQ layer into silicon
2 dioxide comprises exposure the portion by an electron beam.
- 1 48. The method of claim 26, further comprising:
2 forming a cladding layer over the electro-optical layer.
- 1 49. The method of claim 26, further comprising:
2 forming an electrode in electrical communication with the electro-optical layer.
- 1 50. A method for forming an optical waveguide structure, the method comprising the steps
2 of:
3 providing an insulator layer;
4 providing a crystalline semiconductor layer disposed over the insulator layer;
5 forming an electro-optical layer over the crystalline semiconductor layer; and
6 essentially completely oxidizing the crystalline semiconductor layer.
- 1 51. The method of claim 50, wherein oxidizing the crystalline semiconductor layer
2 comprises a high temperature anneal.

1 52. The method of claim 50, wherein oxidizing the crystalline semiconductor layer
2 comprises oxygen diffusion through the electro-optical layer.

1 53. The method of claim 50, further comprising:
2 forming a first buffer layer over the crystalline semiconductor layer.

1 54. The method of claim 53, wherein oxidizing the crystalline semiconductor layer
2 comprises oxygen diffusion through the first buffer layer.

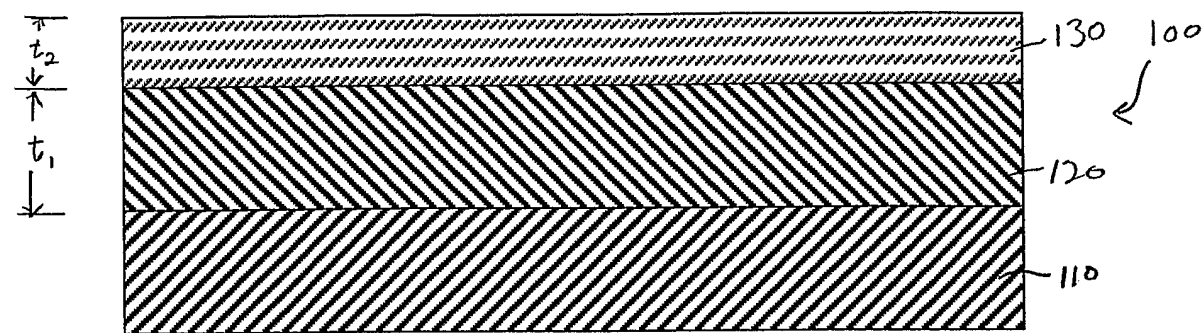


Figure 1A

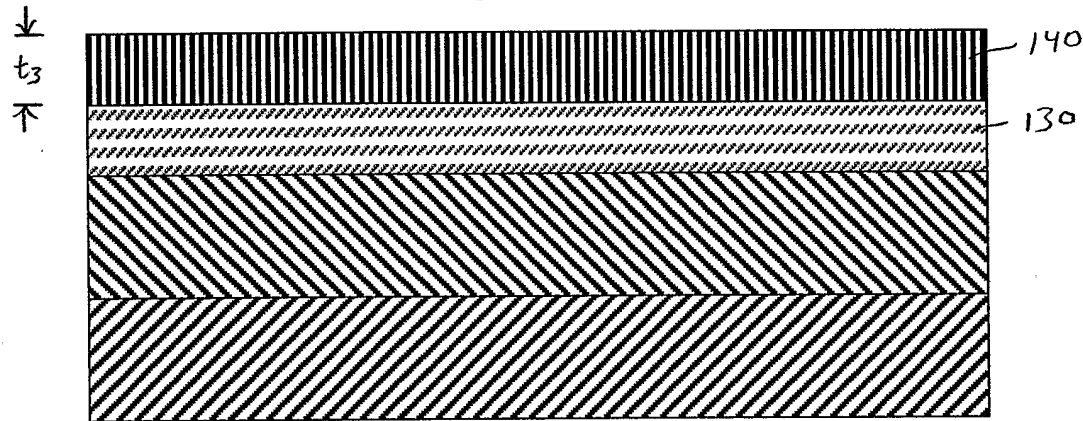


Figure 1B

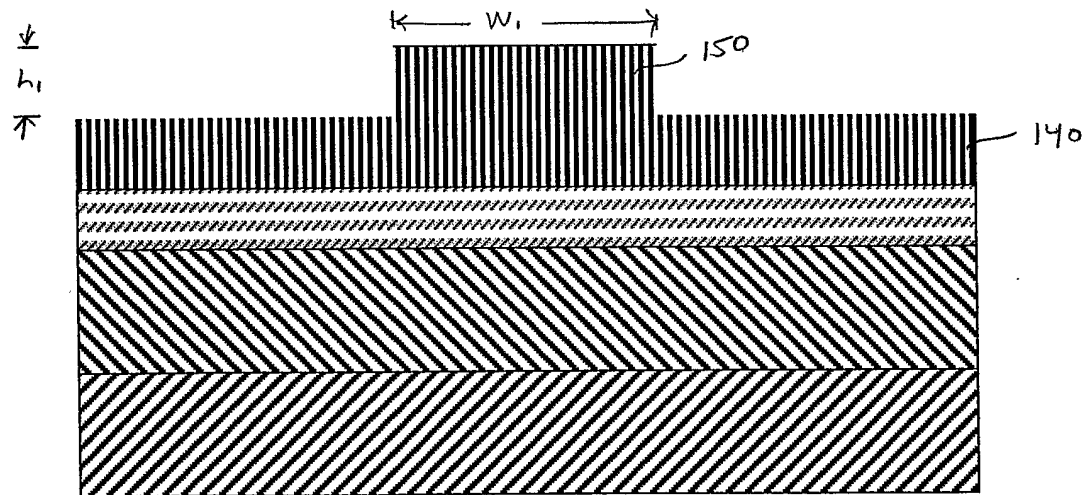


Figure 1C

2/15

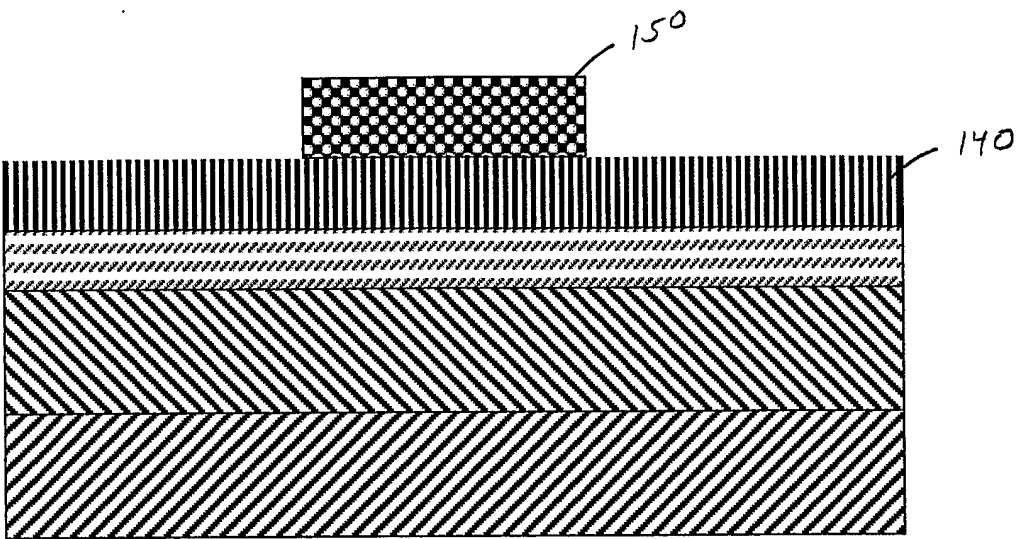


Figure 1D

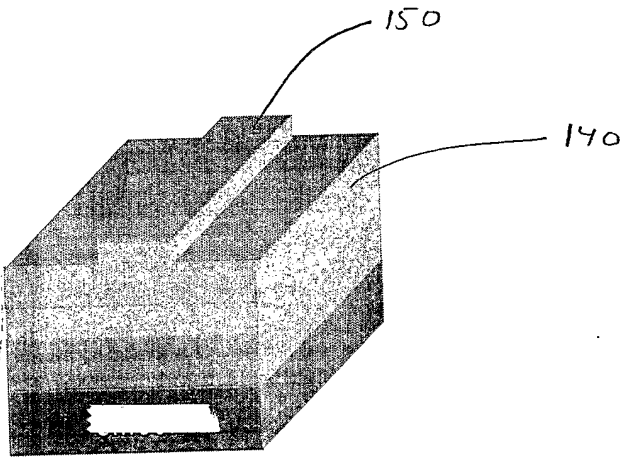


Figure 1E

3/15

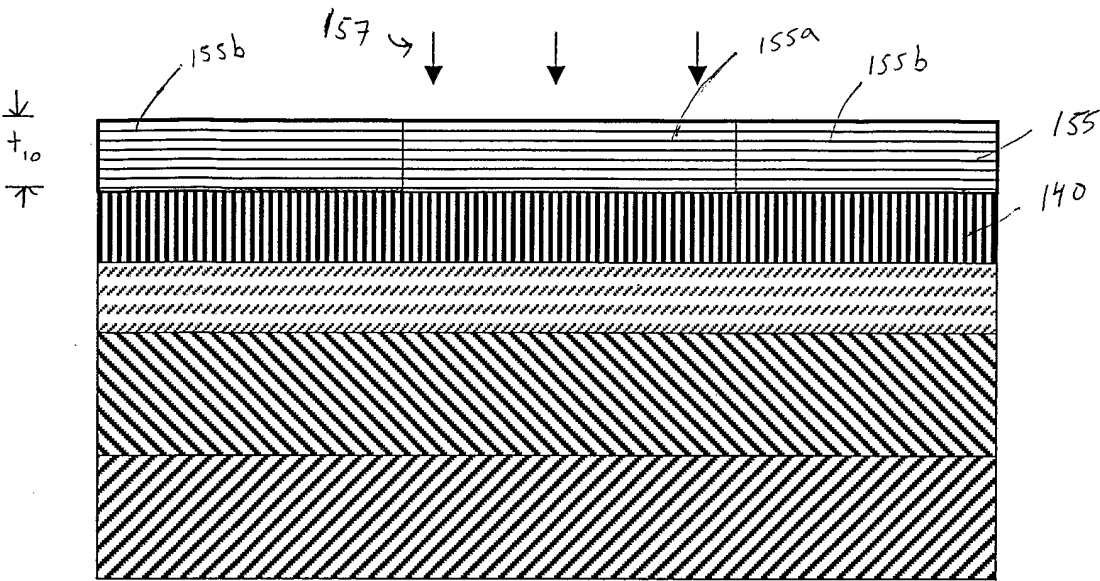


Figure 1F

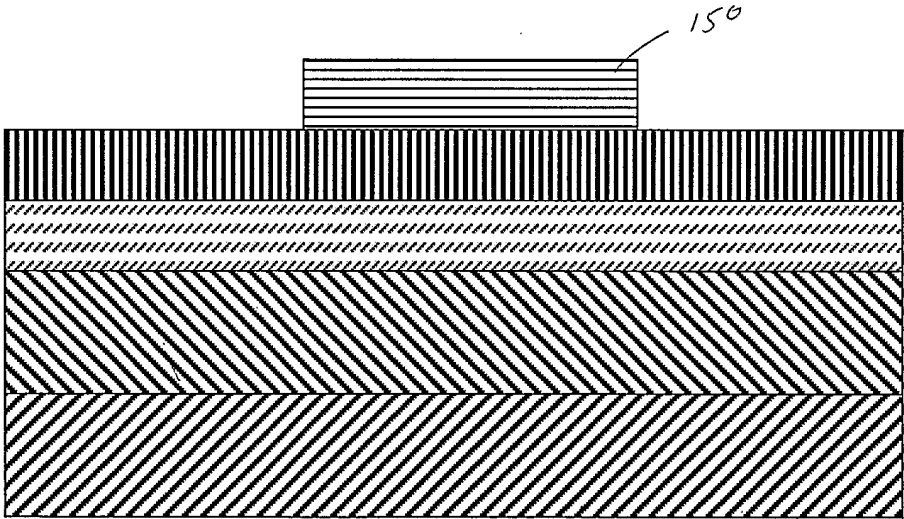


Figure 1G

4/15

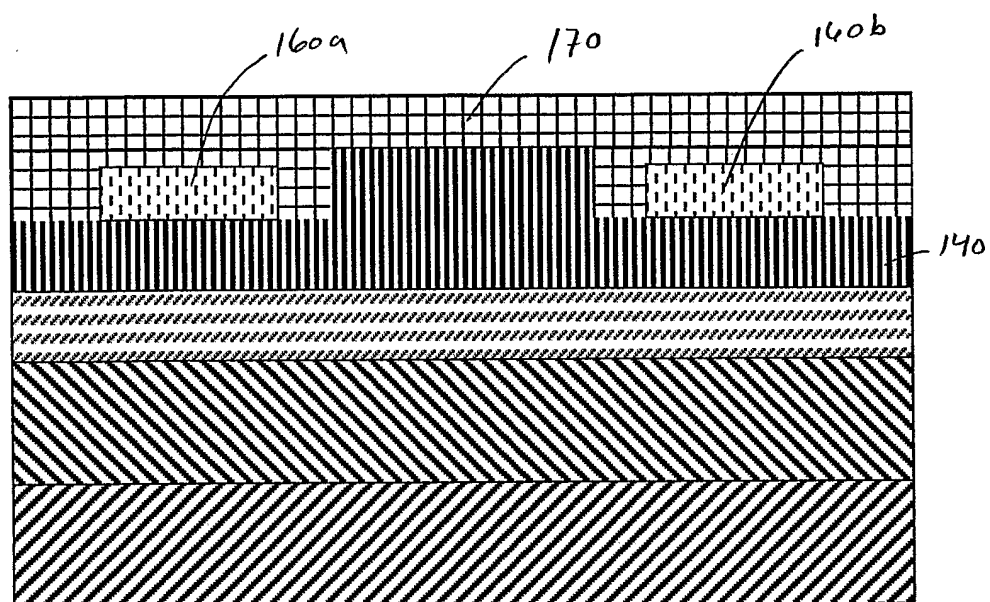


Figure 1H

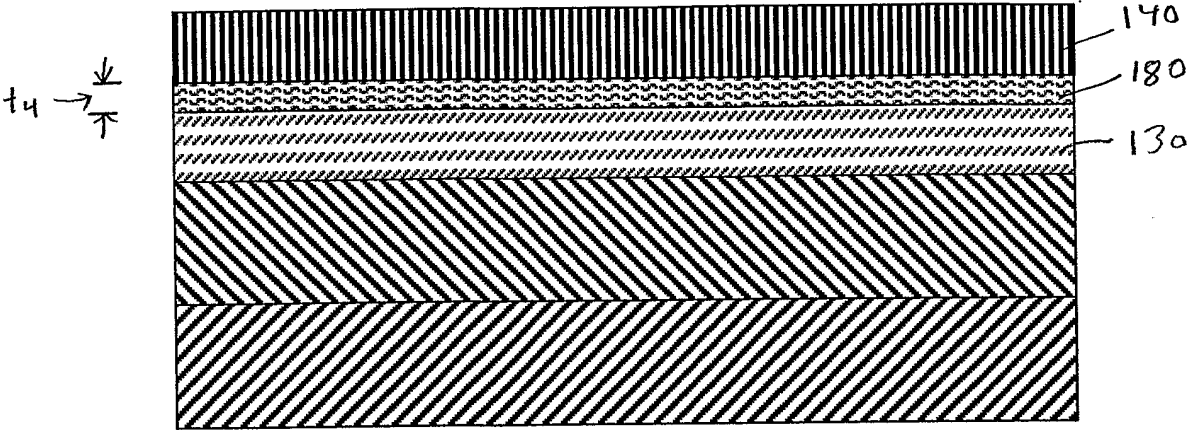


Figure 2A

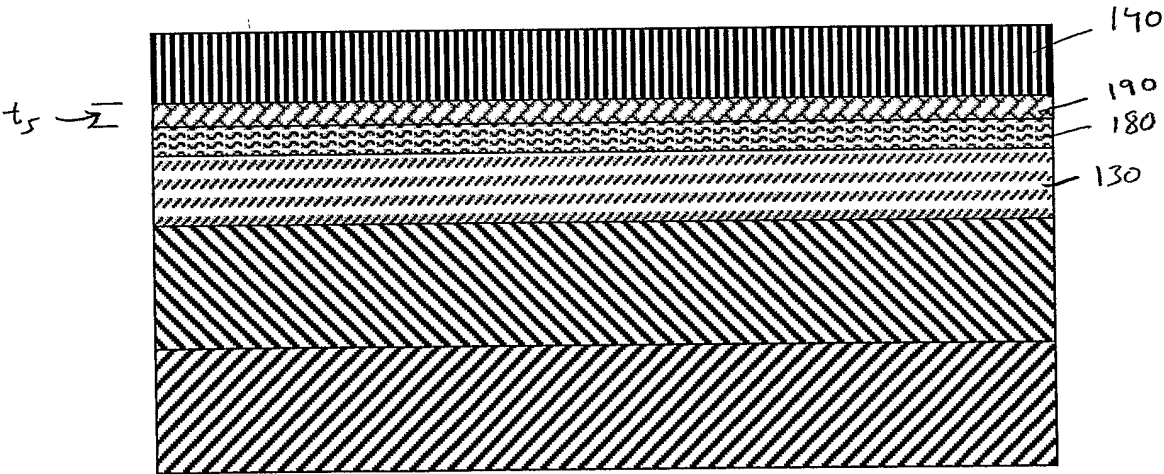


Figure 2B

6/15

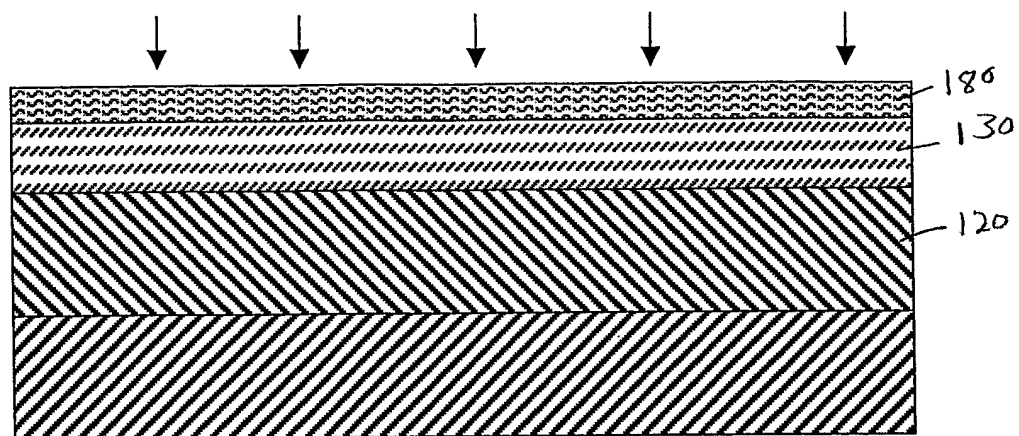


Figure 3A

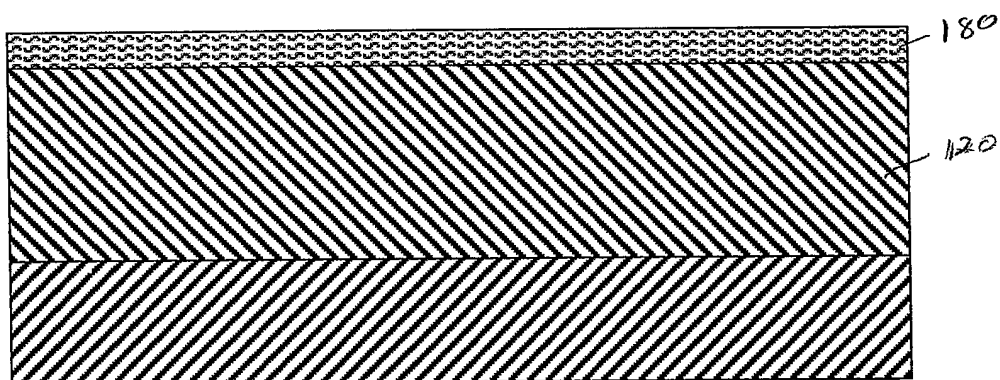


Figure 3B

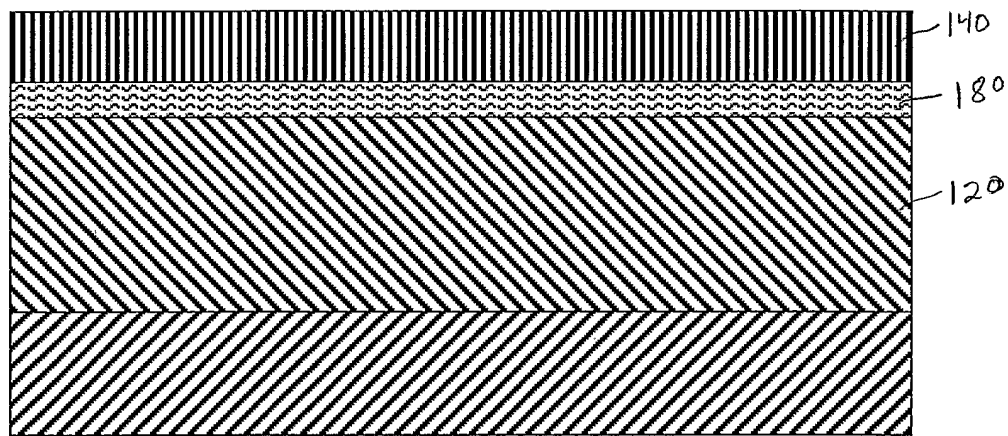


Figure 3C

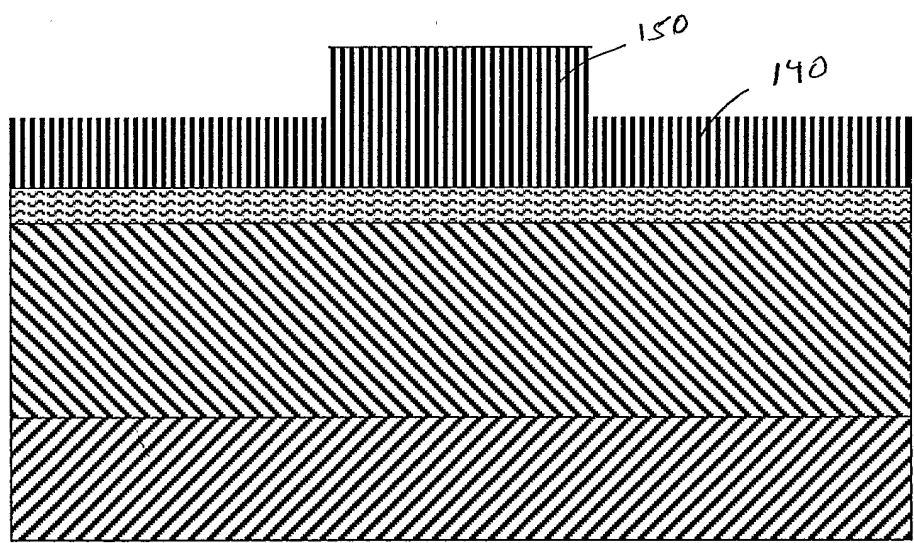


Figure 3D

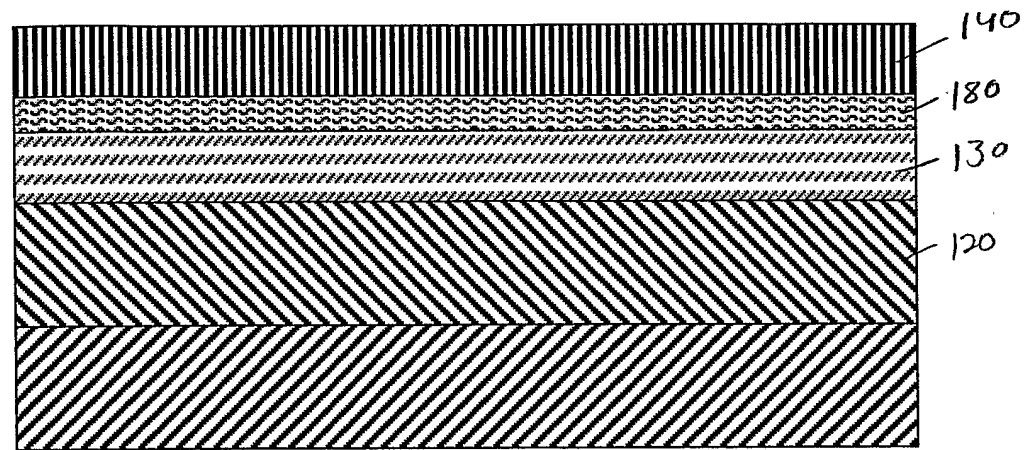


Figure 4A

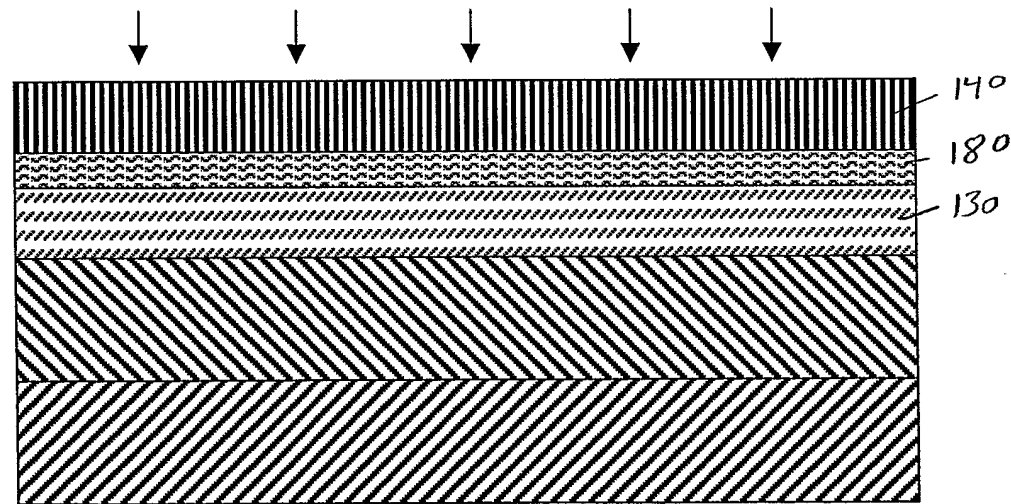


Figure 4B

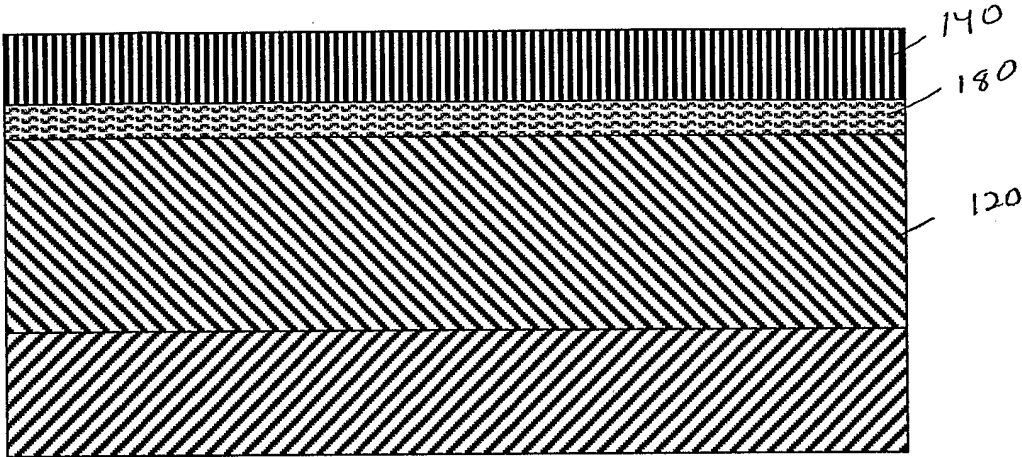


Figure 4C

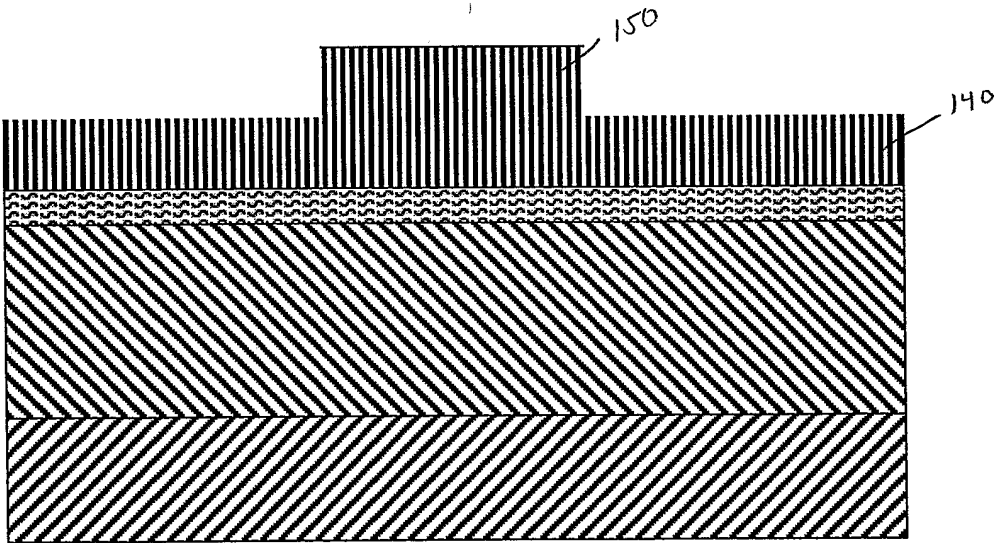


Figure 4D

10/15

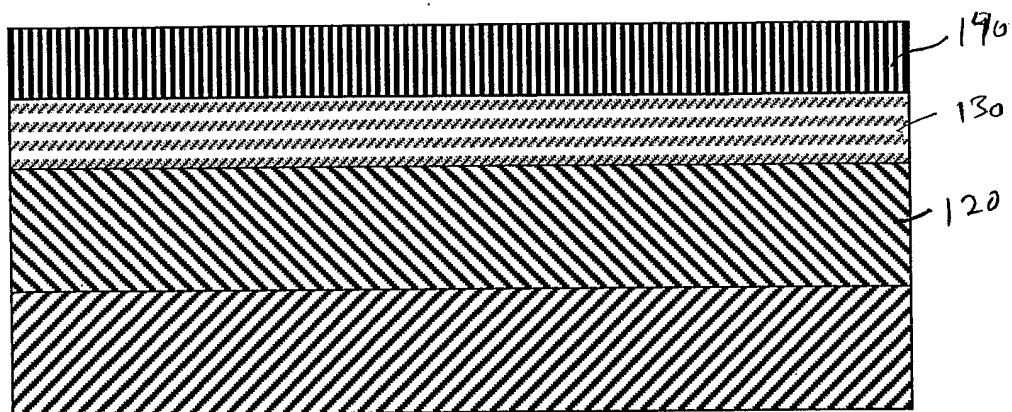


Figure 5A

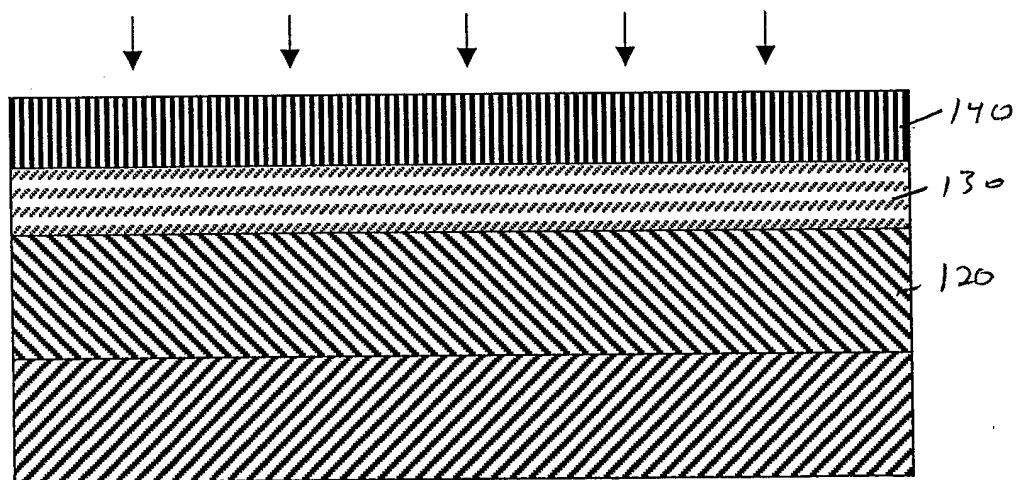


Figure 5B

11/15

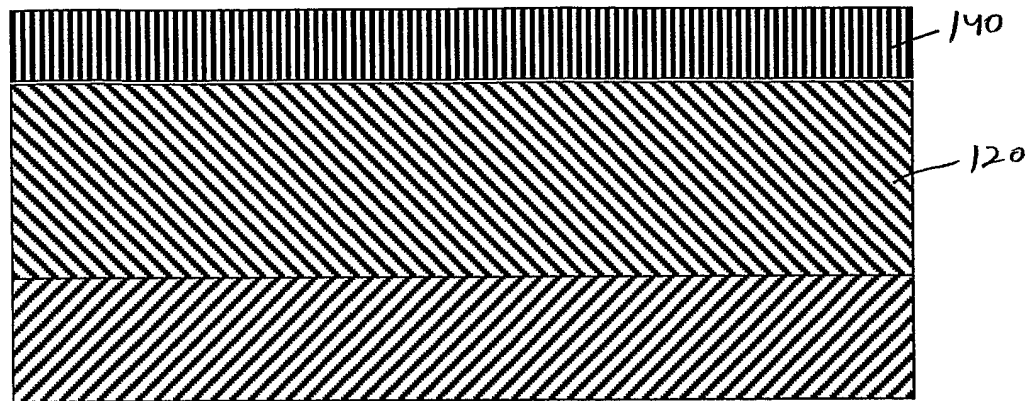


Figure 5C

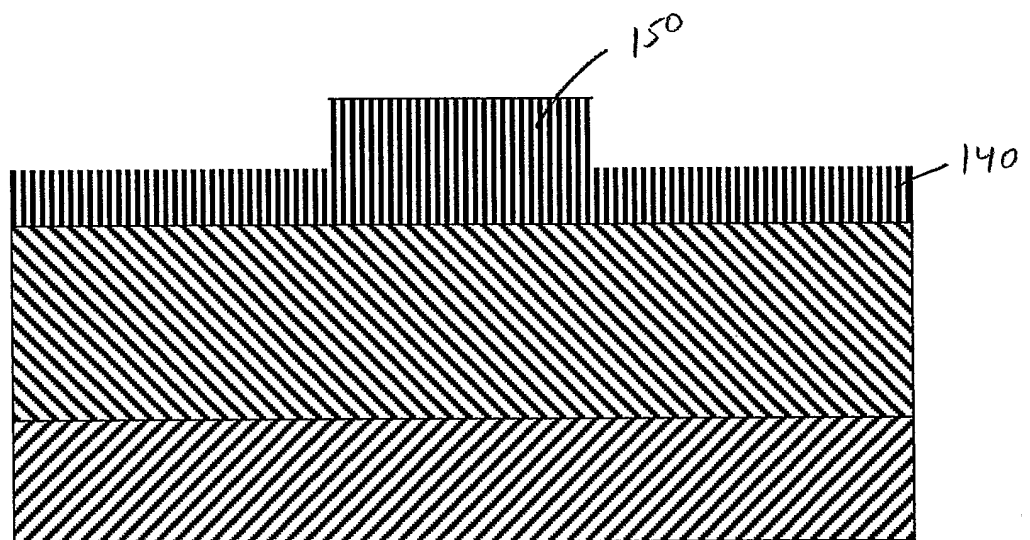


Figure 5D

Waveguide with "thick" Si layer

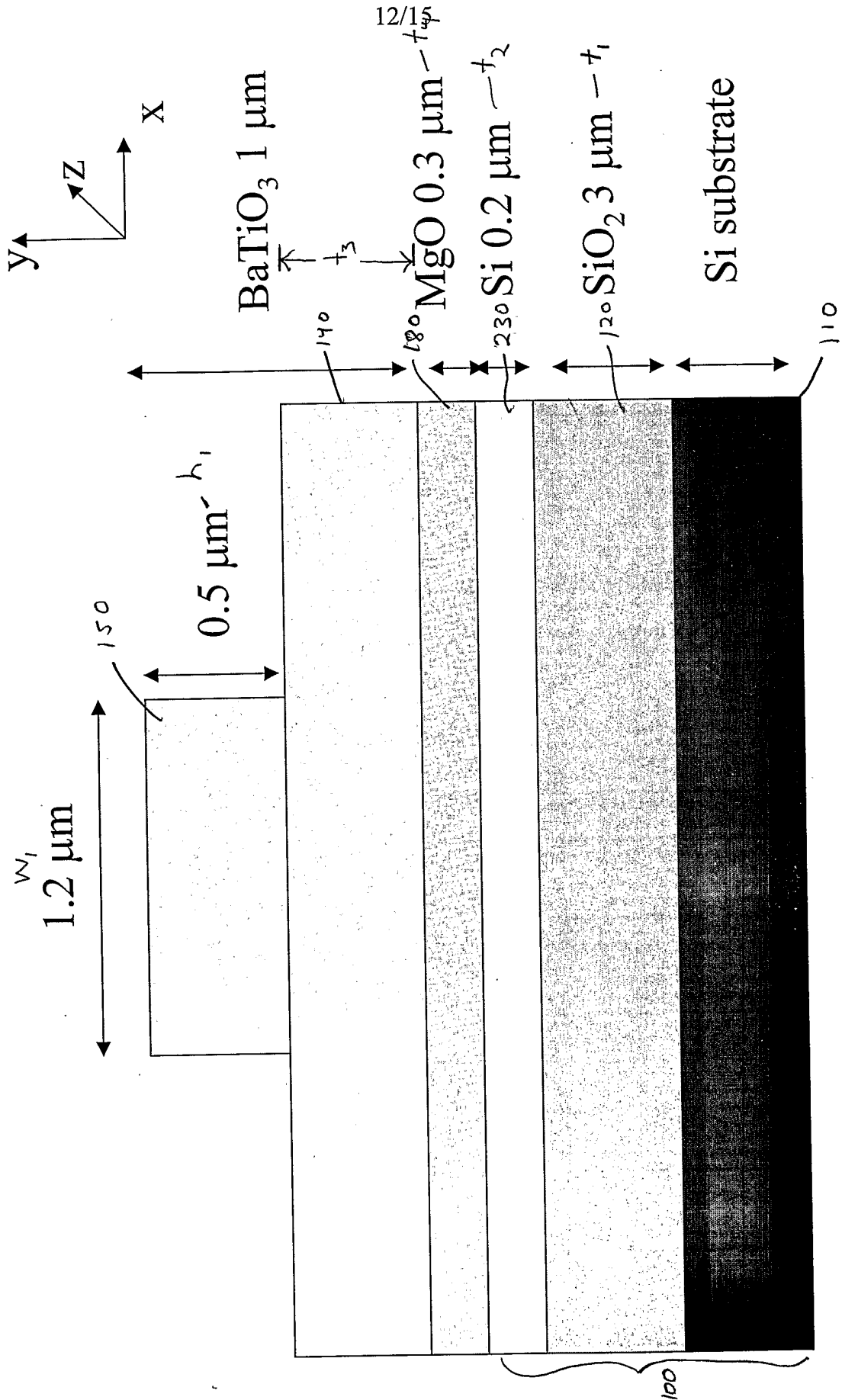


Figure 6A

Mode shape for the waveguide with “thick” Si layer

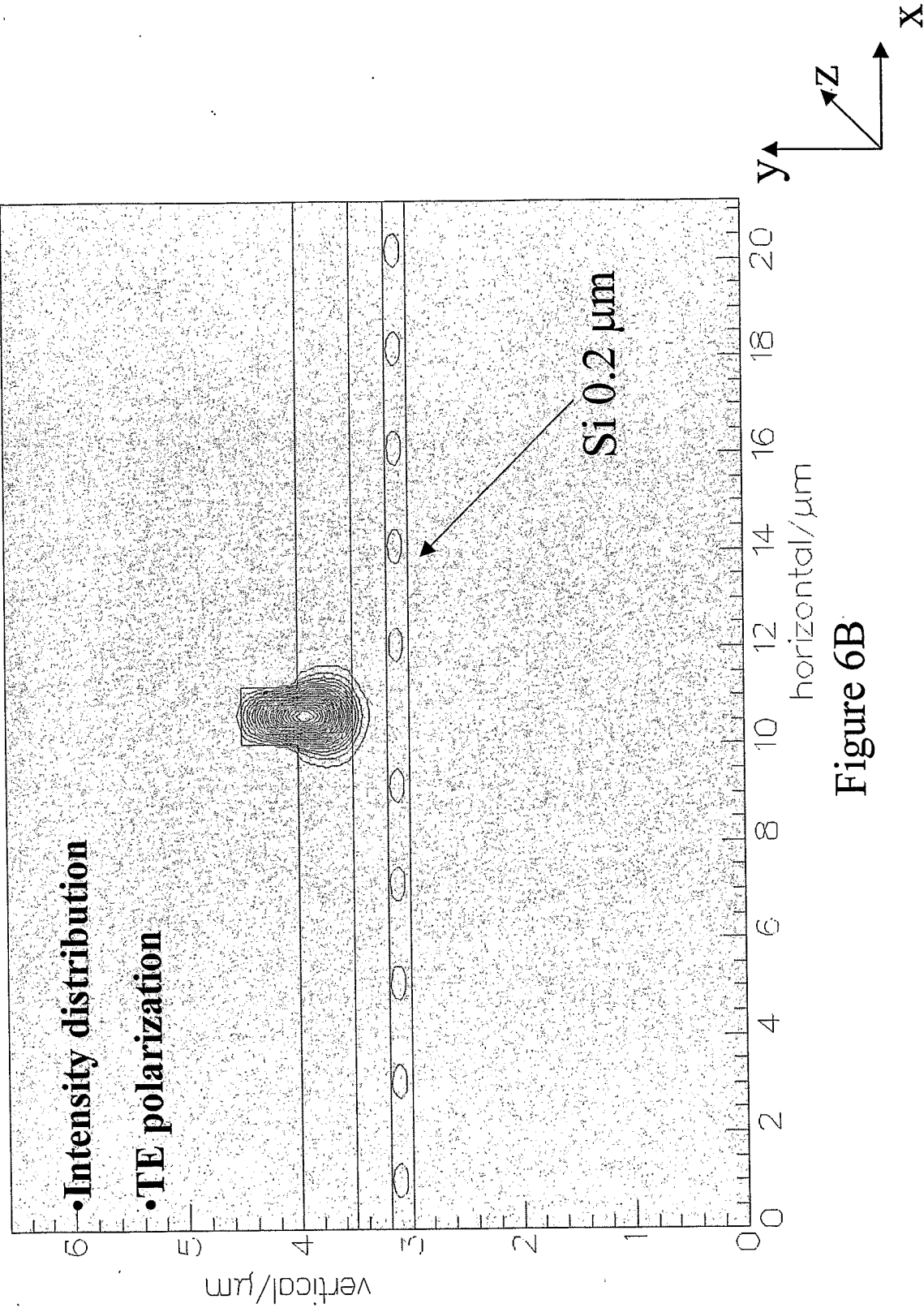


Figure 6B

Waveguide with "thin" Si layer

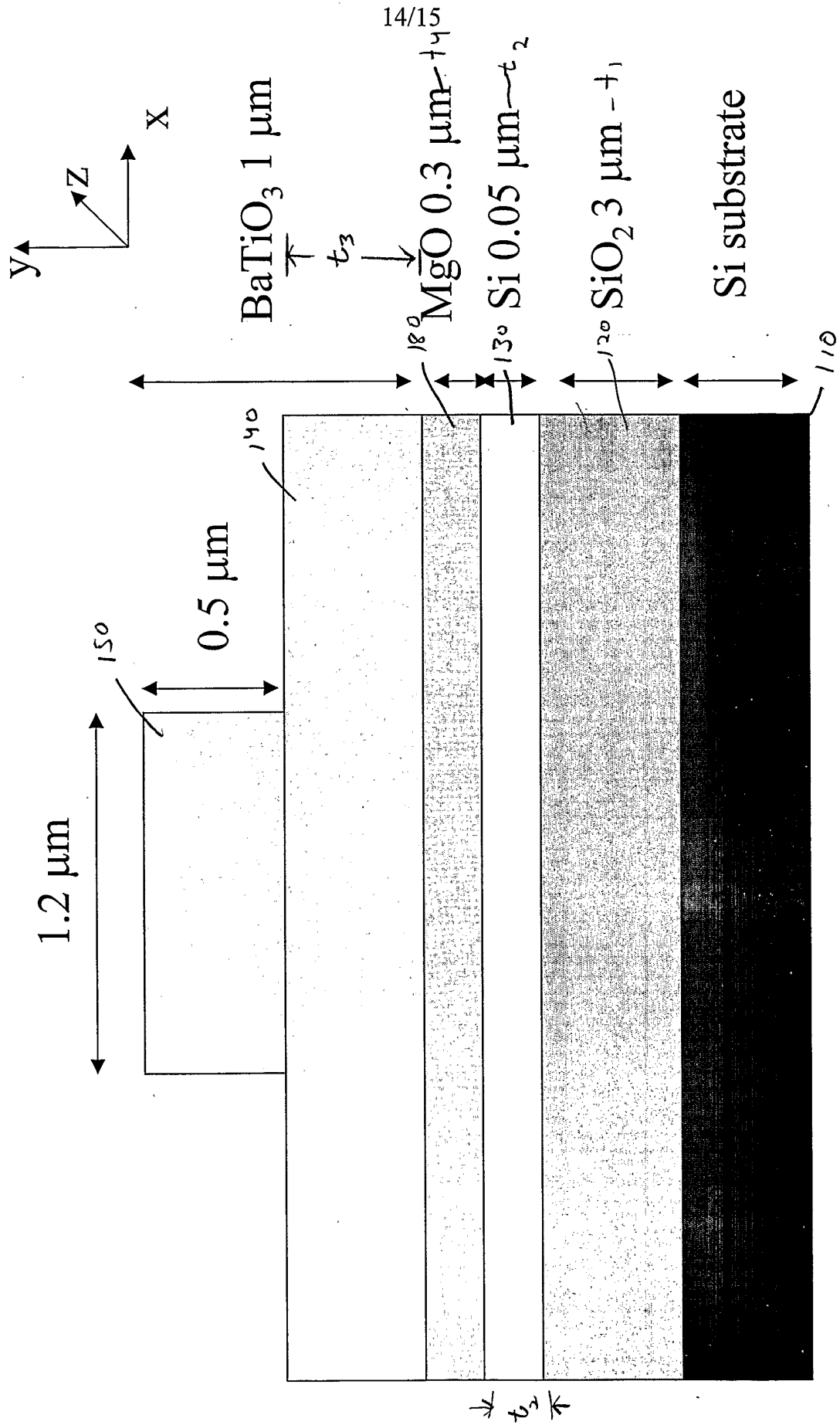


Figure 6C

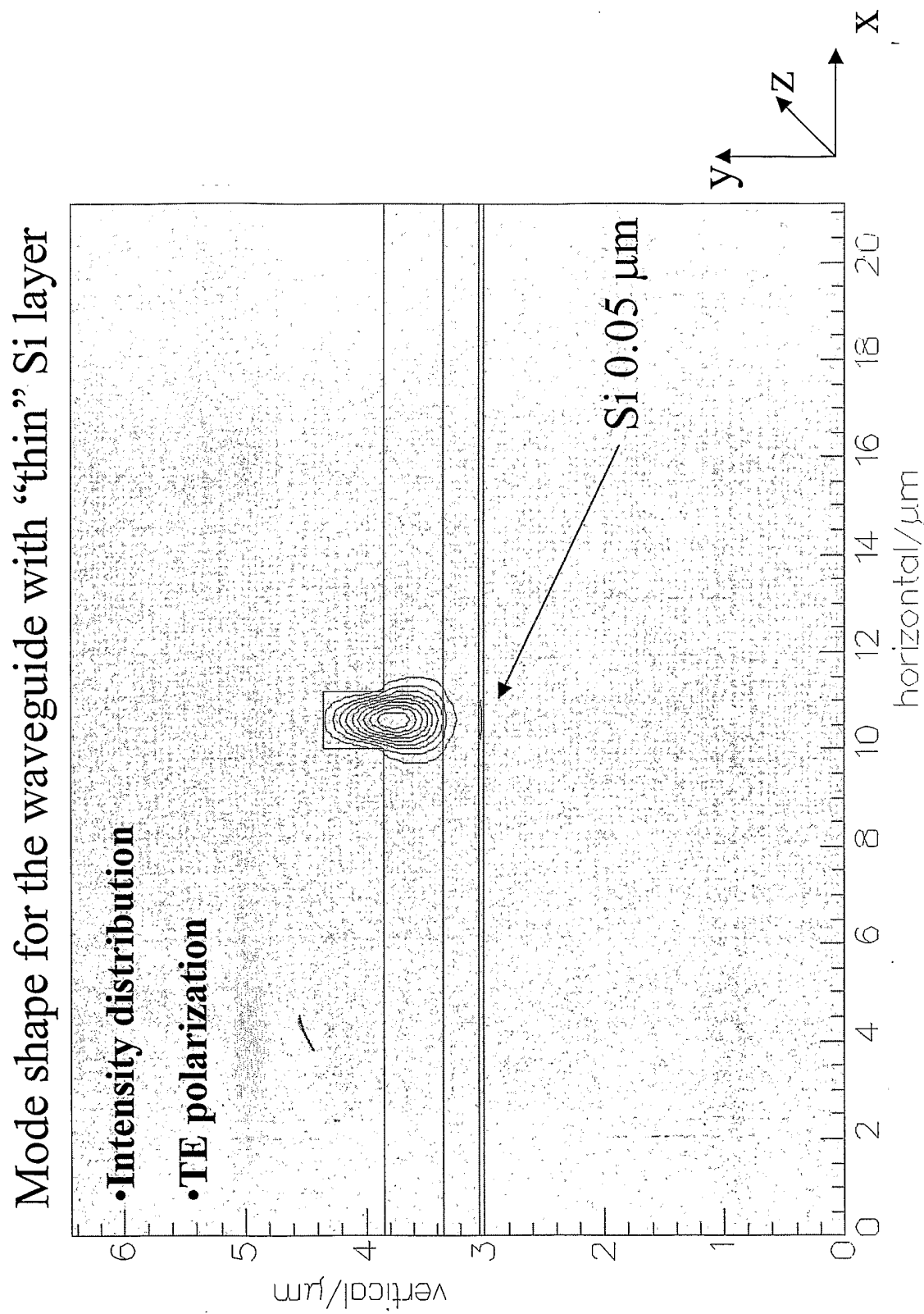


Figure 6D

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/039419

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G02F1/035 G02B6/13

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G02F G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2004/151463 A1 (TALIN ALBERT ALEC ET AL) 5 August 2004 (2004-08-05) paragraph '0010! - paragraph '0017! paragraph '0028! - paragraph '0029! figure 1	1-24
Y	NAMAVAR F ET AL: "ULTRATHIN SOI STRUCTURES BY LOW ENERGY OXYGEN IMPLANTATION" MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS, MATERIALS RESEARCH SOCIETY, PITTSBURG, PA, US, vol. 235, 2 December 1991 (1991-12-02), pages 109-114, XP008045539 ISSN: 0272-9172 the whole document	1-24

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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- *O* document referring to an oral disclosure, use, exhibition or other means
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Date of the actual completion of the international search

19 April 2005

Date of mailing of the international search report

02/05/2005

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INTERNATIONAL SEARCH REPORT

Int

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PCT/US2004/039419

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 064 684 A (MIR ET AL) 12 November 1991 (1991-11-12) column 3, line 7 - line 14 column 3, line 32 - line 39 column 4, line 32 - line 61 column 7, line 30 - line 48 column 9, line 11 - line 14 figures 16,17,20 -----	25
A	US 5 589 407 A (MEYYAPPAN ET AL) 31 December 1996 (1996-12-31) column 3, line 60 - column 4, line 23 column 5, line 17 - line 23 figure 2 -----	26-54
A	US 5 880 491 A (SOREF ET AL) 9 March 1999 (1999-03-09) column 3, line 6 - line 28 column 5, line 48 - line 51 -----	26-54
X	US 6 493 497 B1 (RAMDANI JAMAL ET AL) 10 December 2002 (2002-12-10) column 2, line 60 - column 4, line 34 figure 1 -----	25

INTERNATIONAL SEARCH REPORT

information on patent family members

International Application No
PCT/US2004/039419

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		CN 1543580 A 03-11-2004	
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