A cathode ray tube high voltage supply erase circuit is disclosed which features a transistor switch triggered to conduct periodically to draw current through the primary of the transformer developing a series of capacitor charging pulses through the transformer secondary. The capacitor charged by the transformer secondary is connected in circuit to provide a high voltage supply permitting an image to be written during discharge of the capacitor with the tube anode being drawn to near zero potential as the transistor switch is triggered to conduct to permit erasure of a previously written image on such tube automatically and repetitively without tube damage.
SOLID STATE CATHODE RAY TUBE ERASE CIRCUIT

BACKGROUND OF THE INVENTION

Cathode ray storage tubes are regularly used to present a visual indication and measurement of various functions such as distance, location and velocity between moving radar equipment and fixed or moving objects, or weather phenomena. In many instances that characteristic of storage tubes which serves to maintain an image for a period of time after it is written is undesirable in that the trace of the one object being tracked upon the tube face obscures the positions or traces of other objects also being viewed. This is particularly true where one of the objects being viewed is relatively larger than other objects. For this reason storage tube circuits are provided with means to erase the tube image. This is accomplished usually by energizing a separate electron gun to flood the tube collector screen with electrons. When this is done, however, the tube anode must not be at operating voltage or arcing will occur and probably destroy the tube.

U.S. Pat. No. 2,822,467 to F. L. Washburn, Jr. granted Feb. 4, 1958, shows one example of a CRT system using a separate erase pulse source which is applied to drop the power supply voltage until targets written on a screen have been erased. A later U.S. Pat. No. 2,991,459 to P. F. Dunnington, granted July 4, 1961, relates to a digital oscillograph which includes a separate erase pulse generator capable of being manually operated by energization of vacuum tubes connected up as a one-shot multivibrator. In general, the use of an erase circuit and a separate power supply leads to circuit complexity and an incidental lack of reliability. A specific problem is that the use of a vacuum tube pulse to dump a high voltage supply is an inefficient use of such element and one which materially reduces the life of the tube.

SUMMARY OF THE INVENTION

The present invention relates to a solid state erase circuit for cathode ray storage tubes. It is an object of the invention to provide a simple and inexpensive solid state erase circuit for cathode ray vacuum tubes. It is further object to provide an erase circuit for cathode ray storage tubes which is capable of directly providing the high voltage supply for such tube and automatically providing an erase function without tube damage. It is yet another object to provide a circuit which is long lived in terms of overall power requirements, is more efficient than heretofore available.

The present invention achieves the foregoing objects by utilizing a DC switch in the form of a pair of power transistors triggered to conduct or not to conduct depending on whether the circuit is in use or not. The anode of the transistor is connected to the collector electrode and an electron gun energized for blanking out images previously written. During blanking time the electron gun is energized to flood the collector screen with electrons to effect blanking and erasure of the image previously written. If, during blanking time, the collector is flooded and the anode is maintained at the high voltage necessary for writing, arcing may occur which will seriously damage, if not destroy, the tube.

In accordance with the invention a source of trigger pulses is supplied which is synchronized with the application of the signal causing the electron gun to operate in the flooding mode. These pulses are shown to the left in FIG. 1 and in an actual embodiment are pulses supplied at a 2.5 millisecond rate with a pulse width of approximately 100 microseconds; the fall time of each pulse being on the order of 25 microseconds. In accordance with the invention, the trigger is supplied to an electronic switch in the form of a pair of power transistors Q1 and Q2 as a base connection to Q1, which has its emitter connected to the base of Q2. The emitter of Q2 is tied to ground and there is a bias resistor R1 connected between the base of Q1 and the emitter of Q2, which serves to bias the transistors off in the absence of a pulse. The collectors of Q1 and Q2 are tied in parallel to the primary T1 of a high voltage transformer which is in turn connected to a DC voltage source. When Q1 and Q2 are turned on by the presence of a trigger pulse, DC current is drawn from such supply through T1. The secondary for T1 shown as T2 is connected through a circuit including a high voltage capacitor C1 to the tube anode circuit. Connected across T2 is a first path including a diode D1 and a resistor R2 which forms a clamping circuit to catch voltage peaks generated from the collapsing field in T2 when the switch is cut off, causing current to cease flowing in T1. A further path is connected across T2 to the opposite plate of C1 and includes a diode D2 therein, having a polarity as shown in FIG. 1. The transformer in a preferred and illustrative embodiment includes a turn ratio to boost the voltage from volts to kilovolts, with the secondary being wound to provide a current i1 responsive to current flowing in T1 as shown in FIG. 1. The current i1 is caused to flow through D2 to effectively isolate C1 from the load and drop the voltage across the load to zero, or near to zero, even though C1 contains an appreciable high voltage charge. In an actual embodiment the capacitor was dropped from 7.5 KV to about 7.2 KV. As the switch of the circuit of FIG. 1 cuts off in response to the cessation of a trigger pulse, i1 ceases to flow. This permits C1 to then discharge through the load developing a current shown as i2 and applying full voltage to the tube circuit. The internal resistance of the anode circuit of the load comprising C2 and R2 in conjunction with C1 determines the discharge characteristics of the circuit, as depicted in FIG. 2, so that C1 is not appreciably discharged. As the trigger pulse again turns on the switch to draw current through T1 and establish i1, C1 is then bias isolated again and the anode circuit of the load is again brought to near zero to coincide with the flooding of the tube collector electrode and provide erasure of the previously written image. As can be discerned from FIG. 2, an image is written during the time between trigger pulses and while C1 is discharging through the load circuit to maintain the high voltage supply necessary for image writing.

In an actual embodiment for a Tonotron H-1116-A2 pat cathode ray storage tube the anode circuit parameters include an R1 of approximately 15 megohms and a C1 of approximately 150 microfarads. The invention circuit for such tube included a capacitor C1 of 0.005 microfarads. The switch was comprised of power transistors 2N3772 for Q1 and 2N5055 for Q2 and the bias resistor R1 was approximately 510 ohms. The diodes were standard high voltage diodes. The DC power supply was approximately 25 volts and the transformer had a 1:301 step up ratio. Hyperfil tape wound transformer supplied transformer 2 by Westinghouse Co.

While the invention depicts a switch comprised of power transistors, other solid state elements are also contemplated, including SCR's and/or single transistors or SCR's of appropriate power ratings.
Having now disclosed the invention in terms intended to enable a preferred practice thereof, claims are appended which are believed to assert what is inventive.

What is claimed is:

1. In a circuit for providing a high voltage supply to a cathode ray storage tube with automatic erasure a solid state switch connected to a low voltage power supply and triggered to on and off conditions by trigger pulses synchronized to the blanking time for such tube, a transformer including a primary connecting the power supply to said solid state switch with current being caused to flow through such primary during the on condition of said switch and caused to cease flowing through said primary during the off condition of said switch, a high voltage secondary for said primary having the terminals thereof connected to a high voltage capacitor and to the anode electrode of a cathode ray storage tube, means in said circuit connected to the terminals of said secondary, to said capacitor and to said anode electrode to charge said capacitor to a high voltage during the on condition of said switch while current is flowing in said secondary and to effectively drop said anode electrode to substantially zero voltage to permit an erasure of an image on said tube, the said means causing the voltage of said capacitor to be applied to said anode electrode during the said off condition of said solid state switch when said current is caused to cease flowing in said secondary.

2. The circuit of claim 1 wherein said circuit includes means to prevent said capacitor from being appreciably discharged while supplying a high voltage to said tube.

3. The circuit of claim 1 wherein said circuit includes means to limit discharge of said capacitor to less than 10 percent of the charged voltage level.

4. In a circuit for providing a high voltage supply to a cathode ray storage tube with automatic erasure, a switch connected to a current source and responsive to trigger pulses to draw current from said source, a transformer energized by said current to develop a charging potential, a capacitor connected to said transformer to be charged to a high voltage thereby, means connecting said capacitor to the anode electrode of a tube to impress said high voltage thereon, said means including further means to isolate said anode electrode from said capacitor voltage during charging of said capacitor to provide a low voltage impressed on said anode electrode and permit erasure of images during the periods of charging said capacitor.

5. The circuit of claim 4 wherein said further means is comprised of a diode connected across the anode electrode circuit of said tube.

6. The circuit of claim 4 wherein said switch is comprised of a transistor device.

7. In a circuit for providing a high voltage supply to a cathode ray tube of the type having image erasure by collector flooding, a switch connected to a low voltage source, a source of trigger pulses synchronized with the flooding time of said tube to gate said switch on to draw current from said voltage source, capacitor means, and first means responsive to said current to charge said first capacitor means to a high voltage, said means being connected to the anode electrode of said tube and including second means operating to drop said anode electrode to substantially zero voltage while said capacitor means is being charged and thereby while said collector is being flooded and third means to permit a discharge of said capacitor means through said anode electrode in the absence of charging current and in the absence of flooding to permit images to be written on said tube without arcing of tube electrodes.

8. The circuit of claim 7 wherein said first means includes a transformer having the primary thereof connected between the low voltage source and said switch and the secondary thereof connected to said means capacitor and to said anode electrode.

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UNIVERS STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,657,595 Dated April 18, 1972

Inventor(s) ROBERT LEE BRESSLER ET AL.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Claim 7, column 4, line 20, delete "first".

Claim 7, column 4, line 21, before "means" insert -- first --.

Signed and sealed this 15th day of August 1972.

(SEAL)
Attest:

EDWARD M. FLETCHER, JR. ROBERT GOTTSCALK
Attesting Officer Commissioner of Patents
PO-1050
(5/89)

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