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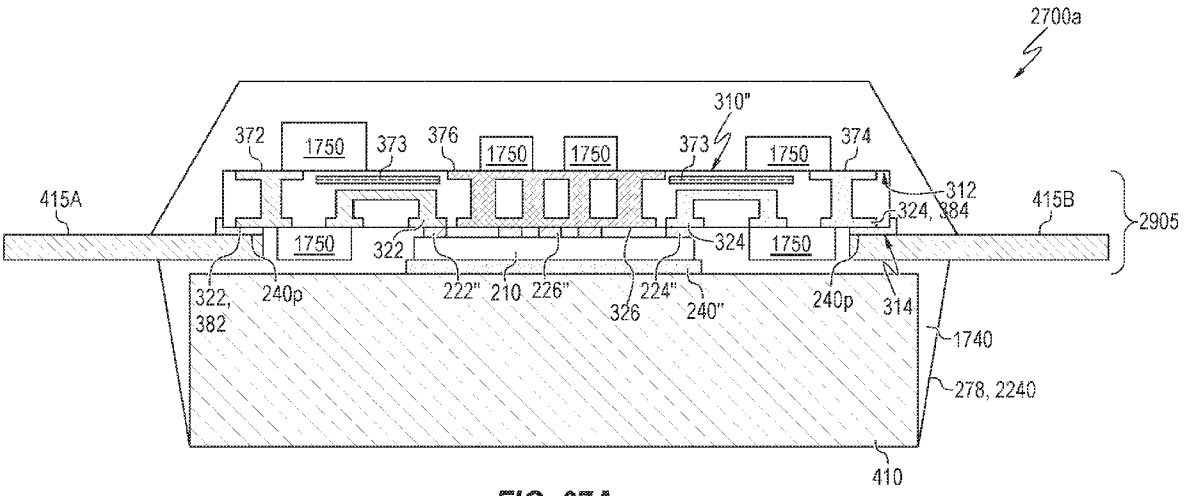


FIG. 27A

(57) Abstract: A transistor device package includes a component assembly comprising an interconnect structure, a transistor die having a front surface including gate, drain, and source terminal on a first surface of the interconnect structure, and one or more passive electrical components electrically coupled to the gate, drain, and/or source terminal by the interconnect structure. A thermally conductive flange is attached to a back surface of the transistor die, which is opposite the front surface, by a conductive adhesive. Respective patterns of the conductive adhesive are provided on the first surface of the interconnect structure, and least one of the respective patterns of the conductive adhesive provides an input, output, or ground signal path for the transistor device package. Related fabrication methods are also discussed.

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RF AMPLIFIER PACKAGE AND MANUFACTURING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims priority from U.S. Patent Application No. 18/334,466 filed on June 14, 2023, which is a continuation-in-part of and claims priority to U.S. Patent Application No. 17/848,546, filed on June 24, 2022, which is a continuation-in-part of and claims priority to U.S. Patent Application No. 17/018,762, filed on September 11, 2020, which is a continuation-in-part of and claims priority to U.S. Patent Application No. 16/906,610, now U.S. Patent No. 11,670,605, filed on June 19, 2020, which claims priority under 35 U.S.C. § 119 to U.S. Provisional Patent Application No. 63/004,765, filed April 3, 2020. U.S. Patent Application No. 18/334,466 is also a continuation-in-part of and claims priority to each of U.S. Patent Application No. 17/018,721, filed on September 11, 2020, and U.S. Patent Application No. 17/737,054, filed on May 5, 2022, which is a continuation of U.S. Patent Application No. 16/888,957, now U.S. Patent No. 11,356,070, filed on June 1, 2020. The entire contents of each of these applications are incorporated herein by reference.

FIELD

[0002] The present disclosure is directed to integrated circuit devices, and more particularly, to structures for integrated circuit device packaging.

BACKGROUND

[0003] RF power amplifiers are used in a variety of applications such as base stations for wireless communication systems, multi-stage and multiple-path amplifiers (e.g., Doherty amplifiers), etc. The signals amplified by the RF power amplifiers often include signals that have a modulated carrier having frequencies in the megahertz (MHz) to gigahertz (GHz) range. For example, Electrical circuits requiring high power handling capability while operating at high frequencies, such as R-band (0.5-1 GHz), S-band (3 GHz), X-band (10 GHz), Ku-band (12-18 GHz), K-band (18-27 GHz), Ka-band (27-40 GHz) and V-band (40-75 GHz) have become more prevalent. In particular, there is now a high demand for radio frequency ("RF") transistor amplifiers that are used to amplify RF signals at frequencies of, for example, 500 MHz and higher (including microwave frequencies). These RF transistor

amplifiers may need to exhibit high reliability, good linearity and handle high output power levels.

[0004] Many RF power amplifier designs utilize semiconductor switching devices as amplification devices. Examples of these switching devices include power transistor devices, such as MOSFETs (metal-oxide semiconductor field-effect transistors), DMOS (double-diffused metal-oxide semiconductor) transistors, HEMTs (high electron mobility transistors), MESFETs (metal-semiconductor field-effect transistors), LDMOS (laterally-diffused metal-oxide semiconductor) transistors, etc.

[0005] RF amplifiers are typically formed as semiconductor integrated circuit chips. Most RF amplifiers are implemented in silicon or using wide bandgap semiconductor materials (i.e., having a band-gap greater than 1.40 eV), such as silicon carbide ("SiC") and Group III nitride materials. As used herein, the term "Group III nitride" refers to those semiconducting compounds formed between nitrogen and the elements in Group III of the periodic table, usually aluminum (Al), gallium (Ga), and/or indium (In). The term also refers to ternary and quaternary compounds, such as AlGaN and AlInGaN. These compounds have empirical formulas in which one mole of nitrogen is combined with a total of one mole of the Group III elements.

[0006] Silicon-based RF amplifiers are typically implemented using LDMOS transistors, and can exhibit high levels of linearity with relatively inexpensive fabrication. Group III nitride-based RF amplifiers are typically implemented using HEMTs, primarily in applications requiring high power and/or high frequency operation where LDMOS transistor amplifiers may have inherent performance limitations.

[0007] RF transistor amplifiers may include one or more amplification stages, with each stage typically implemented as a transistor amplifier. In order to increase the output power and current handling capabilities, RF transistor amplifiers are typically implemented in a "unit cell" configuration in which a large number of individual "unit cell" transistors are arranged electrically in parallel. An RF transistor amplifier may be implemented as a single integrated circuit chip or "die," or may include a plurality of dies. When multiple RF transistor amplifier dies are used, they may be connected in series and/or in parallel.

[0008] RF transistor amplifiers often include matching circuits, such as impedance matching circuits, that are designed to improve the impedance match between the active transistor die (e.g., including MOSFETs, HEMTs, LDMOS, etc.) and transmission lines connected thereto for RF signals at the fundamental operating frequency, and harmonic termination circuits that are designed to at least partly terminate harmonic products that may be generated during

device operation such as second and third order harmonic products. The termination of the harmonic products also influences generation of intermodulation distortion products.

[0009] The RF amplifier transistor die(s) as well as the impedance matching and harmonic termination circuits may be enclosed in a device package. A die or chip may refer to a small block of semiconducting material or other substrate on which electronic circuit elements are fabricated. Integrated circuit packaging may refer to encapsulating one or more dies in a supporting case or package that protects the dies from physical damage and/or corrosion, and supports the electrical contacts for connection to external circuits. The input and output impedance matching circuits in an integrated circuit device package typically include LC networks that provide at least a portion of an impedance matching circuit that is configured to match the impedance of the active transistor die to a fixed value. Electrical leads may extend from the package to electrically connect the RF amplifier to external circuit elements such as input and output RF transmission lines and bias voltage sources.

[0010] Some conventional methods for assembling RF power devices may involve assembling the transistor die and some of the matching network components in a ceramic or over-molded package on a CPC (copper, copper-molybdenum, copper laminate structure) or copper flange, which may be used to dissipate heat, and may be attached to a customer heat sink in some applications. The transistor die, capacitors, and input/output leads may be interconnected with wires, such as gold and/or aluminum wires (also referred to herein as chip-and-wire configurations). Such an assembly process may be slow and sequential (e.g., one package bonded at a time), and assembly costs may be high (e.g., due to cost of gold wires and expensive wire-bond machines). Also, as operating frequencies increase, a chip-and-wire type of RF power device may suffer performance losses from long, high impedance connections using wire bonding.

SUMMARY

[0011] According to some embodiments, a transistor device package includes a component assembly comprising an interconnect structure, a transistor die having a front surface including a gate terminal, a drain terminal, and a source terminal on a first surface of the interconnect structure, and one or more passive electrical components electrically coupled to the gate, drain, and/or source terminal by the interconnect structure. A thermally conductive flange is attached to a back surface of the transistor die, which is opposite the front surface, by a conductive adhesive.

[0012] In some embodiments, respective patterns of the conductive adhesive are on the first surface of the interconnect structure. At least one of the respective patterns of the conductive adhesive provide an input, output, or ground signal path for the transistor device package.

[0013] In some embodiments, the respective patterns of the conductive adhesive attach and electrically connect one or more conductive leads to respective conductive patterns on the first surface of interconnect structure.

[0014] In some embodiments, the respective patterns of the conductive adhesive attach and electrically connect the thermally conductive flange to conductive patterns on the first surface of the interconnect structure.

[0015] In some embodiments, the interconnect structure comprises one or more conductive leads integrated therein that protrude outside a periphery of the transistor device package.

[0016] In some embodiments, one or more support structures extend from the thermally conductive flange to the first surface of the interconnect structure.

[0017] In some embodiments, the one or more support structures comprise one or more conductive support structures that are attached and electrically connected to the conductive patterns on the first surface of the interconnect structure by the respective patterns of the conductive adhesive.

[0018] In some embodiments, the one or more conductive support structures comprise one or more conductive pillar structures that are integral to and protrude from the thermally conductive flange to the first surface of the interconnect structure.

[0019] In some embodiments, the one or more conductive leads comprise a portion that is inside a periphery of the transistor device package and is bent towards or away from the first surface of the interconnect structure.

[0020] In some embodiments, an overmold material is formed on the transistor die between the first surface of the interconnect structure and the thermally conductive flange.

[0021] In some embodiments, the one or more passive electrical components are on a second surface of the interconnect structure that is opposite the first surface.

[0022] In some embodiments, at least one of the passive electrical components is on a portion of the second surface of the interconnect structure that overlaps with the transistor die on the first surface.

[0023] In some embodiments, an overmold material is formed on the one or more passive electrical components on the second surface of the interconnect structure.

[0024] In some embodiments, a lid member defining an open cavity around the one or more passive electrical components is provided on the second surface of the interconnect structure.

[0025] In some embodiments, the one or more passive electrical components comprise a surface mount device and/or an integrated passive device.

[0026] In some embodiments, the transistor device package is free of wire bond connections.

[0027] According to some embodiments, a transistor device package includes a component assembly comprising an interconnect structure, and a transistor die having a front surface including a gate terminal, a drain terminal, and a source terminal on a first surface of the interconnect structure. Respective patterns of a conductive adhesive are provided on the first surface of the interconnect structure. At least one of the respective patterns of the conductive adhesive provides an input, output, or ground signal path for the transistor device package.

[0028] In some embodiments, the respective patterns of the conductive adhesive attach and electrically connect one or more conductive leads to respective conductive patterns on the first surface of interconnect structure.

[0029] In some embodiments, the respective patterns of the conductive adhesive attach and electrically connect a thermally conductive flange to conductive patterns on the first surface of the interconnect structure.

[0030] According to some embodiments, a method of fabricating a transistor device package, includes providing a component assembly comprising an interconnect structure, a transistor die having a front surface including a gate terminal, a drain terminal, and a source terminal on a first surface of the interconnect structure, and one or more passive electrical components electrically coupled to the gate, drain, and/or source terminal by the interconnect structure. The method further includes attaching a back surface of the transistor die, which is opposite the front surface, to a thermally conductive flange by a conductive adhesive.

[0031] In some embodiments, respective patterns of the conductive adhesive are provided on the first surface of the interconnect structure. The respective patterns of the conductive adhesive provide an input, output, or ground signal path for the transistor device package.

[0032] In some embodiments, the method includes applying the conductive adhesive in the respective patterns on one or more conductive leads, and then attaching the one or more conductive leads to conductive patterns on the first surface of the interconnect structure using the respective patterns of the conductive adhesive. The respective patterns of the conductive adhesive electrically connect the one or more conductive leads to the conductive patterns of the interconnect structure.

[0033] In some embodiments, the method includes applying the conductive adhesive in the respective patterns on respective areas of the first surface of the interconnect structure, and then attaching the thermally conductive flange to conductive patterns on the respective areas

of the first surface of the interconnect structure. The respective patterns of the conductive adhesive electrically connect the thermally conductive flange to the conductive patterns of the interconnect structure.

[0034] In some embodiments, the interconnect structure comprises one or more conductive leads integrated therein that protrude outside a periphery of the transistor device package.

[0035] In some embodiments, the thermally conductive flange comprises one or more conductive pillar structures that protrude therefrom, and wherein attaching the thermally conductive flange comprises attaching the one or more conductive pillar structures to the conductive patterns on the first surface of the interconnect structure by the respective patterns of the conductive adhesive.

[0036] In some embodiments, the interconnect structure comprises a respective one of a plurality of interconnect structures of an interconnect array, and the method further includes singulating the interconnect array into the plurality of interconnect structures prior to attaching the thermally conductive flange.

[0037] In some embodiments, the interconnect array comprises slots therein, and attaching the thermally conductive flange includes inserting a clamping device into one or more of the slots, and clamping the thermally conductive flange to the interconnect structure using the clamping device such that the one or more conductive pillar structures contact the respective areas of the first surface of the interconnect structure having the respective patterns of the conductive adhesive thereon.

[0038] In some embodiments, the interconnect structure comprises a respective one of a plurality of interconnect structures of an interconnect array. The method further includes singulating the interconnect array into the plurality of interconnect structures after attaching the thermally conductive flange.

[0039] In some embodiments, the method includes forming an overmold material on the transistor die between the first surface of the interconnect structure and the thermally conductive flange.

[0040] In some embodiments, the one or more passive electrical components are provided a second surface of the interconnect structure that is opposite the first surface.

[0041] In some embodiments, the method includes forming an overmold material structure on the one or more passive electrical components on the second surface of the interconnect structure.

[0042] In some embodiments, the method includes providing a lid member defining an open cavity around the one or more passive electrical components on the second surface of the interconnect structure.

[0043] In some embodiments, the transistor device package is free of wire bond connections.

[0044] In some embodiments, the transistor die comprises a high electron mobility transistor (HEMT) or a laterally-diffused metal-oxide semiconductor (LDMOS) transistor.

[0045] In some embodiments, the transistor die is a Group III nitride-based RF transistor amplifier die.

[0046] Other devices, apparatus, and/or methods according to some embodiments will become apparent to one with skill in the art upon review of the following drawings and detailed description. It is intended that all such additional embodiments, in addition to any and all combinations of the above embodiments, be included within this description, be within the scope of the invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0047] FIG. 1A is a schematic cross-sectional view of a conventional high electron mobility transistor.

[0048] FIG. 1B is a schematic side view of a conventional packaged Group III nitride-based RF transistor amplifier. FIG. 1C is a schematic cross-sectional view taken along line 1C—1C of FIG. 1B that shows the structure of the top metallization of an RF transistor amplifier die that is included in the RF transistor amplifier of FIG. 1B. FIG. 1D is a schematic side view of another conventional Group III nitride-based RF transistor amplifier.

[0049] FIG. 2A is a schematic side view of a Group III nitride-based RF transistor amplifier according to some embodiments of the present invention.

[0050] FIG. 2B is a schematic plan view of an RF transistor amplifier die that is part of the Group III nitride-based RF transistor amplifier of FIG. 2A, taken along line 2B—2B of FIG. 2A.

[0051] FIG. 2C is a cross-sectional view taken along line 2C—2C of FIG. 2B.

[0052] FIG. 2D is a cross-sectional view taken along line 2D—2D of FIG. 2B.

[0053] FIG. 2E is a cross-sectional view taken along line 2E—2E of FIG. 2B.

[0054] FIG. 2F is a cross-sectional view taken along line 2F—2F of FIG. 2B.

[0055] FIGS. 2G to 2L are cross-sectional views of additional embodiments of the present invention.

[0056] FIG. 3A is a schematic cross-sectional view of an RF transistor amplifier coupled to a circuitry module, according to some embodiments of the present invention.

[0057] FIG. 3B is a schematic cross-sectional view of an RF transistor amplifier die coupled to a circuitry module, according to some embodiments of the present invention.

[0058] FIG. 3C is a schematic cross-sectional view of an RF transistor amplifier die incorporating a redistribution layer that is coupled to a circuitry module, according to some embodiments of the present invention.

[0059] FIG. 3D is a schematic cross-sectional view of a circuitry module coupled to a plurality of RF transistor amplifiers, according to some embodiments of the present invention. FIG. 3E is a schematic cross-sectional view of a circuitry module coupled to a plurality of RF transistor amplifier dies, according to some embodiments of the present invention.

[0060] FIG. 4A is a schematic cross-sectional view of an RF transistor amplifier and circuitry module coupled to a carrier substrate, according to some embodiments of the present invention.

[0061] FIG. 4B is a schematic cross-sectional view of an RF transistor amplifier and circuitry module coupled to a carrier substrate without a coupling element, according to some embodiments of the present invention.

[0062] FIG. 4C is a schematic cross-sectional view of a plurality of RF transistor amplifier dies coupled to a circuitry module and placed on a carrier substrate, according to some embodiments of the present invention.

[0063] FIGS. 5A to 5C are schematic views of various packaging options of the RF transistor amplifier, according to some embodiments of the present invention.

[0064] FIGS. 6A to 6C are schematic cross-sectional views of additional embodiments of an RF transistor amplifier coupled to a circuitry module, according to some embodiments of the present invention.

[0065] FIGS. 7A to 7E are schematic diagrams illustrating methods of coupling circuitry modules and RF transistor amplifier dies according to certain embodiments of the present invention.

[0066] FIGS. 8A and 8B are schematic cross-sectional views of various packaging options of a circuitry module, according to some embodiments of the present invention.

[0067] FIGS.9A is a plan view of an embodiment of a circuitry module, according to some embodiments of the present invention.

[0068] FIG. 9B is a cross-sectional view taken along line 9B—9B of FIG. 9A.

[0069] FIG. 9C is a cross-sectional view taken along line 9C—9C of FIG. 9A.

[0070] FIG. 9D is a cross-sectional view of the circuitry module of FIG. 9A, mounted on a substrate according to some embodiments of the present invention.

[0071] FIGS. 10A and 10B are schematic cross-sectional views of various packaging options of the circuitry module, according to some embodiments of the present invention.

[0072] FIGS. 11A, 11B, 11C, and 11D die are schematic cross-sectional views of additional embodiments of an RF transistor amplifier coupled to a circuitry module, according to some embodiments of the present invention.

[0073] FIGS. 12A, 12B, 12C, and 12D are schematic cross-sectional views of additional embodiments of an RF transistor amplifier die coupled to a circuitry module, according to some embodiments of the present invention.

[0074] FIGS. 13A, 13B, 13C, and 13D are schematic cross-sectional views of additional embodiments of an RF transistor amplifier die coupled to a circuitry module and incorporating a spacer, according to some embodiments of the present invention.

[0075] FIGS. 14A, 14B, 14C, and 14D are schematic cross-sectional views of various packaging options of a circuitry module, according to some embodiments of the present invention.

[0076] FIGS. 15A, 15B, 15C, and 15D are schematic cross-sectional views of additional RF transistor amplifier embodiments including circuitry module and incorporating mechanisms to couple to the first and second circuit elements, according to some embodiments of the present invention.

[0077] FIGS. 16A, 16B, 16C, and 16D are schematic cross-sectional views of various packaging options of a circuitry module, according to some embodiments of the present invention.

[0078] FIGS. 17 and 18 are schematic cross-sectional views of RF transistor amplifiers including active and passive component assemblies according to some embodiments of the present invention.

[0079] FIGS. 19A, 19B, and 19C are schematic cross-sectional views of various passive component assemblies according to some embodiments of the present invention.

[0080] FIGS. 20A, 20B, and 20C are schematic cross-sectional views of various active component assemblies according to some embodiments of the present invention.

[0081] FIGS. 21A, 21B, 22, 23A, 23B, 24A, 24B, 24C, 24D, 25A, 25B, and 25C are schematic views of various packaging options for RF transistor amplifiers including active and passive component assemblies according to some embodiments of the present invention.

[0082] FIGS. 26A, 26B, and 26C are schematic circuit diagrams illustrating various circuit topologies that may be implemented by combinations of active and passive component assemblies according to some embodiments of the present invention.

[0083] FIGS. 27A and 27B are schematic cross-sectional views of transistor device packages including flip-chip component assemblies integrated into high power package types according to some embodiments of the present invention.

[0084] FIGS. 28A and 28B are flow diagrams illustrating example operations for fabricating the transistor device packages of FIGS. 27A or 27B.

[0085] FIGS. 29A and 29B are schematic plan views illustrating example implementations of ground signal paths for transistor device packages according to some embodiments of the present invention.

[0086] FIGS. 30A and 30B are schematic cross-sectional views of transistor device packages including flip-chip component assemblies with package leads provided by the interconnect structure and integrated into high power package types according to some embodiments of the present invention.

[0087] FIG. 31A and 31B are flow diagrams illustrating example operations for fabricating the transistor device packages of FIGS. 30A or 30B.

[0088] FIGS. 32A and 32B are schematic plan views and FIG. 32C is a schematic side view illustrating example operations for fabricating transistor device packages according to some embodiments of the present invention. FIG. 32D is a perspective view of a transistor device package formed in accordance with the operations of FIG. 32C.

[0089] FIG. 33 is a flow diagram illustrating example operations for in-strip fabrication of transistor device packages according to some embodiments of the present invention.

[0090] FIGS. 34A, 34B, 34C, and 34D are flow diagrams illustrating example operations for in-strip fabrication of the transistor device packages of FIGS. 30A or 30B according to some embodiments of the present invention.

DETAILED DESCRIPTION

[0091] In the following detailed description, numerous specific details are set forth to provide a thorough understanding of embodiments of the present disclosure. However, it will be understood by those skilled in the art that the present disclosure may be practiced without these specific details. In some instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to obscure the present disclosure. It is intended that all embodiments disclosed herein can be implemented separately or combined

in any way and/or combination. Aspects described with respect to one embodiment may be incorporated in different embodiments although not specifically described relative thereto. That is, all embodiments and/or features of any embodiments can be combined in any way and/or combination.

[0092] Pursuant to embodiments of the present invention, Group III nitride-based RF transistor amplifiers are provided that include RF transistor amplifier dies that have their gate terminals, drain terminals, and source terminals all located on the top side of the RF transistor amplifier die. In some embodiments, the RF transistor amplifiers may not include bond wires for the gate and drain connections, which may reduce an amount of inductance present in the circuit. The top side contacts may allow a coupling element to be coupled directly to the gate, drain, and source terminals of the RF transistor amplifier dies. The coupling element may be further connected to additional circuitry, such as harmonic termination circuitry, input impedance matching circuitry, and/or output impedance matching circuitry in a convenient manner. In particular embodiments where the substrate of the transistor die has a high thermal conductivity, such as a SiC growth substrate for a Group III nitride based HEMT, the die can be mounted with the substrate on a thermally conductive carrier substrate or submount, such as a metal slug, leadframe, or flange, to provide improved thermal dissipation of the heat generated by the die from the amplifier package.

[0093] FIG. 1A is a schematic cross-sectional view of a conventional high electron mobility transistor 10. As shown in FIG. 1A, the high electron mobility transistor 10 may be formed on a substrate 22 such as, for example, a silicon carbide, silicon, or sapphire. A channel layer 24 is formed on the substrate 22. A barrier layer 26 is formed on the channel layer 24 opposite the substrate 22. The channel layer 24 may include, for example, gallium-nitride (GaN) and the barrier layer 26 may include, for example, aluminum gallium-nitride (AlGaN).

[0094] The channel layer 24, and barrier layer 26 may together form a semiconductor structure 90 on the substrate 22. A source contact 56 and a drain contact 54 are formed on an upper surface of the barrier layer 26 and are laterally spaced apart from each other. The source contact 56 and the drain contact 54 may form an ohmic contact to the barrier layer 26.

[0095] A gate contact 52 is formed on the upper surface of the barrier layer 26 between the source contact 56 and the drain contact 54. A two-dimensional electron gas (2DEG) layer is formed at a junction between the channel layer 24 and the barrier layer 26 when the HEMT device 10 is biased to be in its conducting or "on" state. The 2DEG layer acts as a highly conductive layer that allows current to flow between the source and drain regions of the device that are beneath the source contact 56 and the drain contact 54, respectively.

[0096] The source contact 56 may be coupled to a reference signal such as, for example, a ground voltage. The coupling to the reference signal may be provided by a via 66 that extends from a lower surface 22A of the substrate 22, through the substrate 22 to an upper surface 26A of the barrier layer. The via 66 may expose a lower surface 56A of the source contact 56. A backmetal layer 35 may be formed on the lower surface 22A of the substrate 22 and on side walls of the via 66. The backmetal layer 35 may directly contact the source contact 56. Thus, the backmetal layer 35, and a signal coupled thereto, may be electrically connected to the source contact 56.

[0097] In some embodiments, one or more insulating layers 50 may directly contact the upper surface of the semiconductor structure 90 (e.g., contact the upper surface 26A of the barrier layer 26). The one or more insulating layers 50 may serve as passivation layers for the HEMT device 10. In some embodiments, additional metal contacts (not shown) may be provided to contact the gate contact 52 and/or the drain contact 54.

[0098] As noted above, Group III nitride-based RF amplifiers, including the HEMT device illustrated in FIG. 1A, are often used in high power and/or high frequency applications. Typically, high levels of heat are generated within the Group III nitride-based RF amplifier die(s) during operation. If the RF die(s) become too hot, the performance (e.g., output power, efficiency, linearity, gain, etc.) of the RF amplifier may deteriorate and/or the RF amplifier die(s) may be damaged. As such, Group III nitride-based RF amplifiers are typically mounted in packages that may be optimized for heat removal. FIGS. 1B and 1C illustrate a conventional packaged Group III nitride-based RF amplifier. In particular, FIG. 1B is a schematic side view of a conventional packaged Group III nitride-based RF amplifier 100, and FIG. 1C is a schematic cross-sectional view of the RF transistor amplifier die that is included in the packaged Group III nitride-based RF transistor amplifier 100, where the cross-section is taken along line 1C—1C of FIG. 1B. It will be appreciated that FIGS. 1B-1C (and various of the other figures) are highly simplified diagrams and that actual RF amplifiers may include many more unit cells and various circuitry and elements that are not shown in the simplified figures herein.

[0099] As shown in FIG. 1B, the Group III nitride-based RF amplifier 100 includes an RF amplifier die 110 that is mounted within a package 170. The package 170 includes a gate lead 172, a drain lead 174, a carrier substrate 176, and a housing 178. The RF transistor amplifier die 110 is mounted on the upper surface of the carrier substrate 176 which may comprise, for example, a metal flange. The RF amplifier die 110 has a top side 112 and a bottom side 114. The RF amplifier die 110 includes a bottom side (also referred to as a

"back" side) metallization structure 120, a semiconductor layer structure 130 and a top side metallization structure 140 that are sequentially stacked. The back side metallization structure 120 comprises a source terminal 126. The RF amplifier 100 may be a HEMT-based RF amplifier, such as that illustrated in FIG. 1A, in which case the semiconductor layer structure 130 may include at least a channel layer and a barrier layer, which are typically formed on a semiconductor or insulating growth substrate (such as a SiC, silicon, or sapphire substrate). The growth substrate, even if formed of a non-semiconductor material, may be considered to be part of the semiconductor layer structure 130. The top side metallization structure 140 includes, among other things, a gate terminal 142, and a drain terminal 144.

[00100] Input matching circuits 190 and/or output matching circuits 192 may also be mounted within the housing 178. The matching circuits 190, 192 may be impedance matching circuits that match the impedance of the fundamental component of RF signals input to or output from the RF transistor amplifier 100 to the impedance at the input or output of the RF transistor amplifier die 110, respectively, and/or harmonic termination circuits that are configured too short to ground harmonics of the fundamental RF signal that may be present at the input or output of the RF transistor amplifier die 110, such as second order or third order harmonics. As schematically shown in FIG. 1B, the input and output matching circuits 190, 192 may be mounted on the metal flange 176. The gate lead 172 may be connected to the input matching circuit 190 by one or more first bond wires 182, and the input matching circuit 190 may be connected to the gate terminal 142 of RF amplifier die 110 by one or more second bond wires 183. Similarly, the drain lead 174 may be connected to the output matching circuit 192 by one or more fourth bond wires 185, and the output matching circuit 192 may be connected to the drain terminal 144 of RF amplifier die 110 by one or more third bond wires 184. The source terminal 126 of RF transistor amplifier die 110 may be mounted directly on the metal flange 176. The metal flange 176 may provide the electrical connection to the source terminal 126 and may also serve as a heat dissipation structure. The first through fourth bond wires 182-185 may form part of the input and/or output matching circuits. The housing 178 may comprise a ceramic housing, and the gate lead 172 and the drain lead 174 may extend through the housing 178. The housing 178 may comprise multiple pieces, such as a frame that forms the lower portion of the sidewalls and supports the gate and drain leads 172, 174, and a lid that is placed on top of the frame. The interior of the device may comprise an air-filled cavity.

[00101] FIG. 1C is a schematic cross-sectional view of the RF amplifier die 110 that is taken through a portion of the top side metallization structure 140. Dielectric layers that isolate the

various conductive elements of the top-side metallization structure 140 from each other are not shown in FIG. 1C to simplify the drawing.

[00102] As shown in FIG. 1C, the RF transistor amplifier die 110 comprises a Group III nitride-based HEMT RF transistor amplifier that has a plurality of unit cell transistors 116 that each include a gate finger 152, a drain finger 154 and a source finger 156. The gate fingers 152 are electrically connected to a common gate manifold 146, and the drain fingers 154 are electrically connected to a common drain manifold 148. The gate manifold 146 is electrically connected to the gate terminal 142 (e.g., through a conductive via that extends upwardly from the gate manifold 146) which may be implemented as a gate bond pad (see FIG. 1B), and the drain manifold 148 is electrically connected to the drain terminal 144 (e.g., through a conductive via that extends upwardly from the drain manifold 148) which may be implemented as a drain bond pad (see FIG. 1B). The source fingers 156 are electrically connected to the source terminal 126 via a plurality of conductive source vias 166 that extend through the semiconductor layer structure 130. The conductive source vias 166 may comprise metal-plated vias that extend completely through the semiconductor layer structure 130.

[00103] Referring again to FIG. 1B, the carrier substrate 176 (which here is a metal flange) may act as a heat sink that dissipates heat that is generated in the RF amplifier die 110. The heat is primarily generated in the upper portion of the RF amplifier die 110 where relatively high current densities are generated in, for example, the channel regions of the unit cell transistors 116 This heat may be transferred though both the source vias 166 and the semiconductor layer structure 130 to the carrier substrate 176.

[00104] FIG. 1D is a schematic side view of a conventional packaged Group III nitride-based RF transistor amplifier 100' that is similar to the RF transistor amplifier discussed above with reference to FIG. 1B. RF transistor amplifier 100' differs from RF transistor amplifier 100 in that it includes a different package 170'. The package 170' includes a metal submount 176 (which acts as a metal heat sink and can be implemented as a metal slug), as well as gate and drain leads 172', 174'. In some embodiments, a metal lead frame may be formed that is then processed to provide the metal submount 176 and/or the gate and drain leads 172', 174'. RF transistor amplifier 100' also includes a plastic overmold 178' that at least partially surrounds the RF transistor amplifier die 110, the leads 172', 174' and the metal submount 176. The plastic overmold 178' replaces the ceramic sidewalls and lid 178 included in RF transistor amplifier 100.

[00105] Depending on the embodiment, the packaged transistor amplifier 100' can include, for example, a monolithic microwave integrated circuit (MMIC) as the RF transistor amplifier die 110 in which case the RF transistor amplifier die 110 incorporates multiple discrete devices. In some embodiments, the packaged RF transistor amplifier 100 can include multiple RF transistor amplifier die that are connected in series to form a multiple stage RF transistor amplifier and/or may include multiple transistor die that are disposed in multiple paths (e.g., in parallel) to form an RF transistor amplifier with multiple RF transistor amplifier die and multiple paths, such as in a Doherty amplifier configuration

[00106] In other cases, Group III nitride-based RF amplifiers may be implemented as MMIC devices in which one or more RF amplifier die(s) are implemented together with their associated impedance matching and harmonic termination circuits in a single, integrated circuit die. Examples of such Group III nitride-based RF amplifiers are disclosed, for example, in U.S. Patent No. 9,947,616, the entire content of which is incorporated herein by reference. When the RF transistor amplifier die 110 is a MMIC implementation, the input matching circuits 190 and/or the output matching circuits 192 may be omitted (since they may instead be implemented within the RF transistor amplifier die 110) and the bond wires 182 and/or 185 may extend directly from the gate and drain leads 172', 174' to the gate and drain terminals 142, 144.

[00107] Conventional Group III nitride-based RF transistor amplifiers, such as the RF transistor amplifier 100 of FIGS. 1A-1D, may use bond wires 182, 184 to connect the RF transistor amplifier die 110 other portions of the package. These bond wires 182, 184 have inherent inductance that may be used to implement some of the inductors in the impedance matching and/or harmonic termination circuits of the RF transistor amplifiers. The amount of inductance provided may be varied by changing the length and/or the cross-sectional area (e.g., the diameter) of the bond wires 182, 184 so that the bond wires 182, 184 provide a desired amount of inductance. Unfortunately, as applications move to higher frequencies, the inductance of the bond wires 182, 184 may exceed a desired amount of inductance for the impedance matching and/or harmonic termination circuits. When this occurs, bond wires 182, 184 that are very short and/or that have large cross-sectional areas may be used in an effort to decrease the inductance thereof to suitable levels. Very short bond wires 182, 184, however, may be difficult to solder in place, which may increase manufacturing costs, and/or may result in higher device failure rates. Bond wires 182, 184 having large cross-sectional areas may require larger gate and drain bond pads on the RF transistor amplifier die, which may result in an increase in the overall size of the RF transistor amplifier die, which is also

undesirable. Moreover, in some higher frequency applications, even very short bond wires 182, 184 having large cross-sectional areas may have too much inductance such that the matching networks cannot, for example, properly terminate the second or third order harmonics. While the RF transistor amplifiers may be implemented as MMIC devices in order to avoid the problem of too much inductance in the bond wires 182, 184, MMIC RF amplifiers are more expensive to fabricate and can only be used in the frequency range of the matching circuits, reducing flexibility.

[00108] Moreover, wire bonding equipment that is typically used for high volume manufacturing may have a tolerance of +/-1 mil, meaning that the length of any particular wire bond may vary by as much a 2 mils (i.e., +/- 1 mil on each end of the bond wire). For high frequency applications, the variation in inductance associated with 2 mils of a wire bond may be significant, and hence the performance of the matching circuits may be degraded if the bond wires are 1-2 mils too short or long from a desired nominal length. Forming the gate and drain terminals on the top side of the device and using a coupling element to connect these terminals to additional circuitry may largely eliminate this process variation, resulting in improved performance.

[00109] Embodiments of the present invention will now be discussed in further detail with reference to the accompanying figures.

[00110] FIGS. 2A-2G depict a Group III nitride-based RF transistor amplifier 200 according to certain embodiments of the present invention. In particular, FIG. 2A is a schematic side view of the Group III nitride-based RF transistor amplifier 200. FIG. 2B is a schematic plan view of an RF transistor amplifier die 210 that is part of the Group III nitride-based RF transistor amplifier 200 of FIG. 2A that is taken along line 2B—2B of FIG. 2A. FIGS. 2C through 2F are schematic cross-sectional views of the RF transistor amplifier die 210 that are taken along lines 2C—2C through 2F—2F of FIG. 2B, respectively. FIG. 2G is an alternative embodiment of the source terminal illustrated in FIG. 2D. FIGS. 2H to 2L are cross-sectional views of additional embodiments of Group III nitride-based RF transistor amplifiers 200', 200" according to certain embodiments of the present invention.

[00111] As shown in FIG. 2A, in some embodiments, the Group III nitride-based RF transistor amplifier 200 may include an RF transistor amplifier die 210 that is mounted on the bottom surface of a coupling element 270. The RF transistor amplifier die 210 has a top side 212 and a back side 214. The RF transistor amplifier die 210 includes a top side metallization structure 220, a semiconductor layer structure 230, and a bottom side thermal layer 240 that are sequentially stacked. The top side metallization structure 220 comprises a

gate terminal 222, a drain terminal 224, and one or more source terminal(s) 226. The RF transistor amplifier 200 may be a HEMT-based RF transistor amplifier, in which case the semiconductor layer structure 230 may include at least a channel layer and a barrier layer, as will be discussed in greater detail with reference to FIGS. 2C and 2D. In some configurations, as will be discussed further herein, the coupling element 270 may be omitted from the RF transistor amplifier 200.

[00112] The coupling element 270 may be configured to couple to the gate terminal 222, the drain terminal 224, and the one or more source terminal(s) 226. In some cases, the coupling element 270 may comprise a redistribution layer (RDL) laminate structure and/or interposer. An RDL laminate structure refers to a substrate that has conductive layer patterns and/or conductive vias. RDL laminate structures may be fabricated using semiconductor processing techniques by depositing conductive and insulating layers and/or patterns on a base material and by forming vias and routing patterns (e.g., from copper) within the structure for transmitting signals through the RDL laminate structure. For example, as illustrated in FIG. 2A, the coupling element 270 may include conductive patterns 273 formed in an encapsulating structure 277.

[00113] A gate connection pad 272, a drain connection pad 274, and a source connection pad 276 are provided on the top surface of the coupling element 270. Each of these connection pads 272, 274, 276 may comprise, for example, an exposed copper pad, though the present invention is not limited thereto. The gate connection pad 272 may be electrically coupled to the gate terminal 222 by one or more conductive patterns 273 in the coupling element 270. Similarly, the drain connection pad 274 may be electrically coupled to the drain terminal 224 by one or more conductive patterns 273 in the coupling element 270, and the source connection pad 276 may be electrically coupled to source terminal(s) 226 by one or more conductive patterns 273 in the coupling element 270.

[00114] In some embodiments, the conductive patterns 273 of the coupling element 270 may be configured in a fan-out (FO) configuration. The FO configuration may allow for the spacing of the connections to the respective source, gate, and drain terminals to be enlarged, allowing for increased separation of the connections. However, the present invention is not limited to an FO connection. In some embodiments, a fan-in connection, fan-in and fan-out configurations, or other configurations may be used.

[00115] In some embodiments, the coupling element 270 and/or the RDL laminate structure may be formed as part of a wafer level processing (WLP) operation, but the present invention is not limited thereto. For example, the coupling element 270 can be formed by disposing

conductive pillars on the gate terminal 222, drain terminal 224, and the one or more source terminal(s) 226. In some embodiments, the conductive pillars may comprise copper. For example, the conductive pillars may be formed by electroplating a copper seed using one or more masks to form the patterns. The conductive pillars may form the conductive patterns 273. In addition, the gate connection pad 272, the drain connection pad 274, and the source connection pad 276 may be formed on the conductive patterns 273. The conductive patterns 273, gate connection pad 272, drain connection pad 274, and source connection pad 276 may be disposed at least partially within the encapsulating structure 277, which may include an overmold material. The overmold material may include, for example, silicon oxide, silicon nitride, an oxide of the conductive patterns 273, a polymer, a molding compound, and/or a combination thereof. The overmold material may be processed (e.g., planarized) to expose the gate connection pad 272, the drain connection pad 274, and/or the source connection pad 276. In some embodiments, the formation of the coupling element 270 may be performed at the wafer level, and individual ones of the RF transistor amplifier dies 210 and/or RF transistor amplifiers 200 may be singulated from the wafer.

[00116] In some embodiments, the coupling element 270 may be formed in a chip-first or chip-last process. In a chip-first process, the RDL structure may be formed on the die 210 (or wafer including die 210). For example, a seed layer may be deposited (e.g., on one or more of the gate terminal 222, the drain terminal 224, and the one or more source terminal(s) 226. The seed may then be patterned and electroplated to form a layer of conductive material. This process may be repeated multiple times to from the conductive patterns 273 of the coupling element 270. These conductive patterns 273 may then be enclosed in the encapsulating structure 277 to form the coupling element 270.

[00117] In a chip-last process, the RDL layers of the coupling element 270 may be formed on a temporary carrier layer. The conductive patterns 273 may be formed in a manner similar to the chip-first process on the temporary carrier layer. When complete, the coupling element 270 may be decoupled from the temporary carrier layer and then recoupled to the die 210. For example, the coupling element 270 may be coupled to one or more of the gate terminal 222, the drain terminal 224, and the one or more source terminal(s) 226 (e.g., via solder).

[00118] Other coupling elements 270 may alternatively be used such as, for example, a printed circuit board (e.g., a multi-layer printed circuit board), a ceramic substrate that includes conductive vias and/or pads, or any coupling structures for the RF transistor amplifier die 210 that can make electrical connections to the top side 212 of the RF transistor amplifier die 210.

[00119] The arrangement of conductive patterns 273 illustrated in FIG. 2A are merely an example, and other arrangements are possible without deviating from the present invention. For example, in some embodiments, conductive patterns 273 of the coupling element 270 may extend adjacent sides of the RF transistor amplifier die 210. In some embodiments, the coupling element 270 may have terminals other than those illustrated in FIG. 2A

[00120] The thermal layer 240 may be on the back side 214 of the RF transistor amplifier die 210. The thermal layer 240 may be a thermally conductive layer configured to facilitate thermal transfer between the RF transistor amplifier die 210 and a carrier substrate to which the RF transistor amplifier die 210 is mounted. In some embodiments, the thermal layer 240 may be omitted. In some embodiments, the thermal layer 240 may be a die attach layer, such as a eutectic layer. The thermal layer 240 can be on the transistor amplifier die 210 and/or extend onto the encapsulating structure 277. The thermal layer 240 can be a metal layer to form a eutective or other metal bond. In some embodiments, the thermal layer 240 can be a thermal adhesive.

[00121] The RF transistor amplifier die 210 may comprise a Group III nitride-based HEMT RF transistor amplifier that includes a plurality of unit cell transistors 216 that are electrically connected to each other in parallel. This can best be seen in FIG. 2B, which schematically depicts a plan view of RF transistor amplifier die 210 below the top side metallization structure 220. The top side metallization structure 220, including the gate terminal 222, the drain terminal 224, and the one or more source terminals 226, are illustrated as dashed lines in FIG. 2B.

[00122] As shown in FIG. 2B, the RF transistor amplifier die 210 includes a gate manifold 242 and a drain manifold 244, a plurality of gate fingers 252, a plurality of drain fingers 254 and a plurality of source fingers 246, all of which may be formed on an upper surface of the semiconductor layer structure 230. The gate manifold 242 and gate fingers 252 are part of a gate electrode of the RF transistor amplifier die 210. The gate manifold 242 and the gate fingers 252 may be implemented as a first monolithic metal pattern, but the present invention is not limited thereto. The drain manifold 244 and drain fingers 254 are part of a drain electrode of the RF transistor amplifier die 210, and may be implemented as a second monolithic metal pattern, but the present invention is not limited thereto.

[00123] The gate fingers 252 may be formed of materials that are capable of making a Schottky contact to a Group III nitride-based semiconductor material, such as Ni, Pt, Cu, Pd, Cr, W, and/or WSiN. The drain fingers 254 and source fingers 246 may include a metal (e.g., TiAlN, TiSiNi, or the like) that can form an ohmic contact to Group III nitride-based

materials. A dielectric layer (or a series of dielectric layers) that help isolate the gate manifold/fingers 242, 252, the drain manifold/fingers 244, 254 and the source fingers 246 from each other is not shown in FIG. 2B to better illustrate the elements of the RF transistor amplifier die 210.

[00124] The gate terminal 222, drain terminal 224, and source terminal(s) 226 may be provided on the upper surface of the RF transistor amplifier die 210. The gate terminal 222 may be physically and electrically connected to the gate manifold 242 (e.g., by conductive vias), the source terminal(s) 226 may be physically and electrically connected to the source fingers 246 (e.g., by conductive vias), and the drain terminal 224 may be physically and electrically connected to the drain manifold 244 (e.g., by conductive vias). Though the various terminals are illustrated as being directly connected to the gate/drain manifold and/or source fingers, it will be understood that, in some embodiments, intermediate elements may be present. For example, in some embodiments, capacitors, inductors, resistors, etc., may be coupled between the terminal and the respective manifold and/or finger. As an example, a capacitor may be formed on the surface of the RF transistor amplifier die 210 that is coupled to the drain manifold 244, and the drain terminal 224 may be coupled to the capacitor.

[00125] One of the unit cell transistors 216 is also shown in FIG. 2B. As shown, the unit cell transistor 216 includes a gate finger 252, a drain finger 254, and a source finger 246 along with the underlying portion of the semiconductor layer structure 230. Since all of the gate fingers 252 are electrically connected to a common gate manifold 242, all of the drain fingers 254 are electrically connected to a common drain manifold 244, and all of the source fingers 246 are electrically connected together via the source terminal(s) 226 (discussed below), it can be seen that the unit cell transistors 216 are all electrically connected together in parallel.

[00126] The unit cell transistors 216 may be HEMT devices. Suitable structures for Group III-nitride-based HEMT devices that may utilize embodiments of the present invention are described, for example, in commonly assigned U.S. Patent Publication No. 2002/0066908A1 published Jun. 6, 2002, for "Aluminum Gallium Nitride/Gallium Nitride High Electron Mobility Transistors Having A Gate Contact On A Gallium Nitride Based Cap Segment And Methods Of Fabricating Same," U.S. Patent Publication No. 2002/0167023A1 for "Group-III Nitride Based High Electron Mobility Transistor (HEMT) With Barrier/Spacer Layer," published Nov. 14, 2002, U.S. Patent Publication No. 2004/0061129 for "Nitride-Based Transistors And Methods Of Fabrication Thereof Using Non-Etched Contact Recesses," published on April 1, 2004, U.S. Patent No. 7,906,799 for "Nitride-Based Transistors With A Protective Layer And A Low-Damage Recess" issued March 15, 2011, and U.S. Patent No.

6,316,793 entitled "Nitride Based Transistors On Semi-Insulating Silicon Carbide Substrates," issued November 13, 2001, the disclosures of which are hereby incorporated herein by reference in their entirety.

[00127] Referring to FIGS. 2C and 2D, the semiconductor layer structure 230 includes a plurality of semiconductor layers. In the depicted embodiment, a total of two semiconductor layers are shown, namely a channel layer 234 and a barrier layer 236 that is on a top side of the channel layer 234. The semiconductor layer structure 230 may include additional semiconductor and/or non-semiconductor layers. For example, the semiconductor layer structure 230 may include a growth substrate 232 on which the other semiconductor layers are grown. The growth substrate 232 may be a semi-insulating silicon carbide (SiC) substrate that may be, for example, the 4H polytype of silicon carbide. Other silicon carbide candidate polytypes may include the 3C, 6H, and 15R polytypes. The growth substrate 232 may be a High Purity Semi-Insulating (HPSI) substrate, available from Cree, Inc. The term "semi-insulating" is used descriptively herein, rather than in an absolute sense.

[00128] In some embodiments of the present invention, the silicon carbide bulk crystal of the growth substrate 232 may have a resistivity equal to or higher than about $1x10^5$ ohm-cm at room temperature. Exemplary SiC substrates that may be used in some embodiments of the present invention are manufactured by, for example, Cree, Inc., of Durham, N.C., the assignee of the present invention, and methods for producing such substrates are described, for example, in U.S. Pat. No. Re. 34,861, U.S. Pat. No. 4,946,547, U.S. Pat. No. 5,200,022, and U.S. Pat. No. 6,218,680, the disclosures of which are incorporated by reference herein in their entireties. Although silicon carbide may be used as a substrate material, embodiments of the present application may utilize any suitable substrate, such as sapphire (Al_2O_3), aluminum nitride (AlN), aluminum gallium nitride (AlGaN), gallium nitride (GaN), silicon (Si), GaAs, LGO, zinc oxide (ZnO), LAO, indium phosphide (InP), and the like. The growth substrate 232 may be a silicon carbide wafer, and the RF transistor amplifier 200 may be formed, at least in part, via wafer-level processing, and the wafer may then be diced to provide a plurality of individual RF transistor amplifiers 200.

[00129] SiC has a much closer crystal lattice match to Group III nitrides than does sapphire (Al_2O_3) or silicon, which are very common substrate materials for Group III nitride devices. The closer lattice match of SiC may result in Group III nitride films of higher quality than those generally available on sapphire or silicon. SiC also has a very high thermal conductivity so that the total output power of Group III nitride devices on silicon carbide is, typically, not as limited by thermal dissipation of the substrate as in the case of the same

devices formed on sapphire. Also, the availability of semi-insulating SiC substrates may provide for device isolation and reduced parasitic capacitance.

[00130] Optional buffer, nucleation, and/or transition layers (not shown) may be provided on the growth substrate 232 beneath the channel layer 234. For example, an AlN buffer layer may be included to provide an appropriate crystal structure transition between an SiC growth substrate 232 and the remainder of the semiconductor layer structure 230. Additionally, strain balancing transition layer(s) may also be provided as described, for example, in commonly assigned U.S. Patent Publication 2003/0102482A1, published June 5, 2003, and entitled "Strain Balanced Nitride Heterojunction Transistors And Methods Of Fabricating Strain Balanced Nitride Heterojunction Transistors," the disclosure of which is incorporated herein by reference as if set forth fully herein.

[00131] The channel layer 234 and the barrier layer 236 may each be formed by epitaxial growth in some embodiments. Techniques for epitaxial growth of Group III nitrides have been described in, for example, U.S. Pat. No. 5,210,051, U.S. Pat. No. 5,393,993, and U.S. Pat. No. 5,523,589, the disclosures of which are also incorporated by reference herein in their entireties. The channel layer 234 may have a bandgap that is less than the bandgap of the barrier layer 236 and the channel layer 234 may also have a larger electron affinity than the barrier layer 236. The channel layer 234 and the barrier layer 236 may include Group III-nitride based materials.

[00132] In some embodiments, the channel layer 234 is a Group III nitride material, such as $Al_xGa_{1-x}N$ where $0 \leqq x < 1$, provided that the energy of the conduction band edge of the channel layer 234 is less than the energy of the conduction band edge of the barrier layer 236 at the interface between the channel and barrier layers 234, 236. In certain embodiments of the present invention, x=0, indicating that the channel layer 234 is gallium nitride ("GaN"). The channel layer 234 may also be other Group III nitrides such as InGaN, AlInGaN or the like. The channel layer 234 may be undoped or unintentionally doped and may be grown to a thickness of, for example, greater than about 2 nm. The channel layer 234 may also be a multi-layer structure, such as a superlattice or combinations of GaN, AlGaN or the like.

[00133] The channel layer 234 may have a bandgap that is less than the bandgap of at least a portion of the barrier layer 236, and the channel layer 234 may also have a larger electron affinity than the barrier layer 236. In certain embodiments, the barrier layer 236 is AlN, AlInN, AlGaN or AlInGaN with a thickness of between about 0.1 nm and about 10 nm or more. In particular embodiments, the barrier layer 236 is thick enough and has a high enough

Al composition and doping to induce a significant carrier concentration at the interface between the channel layer 234 and the barrier layer 236.

[00134] The barrier layer 236 may be a Group III nitride and may have a bandgap larger than that of the channel layer 234 and a smaller electron affinity than the channel layer 234. Accordingly, in certain embodiments of the present invention, the barrier layer 236 may include AlGaN, AlInGaN and/or AlN or combinations of layers thereof. The barrier layer 236 may, for example, be from about 0.1 nm to about 30 nm thick. In certain embodiments, the barrier layer 236 is undoped or doped with an n-type dopant to a concentration less than about 10^{19} cm^{-3}. In some embodiments of the present invention, the barrier layer 236 is $Al_xGa_{1-x}N$ where $0<x<1$. In particular embodiments, the aluminum concentration is about 25%. However, in other embodiments of the present invention, the barrier layer 236 comprises AlGaN with an aluminum concentration of between about 5% and about 100%. In specific embodiments of the present invention, the aluminum concentration is greater than about 10%.

[00135] Due to the difference in bandgap between the barrier layer 236 and the channel layer 234 and piezoelectric effects at the interface between the barrier layer 236 and the channel layer 234, a two dimensional electron gas (2DEG) is induced in the channel layer 234 at a junction between the channel layer 234 and the barrier layer 236. The 2DEG acts as a highly conductive layer that allows conduction between the source region of each unit cell transistor 216 and its associated drain region, where the source region is the portion of the semiconductor layer structure 230 that is directly underneath the source finger 246 and the drain region is the portion of the semiconductor layer structure 230 that is directly underneath the corresponding drain finger 254.

[00136] While semiconductor structure 230 is shown with channel layer 234 and barrier layer 236 for purposes of illustration, semiconductor structure 230 may include additional layers/structures/elements such as a buffer and/or nucleation layer(s) between channel layer 234 and substrate 232, and/or a cap layer on barrier layer 236. HEMT structures including substrates, channel layers, barrier layers, and other layers are discussed by way of example in U.S. Pat. No. 5,192,987, U.S. Pat. No. 5,296,395, U.S. Pat. No. 6,316,793, U.S. Pat. No. 6,548,333, U.S. Pat. No. 7,544,963, U.S. Pat. No. 7,548,112, U.S. Pat. No. 7,592,211, U.S. Pat. No. 7,615,774, U.S. Pat. No. 7,548,112, and U.S. Pat. No. 7,709,269, the disclosures of which are hereby incorporated herein in their entirety by reference. For example, an AlN buffer layer may be formed on the upper surface of the substrate 232 to provide an appropriate crystal structure transition between the silicon carbide substrate 232 and the

remainder of the RF transistor amplifier 200. Additionally, strain balancing transition layer(s) may also and/or alternatively be provided as described, for example, in commonly assigned U.S. Pat. No. 7,030,428, the disclosure of which is incorporated herein by reference as if set forth fully herein. The optional buffer/nucleation/transition layers may be deposited by MOCVD, MBE, and/or HVPE.

[00137] An interlayer insulating layer 238 is formed over the gate fingers 252, the drain fingers 254, and the source fingers 246. The interlayer insulating layer 238 may include a dielectric material, such as SiN, SiO_2, etc.

[00138] The coupling element 270 may be on and/or coupled to the semiconductor layer structure 230. For example, conductive patterns 273 may be coupled, respectively, between the gate connection pad 272 and the gate terminal 222, between the drain connection pad 274 and the drain terminal 224, and between the source connection pad 276 and the source terminal 226. In FIG. 2C, the encapsulating structure 277 of the coupling element 270 is omitted for ease of description. The gate connection pad 272, the drain connection pad 274, and the source connection pad 276 of the coupling element 270 may extend perpendicularly to the gate fingers 252 and drain fingers 254.

[00139] By placing all of the terminals on the top side of the RF transistor amplifier die 210, the RF transistor amplifier 200 according to certain embodiments of the present invention may be able to omit vias to the back side of the RF transistor amplifier die 210. Without vias on the back side of the RF transistor amplifier die 210 connecting the source to the grounded electrically conductive submount, the conductive submount need not be electrically active. Furthermore, the back side of the substrate 232 of the RF transistor amplifier die 210 may be thermally coupled to a thermally conductive submount such as a heat sink or a flange (not shown) to provide improved thermal dissipation. In some embodiments, the thermal layer 240 may facilitate this thermal coupling. When SiC is used as a substrate material, the thermal properties of the package can be further improved due to the improved thermal conductivity of SiC.

[00140] Moreover, the placement of all of the terminals on the top side of the RF transistor amplifier die 210, allows for the use of the coupling element 270, which can bring all of the transistor connections to respective connection pads. This may allow the RF transistor amplifier die 210 to be further coupled to other elements of the circuit (e.g., other routing elements, grounding elements, harmonic and/or input/output impedance matching elements) through the use of connection methods that avoid bonding wires, such as solder.

[00141] FIG. 2D illustrates an example of the connections between the various source fingers 246 and the source terminals 226. As illustrated in FIG. 2D, each of the source fingers 246 may be coupled to a respective source terminal 226, but the present invention is not limited thereto. In some embodiments, the one or more source terminals 226 may be coupled to more than one source finger 246. For example, as illustrated in FIG. 2G, in some embodiments a single source terminal 226 may be provided, and the source terminal 226 may be connected to each of the individual source fingers 246. In some embodiments, multiple source terminals 226 may be provided, each of which is connected to a plurality of source fingers 246. The one or more source terminals 226 may be coupled to the source connection pad 276 by conductive patterns 273 of the coupling element 270.

[00142] FIG. 2E illustrates an example of the connections between the gate manifold 242 and the gate terminal 222. As illustrated in FIG. 2E, the gate manifold 242 may be coupled to the gate terminal 222 by, for example, a plurality of vias. FIG. 2F illustrates an example of the connections between the drain manifold 244 and the drain terminal 224. As illustrated in FIG. 2E, the drain manifold 244 may be coupled to the drain terminal 224 by, for example, a plurality of vias. In both FIGS. 2E and 2F, the gate terminal 222 and/or drain terminal 224 may be coupled, respectively, to the gate connection pad 272 and/or the drain connection pad 274 of the coupling element 270 by one or more conductive patterns 273.

[00143] Though FIGS. 2C, 2E, and 2F illustrate embodiments in which the gate manifold 242 and the gate terminal 222 are separate elements and drain gate manifold 244 and the drain terminal 224 are separate elements (e.g., connected by vias), the present invention is not limited thereto. For example, FIGS. 2H-2J illustrate examples in which the gate/drain manifold and terminal are a single element. For example, referring to FIGS. 2H and 2I, a device 200' may be configured so that the gate manifold 242 extends to the surface of the RF transistor amplifier die 210 to serve as the gate terminal 222. Similarly, FIGS. 2H and 2J illustrate that the device 200' may be configured so that the drain manifold 244 extends to the surface of the RF transistor amplifier die 210 to serve as the drain terminal 224.

[00144] In some embodiments, additional conductive elements and/or discrete circuit components may be formed as part of the RF transistor amplifier die. FIG. 2K illustrates an additional embodiment of an RF transistor amplifier die 210', according to some embodiments of the present invention. FIG. 2K is an embodiment illustrated from the perspective of line 2C-2C of FIG. 2A, with modifications as described herein. For example, as illustrated in FIG. 2K, an RF transistor amplifier die 210' may utilize a number of conductive patterns 223 between the gate manifold 242 and the gate terminal 222, between

the drain gate manifold 244 and the drain terminal 222, and/or between one or more of the source fingers 246 and the source terminal 246. The conductive patterns 223 may be formed within the interlayer insulating layer 238 of the RF transistor amplifier die 210'.

[00145] The conductive patterns 223 may be utilized to form discrete circuit elements integral to the RF transistor amplifier die 210'. For example, the conductive patterns 223 may form an RDL within the RF transistor amplifier die 210'. FIG. 2K illustrates a fan-in configuration that couples the gate/drain manifolds 242, 244 and the source fingers 246 to the gate, drain, and source terminals 222, 224, 226, respectively. However, the present invention is not limited thereto. In some embodiments, the conductive patterns 223 may also be coupled to discrete circuit elements within the interlayer insulating layer 238, such as in a MMIC configuration. The use of an on-die RDL may allow for more flexible packaging options as well as the integration of certain circuit functions, such as impedance matching and/or harmonic termination.

[00146] FIG. 2L illustrates that the RF transistor amplifier die 210' may also be used with a coupling element 270 in an RF transistor amplifier 200''. The embodiment of FIG. 2L may include a first RDL as part of the RF transistor amplifier die 210' and a second RDL as part of the coupling element 270. In some embodiments, the conductive patterns 223 of the RF transistor amplifier die 210' may provide one or more additional integrated circuits, such as impedance matching or harmonic termination, and the conductive patterns 273of the coupling element 270 may provide a fan-in, fan-out, or other configuration. In some embodiments, the combination of the coupling element 270 and RF transistor amplifier die 210' may be enclosed in an encapsulating structure (not shown).

[00147] Though FIGS. 2A-2L illustrate a semiconductor layer structure 230 that comprises a HEMT it will be understood that other types of semiconductor devices may be formed in the semiconductor layer structure 230 without deviating from the present invention. For example, the semiconductor layer structure 230 may include a MOSFET, a DMOS transistor, a MESFET, and/or an LDMOS transistor. One of ordinary skill in the art will recognize that the arrangement of all of the source/drain/gate contacts on a single side of the semiconductor layer structure 230, including the use of the coupling element 270, may allow for improved connection possibilities and better thermal performance.

[00148] By placing gate, drain, and source contacts on a same side of the RF transistor amplifier 200, connection options may be available that were not previously possible. These connection options may also allow for embodiments that can more strongly leverage the improved thermal conductivity of SiC materials.

[00149] FIG. 3A is a schematic cross-sectional view of the RF transistor amplifier 200 coupled to a circuitry module 310 (also referred to herein as an interconnect structure 310), according to some embodiments of the present invention. FIG. 3A includes elements of the RF transistor amplifier 200 that have been previously discussed. As such, the discussion of FIG. 3A will focus on those portions of the embodiments that are different from those discussed with respect to the prior figures.

[00150] Referring to FIG. 3A, the circuitry module 310 may be configured to couple to the gate connection pad 272, the drain connection pad 274, and the source connection pad 276 of the coupling element 270. For example, the circuitry module 310 may expose interconnection pads 322, 324, 326 that may be configured to be coupled to the gate connection pad 272, the drain connection pad 274, and the source connection pad 276. For example, the first interconnection pad 322 may be configured to couple to the gate connection pad 272, the second interconnection pad 324 may be configured to couple to the drain connection pad 274, and the third interconnection pad 326 may be configured to couple to the source connection pad 276. In some embodiments, a bonding element (e.g., solder balls and/or bumps 320) may be used to respectively couple the first, second, and third interconnection pads 322, 324, 326 to the gate connection pad 272, the drain connection pad 274, and the source connection pad 276. Though illustrated as a single pad, in some embodiments, one or more of the first, second, and/or third interconnection pads 322, 324, 326 may include a plurality of pads.

[00151] Each of the first, second, and third interconnection pads 322, 324, 326 may be coupled to one or more conductive patterns 373 within the circuitry module 310. The conductive patterns 373 may provide various routing and/or circuitry within the circuitry module 310. For example, the conductive patterns 373 may connect the first interconnection pad 322 to one or more first surface connection pads 372 and one or more gate lead connection pads 382. Thus, the gate connection pad 272 may be electrically coupled to the one or more first surface connection pads 372 and the one or more gate lead connection pads 382. The conductive patterns 373 may also connect the second interconnection pad 324 to one or more second surface connection pads 374 and one or more drain lead connection pads 384. Thus, the drain connection pad 274 may be electrically coupled to the one or more second surface connection pads 374 and the one or more drain lead connection pads 384. The conductive patterns 373 may also connect the third interconnection pad 326 to one or more third surface connection pads 376 and one or more source lead connection pads 386. Thus, the source connection pad 276 may be electrically coupled to the one or more third

surface connection pads 376 and the one or more source lead connection pads 386. Thus, the circuitry module 310 may have a surface (e.g., a top surface) having a plurality of first surface connection pads 372, respective ones of which are coupled to the gate connection pad 272 of the coupling element 270, a plurality of second surface connection pads 374, respective ones of which are coupled to the drain connection pad 274 of the coupling element 270, and a plurality of third surface connection pads 376, respective ones of which are coupled to the source connection pad 276 of the coupling element 270.

[00152] The conductive patterns 373 may be encased in an isolation material 315. In some embodiments, the isolation material 315 may include, for example, silicon oxide, silicon nitride, an oxide of the conductive patterns 273, a polymer, a molding compound, or a combination thereof. In some embodiments, circuitry module 310 may be formed as a printed circuit board (PCB). In a PCB embodiment, the isolation material 315 may be the substrate of the PCB, and the conductive patterns 373 may be traces formed within the substrate.

[00153] The presence of the conductive patterns 373 and the first, second, and third surface connection pads 372, 374, 376 may allow for a number of different circuits to be coupled to the RF transistor amplifier 200. For example, circuit elements 350 may be coupled (e.g., via solder or other bonding) between two or more of the first, second, and third surface connection pads 372, 374, 376. The circuit elements 350 may provide various electronic capabilities to the RF transistor amplifier 200. For example, the circuit elements 350 may comprise impedances (including, for example, resistive, inductive, and capacitive elements) that may be used for impedance matching and/or harmonic termination. In some embodiments, the circuit elements 350 may provide stripline components and/or baseband termination to the RF transistor amplifier 200.

[00154] Though illustrated as being on the surface of the circuitry module 310, it will be understood that additional circuit elements 350 may be provided internally within the circuitry module 310. For example, one or more ground planes may be formed as a circuit element 350 within the circuitry module 310. Similarly, a stripline may be formed within the circuitry module 310 (e.g., in conjunction with one or more ground planes). The configuration of the conductive patterns 373 and the circuit elements 350 illustrated in FIG. 3A are merely examples and are not intended to limit embodiments of the present invention. In some embodiments, the circuit elements 350 and/or the conductive patterns 373 may be configured to provide at least part of harmonic terminating circuitry, matching circuitry, splitting circuitry, combining circuitry, and/or biasing circuitry. Other configurations of the

conductive patterns 373 and/or other types of circuit elements 350 may be used without deviating from the scope of the present invention.

[00155] In some embodiments, the circuitry module 310 and the circuit elements 350 may be optionally encased within an encapsulating material 316. In some embodiments, the encapsulating material 316 may include, for example, silicon oxide, silicon nitride, a polymer, a molding compound, or a combination thereof.

[00156] The gate lead connection pads 382, drain lead connection pads 384, and source lead connection pads 386 may provide terminals to connect signals to the respective gate, drain, and source of the RF transistor amplifier 200. For example, a connection for providing an input signal to the RF transistor amplifier 200 may be coupled to one or more of the gate lead connection pads 382. In some embodiments, a connection for receiving an output signal from the RF transistor amplifier 200 may be coupled to the drain lead connection pads 384. In some embodiments, a ground signal may be coupled to the source lead connection pads 386, though the present invention is not limited thereto. Though the gate lead connection pads 382, drain lead connection pads 384, and source lead connection pads 386 are illustrated as being at a bottom surface of the circuitry module 310, this is merely an example and not intended to limit the present invention. In some embodiments, the various lead connections may be on a top or other surface of the circuitry module 310.

[00157] The use of the circuitry module 310 in conjunction with the top-side contacts of the RF transistor amplifier 200 allows for additional functionality, such as impedance matching and/or harmonic termination, to be conveniently added to the RF transistor amplifier 200 without the use of extensive wire bonding. Thus, different functionality and/or capability may be coupled to an RF transistor amplifier 200 simply by using a different circuitry module 310. Because the connection points (e.g., the terminals) of the RF transistor amplifier 200 are consistent, variations in the configuration of the RF transistor amplifier 200 may be accomplished more efficiently than previously available. The reduced or eliminated need for wire bonds may also allow for reduced die size in some applications (where the sizes of the wire bond pads drive die size), and hence the RF transistor amplifier dies according to embodiments of the present invention may also exhibit increased integration density. Thus, the RF amplifier die according to embodiments of the present invention may exhibit improved product assembly consistency, higher yields, increased product integration, reduced cost, and improved RF performance, especially for products operating at high frequencies such as millimeter wave frequencies.

[00158] The techniques disclosed herein may be particularly beneficial in higher frequency applications as the inductance required in the matching circuits may be much lower in such applications, and hence the use of traditional bond wires may inject too much inductance. Additionally, the tolerances in the bond wire lengths may have a larger impact at higher frequencies, and in high frequency applications (particularly if lower power) the size of the bond pads may drive the size of the die. In some embodiments, any of the RF transistor amplifier dies disclosed herein may be configured to operate at frequencies greater than 1 GHz. In other embodiments, these RF transistor amplifier dies may be configured to operate at frequencies greater than 2.5 GHz. In still other embodiments, these RF transistor amplifier dies may be configured to operate at frequencies greater than 3.1 GHz. In yet additional embodiments, these RF transistor amplifier dies may be configured to operate at frequencies greater than 5 GHz. In some embodiments, these RF transistor amplifier dies may be configured to operate in at least one of the 2.5-2.7 GHz, 3.4-4.2 GHz or 5.1-5.8 GHz frequency bands or sub-portions thereof.

[00159] FIG. 3B is a schematic cross-sectional view of an RF transistor amplifier die 210 coupled to a circuitry module 310, according to some embodiments of the present invention. FIG. 3B includes elements of the circuitry module 310, circuit elements 350, and RF transistor amplifier die 210 that have been previously discussed. As such, the discussion of FIG. 3B will focus on those portions of the embodiments that are different from those discussed with respect to the prior figures.

[00160] FIG. 3B illustrates an embodiment in which the circuitry module 310 is directly connected to the RF transistor amplifier die 210 without an intervening coupling element 270. Thus, the circuitry module 310 may be configured to couple to the gate terminal 222, the drain terminal 224, and one or more of the source terminal(s) 226 of the RF transistor amplifier die 210. For example, the first interconnection pad 322 of the circuitry module 310 may be configured to couple to the gate terminal 222, the second interconnection pad 324 of the circuitry module 310 may be configured to couple to the drain terminal 224, and the third interconnection pad 326 of the circuitry module 310 may be configured to couple to one or more of the source terminal(s) 226. In some embodiments, a bonding element (e.g., solder balls and/or bumps) 320 may be used to respectively couple the first, second, and third interconnection pads 322, 324, 326 to the gate terminal 222, the drain terminal 224, and one or more of the source terminal(s) 226. Though illustrated as a single pad, in some embodiments, one or more of the first, second, and/or third interconnection pads 322, 324, 326 may include a plurality of pads. The configuration illustrated in FIG. 3B may be useful

when a fan-in or fan-out configuration of a coupling element 270 is not needed to provide a connection between the RF transistor amplifier die 210 and the circuitry module 310.

[00161] FIG. 3C illustrates an embodiment in which the circuitry module 310 is directly connected to an RF transistor amplifier die 210' that incorporates an on-die RDL utilizing conductive patterns 223 without an intervening coupling element 270. Thus, the circuitry module 310 may be configured to couple to the gate terminal 222, the drain terminal 224, and one or more of the source terminal(s) 226 of the RF transistor amplifier die 210'. The RF transistor amplifier die 210' of FIG. 3C is illustrated in cross-section to show an example of the internal conductive patterns (e.g., of an RDL) coupled to the gate terminal 222, the drain terminal 224, and one or more of the source terminal(s) 226. In some embodiments, the RF transistor amplifier die 210' may be a MMIC. Though illustrated without a coupling element 270, it will be understood that, in some embodiments, the coupling element 270 may also be present between the RF transistor amplifier die 210' and the circuitry module 310.

[00162] The use of the coupling element 270 utilizing conductive patterns 273 (if present), the on-die RDL utilizing conductive patterns 223 (if present), and/or the circuitry module 310 utilizing conductive patterns 373 may provide an connection structure between the gate, drain, and source of the RF transistor amplifier die 210 and the gate lead connection pads 382, drain lead connection pads 384, and source lead connection pads 386. By utilizing various combinations of these element and electric bonding techniques, a semiconductor package may be provided that eliminates and/or reduces wire bonding.

[00163] FIG. 3D is a schematic cross-sectional view of a circuitry module 310' coupled to a plurality of RF transistor amplifiers 200, according to some embodiments of the present invention. FIG. 3E is a schematic cross-sectional view of a circuitry module 310' coupled to a plurality of RF transistor amplifier dies 210, according to some embodiments of the present invention. FIGS. 3E and 3E include elements of a circuitry module 310', circuit elements 350, RF transistor amplifier dies 210, and RF transistor amplifiers 200 that have been previously discussed. As such, the discussion of FIGS. 3D and 3E will focus on those portions of the embodiments that are different from those discussed with respect to the prior figures.

[00164] Referring to FIG. 3D, the circuitry module 310' may be configured to couple to more than one RF transistor amplifier 200. FIG. 3D also illustrates that the conductive patterns 373, interconnection pads, and surface connection pads may be modified without deviating from the scope of the invention. For example, the circuitry module 310' may include a plurality of interconnection pads 327. The interconnection pads 327 may be configured to

couple to terminals of the plurality of RF transistor amplifiers 200. For example, an interconnection pad 327 of the circuitry module 310' may be configured to couple to a gate connection pad 272, a drain connection pad 274, and/or a source connection pad 276 of one or more of the plurality of RF transistor amplifiers 200.

[00165] Similarly, the circuitry module 310' may have surface connection pads 377 coupled to one or more of the interconnection pads 327 via conductive patterns 373. Circuit elements 350 may be coupled to one or more of the surface connection pads 377. By using the conductive patterns 373, interconnection pads 327, surface connection pads 377, and/or circuit elements 350, various circuit connections between the plurality of RF transistor amplifiers 200 may be realized. It will be understood that the configuration illustrated in FIG. 3D is merely a schematic example, and that the routing and connections of the various elements of the circuitry module 310' may be variously modified to generate complex circuits involving the RF transistor amplifiers 200.

[00166] In some embodiments, the circuitry module 310' may include one or more gate lead connection pads 382, one or more drain lead connection pads 384, and one or more source lead connection pads 386. Signals provided to the one or more gate lead connection pads 382, one or more drain lead connection pads 384, and one or more source lead connection pads 386 may be distributed through the circuitry module 310' to various ones of the RF transistor amplifiers 200 via the conductive patterns 373.

[00167] Though FIG. 3D illustrates an embodiment in which each one of the plurality of RF transistor amplifiers 200 has its own coupling element 270, it will be understood that other configurations are possible. For example, in some embodiments, a single coupling element 270 may be coupled to a plurality of RF transistor amplifier dies 210. The use of a single coupling element 270 may allow for the use of a circuitry module 310' having fewer interconnections to the transistor elements of the circuit.

[00168] FIG. 3D illustrates an embodiment in which the circuitry module 310' is coupled to a plurality of RF transistor amplifiers 200 that include coupling element 270. However, the present invention is not limited thereto. In some embodiments, the circuitry module 310' may be directly coupled to a plurality of RF transistor amplifier dies 210, 210' that do not include a coupling element 270. FIG. 3E illustrates an embodiment in which the circuitry module 310' is coupled to a plurality of RF transistor amplifier dies 210. It will be understood that the circuitry module 310' may also be coupled to a plurality of RF transistor amplifier dies 210' (e.g., as illustrated in FIG. 2K) without deviating from the present invention. The circuitry module 310' may be coupled to the RF transistor amplifier die 210, 210' by, for

example, bonding element (e.g., solder ball and/or bump) 320. It will be understood that the circuitry module 310 may be coupled to a combination of RF transistor amplifiers 200 that include coupling element 270 and RF transistor amplifier dies 210, 210'.

[00169] The circuitry module 310' may be used, for example, to provide interconnections to the RF transistor amplifiers 200 that may be used to implement a multistage and/or multipath amplifier circuit, such as a Doherty amplifier. The conductive patterns 373 may provide the electrical connections of the multistage and/or multipath amplifier circuit, which may be coupled to ones of the circuit elements 350 to provide capacitors, inductors, resistors, and/or other circuit elements used in the multistage and/or multipath amplifier circuit. Thus, the circuitry module 310' may be configured to provide modular interconnections that can be easily coupled to a plurality of RF transistor amplifiers without the use of bond wires.

[00170] Though FIGS. 3A to 3E illustrate various combinations of circuitry modules 310, 310', coupling elements 270, and RF transistor amplifier dies 210, 210', it will be understood that the present invention is not limited to the specific combinations illustrated in those figures. As will be understood by one of ordinary skill in the art, the of circuitry modules 310, 310', coupling elements 270, and RF transistor amplifier dies 210, 210' may be combined in multiple variations, including those not specifically illustrated, without deviating from the present invention. For example, embodiments of the present invention include the transistor amplifier die 210, 210' directly coupled to the circuitry module 310, 310'. Some embodiments of the present invention include the transistor amplifier die 210, 210' coupled to the circuitry module 310, 310' via a coupling element 270. The coupling element 270 and/or the circuitry module 310, 310' may include PCB or metal core PCB as well as traces on a patterned dielectric material. In some embodiments, the transistor amplifier die 210' may have conductive patterns such as an RDL at the die level, which may include a fan-in and/or fan-out configuration that may be connected to other structures, such as the coupling element 270 or circuitry module 310, 310'.

[00171] FIG. 4A is a schematic cross-sectional view of the RF transistor amplifier 200 and circuitry module 310 coupled to a carrier substrate 410, according to some embodiments of the present invention. FIG. 4B is a schematic cross-sectional view of the RF transistor amplifier 200 coupled to the carrier substrate 410 without a coupling element 270, according to some embodiments of the present invention. FIGS. 4A and 4B include elements of the RF transistor amplifier 200, coupling element 270, and circuitry module 310 that have been previously discussed. As such, the discussion of FIGS. 4A and 4B will focus on those

portions of the embodiments that are different from those discussed with respect to the prior figures.

[00172] Referring to FIG. 4A, the RF transistor amplifier 200 may be placed upon a carrier substrate 410. The carrier substrate 410 may comprise any structure that provides a suitable mounting surface for the RF transistor amplifier 200. In some embodiments, the carrier substrate 410 may comprise a temperature conductive element such a metal flange. In some embodiments, the carrier substrate 410 may comprise, for example, an RDL laminate structure or a PCB. In some embodiments, the carrier substrate 410 may include copper, molybdenum, and/or combinations thereof. In some embodiments, the carrier substrate 410 may be composed of multiple layers and/or contain vias/interconnections. The carrier substrate 410 may be configured to allow the RF transistor amplifier 200 to be easily packaged. As illustrated in FIG. 4A, a circuitry module 310 may be coupled to the RF transistor amplifier 200 as discussed herein.

[00173] In some embodiments, the thermal layer 240 may be placed between the bottom surface of the RF transistor amplifier 200 and the carrier substrate 410. The thermal layer 240 may assist in the transfer of thermal energy from the RF transistor amplifier 200 to the carrier substrate 410. In embodiments in which SiC is utilized as part of the RF transistor amplifier 200, the excellent thermal conductivity of SiC may allow for the carrier substrate 410 to more efficiently dissipate heat of the device. In some embodiments, the thermal layer 240 may include, or be replaced by, a eutectic layer.

[00174] One or more leads 415 may be coupled to the one or more gate lead connection pads 382, one or more drain lead connection pads 384, and one or more source lead connection pads 386 of the circuitry module 310. For example, a first input lead 415A may be coupled to the one or more gate lead connection pads 382 (e.g., via bonding layer 420A, such as solder) to provide an input signal to the RF transistor amplifier 200, and a second output lead 415B may be coupled to the one or more drain lead connection pads 384 (e.g., via bonding layer 420B, such as solder) to receive an output signal from the RF transistor amplifier 200, though the present invention is not limited thereto.

[00175] The lead connections of FIG. 4A are merely an example and other connection and/or connection pads are possible. For example, in FIG. 4A the one or more source lead connection pads 386 are illustrated as being connected to both of the leads 415A and 415B. However, in some embodiments, the one or more source lead connection pads 386 may not be coupled to the source of the RF transistor amplifier 200 (e.g., through the one or more source terminal(s) 226). For example, in some embodiments, one or more of the circuit

elements 350 and/or conductive patterns 373 may be configured to control whether the one or more source lead connection pads 386 are coupled to an input lead 415A, an output lead 415B, or neither. For example, a circuit element 350 may be provided on the circuitry module 310 to connect the source terminal 226 of the RF transistor amplifier 200 to a lead 415. Similarly, the circuitry module 310 may be configured to allow the removal of a circuit element 350 (e.g., a resistor) to disconnect a coupling between a lead 415A or 415B and the source terminal 226 of the RF transistor amplifier 200.

[00176] In addition, though FIG. 4A illustrates an embodiment in which there are two leads 415A and 415B, this is merely an example and not intended to limit the invention. In some embodiments, multiple leads may be provided, respective ones of which are coupled to the gate lead connection pads 382, drain lead connection pads 384, source lead connection pads 386, and/or combinations thereof. For example, in some embodiments, an additional lead may be provided that is configured to provide a ground connection to the source lead connection pads 386. In some embodiments, the source lead connections pads 386 may be configured to couple, for example, to a lead of an RF semiconductor package, which may be coupled to ground. As used herein, the combination of the RF transistor amplifier 200, the circuitry module 310, the leads 415A, 415B, and the carrier substrate 410 may be referred to as a packaged RF transistor amplifier, an RF transistor amplifier package, or simply an RF transistor amplifier.

[00177] The leads 415A, 415B may be between the circuitry module 310 and the carrier substrate 410, but the present invention is not limited thereto. In some embodiments, the carrier substrate 410 may have pedestals 410p that are under and, in some embodiments, supporting the leads 415A and 415B, though the present invention is not limited thereto. In some embodiments, the pedestals 410p may include an insulating material and/or may be separated from the leads 415A, 415B by an insulating layer 460. In some embodiments, as will be discussed further herein, the leads 415A, 415B may be supported by a portion of the package of the RF transistor amplifier 200.

[00178] Though FIG. 4A illustrates the use of coupling element 270, the present invention is not limited thereto. FIG. 4B illustrates an embodiment in which the coupling element is omitted. In the embodiment of FIG. 4B, the circuitry module 310 may have first, second, and third interconnection pads 322, 324, 326 that are spaced apart from one another at distances similar to those of the gate terminal 222, drain terminal 224, and one or more source terminal(s) 226. For example, the first interconnection pad 322 may be connected (e.g., via a bonding elements such as solder ball and/or bump 320) to the gate terminal 222, the second

interconnection pad 324 may be connected to the drain terminal 224, and the third interconnection pad 326 may be connected to the source terminal 226. The direct connection to the circuitry module 310 may be useful when an adjustment to the spacing (e.g., via a fan-in or fan-out structure) of the terminals of the RF transistor amplifier 200 is not needed. Thus, in some embodiments, the coupling element 270 is optional in the RF transistor amplifier 200.

[00179] FIG. 4C illustrates an embodiment in which a plurality of RF transistor amplifiers 200 are coupled to a circuitry module 310' and placed on a carrier substrate 410. For example, as discussed herein with respect to FIGS. 3D and 3E, a plurality of RF transistor amplifier dies 210, 210' may be coupled to a circuitry module 310'. The plurality of RF transistor amplifier dies 210, 210' may be coupled to the circuitry module 310' via a coupling element 270 or directly to the circuitry module 310' (as illustrated in FIG. 3E. The RF transistor amplifier dies 210, 210' and/or the circuitry module 310' may be further placed on a carrier substrate 410, with leads 415A and 415B coupled thereto. In some embodiments, a thermal layer 240 may be placed between the RF transistor amplifier dies 210, 210' and the carrier substrate 410.

[00180] Though FIGS. 4A to 4C illustrate various combinations of circuitry modules 310, 310', coupling elements 270, and RF transistor amplifier dies 210, 210', it will be understood that the present invention is not limited to the specific combinations illustrated in those figures. As will be understood by one of ordinary skill in the art, the of circuitry modules 310, 310', coupling elements 270, and RF transistor amplifier dies 210, 210' may be combined in multiple variations, including those not specifically illustrated, without deviating from the present invention. Each of these combinations may be placed on a carrier substrate 410, as generally illustrated in FIGS. 4A to 4C, with appropriate leads (e.g., leads 415A, 415B) connected thereto.

[00181] FIGS. 5A to 5C are schematic cross-sectional views of various packaging options 500a, 500b, 500c of the RF transistor amplifier 200, according to some embodiments of the present invention. FIGS. 5A to 5C include elements of the RF transistor amplifier 200, coupling element 270, and circuitry module 310 that have been previously discussed. As such, the discussion of FIGS. 5A to 5C will focus on those portions of the embodiments that are different from those discussed with respect to the prior figures.

[00182] Referring to FIG. 5A, a semiconductor package 500a may incorporate the RF transistor amplifier 200 according to some embodiments of the present invention. The semiconductor package 500a may be, for example, an open-air or open-cavity package. The

semiconductor package 500a may include a carrier substrate 410, sidewalls 520, and a lid 525. The carrier substrate 410, sidewalls 520, and lid 525 may define an internal cavity 530. The RF transistor amplifier 200 and circuitry module 310 may be disposed inside the internal cavity 530. The term "semiconductor package" is not intended to be limiting. As previously noted, the combination of the RF transistor amplifier 200, the circuitry module 310, the leads 415A, 415B, and the carrier substrate 410 may be referred to as a packaged RF transistor amplifier, a semiconductor package, or simply an RF transistor amplifier.

[00183] The carrier substrate 410 may include materials configured to assist with the thermal management of the semiconductor package 500a. For example, the carrier substrate 410 may include copper and/or molybdenum. In some embodiments, the carrier substrate 410 may be composed of multiple layers and/or contain vias/interconnections. In an example embodiment, the carrier substrate 410 may be a multilayer copper/molybdenum/copper metal flange that comprises a core molybdenum layer with copper cladding layers on either major surface thereof. The provided examples of the materials of the carrier substrate 410 are not intended to limit the present invention. In some embodiments, a thermal layer 240 may be between the RF transistor amplifier 200 and the carrier substrate 410.

[00184] The sidewalls 520 and/or lid 525 may be formed of or include an insulating material in some embodiments. For example, the sidewalls 520 and/or lid 525 may be formed of or include ceramic and/or a PCB. In some embodiments, the sidewalls 520 and/or lid 525 may be formed of, for example, Al_2O_3. The lid 525 may be glued to the sidewalls 520 using an epoxy glue. The sidewalls 520 may be attached to the carrier substrate 410 via, for example, brazing. The leads 415A, 415B may be configured to extend through the sidewalls 520, though the present invention is not limited thereto.

[00185] In some embodiments, the RF transistor amplifier 200 may be disposed on the carrier substrate 410 and the leads 415A, 415B, and the circuitry module 310 may be disposed on the RF transistor amplifier 200. The leads 415A, 415B may be coupled to the circuitry module 310 using, for example, a conductive die attach material. In some embodiments, the leads 415A, 415B may extend from the sidewalls 520 to contact the circuitry module 310. As such, in some embodiments, the use of wire bonds to connect the RF transistor amplifier 200 to leads 415A, 415B may be avoided and/or reduced.

[00186] Additional circuit elements 350 are mounted on the circuitry module 310. These additional components may include, for example, input matching components and output matching components that are used to impedance match at the fundamental frequency and/or to terminate intermodulation products to ground. These circuit elements 350 may be passive

RF components that include resistors, capacitors and/or inductors that are implemented (at least partially) in integrated passive devices or printed circuit boards, for example. Leads 415A, 415B allow the RF transistor amplifier 200 to be connected to external devices/circuits/power sources. In the depicted embodiment, circuitry module 310 is used to connect the conductive leads 415A, 415B to circuit elements 350 on the circuitry module 310. An RF signal input to the RF transistor amplifier 200 on a first lead 415A may be passed through the circuitry module 310 to circuit elements 350 and from there to a gate terminal 222 of the RF transistor amplifier die 210, and the amplified output RF signal may be passed from the drain terminal 224 of the RF transistor amplifier die 210 to the circuit elements 350 and from there through the circuitry module 310 where the RF signal is output through lead 415B.

[00187] Referring to FIG. 5B, a semiconductor package 500b may incorporate the RF transistor amplifier 200 according to embodiments of the present invention. The semiconductor package 500b may be, for example, an overmolded plastic (OMP) package. The semiconductor package 500b may include a carrier substrate 410 upon which the RF transistor amplifier 200 is disposed. The circuitry module 310 may be disposed on the RF transistor amplifier 200.

[00188] The RF transistor amplifier 200 and the circuitry module 310 may be encased in an overmold material 540. The overmold material 540 may be formed of a plastic or a plastic polymer compound, which is injection molded around RF transistor amplifier 200 and/or the circuitry module 310, thereby providing protection from the outside environment.

[00189] Methods of manufacturing an OMP semiconductor package 500b that may be modified to incorporate the RF transistor amplifier 200 and/or the circuitry module 310 are described in U.S. Patent No. 9,515,011 entitled "Over-mold plastic packaged wide band-gap power transistors and MMICS," to Wood et al., issued Dec. 6, 2016, the disclosure of which is incorporated herein by reference as if set forth fully herein. In the semiconductor package 500b according to the present invention, leads 415A, 415B may extend from outside the semiconductor package 500b and into the overmold material 540 so as to connect to the circuitry module 310. As such, in some embodiments, the use of wire bonds to connect the RF transistor amplifier 200 to leads 415A, 415B may be avoided and/or reduced.

[00190] As in semiconductor package 500a, the carrier substrate 410 of semiconductor package 500b may include materials configured to assist with thermal management. For example, the carrier substrate 410 may include copper and/or molybdenum. In some embodiments, the carrier substrate 410 may be composed of multiple layers and/or contain

vias/interconnections. In some embodiments, the carrier substrate 410 may include a metal heat sink that is part of a lead frame or metal slug that is at least partially surrounded by a plastic overmold 540. The provided examples of the materials of the carrier substrate 410 are not intended to limit the present invention. In some embodiments, a thermal layer 240 may be between the RF transistor amplifier 200 and the carrier substrate 410.

[00191] FIG. 5C is a schematic cross-sectional view of a packaged RF transistor amplifier 500c that includes an RF transistor amplifier die in a printed circuit board based package. The packaged RF transistor amplifier 500c is very similar to the packaged RF transistor amplifier 500a discussed above with reference to FIG. 5A except that the leads 415A, 415B of packaged RF transistor amplifier 500c are replaced with a printed circuit board 522 that includes traces 415A, 415B that act as the input and output leads. The printed circuit board 522 may be attached to the carrier substrate 410 via, for example, a conductive glue. The carrier substrate 410 may include, for example, pedestals 410P. The pedestals 410P may be constructed of an insulating material and/or a metal. The printed circuit board 652 may include a central opening and the circuitry module 310 is mounted within this opening on the carrier substrate (e.g., metal flange) 410. The RF transistor amplifier 200 and the circuit elements 350 are mounted on the circuitry module 310.

[00192] Though FIGS. 5A to 5C illustrate the use of an RF transistor amplifier 200 having a coupling element 270, the present invention is not limited thereto. In some embodiments, the semiconductor packages 500a, 500b, 500c may be configured to include a circuitry module 310 that is directly coupled to the RF transistor amplifier die 210 as illustrated within FIGS. 3B, 3C, and 4B. In some embodiments, the semiconductor packages 500a, 550b, and 500c may be configured to include a circuitry module 310 that is coupled to a plurality of RF transistor amplifiers 200, 200' and/or a plurality of RF transistor amplifier dies 210, 210 as illustrated in FIGS. 3D, 3E, and 4C.

[00193] It will be appreciated that any of the RF transistor amplifiers according to embodiments of the present invention that are discussed herein may be mounted in packages such as the packages shown in FIGS. 5A through 5C. Thus, the RF transistor amplifier die 210, coupling element 270, and/or circuitry modules 310 shown in FIGS. 5A-5C, may be replaced with the RF transistor amplifier die 210,210', coupling element 270, and/or circuitry modules 310, 310' according to any of the embodiments of the present invention that are discussed herein to provide many further embodiments of packaged RF transistor amplifiers. Depending on the embodiment, the packaged RF transistor amplifier can include a monolithic microwave integrated circuit (MMIC) as the RF transistor amplifier die where

the RF transistor amplifier die incorporates multiple discrete circuits in a single integrated die. Additionally and/or alternatively, the package can comprise multiple RF transistor amplifier die in a path that are connected in series to form a multiple stage RF transistor amplifier and/or multiple RF transistor amplifier die that are disposed in multiple paths (e.g., in parallel) to form an RF transistor amplifier with multiple transistor amplifier die and multiple paths, such as in a Doherty amplifier configuration. In some embodiments, the packaged RF transistor amplifier may include RF transistor amplifier die according to embodiments of the present invention that have conductive gate and/or conductive drain vias that provide electrical connections to a back side interconnection structure as well as traditional RF transistor amplifier die that have gate and drain terminals that are connected to other structures via wire bonds.

[00194] Though in some embodiments described herein, circuit elements 350 may be placed on a top surface of the circuitry module 310, the embodiments described herein are not limited thereto. FIGS. 6A to 6C are schematic cross-sectional views of additional embodiments of an RF transistor amplifier 200 coupled to a circuitry module 610, according to some embodiments of the present invention. FIGS. 6A to 6C correspond to the cross-section of FIG. 3A. FIGS. 6A to 6C include elements of the RF transistor amplifier 200 that have been previously discussed. As such, the discussion of FIGS. 6A to 6C will focus on those portions of the embodiments that are different from those discussed with respect to the prior figures.

[00195] Referring to FIG. 6A, the circuitry module 610 may be configured to couple to the gate connection pad 272, the drain connection pad 274, and the source connection pad 276 of the coupling element 270. The coupling element 270 may be coupled to RF transistor amplifier die 210, as discussed herein with respect to, for example, FIGS. 2A to 2L.

[00196] For example, the circuitry module 610 may have exposed interconnection pads 622, 624, 626 that may be configured to be coupled to the gate connection pad 272, the drain connection pad 274, and the source connection pad 276, respectively. In some embodiments, a bonding element (e.g., solder balls and/or bumps 320) may be used to respectively couple the first, second, and third interconnection pads 622, 624, 626 to the gate connection pad 272, the drain connection pad 274, and the source connection pad 276. Though illustrated as a single pad, in some embodiments, one or more of the first, second, and/or third interconnection pads 622, 624, 626 may include a plurality of pads.

[00197] The circuitry module 610 may be coupled to the coupling element 270 on a first side 601 of the circuitry module 610. On a second side 602 of the circuitry module 610 that is

opposite the first side 601, a plurality of pads may be exposed. For example, a gate lead 682, a drain lead 684, and a source lead 686 may be exposed on the second side 602 of the circuitry module 610. Though only a single gate lead 682, drain lead 684, and source lead 686 are illustrated in FIG. 6A, it will be understood that a plurality of each type of lead may be provided. As will be discussed further herein, the gate lead 682, the drain lead 684, and the source lead 686 may be configured to be respectively coupled to the gate terminal 222, the drain terminal 224, and the source terminal 226 of the RF transistor amplifier die 210. An encapsulating material 625 may be on surfaces of the RF transistor amplifier die 210, the coupling element 270, and/or the circuitry module 610. The encapsulating material 625 may be formed of a plastic or a plastic polymer compound, but the present invention is not limited thereto. In some embodiments, the encapsulating material 625 may be or include a polymer with fillers.

[00198] Each of the first, second, and third interconnection pads 622, 624, 626 may be coupled to one or more conductive patterns 673 within the circuitry module 610. The conductive patterns 673 may provide various routing and/or circuitry within the circuitry module 610. For example, the conductive patterns 673 may connect the first interconnection pad 622 to one or more first surface connection pads 672 and the gate lead 682. In some embodiments, the first surface connection pads 672 may be exposed on the first side 601 of the circuitry module 610. In some embodiments, a first circuit element 650a may be coupled to one or more of the first surface connection pads 672 so as to be electrically coupled between the gate lead 682 and the first interconnection pad 622. In some embodiments, the first circuit element 650a may be coupled between the gate lead 682 and the gate terminal 222 of the RF transistor amplifier die 210 (e.g., through the coupling element 270). Consequently, the first circuit element 650a may be electrically coupled between gates of the RF transistor amplifier die 210 and the gate lead 682. In some embodiments, the first circuit element 650a may be coupled to the first side 601 of the circuitry module 610. Thus, the first circuit element 650a may be coupled to a same side (e.g., the first side 601) of the circuitry module 610 as the coupling element 270.

[00199] Similarly, the conductive patterns 673 may connect the second interconnection pad 624 to one or more second surface connection pads 674 and the drain lead 684. In some embodiments, a second circuit element 650b may be coupled to one or more of the second surface connection pads 674 so as to be electrically coupled between the drain lead 684 and the second interconnection pad 624. In some embodiments, the second surface connection pads 674 may be exposed on the first side 601 of the circuitry module 610. In some

embodiments, the second circuit element 650b may be coupled between the drain lead 684 and the drain terminal 224 of the RF transistor amplifier die 210 (e.g., through the coupling element 270). Consequently, the second circuit element 650b may be electrically coupled between drains of the RF transistor amplifier die 210 and the drain lead 684.

[00200] The first circuit element 650a and/or the second circuit element 650b may provide various electronic capabilities to the RF transistor amplifier 200. For example, the first circuit element 650a and/or the second circuit element 650b may comprise impedances (including, for example, resistive, inductive, and capacitive elements) that may be used for impedance matching and/or harmonic termination. In some embodiments, the first circuit element 650a and/or the second circuit element 650b may be or include surface mount devices. In some embodiments, the first circuit element 650a and/or the second circuit element 650b may be or include integrated passive devices (IPDs). In some embodiments, the first circuit element 650a and/or the second circuit element 650b may be or include harmonic and/or input/output impedance matching elements.

[00201] For example, the first circuit element 650a may be configured to provide input matching capabilities. Due to its location between the gate lead 682 and the RF transistor amplifier die 210, the first circuit element 650a may be capable of affecting and/or conditioning a signal provided to the gates of the RF transistor amplifier die 210. Similarly, the second circuit element 650b may be configured to provide output matching capabilities. Due to its location between the drain lead 684 and the RF transistor amplifier die 210, the second circuit element 650b may be capable of affecting and/or conditioning a signal provided from the drains of the RF transistor amplifier die 210.

[00202] By using the circuitry module 610 with the exposed connection pads, such as the first and second surface connection pads 672, 674, surface mount devices can be used to provide circuit elements that may be coupled to the RF transistor amplifier die 210. The surface mount devices can be replaced and/or configured as necessary to provide a more flexible solution. For example, when a different type of input/output matching and/or harmonic termination is needed, the same circuitry module 610 may be used, but the first and/or second circuit elements 650a, 650b may be swapped to provide different capabilities.

[00203] Though the first circuit element 650a and the second circuit element 650b are each illustrated as a single element, it will be understood that in some embodiments, the first circuit element 650a and/or the second circuit element 650b may include a plurality of discrete devices. Similarly, the interconnections between the first and second circuit elements 650a, 650b and the RF transistor amplifier die 210 are merely examples, and

different configurations of conductive patterns 673 may be provided without deviation from the present invention.

[00204] The conductive patterns 673 may also connect the third interconnection pad 626 to one or more source leads 686. Thus, the source connection pad 276 may be electrically coupled to the one or more source leads 686.

[00205] The conductive patterns 673 may be encased in an isolation material 615. In some embodiments, the isolation material 615 may include, for example, silicon oxide, silicon nitride, an oxide of the conductive patterns 673, a polymer, a molding compound, or a combination thereof. In some embodiments, circuitry module 610 may be formed as a printed circuit board (PCB). In a PCB embodiment, the isolation material 615 may be the substrate(s) of the PCB, and the conductive patterns 673 may be traces formed within the substrate(s).

[00206] Though FIG. 6A illustrates the use of a circuitry module 610 to couple to a RF transistor amplifier die 210 using a coupling element 270, the present invention is not limited thereto. As illustrated in FIG. 6B, in some embodiments, the RF transistor amplifier die 210 may be directly coupled to the circuitry module 610. For example, the gate terminal 222, drain terminal 224, and source terminal 226 of the RF transistor amplifier die 210 may be respectively coupled to the interconnection pads 622, 624, 626 of the circuitry module 610 using, for example, bonding elements 320.

[00207] Similarly, it will be understood that other configurations of the circuitry module 610 and the RF transistor amplifier die 210 are possible, such as those illustrated in FIGS. 3C to 3E. In some embodiments, the circuitry module 610 may be configured to couple to an RF transistor amplifier die 210' incorporating internal conductive patterns, such as that illustrated in FIG. 3C. In some embodiments, the circuitry module 610 may be configured to couple to multiple RF transistor amplifier dies 210, such as that illustrated in FIGS. 3D and 3E.

[00208] It will also be appreciated that the RF transistor amplifier die 210 may have a variety of different configurations. For example, while the RF transistor amplifier dies 210 have top side gate, drain and source terminals 222, 224, 226, they may also, in some embodiments, have one or more of back side gate, drain and source terminals 222', 224', 226'. Such a configuration is schematically shown in FIG. 6C, which is a schematic cross-sectional view of an RF transistor amplifier die 210". As shown in FIG. 6C, gate vias 211, drain vias 213 and/or source vias 215 may be formed through the semiconductor layer structure 230 that connect to respective gate, drain and source terminals 222', 224', 226'. As explained, for example, in U.S. Provisional Patent Application Serial No. 63/004,985, filed April 3, 2020

("the '985 application"), including gate and drain terminals on the back side of an RF transistor amplifier die may have various advantages, such as allowing for more flexible impedance matching circuit implementations. The entire content of the '985 application is incorporated herein by reference. It will be appreciated that back side gate, drain and source terminals 222', 224', 226' and/or corresponding gate, drain and source vias 211, 213, 215 may be included in any of the RF transistor amplifier dies disclosed herein.

[00209] While FIGS. 3A to 3E illustrate embodiments in which a circuit element 350 is on a top surface of the circuitry module 310 (e.g., opposite the circuitry module 310 from the RF transistor amplifier die 210) and FIGS. 6A to 6C illustrate embodiments in which a circuit element 650 is on a bottom surface of the circuitry module 610 (e.g., between the circuitry module 610 and the RF transistor amplifier die 210), it will be understood that other combinations are available. In some embodiments, the circuit elements 350/650 may be on both sides of the circuitry module 310/610. In some embodiments, the circuit elements 350/650 may be on side surfaces of the circuitry module 310/610.

[00210] As illustrated in FIGS. 6A-6C, multiple configurations of RF transistor amplifier die 210 and/or RF transistor amplifier 200 may be coupled to a circuitry module 610. In the subsequent figures, discussion will focus on embodiments in which the RF transistor amplifier die 210 is directly coupled to circuitry module 610. However, it will be understood that this convention is merely for ease of description and the subsequent discussion related to the circuitry module 610 may be equally applied to other types of interconnections between the RF transistor amplifier 210 (e.g., using a coupling element 270) and/or RF transistor amplifier 200 without deviating from the present invention.

[00211] FIGS. 7A to 7E are schematic diagrams illustrating methods of coupling circuitry modules and RF transistor amplifier dies according to certain embodiments of the present invention. As shown in FIG. 7A, a circuitry module 610 may be provided. The circuitry module 610 may have a first side 601 and a second side 602. In some embodiments, the first side 601 may expose first, second, and third interconnection pads 622, 624, 626 as well as a first and second surface connection pads 672, 674. In some embodiments, the second side 602 may have an exposed gate lead 682, drain lead 684, and source lead 686.

[00212] Referring to FIG. 7B, a first circuit element 650a and a second circuit element 650b may be provided on the first side 601 of the circuitry module 610. For example, a bonding element (e.g., solder balls and/or bumps 320) may be used to couple the first circuit element 650a to the first surface connection pad 672. Similarly, a bonding element (e.g., solder balls

and/or bumps 320) may be used to couple the second circuit element 650b to the second surface connection pad 674.

[00213] Referring to FIG. 7C, an RF transistor amplifier die 210 may be provided on the first side 601 of the circuitry module 610. For example, a bonding element (e.g., solder balls and/or bumps 320) may be used to couple the gate terminal 222, the drain terminal 224, and the source terminal 226 of the RF transistor amplifier die 210 to the first, second, and third interconnection pads 622, 624, 626, respectively. In will be understood that the order of FIGS. 7B and 7C may be reversed such that the RF transistor amplifier die 210 is coupled to the circuitry module 610 before the first and second circuit elements 650a, 650b.

[00214] As shown in FIG. 7D, a capillary underfill process may be used to inject encapsulating material 625 between the conductive structures of the RF transistor amplifier die 210, the first and second circuit elements 650a, 650b, and/or the circuitry module 610. The encapsulating material 625 may help prevent short circuits, enhance the structural integrity of the resulting device, and provide for proper impedance matching. In some embodiments, the encapsulating material 625 may also encapsulate the RF transistor amplifier die 210 in protective material.

[00215] FIG. 7E illustrates an additional optional step in which a thermal layer 240 is placed on the back side of the RF transistor amplifier die 210. In some embodiments, additional thermal management structures 642, such as a metal flange, metal fin, heatsink, or other structure may be provided on the thermal layer 240. In some embodiments, the thermal management structures 642 may be part of a larger semiconductor package (e.g., a carrier substrate), as will be discussed further herein. The thermal layer 240 may be a thermally conductive layer configured to facilitate thermal transfer between the RF transistor amplifier die 210 and the thermal management structure 642 to which the RF transistor amplifier die 210 is mounted. In some embodiments, the thermal layer 240 and/or the thermal management structures 642 may be omitted. In some embodiments, the thermal layer 240 may be a die attach layer, such as a eutectic layer. The thermal layer 240 can be on the transistor amplifier die 210 and/or extend onto the encapsulating material 625 and/or the first and second circuit elements 650a, 650b. The thermal layer 240 can be a metal layer to form a eutective or other metal bond. In some embodiments, the thermal layer 240 can be a thermal adhesive.

[00216] The embodiments of FIGS. 6A to 6C provide a common gate lead 682, drain lead 684, and source lead 686 on a common side (e.g., second side 602) of the circuitry module 610. This may allow for the circuitry module 610 to be attached with the second side 602 up

in variety of different configurations. For example, FIGS. 8A and 8B are schematic cross-sectional views of various packaging options 800a, 800b of the circuitry module 610, according to some embodiments of the present invention. FIGS. 8A and 8B include elements of the RF transistor amplifier die 210 and circuitry module 610 that have been previously discussed. As such, the discussion of FIGS. 8A and 8B will focus on those portions of the embodiments that are different from those discussed with respect to the prior figures.

[00217] Referring to FIG. 8A, a semiconductor package 800a may be similar to the semiconductor package 500a discussed herein with respect to FIG. 5A, and duplicate descriptions already discussed with respect to that figure will be omitted. The semiconductor package 800a may be, for example, an open-air or open-cavity package. The semiconductor package 800a may include a carrier substrate 410, sidewalls 520, and a lid 525. The carrier substrate 410, sidewalls 520, and lid 525 may define an internal cavity 530. The RF transistor amplifier die 210 and circuitry module 610 may be disposed inside the internal cavity 530. In some embodiments, a thermal layer 240 may be between the RF transistor amplifier die 210 and the carrier substrate 410.

[00218] The leads 415A, 415B may be configured to extend through the sidewalls 520, though the present invention is not limited thereto. In some embodiments, the RF transistor amplifier 210 may be disposed on the carrier substrate 410 and the leads 415A, 415B, and the circuitry module 610 may be disposed on the RF transistor amplifier die 210. The leads 415A, 415B may be coupled to the circuitry module 610 using, for example, a conductive die attach material. In some embodiments, the leads 415A, 415B may extend from the sidewalls 520 to contact and/or be connected to the circuitry module 610. For example, the lead 415a may be coupled to gate lead 682 and lead 415b may be coupled to drain lead 684. In some embodiments, an additional lead and/or connection (not shown) may be coupled to source lead 686. As such, in some embodiments, the use of wire bonds to connect the RF transistor amplifier die 210 to leads 415A, 415B may be avoided and/or reduced.

[00219] Referring to FIG. 8B, a semiconductor package 800b may incorporate the RF transistor amplifier 210 and circuitry module 610 according to embodiments of the present invention. The semiconductor package 800b may be similar to the semiconductor package 500b discussed herein with respect to FIG. 5B, and duplicate descriptions already discussed with respect to that figure will be omitted. The semiconductor package 800b may be, for example, an overmolded plastic (OMP) package.

[00220] In the semiconductor package 800b according to the present invention, leads 415A, 415B may extend from outside the semiconductor package 800b and into the overmold

material 540 so as to connect to the circuitry module 610. For example, the lead 415a may be coupled to gate lead 682 and lead 415b may be coupled to drain lead 684. In some embodiments, and additional lead and/or connection (not shown) may be coupled to source lead 686. In some embodiments, a thermal layer 240 may be between the RF transistor amplifier die 210 and a carrier substrate 410 within the semiconductor package 800b.

[00221] In addition to semiconductor packages 800a, 800b illustrated with respect to FIGS. 8A and 8B, it will be understood that other packaging configurations are possible without deviating from the present invention. For example, the circuitry module 610 may be utilized with semiconductor packages similar to those of FIG. 5C, as well as other configurations.

[00222] In FIGS. 6A to 6C, the circuit elements 650a, 650b and RF transistor amplifier die 210 are on the same side of the circuitry module 610, while the gate, drain, and source leads 682, 684, 686 are on an opposite side, but the present embodiments are not limited thereto. FIG. 9A is a plan view of an embodiment of a circuitry module 610B, according to some embodiments of the present invention, in which the leads 682, 684, 686, circuit elements 650a, 650b, and RF transistor amplifier die 210 are all on a same side of the circuitry module 610B. FIG. 9B is a cross-sectional view taken along line 9B—9B of FIG. 9A. FIG. 9C is a cross-sectional view taken along line 9C—9C of FIG. 9A. FIGS. 9A to 9C include elements of the RF transistor amplifier die 210 and circuitry module 610 that have been previously discussed. As such, the discussion of FIGS. 9A to 9C will focus on those portions of the embodiments that are different from those discussed with respect to the prior figures.

[00223] Referring to FIGS. 9A to 9C, the circuitry module 610B may be mounted on the RF transistor amplifier die 210. The RF transistor amplifier die 210 is mounted below the circuitry module 610B in the schematic plan view of FIG. 9A, and hence is shown using dashed lines. The circuitry module 610B may be configured to couple to the gate terminal 222, the drain terminal 224, and/or the source terminal 226 of the RF transistor amplifier die 210. Though FIGS. 9A to 9C illustrate that the circuitry module 610B is coupled directly to the RF transistor amplifier die 210, it will be understood that other connection types are possible, such as other configurations of RF transistor amplifier 200, including those illustrated with respect to FIGS. 2A to 2L. For example, a coupling element 270 may be coupled between the circuitry module 610B and the RF transistor amplifier die 210.

[00224] For example, the circuitry module 610B may have exposed interconnection pads 622, 624, 626 that may be configured to be respectively coupled to the gate terminal 222, the drain terminal 224, and the source terminal 226 of the RF transistor amplifier die 210. For example, the first interconnection pad 622 may be configured to couple to the gate terminal

222, the second interconnection pad 624 may be configured to couple to the drain terminal 224, and the third interconnection pad 626 may be configured to couple to the source terminal 226. In some embodiments, a bonding element (e.g., solder balls and/or bumps 320) may be used to respectively couple the first, second, and third interconnection pads 622, 624, 626 to the gate terminal 222, the drain terminal 224, and the source terminal 226, respectively. Though illustrated as a single pad, in some embodiments, one or more of the first, second, and/or third interconnection pads 622, 624, 626 may include a plurality of pads.

[00225] The circuitry module 610B may be coupled to the RF transistor amplifier die 210 on a first side 601 of the circuitry module 610B. In addition, a gate lead 682B, a drain lead 684B, and a source lead 686B may be exposed on the first side 601 of the circuitry module 610B. As will be discussed further herein, the gate lead 682B, the drain lead 684B, and the source lead 686B may be configured to be respectively coupled to the gate terminal 222, the drain terminal 224, and the source terminal 226 of the RF transistor amplifier die 210. An encapsulating material 625 may be on surfaces of the RF transistor amplifier die 201, and/or the circuitry module 610B.

[00226] Each of the first, second, and third interconnection pads 622, 624, 626 may be coupled to one or more conductive patterns 673B within the circuitry module 610B. The conductive patterns 673B may provide various routing and/or circuitry within the circuitry module 610B. For example, the conductive patterns 673B may connect the first interconnection pad 622 to one or more first surface connection pads 672 and the gate lead 682B. In some embodiments, the first surface connection pads 672 may be exposed on the first side 601 of the circuitry module 610B. In some embodiments, a first circuit element 650a may be coupled to one or more of the first surface connection pads 672 so as to be electrically coupled between the gate lead 682B and the first interconnection pad 622. In some embodiments, the first circuit element 650a may be coupled between the gate lead 682B and the gate terminal 222 of the RF transistor amplifier die 210. Consequently, the first circuit element 650a may be electrically coupled between gates of the RF transistor amplifier die 210 and the gate lead 682B. In some embodiments, the first circuit element 650a may be coupled to the first side 601 of the circuitry module 610B. Thus, the first circuit element 650a may be coupled to a same side (e.g., the first side 601) of the circuitry module 610B as the RF transistor amplifier die 210 and the gate lead 682B.

[00227] Similarly, the conductive patterns 673B may connect the second interconnection pad 624 to the drain terminal 224 and the drain lead 684B. In some embodiments, a second circuit element 650b may be coupled to one or more of the second surface connection pads

674 so as to be electrically coupled between the drain lead 684B and the second interconnection pad 624. In some embodiments, the second surface connection pads 674 may be exposed on the first side 601 of the circuitry module 610B. In some embodiments, the second circuit element 650b may be coupled between the drain lead 684B and the drain terminal 224 of the RF transistor amplifier die 210. Consequently, the second circuit element 650b may be electrically coupled between drains of the RF transistor amplifier die 210 and the drain lead 684B.

[00228] The conductive patterns 673B may also connect the third interconnection pad 626 to one or more source leads 686B. The source leads 686B may be on the same first side 601 as the third interconnection pad 626 and the RF transistor amplifier die 210. In some embodiments, as illustrated in FIG. 9A, the gate lead 682B and the drain lead 684B may be on two opposite sides of the RF transistor amplifier die 210 and the source leads 686B may be on different sides of the RF transistor amplifier die 210 than the two opposite sides. Stated another way, in some embodiments, the gate lead 682B may be adjacent a first side of the RF transistor amplifier die 210, the drain lead 684B may be adjacent a second side of the RF transistor amplifier die 210, and one or more of the source leads 686B may be adjacent a third side of the RF transistor amplifier die 210 that is different from the first and second sides of the RF transistor amplifier die 210.

[00229] The circuitry module 610B of FIGS. 9A to 9C may differ from the circuitry module 610 of FIGS. 6A to 6C in that the circuitry module 610B provides the gate, drain, and source leads 682B, 684B, 686B on a same side of the circuitry module 610B as the RF transistor amplifier die 210. That is to say that the conductive patterns 673 of the circuitry module 610B may be configured to allow the gate, drain, and source leads 682B, 684B, 686B to be exposed on a different portion of the circuitry module 610B. By shifting the side at which the gate, drain, and source leads 682B, 684B, 686B are located, additional packaging options are possible.

[00230] FIG. 9D is a cross-sectional view of the circuitry module 610B of FIG. 9A, mounted on a carrier substrate 410 according to some embodiments of the present invention. As illustrated in FIG. 9D, the circuitry module 610B may be coupled on the RF transistor amplifier die 210, which may be, in turn, on the carrier substrate 410.

[00231] In some embodiments, a thermal layer 240 may be between the RF transistor amplifier die 210 and the carrier substrate 410. In some embodiments, an additional thermal management structure 642, such as a metal flange, metal fin, heatsink, or other structure may be provided on the thermal layer 240 and/or between the thermal layer 240 and the carrier

substrate 410. The thermal layer 240 may be a thermally conductive layer configured to facilitate thermal transfer between the RF transistor amplifier die 210 and a carrier substrate 410 to which the RF transistor amplifier die 210 is mounted. In some embodiments, the thermal layer 240 and/or the thermal management structure 642 may be omitted. In some embodiments, the thermal layer 240 may be a die attach layer, such as a eutectic layer. The thermal layer 240 can be on the RF transistor amplifier die 210 and/or extend onto the encapsulating material 625 and/or the first and second circuit elements 650a, 650b. The thermal layer 240 can be a metal layer to form a eutective or other metal bond. In some embodiments, the thermal layer 240 can be a thermal adhesive.

[00232] In some embodiments additional contacts may be provided in the carrier substrate 410, though the present invention is not limited thereto. For example, a gate connector 982, a drain connector 984, and/or a source connector (not shown) may be provided on and/or in the carrier substrate 410. For example, the gate lead 682B of the circuitry module 610B may be configured to be coupled (e.g., via a bonding element such as solder balls and/or bumps 320) to the gate connector 982, the drain lead 684B may be configured to be coupled to the drain connector 984, and the source lead 686B may be configured to be coupled to a source connector (not shown).

[00233] It will be understood that the packaging example of FIG. 9B is merely an example, and the present invention is not limited thereto. In some embodiments, the circuitry module 610B of FIGS. 9A to 9C can be coupled within other semiconductor packages described herein, such as those discussed with respect to FIGS. 5A to 5C and FIGS. 8A and 8B. For example, FIGS. 10A and 10B are schematic cross-sectional views of various packaging options 1000a, 1000b of the circuitry module 610B, according to some embodiments of the present invention. FIGS. 10A and 10B include elements of the RF transistor amplifier die 210 and circuitry module 610B that have been previously discussed. As such, the discussion of FIGS. 10A and 10B will focus on those portions of the embodiments that are different from those discussed with respect to the prior figures.

[00234] Referring to FIG. 10A, a semiconductor package 1000a may be similar to the semiconductor packages 500a and 800a discussed herein with respect to FIGS. 5A and 8A, respectively, and duplicate descriptions already discussed with respect to those figures will be omitted. The semiconductor package 1000a may be, for example, an open-air or open-cavity package. The semiconductor package 1000a may include a carrier substrate 410, sidewalls 520, and a lid 525. The carrier substrate 410, sidewalls 520, and lid 525 may define an internal cavity 530. The RF transistor amplifier die 210 and circuitry module 610B may be

disposed inside the internal cavity 530. In some embodiments, a thermal layer 240 may be between the RF transistor amplifier die 210 and the carrier substrate 410.

[00235] The leads 415A, 415B may be configured to extend through the sidewalls 520, though the present invention is not limited thereto. In some embodiments, the RF transistor amplifier 210 may be disposed on the carrier substrate 410 and the leads 415A, 415B, and the circuitry module 610B may be disposed on the RF transistor amplifier die 210. The leads 415A, 415B may be coupled to the circuitry module 610B using, for example, a conductive die attach material. For example, the lead 415a may be coupled to gate lead 682B and lead 415b may be coupled to drain lead 684B. In some embodiments, an additional lead and/or connection (not shown) may be coupled to source lead 686B. As such, in some embodiments, the use of wire bonds to connect the RF transistor amplifier die 210 to leads 415A, 415B may be avoided and/or reduced.

[00236] Referring to FIG. 10B, a semiconductor package 1000b may incorporate the RF transistor amplifier 210 and circuitry module 610B according to embodiments of the present invention. The semiconductor package 1000b may be similar to the semiconductor package 500b and 800b discussed herein with respect to FIGS. 5B and 8B, and duplicate descriptions already discussed with respect to that figure will be omitted. The semiconductor package 1000b may be, for example, an overmolded plastic (OMP) package.

[00237] In the semiconductor package 1000b according to the present invention, leads 415A, 415B may extend from outside the semiconductor package 800b and into the overmold material 540 so as to connect to the circuitry module 610B. For example, the lead 415a may be coupled to gate lead 682B and lead 415b may be coupled to drain lead 684B. In some embodiments, an additional lead and/or connection (not shown) may be coupled to source lead 686B.

[00238] In addition to semiconductor packages 1000a, 1000b illustrated with respect to FIGS. 10A and 10B, it will be understood that other packaging configurations are possible without deviating from the present invention. For example, the circuitry module 610B may be utilized with semiconductor packages similar to those of FIG. 5C, as well as other configurations.

[00239] As discussed herein, circuitry modules may include circuit elements on surfaces of the circuitry modules, but may also include circuit elements within the circuitry module itself. FIGS. 11A to 11D are schematic cross-sectional views of additional embodiments of an RF transistor amplifier die 210 coupled to a circuitry module 610C, according to some embodiments of the present invention. FIGS. 11A to 11D include elements of the RF

transistor amplifier die 210 and circuitry module 610C that have been previously discussed. As such, the discussion of FIGS. 11A to 11D will focus on those portions of the embodiments that are different from those discussed with respect to the prior figures.

[00240] Referring to FIG. 11A, the circuitry module 610C may be mounted on the RF transistor amplifier die 210. The circuitry module 610C may be configured to couple to the gate terminal 222, the drain terminal 224, and the source terminal 226 of the RF transistor amplifier die 210. Though FIG. 11A illustrates that the circuitry module 610C is coupled directly to the RF transistor amplifier die 210, it will be understood that other connection types are possible, such as other configurations of RF transistor amplifier 200, including those illustrated with respect to FIGS. 2A to 2L. For example, a coupling element 270 may be coupled between the circuitry module 610C and the RF transistor amplifier die 210.

[00241] The circuitry module 610C may have exposed interconnection pads 622, 624, 626 that may be configured to be respectively coupled to the gate terminal 222, the drain terminal 224, and the source terminal 226. In some embodiments, a bonding element (e.g., solder balls and/or bumps 320) may be used to respectively couple the first, second, and third interconnection pads 622, 624, 626 to the gate terminal 222, the drain terminal 224, and the source terminal 226. Though illustrated as a single pad, in some embodiments, one or more of the first, second, and/or third interconnection pads 622, 624, 626 may include a plurality of pads.

[00242] The circuitry module 610C may be coupled to the RF transistor amplifier die on a first side 601 of the circuitry module 610C. In addition, a gate lead 682C, a drain lead 684C, and/or a source lead (not shown) may be exposed on the first side 601 of the circuitry module 610C. The gate lead 682C, the drain lead 684C, and/or the source lead may be configured to be respectively coupled to the gate terminal 222, the drain terminal 224, and the source terminal 226 of the RF transistor amplifier die 210.

[00243] The circuitry module 610C may contain one or more conductive patterns 1173, a first circuit element 1150a, and a second circuit element 1150b. The first and second circuit elements 1150a and 1150b are illustrated schematically in FIG. 11A. The circuitry module 610C may differ from that of circuitry modules 610, 610B described herein in that first and second circuit elements 1150a and 1150b may be incorporated within the structure of the circuitry module 610C. For example, plate capacitors, interdigitated finger capacitors and/or capacitors may be implemented using the conductive patterns 1173 within the circuitry module 610C. Likewise spiral inductors or other inductive elements may also be implemented within the circuitry module 610C. Resistive elements may be formed on or

within the circuitry module 610C by, for example, forming trace segments or conductive vias using higher resistance conductive materials.

[00244] In some embodiments, the first and second circuit elements 1150a, 1150b and/or the conductive patterns 1173 may be configured to provide at least part of harmonic terminating circuitry, matching circuitry, splitting circuitry, combining circuitry, and/or biasing circuitry. Other configurations of the conductive patterns 1173 and/or other types of circuit elements 1150a, 1150b may be used without deviating from the scope of the present invention. It will also be appreciated that the configuration of the conductive patterns 1173 and circuit elements 1150a, 1150b illustrated in FIG. 11A are merely examples and are not intended to limit embodiments of the present invention.

[00245] In some embodiments, the circuitry module 610C may be formed as a PCB module and the first and second circuit elements 1150a, 1150b may be formed from traces within the PCB. In some embodiments, the circuitry module 610C may be formed of an insulating material 615, and the conductive patterns 1173 may be conductive material within the insulating material 615, such as conductive pillars and/or vias (e.g., copper pillars).

[00246] Each of the first, second, and third interconnection pads 622, 624, 626 may be coupled to one or more of the conductive patterns 1173 within the circuitry module 610C. The conductive patterns 1173 may provide various routing and/or circuitry within the circuitry module 610C. For example, the conductive patterns 1173 may connect the first interconnection pad 622 to the gate lead 682C via the first circuit element 1150a. The first circuit element 1150a may provide input matching and/or harmonic termination functionality between the gate lead 682C and the first interconnection pad 622.

[00247] Similarly, the conductive patterns 1173 may connect the second interconnection pad 624 to the drain lead 684C via the second circuit element 1150b. The second circuit element 1150b may provide output matching and/or harmonic termination functionality between the drain lead 684C and the second interconnection pad 624.

[00248] As illustrated in FIG. 11A, in some embodiments, an encapsulating material 1125 may be formed on the RF transistor amplifier die 210, the circuitry module 610C, the gate lead 682C, and/or the drain lead 684C. The encapsulating material 1125 may help prevent short circuits, enhance the structural integrity of the resulting device, and provide for proper impedance matching. In some embodiments, the encapsulating material 1125 may also encapsulate the RF transistor amplifier die 210 in protective material.

[00249] In some embodiments, through vias 1115 may be formed in the encapsulating material 1125. The through vias 1115 may include conductive material and provide a

conductive path to the gate lead 682C and/or drain lead 684C. For example, the through vias 1115 may expose gate connection 1182 and/or drain connection 1184 on a bottom surface of the encapsulating material 1125. The gate connection 1182 and/or drain connection 1184 may provide connection points for the gate lead 682C and the drain lead 684C, respectively.

[00250] In some embodiments, the gate connection 1182 and the drain connection 1184 may be approximately coplanar. In some embodiments, the encapsulating material 1125 may be configured to expose a bottom surface of the RF transistor amplifier die 210, and the gate connection 1182 and the drain connection 1184 may also be approximately coplanar with the bottom surface of the RF transistor amplifier die 210, though the present invention is not limited thereto. Though only the gate connection 1182 and the drain connection 1184 are illustrated in FIG. 11A, it will be understood that source connections may also be provided in a similar manner.

[00251] The use of the gate connection 1182 and the drain connection 1184 may allow for the use of direct bonding between the combination of the RF transistor amplifier die 210 and the circuitry module 610C and other pads and/or dies. For example, as illustrated in FIG. 11B, the gate connection 1182 may be coupled to a gate pad 1192 (e.g., via a bonding element such a solder) and the drain connection 1184 may be coupled to a gate pad 1194. In some embodiments, a thermal layer 240 may also be provided beneath the RF transistor amplifier die 210, though the present invention is not limited thereto. In some embodiments, the thermal layer 240 may be omitted. In some embodiments, additional contacts may be provided to connect to the third interconnection pad 626 and/or the source terminal 226 of the RF transistor amplifier die 210.

[00252] It will be understood that the packaging example of FIG. 11B is merely an example, and the present invention is not limited thereto. FIGS. 11C and 11D illustrate the use of packaging similar to that discussed herein with respect to FIGS. 5A to 5C, 8A, 8B, 10A, and 10B. For example, the circuitry module 610C, the RF transistor amplifier die 210, and the encapsulating material 1125 including the gate and drain connection 1182, 1184 may be placed in an open-cavity semiconductor package 1100a (FIG. 11C) or an OMP package 1100b (FIG. 11D). Elements in FIGS. 11C and 11D of the semiconductor package 1100a and semiconductor package 1100b that are similar to those previously discussed with respect to FIGS. 5A to 5C, 8A, 8B, 10A, and 10B will be omitted for brevity.

[00253] In some embodiments, the gate connection 1182 may be coupled to gate lead 415A by a bonding element (e.g., solder balls and/or bumps) and the drain connection 1184 may also be coupled to drain lead 415B. The gate lead 415A and the drain lead 415B may be

electrically insulated from the carrier substrate 410 (e.g., by an insulating layer and/or the overmold material 540). In some embodiments, a thermal layer 240 may be between the RF transistor amplifier die 210 and the carrier substrate 410. In some embodiments, the thermal layer 240 may be omitted. In some embodiments, the thermal layer 240 may be a die attach layer, such as a eutectic layer. The thermal layer 240 can be on the transistor amplifier die 210 and/or extend onto the encapsulating material 1125. The thermal layer 240 can be a metal layer to form a eutective or other metal bond. In some embodiments, the thermal layer 240 can be a thermal adhesive. Though not shown in FIGS. 11C and 11D, in some embodiments additional thermal management structures such as those illustrated in FIGS. 7E and 9D may be used.

[00254] The packaging embodiments illustrated in FIGS. 11C and 11D are merely examples meant to illustrate how the circuitry module 610C and the RF transistor amplifier die 210 may be coupled within a semiconductor package. It will be understood that multiple other possible configurations and/or orientations of the semiconductor package are possible without deviating from the present invention.

[00255] In some embodiments, the through vias 1115 and/or encapsulating material 1125 may be omitted. For example, FIGS. 12A to 12D are schematic cross-sectional views of additional embodiments of RF transistor amplifier die 210 coupled to circuitry module 610C, according to some embodiments of the present invention. As illustrated in FIG. 12A, the circuitry module 610C may be substantially similar to that of FIGS. 11A to 11D and, as such, a duplicate description thereof will be omitted. The embodiment of FIG. 12A, for example, may omit the encapsulating material 1125, through vias 1115, and/or the gate/drain connections 1182, 1184 and directly expose the gate lead 682C and the drain lead 684C. Though FIG. 12A illustrates that all of the encapsulating material 1125 is removed, it will be understood that, in some embodiments, some encapsulating material 1125 may be present. For example, in some embodiments, encapsulating material 1125 may be on portions of the RF transistor amplifier die 210 and the circuitry module 610C, but may expose the gate lead 682C and the drain lead 684C.

[00256] The embodiments illustrated in FIG. 12A may be utilized in multiple packaging configurations. FIGS. 12B and 12C illustrate the use of packaging similar to that discussed herein with respect to FIGS. 5A to 5C, 8A, 8B, 10A, and 10B. For example, the circuitry module 610C and the RF transistor amplifier die 210 may be placed in an open-cavity semiconductor package 1200a (FIG. 12B) or an OMP package 1200b (FIG. 12C). Elements in FIGS. 12B and 12C of the semiconductor package 1200a and semiconductor package

1200b that are similar to those previously discussed with respect to FIGS. 5A to 5C, 8A, 8B, 10A, and 10B will be omitted for brevity. In some embodiments, the gate lead 682C may be coupled to gate lead 415A by a bonding element (e.g., solder balls and/or bumps 320) and the drain lead 684C may also be coupled to drain lead 415B. It will be understood that multiple other possible configurations and/or orientations of the semiconductor package are possible without deviating from the present invention.

[00257] Though many of the embodiments described herein have reduced and/or omitted wire bonds, it will be understood that the present invention may still improve configurations utilizing wire bonds. For example, FIG. 12D illustrates a semiconductor package 1200c utilizing circuitry module 610C that utilizes wire bonds. Referring to FIG. 12D, a semiconductor package 1200c may be, for example, an open-air or open-cavity package. The semiconductor package 1200c may include a carrier substrate 410, sidewalls 520, and a lid 525. The carrier substrate 410, sidewalls 520, and lid 525 may define an internal cavity 530. The RF transistor amplifier die 210 and circuitry module 610C may be disposed inside the internal cavity 530.

[00258] The leads 415A, 415B may be configured to extend through the sidewalls 520, though the present invention is not limited thereto. In some embodiments, the circuitry module 610C may be disposed on the carrier substrate 410 and the leads 415A, 415B, and the RF transistor amplifier die 210 may be disposed on the circuitry module 610C. The leads 415A, 415B may be coupled to the circuitry module 610C using, for example, wire bonds 1280. For example, the lead 415a may be coupled to gate lead 682C and lead 415b may be coupled to drain lead 684C. Though the semiconductor package 1200c utilizes wire bonds 1280, it still benefits from the direct connection between the RF transistor amplifier die 210 and the circuitry modules 610C. Moreover, the circuitry module 610C incorporates the first and second circuit elements 1150a, 1150b that may allow for additional internalized functionality, such as harmonic termination and/or input/output impedance matching. In addition, the use of the circuitry modules 610C allows for greater flexibility in that different performance characteristics (e.g., to address harmonics at different frequencies, different impedances, etc.) may be achieved simply by swapping circuitry modules 610C.

[00259] While FIG. 12D utilizes the circuitry module 610C, it will be understood that the wire bonds 1280 may be incorporated into other semiconductor packaging configurations utilizing any of the circuitry modules and/or RF transistor amplifiers described herein.

[00260] Referring back to FIGS. 6A to 6C, various embodiments are illustrated that provide an RF transistor amplifier die 210 coupled to a circuitry module 610. In some embodiments,

the RF transistor amplifier die 210 is directly coupled to the circuitry module 610 (e.g., FIG. 6B) and, in some embodiments, the RF transistor amplifier die 210 is coupled to the circuitry module 610 via a coupling element 270 (e.g., FIG. 6A). In embodiments of those such as FIGS. 6A to 6C, an encapsulating material 625 may be on one or more sides of the RF transistor amplifier die 210, which may protect/enclose the RF transistor amplifier die 210. In some embodiments, as illustrated in FIGS. 6A to 6C, a bottom surface of the RF transistor amplifier die 210 may be exposed by the encapsulating material 625, but the present invention is not limited thereto.

[00261] FIGS. 13A to 13D are schematic cross-sectional views of additional embodiments of an RF transistor amplifier die 210 coupled to a circuitry module 610 and incorporating a spacer, according to some embodiments of the present invention. Portions of FIGS. 13A to 13D that are previously described will not be described again here for brevity. Referring to FIG. 13A, in some embodiments a spacer 245 may be placed on a bottom surface 210a of the RF transistor amplifier die 210. The encapsulating material 625 may expose a bottom surface 245a of the spacer 245.

[00262] In some embodiments, the spacer 245 may be formed of an electrically and/or thermally conductive material, such as metal. In some embodiments, the spacer 245 may be or include gold (Au) Copper (Cu), a Cu alloy, gold-tin (AuSn), and/or epoxy, though the present invention is not limited thereto. In some embodiments, the spacer 245 may be electrically insulating and/or may be or include, for example, a dielectric material, such as silicon oxide, silicon nitride, a polymer, a molding compound, or a combination thereof, though the present invention is not limited thereto. In some embodiments, the spacer 245 may be thermally conductive. As such, the spacer 245 may be configured to dissipate heat transferred from the RF transistor amplifier die 210. In some embodiments, the spacer 245 may be composed of a plurality of layers, though the present invention is not limited thereto. In some embodiments, the spacer 245 may perform similar functions and/or be composed of similar material as the thermal layer 240 described herein. Incorporating the spacer 245 onto the RF transistor amplifier die 210 within the encapsulating material 625 may provide a packaging option that is easier to distribute and attach. Though FIG. 13A illustrates an embodiment in which the RF transistor amplifier die 210 is directly coupled to the circuitry module 610, the present invention is not limited thereto. In some embodiments, the transistor amplifier die 210 may be coupled to the circuitry module 610 via a coupling element 270 in a manner similar to that illustrated in FIG. 6B. Similarly, in some embodiments the RF

transistor amplifier die 210 may incorporate on-die RDL, such as in the RF transistor amplifier die 210' of FIG. 3C.

[00263] As illustrated in FIG. 13A, the encapsulating material 625 may be on the RF transistor amplifier die 210 and on the first and second circuit elements 650a, 650b. However, the present invention is not limited to such a configuration. Depending on the electrical and thermal requirements for the first and second circuit elements 650a, 650b, alternative and/or additional terminal/bonding/spacer structures can be utilized with at least one of the first and second circuit elements 650a, 650b to provide electrical conductivity, thermal conductivity and/or a mechanical interface to one of more of the first and second circuit elements 650a, 650b.

[00264] In some embodiments, surfaces of the first and second circuit elements 650a, 650b may be exposed and/or coupled to auxiliary spacers as part of the RF transistor amplifier. For example, FIG. 13B is a schematic cross-sectional view of an RF transistor amplifier die 210 coupled to a circuitry module 610, according to some embodiments of the present invention. As illustrated in FIG. 13B, the circuitry module 610 and/or RF transistor amplifier die 210 may be substantially similar to embodiments previously described and, as such, a duplicate description thereof will be omitted. The embodiment illustrated in FIG. 13B, for example, may include a first auxiliary spacer 246a and a second auxiliary spacer 246b.

[00265] In some embodiments, first auxiliary spacer 246a may be formed on the first circuit element 650a. In some embodiments, second auxiliary spacer 246b may be formed on the second circuit element 650B. For example, the first auxiliary spacer 246a may be formed to be on and/or contact the first circuit element 650a and the second auxiliary spacer 246b may be formed to be on and/or contact the second circuit element 650b. In some embodiments, the first and/or second auxiliary spacers 246a, 246b may be formed of an electrically and/or thermally conductive material, such as metal. In some embodiments, a surface of the first and/or second auxiliary spacers 246a, 246b may be exposed from the encapsulating material 625. In some embodiments, the first and/or second auxiliary spacers 246a, 246b may be or include gold (Au) Copper (Cu), a Cu alloy, gold-tin (AuSn), and/or epoxy, though the present invention is not limited thereto. The first and/or second auxiliary spacers 246a, 246b may be configured to be electrically coupled to the first and/or second circuit elements 650a, 650b and may, for example, provide a mechanism by which a ground signal is provided to the first and/or second circuit elements 650a, 650b. In some embodiments, the first and/or second auxiliary spacers 246a, 246b may be thermally conductive. As such, the first and/or second auxiliary spacers 246a, 246b may be configured to dissipate heat transferred from the first

and/or second circuit elements 650a, 650b. In some embodiments, the first and/or second auxiliary spacers 246a, 246b may be electrically insulating and/or may be or include, for example, a dielectric material, such as silicon oxide, silicon nitride, a polymer, a molding compound, or a combination thereof, though the present invention is not limited thereto. In some embodiments, the first and/or second auxiliary spacers 246a, 246b may be composed of a plurality of layers, though the present invention is not limited thereto.

[00266] In some embodiments the first and/or second auxiliary spacers 246a, 246b may be composed of a similar material as the spacer 245, though the present invention is not limited thereto. In some embodiments, the first and/or second auxiliary spacers 246a, 246b may be composed of a different material than the spacer 245. In some embodiments, the first and/or second auxiliary spacers 246a, 246b may be electrically disconnected from the spacer 245. Forming the first and/or second auxiliary spacers 246a, 246b from a different material than, and/or electrically disconnected from, the spacer 245 may assist in limiting current sharing and/or current eddies between the RF transistor amplifier die 210 and the first and/or second circuit elements 650a, 650b. Though the first auxiliary spacer 246a, the second auxiliary spacer 246b, and the spacer 245 are illustrated as separate discrete elements, the present invention is not limited thereto. In some embodiments, the first auxiliary spacer 246a, the second auxiliary spacer 246b, and the spacer 245 may be connected together as an integral layer (see, e.g., FIG. 13C).

[00267] The materials/thicknesses of the first and second auxiliary spacers 246a, 246b can be the same or different materials/thicknesses as the spacer 245. In some embodiments, the spacer 245 and the first and second auxiliary spacers 246a, 246b may have different thicknesses so that the bottoms of the first and second auxiliary spacers 246a, 246b are planar with the bottom of the spacer 245 for ease of packaging/manufacture/bonding of the RF transistor amplifier die 210 and circuitry module 610 to a package substrate or a circuit board. In some embodiments, the spacer 245 and the first and second auxiliary spacers 246a, 246b are the same thickness. In still other embodiments, the spacer 245 spans across the RF transistor amplifier die 210 and at least one or all of the first and second circuit elements 650, 650b to provide, for example, the benefits of a planar interface surface.

[00268] Additional and/or intervening spacers, bonds and other layers can be provided to provide desired electrical, thermal, and mechanical interfaces. Depending on the desired electrical, thermal, and/or mechanical properties desired, the layers can be made of electrically and/or thermally conductive and/or insulative materials. For example, in some embodiments, the spacer 245 may be thermally conductive and electrically insulating, while

the first and second auxiliary spacers 246a, 246b may be both electrically and thermally conductive. In some embodiments, only the spacer 245 may be present on the RF transistor amplifier die 210. In some embodiments, only the first auxiliary spacer 246a may be present on the first circuit element 650a. In some embodiments, only the second auxiliary spacer 246b may be present on the second circuit element 650b. In other embodiments, any combination of spacer 245, first auxiliary spacer 246a, and second auxiliary spacer 246b may be present.

[00269] In some embodiments, exposed surfaces of the first auxiliary spacer 246a, the second auxiliary spacer 246b, and the spacer 245 may be substantially coplanar. That is, the exposed surfaces of the first auxiliary spacer 246a, the second auxiliary spacer 246b, and the spacer 24 may be configured to be mounted to a separate board (e.g., via an attachment method such as solder and the like).

[00270] It will be understood a method of manufacturing of the embodiment of FIGS. 13A to 13C may be similar to that illustrated with respect to FIGS. 7A to 7D. For example, manufacturing the RF transistor amplifier device may include the placement of the spacer 245 on the RF transistor amplifier die 210, the placement of the first auxiliary spacer 246a on the first circuit element 650a, and the placement of the second auxiliary spacer 246b on the second circuit element 650b. For example, the spacer 245 may be electrically and/or thermally connected to the RF transistor amplifier die 210 (e.g., via die attach material). For example, the first auxiliary spacer 246a and the second auxiliary spacer 246b may be electrically and/or thermally connected to the first and second circuit elements 650a, 650b, respectively (e.g., via die attach material). This step could be performed, for example, after the placement of the first and second circuit elements 650a, 650b and the RF transistor amplifier die 210 on the circuitry module 610 (illustrated with respect to FIGS. 7B and 7C). In some embodiments, the placement of the spacer 245, first auxiliary spacer 246a, and second auxiliary spacer 246b may be performed before or after the formation of the encapsulating material 625 on the RF transistor amplifier die 210 (illustrated with respect to FIG. 7D). In some embodiments, depositing the spacer 245 may be performed by a different process than the first auxiliary spacer 246a and/or second auxiliary spacer 2465b. .

[00271] As discussed above, in some embodiments, the first auxiliary spacer 246a, the second auxiliary spacer 246b, and the spacer 245 may be interconnected and/or integrally formed. FIG. 13C illustrates an embodiment having an integrated spacer layer 245'. The integrated spacer layer 245' may extend to be connected to and/or contact the first circuit element 350a, the second circuit element 350b, and the RF transistor amplifier die 10 (e.g.,

source terminal 26 of the RF transistor amplifier die 10). In some embodiments, a surface 245a' of the integrated spacer layer 245' may be exposed from the encapsulating material 325. In some embodiments, the integrated spacer layer 245' may be formed of a same or similar material as the first auxiliary spacer 246a, the second auxiliary spacer 246b, and/or the spacer 245 described with respect to previous embodiments. For example, the integrated spacer layer 245' may be formed of an electrically and/or thermally conductive material, such as metal. In some embodiments, the integrated spacer layer 245' may be or include gold (Au) Copper (Cu), a Cu alloy, gold-tin (AuSn), and/or epoxy, though the present invention is not limited thereto. In some embodiments, the integrated spacer layer 245' may be electrically insulating and/or may be or include, for example, a dielectric material, such as silicon oxide, silicon nitride, a polymer, a molding compound, or a combination thereof, though the present invention is not limited thereto. In some embodiments, the integrated spacer layer 245' may be composed of a plurality of layers, though the present invention is not limited thereto. As used herein, an "integrated" spacer layer 245' refers to a spacer layer 245' that is substantially continuous, though not necessarily of a uniform composition. In some embodiments, different portions of the integrated spacer layer 245' may be composed of different materials. As an example, a portion of the integrated spacer layer 245' on the first auxiliary spacer 246a and/or second auxiliary spacer 246b may be different than a portion of the integrated spacer layer 245' on the RF transistor amplifier die 210.

[00272] Though the integrated spacer layer 245' is illustrated as a uniform layer having a relatively planar upper surface 245b', the present invention is not limited thereto. In some embodiments, the upper surface 245b' of the integrated spacer layer 245' may be non-planar. For example, in some embodiments the first circuit element 650a, the second circuit element 650b, and the RF transistor amplifier die 210 may have different heights, and the integrated spacer layer 245' may be formed to have an upper surface 245b' with portions at each of the different heights of the first circuit element 650a, the second circuit element 650b, and the RF transistor amplifier die 210.

[00273] FIG. 13D illustrates an example embodiment of an RF transistor amplifier device in which the first auxiliary spacer 246a and the second auxiliary spacer 246b are omitted. Referring to FIG. 13D, a surface 650a_s of the first circuit element 650a and/or a surface 650b_s of the second circuit element 650b may be exposed by the encapsulating material 625. The exposure of the surfaces 650a_s, 650b_s of the first and/or second circuit elements 650a, 650b may allow for additional external connections to be applied to the first and/or second circuit elements 650a, 650b. For example, separate electrical connections, such as to

a ground signal, may be connected to the first and/or second circuit elements 650a, 650b by way of their respective exposed surfaces 650a_s, 650b_s.

[00274] The RF transistor amplifier device of FIG. 13D may be formed, for example, by constructing an embodiment similar to that of FIG. 13A and then performing a planarizing operation on portions of the encapsulating material 625 to expose the surfaces 650a_s, 650b_s of the first and/or second circuit elements 650a, 650b.

[00275] The RF transistor amplifiers dies 210 coupled to circuitry modules 610 illustrated in FIGS. 13A to 13D may be utilized in multiple packaging configurations. FIGS. 14A to 14D illustrate the use of packaging similar to that discussed herein with respect to FIGS. 8A and 8B. For example, the circuitry module 610 and the RF transistor amplifier die 210 may be placed in an open-cavity semiconductor package 1400a_1, 1400a_2 (FIGS. 14A and 14B) or an OMP package 1400b_1, 1400b_2 (FIGS. 14C and 14D). Elements in FIGS. 14A and 14B of the semiconductor package 1400a_1 and semiconductor package 1400a_2 that are similar to those previously discussed, such as with respect to FIG. 8A, will not be discussed further for the sake of brevity. Elements in FIGS. 14C and 14D of the semiconductor package 1400b_1 and semiconductor package 1400b_2 that are similar to those previously discussed, such as with respect to FIG. 8B, will not be discussed further for the sake of brevity.

[00276] In FIGS. 14A and 14C, semiconductor packages 1400a_1 and 1400b_1 illustrate the use of circuitry module 610 coupled to RF transistor amplifier die 210 within an open-cavity package and an OMP package. FIG. 14A illustrates an open-cavity semiconductor package 1400a_1 and FIG. 14C illustrates an OMP semiconductor package 1400b_1. The semiconductor packages 1400a_1 and 1400b_1 further include the spacer 425, the first auxiliary spacer 246a, and the second auxiliary spacer 246b such as those illustrated and described with respect to FIG. 13B. The circuitry module 610 may expose gate lead 682 and drain lead 684 that may be connected to leads 415A, 415B, respectively. In some embodiments, the semiconductor packages 1400a_1 and 1400b_1 may include the first auxiliary spacer 246a, the second auxiliary spacer 246b, and the spacer 245, that are substantially coplanar. Depending on the electrical and thermal requirements for the first and second circuit elements 650a, 650b, additional terminal/bonding/spacer structures can be utilized with at least one of the first and second circuit elements 650a, 650b to provide an electrical, thermal, and/or mechanical interface between one of more of the at least one of the first and second circuit elements 650a, 650b and the carrier substrate 410.

[00277] In some embodiments, the first auxiliary spacer 246a and the second auxiliary spacer 246b may be composed of different materials than the spacer 425. For example, in some

embodiments, the first auxiliary spacer 246a and the second auxiliary spacer 246b may be electrically conductive so as to be electrically coupled to the carrier substrate 410. For example, the first auxiliary spacer 246a and the second auxiliary spacer 246b may provide an electrical connection (e.g., a ground signal) to the first and second circuit elements 650a, 650b. In some embodiments, the spacer 245 may be thermally conductive but an electric insulator. This may allow for the spacer 245 to dissipate heat from the RF transistor amplifier die 210. In some embodiments, first and second auxiliary spacers 246a, 246b may be electrically insulating or conductive, but may thermally connect the first and second circuit elements 650a, 650b to the carrier substrate 410 so as to dissipate thermal energy (e.g., heat) from the first and second circuit elements 650a, 650b.

[00278] FIGS. 14B and 14D illustrate example semiconductor packages 1400a_2, 1400b_2 that incorporate an integrated spacer layer 245 within an open-cavity package and an OMP package. FIG. 14B illustrates an open-cavity semiconductor package 1400a_2 and FIG. 14D illustrates an OMP semiconductor package 1400b_2. The semiconductor packages 1400a_2, 1400b_2 may utilize the integrated spacer layer 245' as discussed herein with respect to FIG. 13C. The integrated spacer layer 245' may be connected and/or directly contact the carrier substrate 410. The integrated spacer 245' may be coupled to the to the first circuit element 650a, the second circuit element 650b, and/or the RF transistor amplifier die 210. In some embodiments, the integrated spacer layer 245' may be configured to have a surface (e.g., an upper surface) that is non-planar so as to couple to the first circuit element 650a, the second circuit element 650b, and the RF transistor amplifier die 210. The present invention is not limited thereto and, in some embodiments, an upper surface of the integrated spacer layer 245' may be planar. In some embodiments, different portions of the integrated spacer layer 245' may be composed of different materials. In some embodiments, additional layers may be respectively disposed between the first and second circuit elements 650a, 650b and the integrated spacer layer 245' or between the integrated spacer layer 245' and the carrier substrate 410. (e.g., additional spacer layers).

[00279] In FIGS. 14A to 14D, RF transistor amplifier die 210 is illustrated as being directly coupled to the circuitry module 610 in the semiconductor packages 1400a_1, 1400a_2, 1400b_1, and 1400b_2, but it will be understood that the RF transistor amplifier die 210 could also be coupled to the circuitry module via coupling element 270 or utilizing an on-die RDL, *mutatis mutandis*.

[00280] FIGS. 15A to 15D are schematic cross-sectional views of additional RF transistor amplifier embodiments including circuitry module 610B and incorporating mechanisms to

couple to the first and second circuit elements 650a,650b, according to some embodiments of the present invention. Portions of the RF transistor amplifiers die 210 and the circuitry module 610B may be substantially similar to that of FIGS. 9A to 9D, as well as other previously described figures, and, as such, a duplicate description thereof will be omitted. The embodiments of FIGS. 15A to 15D may, for example, incorporate a circuitry module 610B that exposes a gate lead 682B and/or a drain lead pad 684B on same side 601 (e.g., a lower surface) of the circuitry module 610B to which the RF transistor amplifier die 210 is coupled. The embodiment of the RF transistor amplifier of FIGS. 15A to 15D, for example, may include an embodiment similar to that of FIG. 9B with the addition of a spacer 245, a first auxiliary spacer 246a, and/or a second auxiliary spacer 246b.

[00281] For example, FIG. 15A illustrates the RF transistor amplifier die 210 coupled to the circuitry module 610B, with spacer 245 placed on a bottom surface 210a of the RF transistor amplifier die 210. The encapsulating material 625 may expose a bottom surface 245a of the spacer 245.

[00282] In some embodiments, the spacer 245 may be formed of an electrically and/or thermally conductive material, such as metal. In some embodiments, the spacer 245 may be or include gold (Au) Copper (Cu), a Cu alloy, gold-tin (AuSn), and/or epoxy, though the present invention is not limited thereto. In some embodiments, the spacer 245 may be electrically insulating and/or may be or include, for example, a dielectric material, such as silicon oxide, silicon nitride, a polymer, a molding compound, or a combination thereof, though the present invention is not limited thereto. In some embodiments, the spacer 245 may be thermally conductive. As such, the spacer 245 may be configured to dissipate heat transferred from the RF transistor amplifier die 210. In some embodiments, the spacer 245 may perform similar functions and/or be composed of similar material as the thermal layer 240 described herein. In some embodiments, the spacer 245 may be composed of a plurality of layers, though the present invention is not limited thereto. Though FIG. 15A illustrates an embodiment in which the RF transistor amplifier die 210 is directly coupled to the circuitry module 610, the present invention is not limited thereto. In some embodiments, the transistor amplifier die 210 may be coupled to the circuitry module 610 via a coupling element 270 in a manner similar to that illustrated in FIG. 6B. Similarly, in some embodiments the RF transistor amplifier die 210 may incorporate on-die RDL, such as in the RF transistor amplifier die 210' of FIG. 3C.

[00283] FIG. 15B illustrates an embodiment similar to that of FIG. 15A, with the addition of a first auxiliary spacer 246a and a second auxiliary spacer 246b. In some embodiments, the

first auxiliary spacer 246a may be formed to be on and/or contact the first circuit element 650a and the second auxiliary spacer 246b may be formed to be on and/or contact the second circuit element 650b. In some embodiments, the first and/or second auxiliary spacers 246a, 246b may be formed of an electrically and/or thermally conductive material, such as metal. In some embodiments, a surface of the first and/or second auxiliary spacers 246a, 246b may be exposed from the encapsulating material 625. In some embodiments, the first and/or second auxiliary spacers 246a, 246b may be or include gold (Au) Copper (Cu), a Cu alloy, gold-tin (AuSn), and/or epoxy, though the present invention is not limited thereto. The first and/or second auxiliary spacers 246a, 246b may provide a mechanism by which a ground signal is provided to, or thermal energy is dissipated from, the first and/or second circuit elements 650a, 650b, as discussed herein with respect to other embodiments.

[00284] In some embodiments, the first and/or second auxiliary spacers 246a, 246b may be composed of a similar material as the spacer 245, though the present invention is not limited thereto. In some embodiments, the first and/or second auxiliary spacers 246a, 246b may be composed of a different material than the spacer 245. In some embodiments, the first and/or second auxiliary spacers 246a, 246b may be electrically disconnected (e.g., isolated) from the spacer 245. In some embodiments, the first and/or second auxiliary spacers 246a, 246b may be composed of a plurality of layers, though the present invention is not limited thereto.

[00285] Though the first auxiliary spacer 246a, the second auxiliary spacer 246b, and the spacer 245 are illustrated as separate discrete elements, the present invention is not limited thereto. In some embodiments, the first auxiliary spacer 246a, the second auxiliary spacer 246b, and the spacer 245 may be formed as an integrated (e.g., interconnected) spacer layer 245'. Such an embodiment is illustrated in FIG. 15C, which represents an RF transistor amplifier die 210 coupled to a circuity module 610B including an integrated spacer layer 245'. The integrated spacer layer 245' may be similar to that discussed herein with respect to FIG. 13C. The integrated spacer layer 245' may extend to contact the first circuit element 650a, the second circuit element 650b, and/or the RF transistor amplifier die 210. In some embodiments, a surface 245a of the integrated spacer layer 245' may be exposed from the encapsulating material 625. In some embodiments, the integrated spacer layer 245' may be formed of a same or similar material as the first auxiliary spacer 246a, the second auxiliary spacer 246b, and/or the spacer 245. In some embodiments, the upper surface 245b' of the integrated spacer layer 245' may be non-planar or planar. For example, in some embodiments the first circuit element 650a, the second circuit element 650b, and/or the RF transistor amplifier die 210 may have different heights, and the integrated spacer layer 245' may be

formed to have an upper surface 245b' with portions at each of the different heights of the first circuit element 650a, the second circuit element 650b, and the RF transistor amplifier die 210.

[00286] FIG. 15D illustrates an embodiment of an RF transistor amplifier device in which the first auxiliary spacer 246a and the second auxiliary spacer 246b are omitted. The RF transistor amplifier die 210 may be coupled to a circuitry module 610B similarly to that of FIG. 15A and, as such, a duplicate description thereof will be omitted. Referring to FIGS. 15A and 15D, an upper surface 650a_s of the first circuit element 650a and/or an upper surface 650b_s of the second circuit element 650b may be exposed from the encapsulating material 625. The exposure of the surfaces 650a_s, 650b_s of the first and/or second circuit elements 650a, 650b may allow for additional external connections to be applied to the first and/or second circuit elements 650a, 650b. For example, separate electrical connections, such as to a ground signal, may be connected to the first and/or second circuit elements 650a, 650b by way of their respective exposed surfaces 650a_s, 650b_s.

[00287] The RF transistor amplifier device of FIG. 15D may be formed, for example, by constructing the RF transistor amplifier device of FIG. 15A and then performing a planarizing operation on portions of the encapsulating material 625 to expose the surfaces 650a_s, 650b_s of the first and/or second circuit elements 650a, 650b.

[00288] The RF transistor amplifier devices illustrated in FIGS. 15A to 15D may be utilized in multiple packaging configurations. FIGS. 16A to 16D illustrate the use of packaging similar to that discussed herein with respect to FIGS. 10A, 10B, and 14A to 14D. For example, the circuitry module 610B and the RF transistor amplifier die 210 may be placed in an open-cavity semiconductor package 1600a_1, 1600a_2 (FIGS. 16A, 16B) or an OMP package 1600b_1, 1600b_2 (FIGS. 16C, 16D). In some embodiments, a spacer layer 245 may be utilized with first and second auxiliary spacers 246a, 246b in an open-cavity semiconductor package 1600a_1 (FIG. 16A) or an OMP package 1600b_1 (FIG. 16C). In some embodiments, an integrated spacer layer 245' may be utilized with an open-cavity semiconductor package 1600a_2 (FIG. 16B) or an OMP package 1600b_2 (FIG. 16D). Elements in FIGS. 16A to 16D of the semiconductor packages 1600a_1, 1600a_2, 1600b_1, and 1600b_2 that are similar to those previously discussed with respect to other figures, such as FIGS. 10A and 10B, will not be discussed further for the sake of brevity. In some embodiments, the semiconductor packages 1600a_1, 1600a_2, 1600b_1, and 1600b_2 may accommodate an RF transistor amplifier device where the gate lead pad 682B and drain lead pad 684B are exposed on a lower surface of the circuitry module 610B. In FIGS. 16A to

16D, RF transistor amplifier die 210 is illustrated as being directly coupled to the circuitry module 610B in the semiconductor packages 1600a_1, 1600a_2, 1600b_1, and 1600b_2, but it will be understood that the RF transistor amplifier die 210 could also be coupled to the circuitry module via coupling element 270 or utilizing an on-die RDL, *mutatis mutandis*.

[00289] Referring to FIGS. 16A and 16C, the first and second auxiliary spacers 246a, 246b may be connected and/or directly contact the carrier substrate 410. In this manner, the first and second auxiliary spacers 246a, 246b may be configured to thermally dissipate heat from and/or provide an electrical signal (e.g., a ground signal) to the first and second circuit elements 650a, 650b. Depending on the electrical and thermal requirements for the first and second circuit elements 650a, 650b, additional terminal/bonding/spacer structures can be utilized with at least one of the first and second circuit elements 650a, 650b to provide an electrical, thermal, and/or mechanical interface between one of more of the at least one of the first and second circuit elements 650a, 650b and the substrate 410.

[00290] Referring to FIGS. 16B and 16D, the first and second auxiliary spacers 246a, 246b may be replaced with an integrated spacer layer 245' that is coupled to the first circuit element 650a, the second circuit element 650b, and/or the RF transistor amplifier die 210. The integrated spacer layer 245' may be connected and/or directly contact the carrier substrate 410. The integrated spacer layer 245' may have a planar or a non-planar upper surface. In some embodiments, additional layers may be respectively disposed between the first and second circuit elements 650a, 650b and the integrated spacer layer 245' or between the integrated spacer layer 245' and the carrier substrate 410. (e.g., additional spacer layers).

[00291] The embodiments described herein provide an improved RF transistor amplifier and improved packaging incorporating such an RF transistor amplifier. By avoiding and/or reducing the use of back side vias, some embodiments of the present invention provide for improved thermal management of a power amplifier. Moreover, by locating the contacts of the power amplifier on a same side of the device, interconnect structures or circuitry modules may be utilized which may reduce the need for wire bonding. As a result, the RF transistor amplifier and associated package may exhibit improved performance and thermal properties over conventional devices. The benefits of the direct bonding provided by embodiments of the present invention are reduction of form factor, low electrical resistance, as well as improvement of communication speed.

[00292] As discussed above, pursuant to embodiments of the present invention, Group III nitride-based RF transistor amplifiers 200, 200', 200" (collectively 200) may include transistor dies 210 having gate terminals, drain terminals, and source terminals all located on

the same (e.g., top or front) side or surface 212 of the RF transistor amplifier die 210, also referred to herein as the transistor die 210 or die 210. The RF transistor amplifiers 200 may not include bond wires for the gate and/or drain connections, which may reduce an amount of inductance present in the circuit. Since all three of the gate, drain and source terminals are on the top side 212 of the transistor die 210, the RF transistor amplifiers according to embodiments of the present invention may be mounted in a flip chip arrangement in which the transistor die 210 is mounted on another substrate, such as on the surface of an interconnect structure 310, 610 as described above. In some embodiments, the opposite (e.g., back) side or surface 214 of the transistor die 210 can be mounted on a thermally conductive carrier substrate or submount 410, such as a metal slug, leadframe, or flange, to provide improved thermal dissipation of the heat generated by the die from the amplifier package.

[00293] The interconnect structure may be implemented by any of the circuitry modules (e.g., 310, 310', 310" (collectively 310) or 610, 610', 610A-C (collectively 610)) discussed herein. The interconnect structure may be an interposer structure, such as a dielectric base structure with integrated conductive traces, vias and/or circuitry extending therein and/or thereon, or other multi-layer laminate or PCB structure. The conductive traces or patterns (e.g., 373, 673, 1173) may provide various routing and/or circuitry within the interconnect structure.

[00294] The interconnect structure may include circuit elements (e.g., 350a-b (collectively 350) or 650a-b (collectively 650)) of the RF transistor amplifier, on one more surfaces thereof. The circuit elements may be configured to provide, for example, impedance matching and/or harmonic termination circuitry. For instance, the conductive traces or patterns of the interconnect structure 310, 610 may electrically couple the circuit elements between the gate terminal 222 and an input lead 415A, and/or between the drain terminal 224 and an output lead 415B.

[00295] As described above, the circuit elements 350, 650 may include passive electrical components, including resistors/transmission lines, capacitors, and/or inductors, which may be implemented (at least partially) in surface mount devices (SMD), integrated passive devices (IPD), and combinations thereof. IPDs may include inductors, capacitors, and/or other passive electrical components, and may be fabricated using standard semiconductor processing techniques such as thin film and/or photolithography processing. IPDs can be flip chip mountable or wire bondable components, and may include thin film substrates such as silicon, alumina, or glass.

[00296] In further embodiments described herein, the interposer or other interconnect structure and the passive electrical components on a surface thereof may collectively implement a "passive module," also referred to herein as a passive component assembly. An active transistor die and any conductive structures (e.g., pillars or coupling elements thereon) may collectively implement an "active module," also referred to herein as an active component assembly. The active component assembly may be provided on a surface of the passive component assembly (e.g. on a top surface or on a bottom surface). The active module and passive module may be coupled by flip chip connection, in some embodiments with a standoff for mechanical support and/or thermal conduction. The active module may include an active GaN on SiC die and RDL or heat spreader. Examples of active modules are shown and described herein with reference to FIGS. 20A to 20C. The passive module may include various passive components, such as IPDs, SMDs, laminate-based transmission lines etc., e.g., for impedance matching and/or harmonic termination. Examples of passive modules are shown and described herein with reference to FIGS. 19A to 19C. The passive modules described herein may be electrically tested and screened before integration with the active modules, which may improve yield and reduce costs.

[00297] Embodiments of the present invention may also allow for stacked component connections (e.g., in the Z-direction) and separate electrical ground paths from the main heat conduction path, which may otherwise be difficult or impossible without a flip chip interconnection scheme. Also, separating the active and passive modules of a packaged device may allow for electrical testing and/or screening before final packaging/assembly, which can improve yield and reduce costs. The standoff structures may not only provide mechanical support to the laminate or interposer for assembly flexibility, but may also provide another heat extraction path if a high thermal conductivity material is chosen.

[00298] In some embodiments, the passive component assembly or module may include the transistor die 210 on the same side or surface of the interconnect structure as the passive electrical components. For example, as described above with reference to FIGS. 6A-6B, 7C-7E, and 8A-8B, the circuit elements 650 and the die 210 are provided on the same surface of the interconnect structure 610, which may be referred to herein as an active module on same side of passive module (AMSPM) configuration. In some embodiments, the passive component assembly or module may include the transistor die 210 on an opposite surface of the interconnect structure than the passive electrical components. For example, in FIGS. 3A to 3E, 4A to 4C, and 5A to 5C, the circuit elements 350 and the die 210 are provided on

opposite sides or opposing surfaces of the interconnect structure 310, which may be referred to herein as an active module on backside of passive module (AMBPM) configuration.

[00299] The AMSPM and AMBPM configurations described herein may include many variations of active and passive component assemblies. FIGS. 19A, 19B, and 19C illustrate various examples of passive component assemblies 1905a, 1905b, 1905c (collectively 1905) according to some embodiments of the present invention. As shown in FIGS. 19A-19C, the passive component assemblies 1905 respectively include a circuitry module or other interconnect structure 310". The circuitry module 310" includes internal conductive patterns 373 and one or more passive electrical components 1750a, 1750b, 1750c/c'/c" (collectively 1750) on a first surface 312. In some embodiments, circuitry module 310" may be formed as a printed circuit board (PCB) or redistribution layer (RDL) laminate structure, with the conductive patterns 373 implemented as conductive structures within the substrate of the PCB or the RDL laminate structure.

[00300] The conductive patterns 373 may provide various routing and/or circuitry within the circuitry module 310", such that a die 210 may be mounted on the first surface 312 (in an AMSPM configuration) and/or on the second surface 314 (in an AMBPM configuration) of the interconnect structure 310". For example, the conductive patterns 373 may electrically connect interconnection pads 372, 374, 376 on the first surface 312 of the circuitry module 310" to one another and/or to interconnection pads 322, 324, 326 on a second surface 314 of the circuitry module 310".

[00301] In particular, in FIGS. 19A, 19B, and 19C, the interconnection pads 322, 324, 326 are configured to be coupled to the gate terminal 222", the drain terminal 224", and the source terminal 226" of a die 210 that is mounted on the second surface 314 opposite the passive component(s) 1750. In some embodiments, the interconnection pads 372, 374, 376 may be configured to be coupled to the gate terminal 222", the drain terminal 224", and the source terminal 226" of a die 210 that is mounted on the first surface 312 adjacent the passive component(s) 1750. Though illustrated by way of example as a single pads, one or more of the interconnection pads 322, 324, 326, 372, 374, 376 may be implemented by multiple pads.

[00302] The passive electrical components 1750 may include resistors/transmission lines, capacitors, and/or inductors, that are implemented in SMDs and/or IPDs. In the examples of FIGS. 19A-19C, the passive electrical components 1750a are arranged for electrical connection to an input lead of a package, the passive electrical components 1750b are arranged for electrical connection to an output lead of the package, and the passive electrical

components 1750c are arranged for electrical connection between the components 1750a and 1750b and one or more terminals 222", 224", 226" of the die 210.

[00303] The passive electrical components 1750 may be attached to respective interconnection pads 372, 374, 376 on the first surface 312 of the circuitry module 310" in surface mount (e.g., 1750c), wirebond (e.g., 1750c'), or flip-chip (e.g., 1750c") configurations. In particular, FIG. 19A illustrates each of the passive electrical components 1750a, 1750b, 1750c in a surface mount configuration. FIG. 19B illustrates a combination of surface mount components 1750a, 1750b with a wirebond component 1750c'. FIG. 19C illustrates a combination of surface mount components 1750a, 1750b with a flip-chip component 1750". In the flip-chip configuration, the passive electrical components 1750c" may include conductive pads that are aligned with and electrically coupled to one or more interconnection pads 372, 374, 376. In any of the examples of FIGS. 19A-19C, the passive electrical components 1750 may be preassembled, e.g., encased in a mold structure (e.g., 2240 as shown in FIG. 22) that is separate from a package overmold material (e.g., 1740), on the first surface 312 of the circuitry module 310".

[00304] Conductive leads 415A, 415B (as shown in FIGS. 17-18 and 21A to 24C) allow the RF transistor amplifier 200 to be connected to external devices/circuits/power sources. The leads 415A, 415B may be coupled to the circuitry module 310" using, for example, wire bonds or a conductive die attach material. In some embodiments (e.g., FIG. 18), the leads 415A and 415B may be coupled to the interconnection pads on the first surface 312 of the circuitry module 310" (e.g., to interconnection pads 372 and 374, respectively). In some embodiments (e.g., FIG. 17), the leads 415A and 415B may be coupled to the interconnection pads on the second surface 314 (e.g., to interconnection pads 322 and 324, respectively). In some embodiments, the leads 415A, 415B may be directly coupled to the interconnection pads, such that the use of wire bonds to connect the RF transistor amplifier 200 to leads 415A, 415B may be avoided and/or reduced. Although primarily illustrated with reference to two leads 415A and 415B, embodiments of the present invention are not so limited. In some embodiments, three or more leads may be provided, for example, coupled to the interconnection pads 322 or 372 (e.g., as gate leads), 324 or 374 (e.g., as drain leads), and 326 or 376 (e.g., as source leads).

[00305] The passive electrical components 1750 may thereby be electrically coupled between the gate terminal 222" and the first (e.g., input) lead 415A of the transistor amplifier, and/or between the drain terminal 224" and the second (e.g., output) lead 415B of the transistor amplifier. In particular, an RF signal input to the RF transistor amplifier 200 on the input

lead 415A may be passed through the circuitry module 310" to passive electrical components 1750a, 1750c and from there to a gate terminal 222" of the transistor die 210, and the amplified output RF signal may be passed from the drain terminal 224" of the transistor die 210 to the passive electrical components 1750c, 1750b and from there through the circuitry module 310" where the RF signal is output through output lead 415B.

[00306] The passive electrical components 1750 coupled by the circuitry module 310" may be configured to provide, for example, input matching circuits, output matching circuits, and/or harmonic termination circuits that are used to impedance match at the fundamental frequency and/or to terminate intermodulation products to ground. The use of passive component assemblies 1905 described herein may thus provide greater flexibility in that different performance characteristics (e.g., to address harmonics at different frequencies, different impedances, etc.) for different applications may be achieved by swapping passive component assemblies 1905 and/or the passive electrical components 1750. In addition, the passive component assemblies 1905 may be electrically tested before integration with the active component assemblies described herein, which may improve yield and reduce product costs. As such, passive component assemblies 1905 in accordance with embodiments of the present invention may be configured to provide a modular approach for achieving RF transistor amplifiers with desired performance characteristics.

[00307] The AMSPM and AMBPM configurations described herein may likewise include variations of the active component assemblies. FIGS. 20A, 20B, and 20C illustrate examples of active component assemblies 2005a, 2005b, 2005c (collectively 2005) according to some embodiments of the present invention. As shown in FIG. 20A, an example active component assembly 2005a may include an active die 210 (e.g., a Group III-nitride or SiC-based semiconductor die). The gate terminal 222", drain terminal 224", and/or source terminal 226" may be implemented by conductive pillar structures (e.g., copper pillars). In the example of FIG. 20A, all of the conductive pillar structures 222", 224", 226" protrude from a first or active surface 212 of the die 210, i.e., the "top" or front surface 212 adjacent the active channel 2 (e.g., the 2DEG layer). FIG. 20A thus illustrates a flip-chip configuration of the active die 210, with the contacts 222", 224", and 226" on one side 212 of the die 210 (e.g., facing "down" when connected to the circuitry module 310"), and the growth substrate on the opposite side 214 (e.g., facing "up" when connected to the circuitry module 310"). However, it will be understood that one or more of the gate terminal 222", drain terminal 224", and source terminal 226" may protrude from or may otherwise be implemented on the second or inactive surface 214 of the die 210.

[00308] FIG. 20B illustrates an example active component assembly configuration 2005b in which the die 210 including the conductive pillar structures 222", 224", 226" are electrically connected to a coupling element 270. The coupling element 270 includes a gate connection pad 272, a drain connection pad 274, a source connection pad 276, and conductive patterns 273. The conductive patterns 273 electrically connect the gate connection pad 272 and the drain connection pad 274, and the source connection pad 276 to the gate terminal 222", drain terminal 224", and source terminal 226" of the die 210 (which, as noted above, may be implemented by conductive pillar structures). An encapsulating structure 277 provides a package including the die 210 and the coupling element 270. For example, the die 210, conductive pillar structures 222", 224", 226", and the coupling element 270 may be implemented in a redistribution layer (RDL) package. The encapsulating material 277 may be formed of a plastic or a plastic polymer compound, but the present invention is not limited thereto. In some embodiments, the encapsulating material 277 may include a polymer with fillers. In the example shown in FIG. 20B, the connection pads 272, 274, 276 and conductive patterns 273 are arranged in a fan-out configuration that increases separation of the connections to the respective source, gate, and drain terminals, but it will be understood that other configurations (e.g., a fan-in configuration) may be similarly implemented.

[00309] FIG. 20C illustrates an example active component assembly configuration 2005c in which the conductive pillar structures 222", 224", 226" protrude from the first or active surface 212 of the die 210, and the second or inactive surface 214 of the die 210 is mounted on a thermally conductive substrate 410 (such as a metal slug, leadframe, flange, or other heatsink). The thermally conductive substrate 410 can provide improved thermal dissipation of the heat generated by the die 210 from the amplifier package.

[00310] In any of the example active component assemblies 2005a, 2005b, 2005c, the die 210 may be mounted in a flip chip arrangement on the first surface 312 (in an AMSPM configuration) or the second surface 314 (in an AMBPM configuration) of an interconnect structure 310", that is, with the gate terminal 222", the drain terminal 224", and the source terminal 226" facing the surface 312 or 314 of interconnect structure 310". In the example of FIG. 20B, the coupling element 270 may be provided between the first surface 212 of the die and the interconnect structure 310". Also, while illustrated in FIGS. 20A-20C with reference to specific examples, elements of one or more the example active component assemblies 2005a, 2005b, 2005c may be combined in some embodiments. For example, the inactive surface 214 of the die 210 may be exposed by the encapsulating structure 277 in the active

component assembly 2005b of FIG. 20B, and may be mounted on the thermally conductive substrate 410 of FIG. 20C.

[00311] Further embodiments of the present invention are described below with reference to various combinations of active component assemblies (e.g., 2005a, 2005b, 2005c) and passive component assemblies (e.g., 1905a, 1905b, 1905c), mounted on the first side 312 or second side 314 of the passive component assemblies. It will be understood that these embodiments are provided by way of illustration rather than limitation, and that any and all configurations of the passive component assembly 1905 and active component assembly 2005 are included in the scope of the present invention.

[00312] FIG. 17 is a schematic cross-sectional view of a semiconductor package 1700 for an RF transistor amplifier according to some embodiments of the present invention. In particular, FIG. 17 illustrates an example package 1700 including an active component assembly 2005 coupled to a passive component assembly 1905 in an AMSPM configuration, where the die 210 is on a surface 312 of the interconnect structure or circuitry module 310" adjacent one or more passive electrical components 1750 on the same surface 312. The description of FIG. 17 will focus on elements of the RF transistor amplifier that may differ from those previously described in detail above.

[00313] As shown in FIG. 17, an active component assembly 2005 (e.g., the active component assembly 2005b) is provided on a passive component assembly 1905, such that exposed interconnection pads 372, 374, and 376 on the first surface 312 of the circuitry module 310" are electrically coupled to the gate connection pad 272, the drain connection pad 274, and the source connection pad 276 of the coupling element 270, respectively (and thus, are electrically coupled to the gate terminal 222", drain terminal 224", and source terminal 226" of the die 210, respectively). However, it will be understood that the coupling element 270 may be omitted in some active component assemblies (e.g., 2005a, 2005c), and the transistor die 210 may be mounted on the first surface 312 with the gate terminal 222", drain terminal 224", and source terminal 226" directly coupled to the interconnection pads 322, 324, and 326. The passive electrical components 1750 are attached to respective interconnection pads 372, 374, 376 on the surface 312 of the circuitry module 310", in surface mount (e.g., 1750a, 1750b), wirebond (e.g., 1750c'), and/or flip-chip configurations, adjacent to the active component assembly 2005.

[00314] In the example AMSPM configuration of FIG. 17, a thermally conductive substrate 410 (e.g., a metal slug, leadframe, or flange) is mounted on a surface of the active component assembly 2005 (in particular, on a surface of the encapsulating material 277) opposite the

passive component assembly 1905 for improved thermal dissipation of the heat generated by the die 210. The active component assembly 2005 and passive component assembly 1905 may be at least partially encased in an overmold material 1740. The overmold material 1740 may be formed of a plastic or a plastic polymer compound, which may be injection molded around the active component assembly 2005 and/or the passive component assembly 1905, thereby providing protection from the outside environment.

[00315] In FIG. 17, the conductive leads 415A and 415B are mounted on the passive component assembly 1905 (in particular, on the second surface 314 of the circuitry module 310" and electrically coupled to the exposed interconnection pads 322 and 324, respectively) opposite the die 210 to provide input RF signals to the die (e.g., to the gate terminal 222" via passive components 1750a, 1750c', and coupling element 270) and to provide amplified output RF signals from the die 210 (e.g., from the drain terminal 224" via coupling element 270 and passive components 1750c', 1750b). However, it will be understood that the leads 415A, 415B may be mounted on the same surface as the die 210 (e.g., on the first surface 312 of the circuitry module 310" and protruding from the overmold material 1740) in some embodiments.

[00316] FIG. 18 is a schematic cross-sectional view of a semiconductor package 1800 for an RF transistor amplifier according to some embodiments of the present invention. In particular, FIG. 18 illustrates an example package 1800 including an active component assembly 2005 coupled to a passive component assembly 1905 in an AMBPM configuration, where the die 210 is on a surface 314 of the interconnect structure or circuitry module 310" opposite the surface 312 having the passive electrical components 1750 thereon. The description of FIG. 18 will focus on elements of the RF transistor amplifier that may differ from those previously described in detail above.

[00317] As shown in FIG. 18, an active component assembly 2005 (e.g., the active component assembly 2005a) is provided on a passive component assembly 1905 (e.g., the passive component assembly 1905b) such that exposed interconnection pads 322, 324, and 326 on the second surface 314 of the circuitry module 310" are electrically coupled to the gate terminal 222", drain terminal 224", and source terminal 226" of the die 210, respectively. In particular, the transistor die 210 is mounted on the surface 314 of the circuitry module 310", with the conductive pillars 222", 224", and 226" (defining the gate, drain, and source terminals) directly coupled to the interconnection pads 322, 324, and 326, respectively. The passive electrical components 1750 are attached to respective interconnection pads 372, 374, 376 on the opposite surface 312 of the circuitry module 310",

in surface mount (e.g., 1750a, 1750b), wirebond (e.g., 1750c`), and/or flip-chip configurations.

[00318] In the example AMBPM configuration of FIG. 18, a thermally conductive substrate 410 (e.g., a metal slug, leadframe, or flange) is mounted (e.g., using a thermal layer 240) on a surface of the active component assembly 2005 opposite the passive component assembly 1905 for improved thermal dissipation of the heat generated by the die 210. In some embodiments, the thermal layer 240 may be omitted.

[00319] The active component assembly 2005 and passive component assembly 1905 are encased in an overmold material 1740. The conductive leads 415A and 415B protrude from the overmold 1740 to provide input RF signals to the die 210 (e.g., to the gate terminal 222") and amplified output RF signals from the die 210 (e.g., from the drain terminal 224"). In the example of FIG. 18, the leads 415A and 415B are mounted on the first surface 312 of the circuitry module 310" and electrically coupled to the exposed interconnection pads 372 and 374, opposite the second surface 314 having the die 210 thereon. However, it will be understood that the leads 415A, 415B may be mounted on the same surface as the die 210 (e.g., on the second surface 314 of the circuitry module 310" and electrically coupled to the exposed interconnection pads 322 and 324) in some embodiments.

[00320] FIGS. 21A to 24D illustrate various example packages for RF transistor amplifiers in AMBPM configurations according to some embodiments of the present invention. The examples of FIGS. 21A to 24B include package leads 415A and 415B that are electrically coupled to the passive component assembly modules 1905 by wirebond connections 2115, and may be also referred to herein as wirebond-to-lead packages. The examples of FIGS. 24C and 24D illustrate package leads 415A and 415B implemented on the laminate structure of the circuitry module 310" itself, in overmold and open-cavity configurations, respectively. While illustrated with leads 415A and 415B electrically connected to interconnection pads 372 and 374 on the top surface 312 of the circuitry modules 310", it will be understood that one or more of the leads 415A and 415B may be similarly connected to the interconnection pads on the bottom surface 314 in some embodiments. The description of FIGS. 21A to 24D will focus on elements of the RF transistor amplifier that may differ from those previously described in detail above.

[00321] In particular, FIG. 21A is a schematic cross-sectional view and FIG. 21B is a schematic plan view of a semiconductor package 2100 including an active component assembly 2005 (e.g., the active component assembly 2005a) provided on a passive component assembly 1905 (e.g., the passive component assembly 1905b) in an AMBPM

configuration, where the die 210 is on a surface 314 of the interconnect structure or circuitry module 310" opposite the surface 312 having the passive electrical components 1750 thereon. Exposed interconnection pads 322, 324, and 326 on the second surface 314 of the circuitry module 310" are electrically coupled to the gate terminal 222", drain terminal 224", and source terminal 226" of the die 210, respectively. The passive electrical components 1750 are attached to respective interconnection pads 372, 374, 376 on the opposite surface 312 of the circuitry module 310", in surface mount (e.g., 1750a, 1750b), wirebond (e.g., 1750c'), and/or flip-chip configurations.

[00322] Still referring to FIGS. 21A and 21B, a thermally conductive substrate 410 (e.g., a metal slug, leadframe, or flange) is mounted (e.g., using a thermal layer 240) on a surface of the active component assembly 2005 opposite the passive component assembly 1905 for improved thermal dissipation of the heat generated by the die 210. In some embodiments, the thermal layer 240 may be omitted.

[00323] The active component assembly 2005 and passive component assembly 1905 are encased in an overmold material 1740. As shown in FIG. 21B, the passive component assembly 1905 includes one or more cavities 2140 (e.g., holes or openings 2140 in the circuitry module 310"). The overmold material 1740 may extend into or may otherwise be provided in the opening(s) 2140, which may enhance adhesion. The conductive leads 415A and 415B are electrically coupled to the exposed interconnection pads 372 and 374 of the circuitry module 310" by wirebonds 2115, and protrude from the overmold 1740 to provide input RF signals to the die 210 (e.g., to the gate terminal 222") and amplified output RF signals from the die 210 (e.g., from the drain terminal 224").

[00324] FIG. 22 is a schematic cross-sectional view of a semiconductor package 2200 including an active component assembly 2005 (e.g., the active component assembly 2005a) provided on a passive component assembly 1905 (e.g., the passive component assembly 1905b) in an AMBPM configuration, where the die 210 is on a surface 314 of the interconnect structure or circuitry module 310" opposite the surface 312 having the passive electrical components 1750 thereon. As shown in FIG. 22, the passive electrical components 1750 are pre-assembled in an initial mold structure 2240, which is provided on the surface 312 of the circuitry module 310". The mold structure 2240 is distinct from the overmold material 1740, which is subsequently formed to encapsulate the active and passive component assemblies 2005 and 1905 in the package 2200 (e.g., on the thermally conductive substrate 410). As such, the surface 314 including the die 210 thereon may be free of the mold structure 2240. In some embodiments the mold structure 2240 may be formed of a

harder or softer material than the overmold material 1740. The example package 2200 of FIG. 22 may include other components or may otherwise be similar to wirebond-to-lead package 2100 of FIGS. 21A and 21B.

[00325] FIGS. 23A and 23B are schematic cross-sectional views of semiconductor packages 2300a and 2300b including an active component assembly 2005 (in particular, the active component assemblies 2005a and 2005b, respectively) provided on a passive component assembly 1905 (in particular, the passive component assembly 1905b) in an AMBPM configuration, where the die 210 is on a surface 314 of the interconnect structure or circuitry module 310" opposite the surface 312 having the passive electrical components 1750 thereon. The packages 2300a and 2300b are implemented as an open-air or open-cavity package.

[00326] As shown in FIGS. 23A and 23B, the packages 2300a and 2300b may include a carrier substrate (e.g., thermally conductive substrate 410), sidewalls 2320, and a lid 2325. The substrate 410, sidewalls 2320, and lid 2325 may define an internal cavity 2330. The active component assembly 2005 and the passive component assembly 1905 are disposed inside the internal cavity 2330, and may be enclosed in and protected by the sidewalls 2320 and the lid 2325. The sidewalls 2320 may provide mechanical support for the leads 415A, 415B, which are electrically connected to the exposed interconnection pads 372, 374 by wirebond connections 2115. In some embodiments, the passive component assembly 1905 may include the passive electrical components 1750 pre-assembled in a mold structure 2240 on the first surface 312 of the circuitry module 310". As such, the packages 2300a, 2300b may include characteristics of both molded and open-cavity packages. The example packages 2300a and 2300b of FIG. 23A and 23B may include other components or may otherwise be similar to wirebond-to-lead packages 2100, 2200 described herein.

[00327] FIG. 24A is a schematic cross-sectional view and FIG. 24B is a schematic plan view of a semiconductor package 2400 including an active component assembly 2005 (e.g., the active component assembly 2005a) provided on a passive component assembly 1905 (e.g., the passive component assembly 1905b) in an AMBPM configuration, where the die 210 is on a surface 314 of the interconnect structure or circuitry module 310" opposite the surface 312 having the passive electrical components 1750 thereon. In some embodiments, the passive component assembly 1905 may include the passive electrical components 1750 pre-assembled in a mold structure 2240 on the first surface 312 of the circuitry module 310".

[00328] The package 2400 further includes one or more mechanical support structures 2000s on the second surface 314 of the circuitry module 310" adjacent the die 210. The mechanical support structure(s) 2000s (also referred to herein as a standoff assembly 2000s) extend

between the substrate (e.g., the thermally conductive flange 410) and the second surface 314 of the circuitry module 310". The mechanical support structure(s) 2000s may extend along or adjacent one or more sides of the die 210, and may have a thickness substantially similar to a thickness of the active component assembly 2005, and can provide improved mechanical support for the passive component assembly 1905 stacked thereon. In some embodiments, the mechanical support structure(s) 2000s may be formed of one or more materials that may improve thermal conduction, e.g., to conduct heat away from the active component assembly 2005 and/or the passive component assembly 1905 and toward the thermally conductive substrate 410. An overmold material 1740 is subsequently formed to encapsulate the active and passive component assemblies 2005 and 1905 in the package 2400.

[00329] FIG. 24C is a schematic cross-sectional view of a semiconductor package 2400' including an active component assembly 2005 (e.g., the active component assembly 2005a) provided on a passive component assembly 1905 (e.g., the passive component assembly 1905c) in an AMBPM configuration, where the die 210 is on a surface 314 of the interconnect structure or circuitry module 310" opposite the surface 312 having the passive electrical components 1750 thereon. The package 2400' is similar to the package 2400 of (including the mechanical support structure(s) 2000s between the flange 410 and the second surface 314 of the circuitry module 310"), but with the package leads 415A and 415B implemented on the circuitry module 310" itself (rather than coupled to the passive component assembly module 1905 by wirebond connections).

[00330] Although illustrated in FIGS. 24A to 24C as an overmold package 2400 including an overmold material 1740 by way of example, the packages 2400, 2400' may be implemented as an open-air or open-cavity package in some embodiments, as shown in FIG. 24D. In particular, FIG. 24D is a schematic cross-sectional view of an open-cavity package 2400" in which the package leads 415A and 415B are implemented on the circuitry module 310" (rather than coupled to the passive component assembly module 1905 by wirebond connections) The open-cavity package 2400" is otherwise similar to the package 2400' of FIG. 24C (including the mechanical support structure(s) 2000s between the flange 410 and the second surface 314 of the circuitry module 310"), but with the active component assembly 2005 and the passive component assembly 1905 disposed inside an internal air cavity 2330 and enclosed in and protected by sidewalls 2320 and a lid 2325.

[00331] The example packages 2400, 2400', 2400" of FIGS. 24A to 24D may include other components or may otherwise be similar to wirebond-to-lead packages 2100, 2200, 2300a, 2300b described herein.

[00332] FIGS. 25A, 25B, and 25C illustrate various example packages for RF transistor amplifiers in AMBPM configurations according to some embodiments of the present invention. In particular, FIGS. 25A, 25B, and 25C are schematic cross-sectional views of semiconductor packages 2500a, 2500b, and 2500c including an active component assembly 2005 (in particular, the active component assembly 2005a in FIGS. 25A and 25B, and the active component assembly 2005b in FIG. 25C) provided on a passive component assembly 1905 (in particular, the passive component assembly 1905b) in an AMBPM configuration, where the die 210 is on a surface 314 of the interconnect structure or circuitry module 310" opposite the surface 312 having the passive electrical components 1750 thereon. The description of FIGS. 25A-25C will focus on elements of the RF transistor amplifier that may differ from those previously described in detail above.

[00333] The examples of FIGS. 25A to 25C include package leads 415A and 415B that are directly mounted on the passive component assembly 1905, that is, without wirebond connections. For instance, FIG. 25A illustrates an example package 2500a in which the leads 415A, 415B are mounted on the second surface 314 of the circuitry module 310" of the passive component assembly 1905, adjacent the active component assembly 2005. FIG. 25B illustrates an example package 2500b in which the leads 415A, 415B are mounted on the first surface 312 of the circuitry module 310" of the passive component assembly 1905, adjacent the passive electrical components 1750. FIG. 25C illustrates an example package 2500c in which the leads 415A, 415B are mounted on the second surface 314 of the circuitry module 310" adjacent the active component assembly 2005, which includes the die 210 and a coupling element 270 in an RDL package.

[00334] In FIGS. 25A to 25C, the passive component assembly 1905 includes the passive electrical components 1750 pre-assembled in a mold structure 2240 on the first surface 312 of the circuitry module 310", but it will be understood that the mold structure 2240 may be omitted in some embodiments. Likewise, the packages 2500a, 2500b, 2500c are illustrated as overmold packages including an overmold material 1740 by way of example, but may be implemented as open-air or open-cavity packages in some embodiments. The example package 2500a, 2500b, 2500c of FIGS. 25A to 25C may include other components or may otherwise be similar to the package 1800 described herein.

[00335] More generally, embodiments of the present invention may include any combination of the active component assemblies shown in FIGS. 20A to 20C and the passive component assemblies shown in FIGS. 19A to 19C, and are not limited to the examples specifically shown in the figures. Such combinations of active and passive component assemblies may be

used to provide various electronic capabilities to the RF transistor amplifier 200. For example, the circuit elements 1750a, 1750b, 1750c may implement impedances (including, for example, resistive, inductive, and capacitive elements) that may be used for impedance matching and/or harmonic termination. As noted above, the circuit elements 1750a, 1750b, 1750c may be or may include surface mount devices, IPDs, and/or other passive electrical components, and may implement harmonic and/or input/output impedance matching elements.

[00336] FIGS. 26A, 26B, and 26C are schematic circuit diagrams illustrating various circuit topologies that may be implemented by combinations of active and passive component assemblies according to some embodiments of the present invention. For example, the circuit elements 1750a, 1750c may be configured to provide input impedance matching capabilities. Due to coupling between the input lead 415A and the transistor die 210, the circuit elements 1750a, 1750c may be capable of affecting and/or conditioning a signal provided to the gate terminals of the transistor die 210. Similarly, the circuit element 1750b, 1750c may be configured to provide output impedance matching capabilities. Due to coupling between the output lead 415B and the transistor die 210, the circuit elements 1750b, 1750c may be capable of affecting and/or conditioning a signal provided from the drain terminal of the transistor die 210. More generally, the circuit elements 1750 may be configured to provide input impedance matching circuitry, output impedance matching circuitry, and/or harmonic termination circuitry for packaged transistor amplifiers as described herein.

[00337] The passive component assemblies 1905 can allow for ease of assembly of RF transistor amplifier packages with different characteristics and/or additional functionality, such as impedance matching and/or harmonic termination. For example, by providing passive component assemblies 1905 including circuitry modules 310" with exposed interconnection pads, one or more of the circuit elements 1750a, 1750b, 1750c can be replaced and/or configured to provide application-specific impedance characteristics. That is, transistor packages may be designed and/or reconfigured to provide different input/output matching and/or harmonic termination characteristics using the same circuitry module 310" populated with different arrangements and/or combinations of the passive electronic components 1750 on the exposed interconnection pads 322, 324, 326, 372, 374, 376. Thus, different functionality and/or capability may be coupled to an RF transistor amplifier 200 of an active component assembly 2005 simply by using a different passive component assembly 1905 and/or differently populating the passive component assembly 1905 with different combinations and/or arrangements of passive electrical components 1750.

[00338] In still further embodiments, the interconnect structure and the active and/or passive electrical components on one or more surfaces thereof (e.g., a combination of the active component assembly 2005 and passive component assembly 1905 described above) may collectively implement a flip-chip module or component assembly (e.g., 2905 herein). In a flip-chip component assembly, the active transistor die(s) and any conductive structures (e.g., pillars or coupling elements thereon) may be coupled to the interconnect structure (e.g., a PCB or other substrate with conductive interconnection patterns) by flip chip connection, that is, with the gate terminal, the drain terminal, and the source terminal of the die(s) facing the surface of the interconnect structure. This provides the possibility to add and connect matching components (e.g., base band termination capacitors, matching networks, etc.) in close proximity to the transistor die(s). The flip-chip modules or component assemblies described herein may be electrically tested and screened before integration with the remainder of the packaging, which may improve yield and reduce costs. The flip-chip module may be assembled into high power packages that include a thermally conductive flange (e.g., a Cu-based or other solid metal coin) to be able to dissipate heat out of the device package. The thermally conductive flange may be soldered or bonded to a customer heat sink in some applications.

[00339] In contrast, some conventional high power applications may typically attach one or more transistor dies onto a heat sink with the source facing down, and with chip- and-wire connections to implement matching networks, termination, etc. Also, while some conventional flip-chip implementations may have power limitations due to thermal management issues (as heat may be required to be dissipated through the PCB on which the transistor die is attached), embodiments of the present invention may reorient the flip-chip module for assembly into high power packages by placing the back surface of the transistor die facing the thermally conductive flange (i.e., by rotating the flip-chip component assembly by 180 degrees), and attached "upside-down" to the conductive flange using a thermally and electrically conductive adhesive (e.g., solder, conductive epoxies or silver and copper nanoparticle materials).

[00340] In particular, a transistor device package according to further embodiments of the present invention includes a component assembly that is rotated (or "flipped") 180 degrees and integrated into the package such that the back surface 214 of the transistor die 210 is attached to a thermally conductive flange 410 by a conductive adhesive 240". The component assembly includes an interconnect structure 310", a transistor die, and one or more passive electrical components 1750. The front surface 212 of the transistor die 210

includes a gate terminal 222", a drain terminal 224", and a source terminal 226" attached to a first surface 312 of the interconnect structure 310" (i.e. in a flip-chip configuration. The passive electrical component(s) may be on the first surface 312 and/or on an opposing second surface 314 of the interconnect structure 310", and may be electrically coupled to the gate, drain, and/or source terminal 222", 224", and/or 226" by the interconnect structure 310". For example, the interconnect structure 310" may be a multi-layer structure including conductive patterns (including conductive pads and traces) and/or vias that electrically couple the one or more passive electrical components 1750 to the gate terminal 222", drain terminal 224", and/or source terminal 226" of the transistor die, which are on the first surface 312 of the interconnect structure 310". The passive electrical components 1750 may include surface mount devices (SMDs) and/or integrated passive devices (IPDs), and may be attached to respective conductive patterns (e.g., interconnection pads 372, 374, 376) on one or more surfaces 312, 314 of the interconnect structure 310", in surface mount, wirebond, and/or flip-chip configurations.

[00341] In addition, as shown in greater detail in FIGS. 27A to 34D, the transistor device package includes patterns 240p of conductive adhesive 240" (e.g., drops or other dispensed portions of the conductive adhesive material) provided on the interconnect structure 310", for example, adjacent the transistor die 210 on the first surface 312. The conductive adhesive patterns 240p mechanically couple the interconnect structure 310" to one or more components of the transistor device package (e.g., the conductive leads 415A, 415B and/or the thermally conductive flange 410). Also, one or more of the conductive adhesive patterns 240p may electrically couple the gate, drain, or source terminals of the transistor die 210 to one or more components of the transistor device package (e.g., the conductive leads 415A, 415B and/or the thermally conductive flange 410) so as to provide an input, output, or ground signal path for the transistor device package. In addition, as noted above, the conductive adhesive 240" on the back surface 214 of the transistor die 210 thermally couples the die to the thermally conductive flange 410. As such, the conductive adhesive patterns 240p described herein may be used to integrate component assemblies into a desired transistor device package form factor, and may provide (i) mechanical coupling, (ii) thermal coupling, and/or (iii) electrical coupling between components of the package.

[00342] FIGS. 27A and 27B are schematic cross-sectional views of transistor device packages 2700a, 2700b including flip-chip component assemblies 2905 integrated into high power package types according to some embodiments of the present invention. In particular, FIGS. 27A and 27B illustrate a double-sided component assembly 2905, with passive

electrical components 1750 on opposing first and second surfaces 312 and 314 of an interconnect structure 310", and a transistor die 210 mounted in a flip-chip configuration on one of the opposing first and second surfaces 312 and 314. The component assembly 2905 (also referred to as a flip chip module) is attached "upside down" on a thermally conductive flange 410 (i.e., with the back surface 214 of the transistor die 210 attached to the surface of the flange 410) by a conductive adhesive 240", such as a silver (Ag) nanoparticle sintering material (also referred to herein as Ag nano) , conductive epoxy or a solder material. A heat dissipation path is thus provided at the bottom of the package 2700a, 2700b through the flange 410, whereas the input and output signal paths are provided by the conductive leads 415A, 415B protruding from the package housing 278.

[00343] Also, as shown in FIGS. 27A and 27B, the respective patterns 240p of the conductive adhesive 240" may attach and electrically connect the conductive leads 415A, 415B to the first surface 312 of interconnect structure 310", and in particular, to conductive patterns (e.g., exposed interconnection pads 322/382, 324/384, 326) on the first surface 312 that are electrically coupled to the gate 222" and drain terminals 224" (as shown in FIGS. 27A and 27B) and/or to the source terminal 226" (as shown in FIG. 29A) of the transistor die to provide input RF signals, RF output signals, and/or ground signals to/from the transistor die 210. As such, the conductive adhesive patterns 240p may provide at least a portion of the input, output, and/or ground signal paths between the conductive leads 415A, 415B and the gate, drain, and/or terminals of the transistor die. It will be understood that the leads 415A, 415B may be mounted on the opposite surface (e.g., on the second surface 314) than the die 210 in some embodiments.

[00344] Additionally or alternatively, the respective patterns 240p of the conductive adhesive 240" may attach and electrically connect the thermally conductive flange 410 to the first surface 312 of the interconnect structure 310", and in particular, to conductive patterns on the first surface 312 that are electrically coupled to the source terminal 226" of the transistor die. For example, the thermally conductive flange 410 may include one or more conductive pillar portions 2410 protruding from a surface thereof, which may be attached to the first surface 312 of the interconnect structure 310" and electrically coupled to the conductive pads thereon by respective conductive adhesive patterns 240p (as shown in FIGS. 28 and 29B). As such, the conductive adhesive patterns 240p may provide at least a portion of a ground signal path between the thermally conductive flange 410 and the source terminal 226" of the transistor die. In some embodiments, the electrical connections between the terminals of the transistor die(s) 210, the passive electrical component(s), the input and output leads, and the thermally

conductive flange 410 may be implemented such that the package 2700a, 2700b is free of wire bond connections.

[00345] The passive electrical components 1750 may be provided on the first surface 312 of the interconnect structure 310" (i.e., on the surface adjacent the transistor die(s) 210), on a second surface 314 of the interconnect structure 310" (i.e., opposite the surface having the transistor die(s) 210 thereon), or on both the first surface 312 and the second surface 314 of the interconnect structure 310". As shown in FIG. 27A, in some embodiments, one or more of the passive electrical components 1750 may be arranged on a portion of the second surface 314 of the interconnect structure 310" that overlaps with the transistor die 210 on the first surface 312. Such an arrangement can provide the passive electrical component(s) in closer proximity to the transistor die(s) 210, thereby reducing and/or minimizing lengths of electrical connections therebetween. For example, providing a transistor die 210 and its base band termination and/or matching circuitry on directly opposing surfaces of the interconnect structure 310" may provide extremely low impedances (and low impedance variability) therebetween, which may be critical to achieving and maintaining desired performance at higher frequencies.

[00346] In FIGS. 27A and 27B, an encapsulating material (such as an overmold material 1740) is provided on the interconnect structure 310", the transistor die, and the thermally conductive flange 410 to form a mold structure 2240. The conductive leads 415A, 415B may protrude outside the mold structure 2240 and beyond a periphery of the package housing 278. In FIG. 27A, the conductive leads 415A, 415B are substantially planar structures that are spaced apart from the thermally conductive flange 410 by a uniform distance inside and outside the periphery of the package housing 278 as defined by the mold structure 2240.

[00347] In contrast, in FIG. 27B, the conductive leads 415A, 415B include portions that are bent (e.g., towards or away from the first surface 312 of the interconnect structure) inside the package housing 278 so as to accommodate for height differences of the transistor dies, while exiting the package 2700b at a height or level H that corresponds to other standardized packages or to otherwise meet customer demand. In particular, the conductive leads 415A, 415B (e.g., input and/or output RF leads) may include first portions 415Ai, 415Bi that overlap the surface of the flange 410 and are separated therefrom by a first spacing or gap G1, and second portions 415Ae, 415Be that extend beyond the surface of the flange 410 and are separated or spaced apart from the plane of the surface of the flange 410 by a second spacing or gap G2 that is different than the first spacing or gap G1.

[00348] FIGS. 28A and 28B are flow diagrams illustrating example operations for fabricating transistor device packages according to some embodiments. In particular, FIGS. 28A and 28B illustrate a method of providing a component assembly 2905 (including an interconnect structure 310", a transistor die, and one or more passive electrical components 1750 electrically coupled to the gate terminal 222" and/or the drain terminal 224" of the transistor die 210 by the interconnect structure), and attaching a back surface 214 of the transistor die 210 to a thermally conductive flange 410 by a conductive adhesive 240" as shown in FIGS. 27A or 27B. However, it will be understood that the operations shown in FIGS. 28A and 28B are not limited to fabricating the packages 2700a, 2700b of FIGS. 27A or 27B.

[00349] As shown in FIGS. 28A and 28B, solder or other electrically conductive bonding material is provided on a first surface 312 of the interconnect structure 310", e.g. using a printing process, at block 2805. The interconnect structure 310" may be a multi-layer structure including conductive pads, traces, and/or vias that extend on or between opposing first and second surfaces 312 and 314. At block 2810, transistor dies and passive electrical components 1750 are attached and electrically connected to the conductive patterns on the first surface 312 of the interconnect structure 310" by the bonding material (e.g., using a solder reflow process), also referred to as populating the interconnect structure 310". The transistor dies are attached to the interconnect structure 310" in a flip-chip manner, that is, with the gate, drain, and source terminals facing the first surface 312 and electrically connected to the conductive patterns thereon. The passive electrical components 1750 (such as SMDs and/or IPDs) are similarly attached to the first surface 312 and electrically connected to conductive patterns, such that the passive electrical components 1750 are electrically coupled to the gate terminal 222", drain terminal 224", and/or source terminal 226" of the transistor dies on the first surface 312 thereof.

[00350] At block 2815, the populated interconnect structures 310" are singulated, for example, using a sawing or dicing process, to provide a plurality of individual component assemblies 2905. Each component assembly 2905 may include an interconnect structure 310", one or more transistor dies, and one or more passive electrical components 1750 electrically connected to gate, drain, and/or source terminals 222", 224", and/or 226" of the transistor die 210 by the interconnect structure 310". The individual component assemblies 2905 may be electrically tested (and defective component assemblies 2905 may be repaired or discarded) before performing the remaining packaging operations, thereby improving the yield of the packaged device which may contain multiple of those component assemblies.

[00351] At block 2820, a conductive adhesive 240" (for example, solder or Ag nano), may be dispensed to provide respective patterns 240p of the conductive adhesive 240" on one or more surfaces of a thermally conductive flange 410 (for example, a Cu coin) of the package 2700a, 2700b. The conductive adhesive patterns 240p may also be dispensed on surfaces of one or more conductive leads 415A, 415B of the package 2700a, 2700b. In some embodiments, one or more of the conductive leads 415A, 415B may be bent so as to accommodate for height differences of the transistor dies, while exiting the package at a height or level that corresponds to other standardized packages. In some embodiments, the thermally conductive flange 410 may include one or more conductive pillar portions (e.g., extruded Cu pillar) protruding from a surface thereof, and the conductive adhesive patterns 240p may be dispensed on respective surfaces of the protruding conductive pillar(s).

[00352] At block 2825, the component assembly 2905 is rotated (or "flipped") such that the first surface 312 of the interconnect structure 310" (including the transistor die(s) 210 and the passive electrical component(s) thereon) faces the thermally conductive flange 410, and the component assembly 2905 is attached to thermally conductive flange 410 and the conductive leads 415A, 415B by the respective patterns 240p of the conductive adhesive 240" (e.g., using a sintering or other attachment process). In particular, a back surface 214 of one or more of the transistor dies is attached to the surface of the thermally conductive flange 410 by patterns 240p of the conductive adhesive 240", and the conductive leads 415A, 415B are attached to the first surface 312 of the interconnect structure 310" by patterns 240p of the conductive adhesive 240". The conductive leads 415A, 415B may be held in place or supported by one or more support members or other support tooling during the attachment process. For example, the support members can be retractable support members, which may be extended between the one or more conductive leads 415A, 415B and the thermally conductive flange 410 to support the one or more conductive leads 415A, 415B during the attachment process, and may be retracted after the attachment process.

[00353] The conductive leads 415A, 415B may thereby be mechanically attached and electrically connected to the interconnect structure 310" by the conductive adhesive patterns 240p, such that one or more of the conductive adhesive patterns 240p provide portions of input, output, and/or ground signal paths for the transistor device package 2700a, 2700b. For example, the conductive leads 415A, 415B may include input and output leads for the package 2700a, 2700b, and may be mechanically attached to the first surface 312 of the interconnect structure 310" and may be electrically connected to conductive pads on the first surface 312 (which are coupled to the gate 222" and drain terminals 224" of the transistor

die(s) 210) by the respective patterns 240p of the conductive adhesive 240" to provide the input and output signal paths. In some embodiments (e.g., as shown in FIG. 29A), the conductive leads 415A, 415B may further include ground leads for the package 2700a, 2700b, which may be mechanically attached to the first surface 312 of the interconnect structure 310" and may be electrically connected to conductive pads on the first surface 312 (which are coupled to the source terminal 226" of the transistor die(s) 210) by the respective patterns 240p of the conductive adhesive 240" to provide the ground signal path. In other embodiments (e.g., as shown in FIG. 29B), the one or more conductive pillar structures 2410 protruding from the surface of the thermally conductive flange 410 may be mechanically attached to the first surface 312 of the interconnect structure 310" and may be electrically connected to conductive pads on the first surface 312 (which are coupled to the source terminal 226" of the transistor die(s) 210) by the respective patterns 240p of the conductive adhesive 240" to provide the ground signal path.

[00354] As shown at (optional) block 2830, solder or other electrically conductive bonding material may be provided on an opposing second surface 314 of the interconnect structure 310", and one or more passive electrical components 1750 may be attached to the second surface 314 and electrically connected to conductive patterns such that the passive electrical components 1750 are electrically coupled to the gate terminal 222", drain terminal 224", and/or source terminal 226" of the transistor dies on the first surface 312 thereof. In some embodiments, the passive electrical component(s) may be on portions of the second surface 314 that overlap with the transistor die(s) 210 on the first surface 312, to reduce or minimize the distances or lengths of electrical connections therebetween. In some embodiments, the first surface 312 of the interconnect structure 310" may be free of passive electrical components 1750, such that the first surface 312 includes only one or more transistor dies thereon, and the second surface 314 includes only one or more passive components thereon. That is, the component assembly 2905 may be a passive component assembly (e.g., 1905) as described herein, which may be assembled with an active component assembly (e.g., 2005) described herein for integration into a transistor device package 2700a, 2700b. As shown at (optional) block 2835, in some embodiments, one or more wire bonds 282 may be attached (e.g., to the second surface 314) to provide additional electrical connections. In other embodiments, the packages 2700a, 2700b may be free of wire bond connections.

[00355] At block 2840, a package housing 278 is formed on the component assembly 2905 to complete the transistor device package 2700a, 2700b. In particular, an encapsulating material 625 (such as an overmold material 1740) is formed on surfaces of the interconnect structure

310", the transistor die(s) 210, and the thermally conductive flange 410 to form a mold structure 2240. The overmold material 1740 may be a highly silica or other inorganic materials filled plastic or a plastic polymer compound in some embodiments. The mold structure 2240 may provide a package housing 278 for environmental protection of the component assembly 2905. The conductive leads 415A, 415B may protrude beyond or outside a periphery of the package housing 278 defined by the mold structure 2240, and the bottom surface of the thermally conductive flange 410 may be exposed by the mold structure 2240 to provide a heat dissipation path at the bottom of the package 2700a, 2700b. Alternatively, a lid member 2325 may be provided as the package housing 278, instead of (or in addition to) the encapsulating material. As shown at block 2840, in embodiments where the flange 410 includes one or more extruded pillar portions that provide conductive ground pins, the bottom surface of the flange 410 may include recesses 410r at locations on the bottom surface that correspond to the locations of the extruded pillar portions 2410 on the opposing surface of the flange 410.

[00356] FIGS. 29A and 29B are schematic plan views illustrating example implementations of ground signal paths for transistor device packages according to some embodiments of the present invention. FIG. 29A illustrates implementation of ground signal paths using ground-signal-ground (GSG) leads as the conductive leads 415A, 415B. In particular, the input leads 415A each include an input conductor 415Ain between two ground conductors 415Ag, which are attached and electrically connected by conductive adhesive patterns 240p to respective conductive patterns on the first or second surface 312 or 314 of the interconnect structure 310", where the middle conductive pattern is electrically coupled to the gate terminal 222" of the transistor die. Similarly, the output leads 415B each include an output conductor 415Bout between two ground conductors 415Bg, which are attached and electrically connected by conductive adhesive patterns 240p to respective conductive patterns on the first or second surface 312 or 314 of the interconnect structure 310", where the middle conductive pattern is electrically coupled to the drain terminal 224" of the transistor die. FIG. 29B illustrates implementation of ground signal paths using ground conductive pads 386' on the first surface 312 of the interconnect structure 310", for attachment and electrical connection by the conductive adhesive patterns 240p to conductive pillar structures (as described below with reference to FIG. 30B) or other conductive support structures to provide electrical ground signal paths between the source terminal 226" of the transistor die(s) 210 and the thermally conductive flange 410.

[00357] FIGS. 30A and 30B are schematic cross-sectional views of transistor device packages 3000a, 3000b including flip-chip component assemblies 2905 with package leads provided by the interconnect structure 310" and integrated into high power package types according to some embodiments of the present invention. In particular, FIGS. 30A and 30B illustrate a double-sided component assembly 2905 (with passive electrical components 1750 on opposing first and second surfaces 312 and 314 of an interconnect structure 310", and a transistor die 210 mounted in a flip-chip configuration on one of the opposing first and second surfaces 312 and 314), where the conductive leads 415A, 415B are integrated in portions of the interconnect structure 310" that protrude outside a periphery of the package housing 278. Similar to the packages 2700a, 2700b of FIGS. 27A and 27B, the interconnect structure 310" is attached upside down on a thermally conductive flange 410, with the back surface 214 of the transistor die 210 attached to the surface of the flange 410 by a conductive adhesive 240" (e.g., Ag or Cu nano, conductive epoxies or solder). A heat dissipation path is thus provided at the bottom of the package through the flange 410, whereas the input and output signal paths are provided by the conductive leads 415A, 415B that are integrated in portions of the interconnect structure 310" protruding from the package housing 278. FIG. 30A illustrates an example package 3000a including components on both sides of the interconnect structure 310" encased in a mold structure 2240 as the package housing 278, while FIG. 30B illustrates an example package 3000b including components on one surface (e.g., 312) encased in an overmold material 1740, with components on the other surface (e.g., 314) covered by a lid member 2325. As such, the package 3000b may include characteristics of both molded and open-cavity packages.

[00358] Also, as shown in FIGS. 30A and 30B, one or more support structures 2000s extend from the thermally conductive flange 410 to the first surface 312 of the interconnect structure 310", and are attached to one or more areas of the first surface 312 of the interconnect structure 310" by respective patterns 240p of the conductive adhesive 240". In some embodiments, the support structure(s) 2410 may include a conductive component or may otherwise be formed of an electrically conductive material. For example, one or more of such conductive support structures 2410 may be electrically connected to the source terminal 226" of the transistor die 210 by the interconnect structure 310", and thus, may function as a ground pin that electrically couples the source terminal 226" of the transistor die 210 to the thermally conductive flange 410.

[00359] In some embodiments, the support structure(s) may include conductive pillar portions of the thermally conductive flange 410 that protrude from the surface from the

flange 410 to the first surface 312 of the interconnect structure 310". For example, as shown in FIG. 30B, the conductive pillar structures 2410 may be extruded from or may otherwise be integral to the thermally conductive flange 410. In particular, an extrusion process may be used to form the conductive pillar structures 2410 as protrusions that extend from a surface of the thermally conductive flange 410, (e.g., Cu pillars that are extruded from the surface of a Cu flange 410), leaving recesses 410r in the surface of the flange 410 at positions corresponding the positions of the extruded conductive pillar portions 2410 on the opposing surface of the flange 410. The respective patterns 240p of the conductive adhesive 240" may attach and electrically connect the conductive pillar structures 2410 of the flange 410 to the conductive patterns on the first surface 312 of the interconnect structure 310", such that the conductive adhesive patterns 240p may provide at least a portion of an electrical ground signal path between the transistor die(s) 210 on the first surface 312 of the interconnect structure 310" and the flange 410.

[00360] FIGS. 31A and 31B are flow diagrams illustrating example operations for fabricating transistor device packages according to some embodiments. In particular, FIGS. 31A and 31B illustrate a method of providing a component assembly 2905 (including an interconnect structure 310", a transistor die, and one or more passive electrical components 1750 electrically coupled to the gate terminal 222" and/or the drain terminal 224" of the transistor die 210 by the interconnect structure), and attaching a back surface 214 of the transistor die 210 to a thermally conductive flange 410 by a conductive adhesive 240" as shown in FIGS. 30A or 30B. However, it will be understood that the operations shown in FIGS. 31A and 31B are not limited to fabricating the packages 3000a, 3000b of FIGS. 30A or 30B.

[00361] As shown in FIGS. 31A and 31B, solder or other electrically conductive bonding material is provided on a first surface 312 of the interconnect structure 310", e.g. using a printing process, at block 310"5. At block 3110, the interconnect structure 310" is populated by attaching and electrically connecting transistor dies and passive electrical components 1750 to the conductive patterns on the first surface 312 of the interconnect structure 310" by the bonding material (e.g., using a solder reflow process). The transistor dies are attached to the interconnect structure 310" in a flip-chip manner, and the passive electrical components 1750 are similarly attached to the first surface 312 and electrically connected to conductive patterns such that the passive electrical components 1750 are electrically coupled to the gate terminal 222", drain terminal 224", and/or source terminal 226" of the transistor dies on the first surface 312 thereof. At block 3115, the populated interconnect structures 310" are singulated, for example, using a sawing or dicing process, to provide a plurality of individual

component assemblies 2905, which may be electrically tested before performing the remaining packaging operations.

[00362] At block 3120, a conductive adhesive 240" (for example, solder or Ag nano), may be dispensed to provide respective patterns 240p of the conductive adhesive 240" on respective areas of the first surface 312 of the interconnect structure 310", and on back surfaces 214 of the transistor die(s) 210, in each component assembly 2905. Also, a thermally conductive flange 410 is provided for each component assembly 2905. The flange 410 includes conductive support structures 2410 (for example, conductive pillar structures 2410) that protrude from a surface thereof. The conductive pillar structures 2410 may be extruded from or may otherwise be integral to the thermally conductive flange 410.

[00363] At block 3125, each component assembly 2905 is attached to a respective thermally conductive flange 410 by the conductive adhesive 240" (e.g., using a sintering or other attachment process). In particular, a back surface 214 of one or more of the transistor dies is attached to the surface of the thermally conductive flange 410 by the conductive adhesive 240" thereon, and the conductive pillar structures 2410 protruding from the thermally conductive flange 410 are attached to the respective areas of the first surface 312 of the interconnect structure 310" by the conductive adhesive patterns 240p thereon. The respective patterns 240p of the conductive adhesive 240" may provide a ground signal path for the transistor device package 3000a, 3000b. For example, the conductive pillar portions protruding from the surface of the thermally conductive flange 410 may be mechanically attached to the first surface 312 of the interconnect structure 310" and may be electrically connected to conductive pads on the first surface 312 (which are coupled to the source terminal 226" of the transistor die(s) 210) by the respective patterns 240p of the conductive adhesive 240" to provide portions of the ground signal path between the source terminal 226" of the transistor die(s) 210 and the thermally conductive flange 410.

[00364] As shown at block 3130, after attachment of the flange 410 to the first surface 312 of the interconnect structure 310", the assembly is rotated or flipped by 180 degrees. As shown at (optional) block 3135, solder or other electrically conductive bonding material may be provided on an opposing second surface 314 of the interconnect structure 310", and one or more passive electrical components 1750 may be attached to the second surface 314 and electrically connected to conductive patterns such that the passive electrical components 1750 are electrically coupled to the gate terminal 222", drain terminal 224", and/or source terminal 226" of the transistor dies on the first surface 312 thereof. In some embodiments, the passive electrical component(s) may be on portions of the second surface 314 that overlap with the

transistor die(s) 210 on the first surface 312, to reduce or minimize the distances or lengths of electrical connections therebetween. In some embodiments, the first surface 312 may be free of passive electrical components 1750. In some embodiments, one or more wire bonds may be attached to provide additional electrical connections. In other embodiments, the packages 3000a, 3000b may be free of wire bond connections.

[00365] At block 3140, a package housing 278 is formed on the component assembly 2905 to complete the transistor device package 3000a, 3000b. In particular, an encapsulating material 625 (such as an overmold material 1740) is formed on surfaces of the interconnect structure 310", the transistor die(s) 210, and the thermally conductive flange 410 to form a mold structure 2240. The overmold material 1740 may be a highly silica or other inorganic materials filled plastic or a plastic polymer compound and may provide a package housing 278 for environmental protection of the component assembly 2905. The interconnect structure 310" may protrude beyond or outside a periphery of the package housing 278 defined by the mold structure 2240. Portions of the interconnect structure 310" that are outside the package housing 278 may include conductive leads 415A, 415B (e.g., input and/or output leads) integrated therein, for example, as implemented by exposed contact patterns on portions of the first and/or second surfaces 312 and/or 314 of the interconnect structure 310" that are outside the mold structure 2240. The bottom surface of the thermally conductive flange 410 may be exposed by the mold structure 2240 to provide a heat dissipation path at the bottom of the package 3000a, 3000b. Additionally or alternatively, as shown in FIG. 30B, a lid member 2325 may be provided as part of the package housing 278 (i.e., instead of or in addition to the encapsulating material 1740).

[00366] While described above with reference to singulating arrays 310a of populated interconnect structures 310" into individual component assemblies 2905 prior to integrating the component assemblies 2905 into respective transistor device packages (each including a respective thermally conductive flange 410 and package housing 278), FIGS. 32A to 32C illustrate that further operations for fabricating the transistor device packages 3000a, 3000b can be performed with the array format. In particular, FIGS. 32A and 32B illustrate that, in some embodiments, rather than performing the singulation operation at block 3115 before attachment of the flange 410 at block 3125 of FIG. 31, an array 310a including multiple interconnect structures 310" (collectively referred to as an interconnect array 310a) may be provided with dicing or snapping lines delineating boundaries of respective interconnect structures 310", and a plurality of flanges 410 may be attached to the respective interconnect structures 310" to form an array of component assemblies 2905 before performing the

singulation operation. As shown in FIG. 32B, in some embodiments, the interconnect array 310a may include one or more slots therein that are sized and/or otherwise configured to accept a clamping device used during the molding process. As shown in FIG. 32C, the clamping device is configured to clamp the thermally conductive flange 410 to the bottom of the mold chase during the molding. Conductive pillars 2410, in some embodiments extruded from the flange material itself, may be used to provide stability and the proper spacing between the conductive flange 410 and the interconnect structure 310. That is, the attachment of the interconnect structure 310" to the flange 410 as shown at block 3125 of FIG. 31 may be performed before the singulation operation shown at block 3115 in some embodiments. Likewise, the attachment of the passive electrical components 1750 at (optional) block 3135 and/or the forming of the package housing 278 shown at block 3140 may be performed before the singulation operation shown at block 3115 in some embodiments. The slots may include edge plating to improve solderability at the edges. Also, as shown in FIG. 32D, portions of the package housing 278 (e.g., the mold structure 2240) may include respective recess features 3240 along one or more edges, where each recess feature 3240 has a dimension corresponding to at least one dimension of the clamping device that was used to secure the flange 410 during formation of the housing 278.

[00367] FIG. 33 is a flow diagram illustrating example operations for fabricating transistor device packages (e.g., 3000a, 3000b) in array format (also referred to as in-strip manufacturing) according to some embodiments of the present invention. As shown in FIG. 33, solder or other electrically conductive bonding material is provided on a first surface 312 of an interconnect array 310a (e.g. using a printing process) at block 3305. The interconnect array 310a may include a plurality of interconnect structures 310" that are mechanically connected, in some embodiments including dicing or snapping lines that are configured for separation along boundaries between respective interconnect structures 310". At block 3310", passive electrical components 1750 are attached to the first surface 312 of the interconnect array 310a, and at block 3315, transistor dies are attached (e.g., in a flip chip manner) to the first surface 312 of the interconnect array 310a, thereby populating the respective interconnect structures 310". At block 3320, a reflow process is performed to attach and electrically connect the passive electrical components 1750 and the transistor dies to the conductive patterns on the first surface 312 of the interconnect array 310a by the bonding material, such that the passive electrical components 1750 are electrically coupled to respective gate terminals 222", drain terminals 224", and/or source terminals 226" of the transistor dies.

[00368] Still referring to FIG. 33, at block 3325, a conductive adhesive 240" (for example, solder or Ag nano), may be dispensed to provide respective patterns 240p of the conductive adhesive 240" on respective areas of the first surface 312 of the interconnect array 310a, and on back surfaces 214 of the transistor dies. At block 3330, a thermally conductive flange 410 is provided on each interconnect structure 310" of the interconnect array 310a. At block 3335, a sintering or other thermal process is performed to attach and electrically connect the thermally conductive flange 410 to conductive patterns on the respective interconnect structures 310" by the patterns 240p of conductive adhesive 240", such that the conductive adhesive patterns 240p may provide at least a portion of a ground signal path between the transistor die(s) 210 and a corresponding thermally conductive flange 410. At block 3340, a molding process is performed to encapsulate the transistor dies, the passive electrical components 1750, and the thermally conductive flanges 410 (e.g., using a single-side or double-side cavity molding process), and at block 3345, an exposure process (e.g., grinding or laser ablation) is performed to expose the bottom surface of each thermally conductive flange 410. A plating process (e.g., an Ag plating process) is performed at block 3350 (for example, to provide a metal plating on portions of conductive leads 415A, 415B that protrude outside the periphery of the package housing 278), and a laser marking process is performed at block 3355. The interconnect array 310a is mounted on tape at block 3360, and singulated (e.g., by dicing, sawing, laser ablation, etc.) at block 3365 to provide the respective transistor device packages 3000a, 3000b. In some embodiments, operations (for single-piece handling) may continue at block 3370 by transferring the respective transistor device packages 3000a, 3000b from the tape to a tray (e.g., using pick and place operations), performing electrical (e.g. RF and/or DC) testing at block 3375, performing a moisture removal process (e.g., baking) at block 3380, and transferring the respective transistor device packages 3000a, 3000b to tape or reel at block 3385.

[00369] FIGS. 34A to 34D are flow diagrams illustrating more specific operations for fabricating transistor device packages in array format with passive components on both top/first 312 and bottom/second 314 surfaces of the interconnect structure 310" according to some embodiments of the present invention. For example, the operations shown in FIGS. 34A to 34D are illustrated with reference to in-strip manufacturing processes to fabricate the transistor device package 3000a of FIG. 30A (with a mold structure 2240 providing at least part of the package housing 278) and the package 3000b of FIG. 30B (with a lid member 2325 providing at least part of the package housing 278). However, it will be understood that

the operations shown in FIGS. 34A to 34Dare not limited to fabricating the packages 3000a, 3000b of FIGS. 30A and 30B.

[00370] As shown in FIG. 34A, solder or other electrically conductive bonding material is provided on the second surface 314 of an interconnect array 310a (e.g., by performing a first printing process) at block 3405. As noted above, the interconnect array 310a may include a plurality of interconnect structures 310" that are mechanically connected, in some embodiments including dicing or snapping lines that are configured for separation along boundaries between respective interconnect structures 310". At block 3410, passive electrical components 1750 are attached to the second surface 314 of the interconnect array 310a, and at block 3415, a first reflow process is performed to attach and electrically connect the passive electrical components 1750 to the conductive patterns on the second surface 314 of the interconnect array 310a by the bonding material. As shown at (optional) block 3420, in some embodiments, one or more wire bonds may be attached to the second surface 314 to provide additional electrical connections. In other embodiments, the packages 3000a, 3000b may be free of wire bond connections.

[00371] As shown in FIG. 34B, at block 3425, one or more operations are performed to provide environmental protection for the passive electrical components 1750 on the second surface 314 of the interconnect array 310a. For example, in some embodiments, overmold, glob top, and/or dam-and-fill operations may be performed to encapsulate the passive electrical components 1750 of respective component assemblies 2905 on the second surface 314 of the interconnect array 310a. Additionally or alternatively, respective lid members 2325 (e.g., ceramic lids) may be provided on the second surface 314 of the interconnect array 310a to provide respective open cavities around the passive electrical components 1750 of respective component assemblies 2905. As such, an encapsulant material 1740 and/or a lid member 2325 may be formed on the passive electrical components 1750 of the respective component assemblies 2905 on the second surface 314 of the respective interconnect structures 310" thereof.

[00372] At block 3430, the interconnect array 310a is rotated or flipped, and solder or other electrically conductive bonding material is provided on the first surface 312 of the interconnect array 310a (e.g. by performing a second printing process). At block 3435, passive electrical components 1750 and transistor dies are attached (e.g., in a flip chip manner) to the first surface 312 of the interconnect array 310a, and a second reflow process is performed to attach and electrically connect the passive electrical components 1750 and the transistor dies to the conductive patterns on the first surface 312 of the interconnect array

310a by the bonding material, such that the passive electrical components 1750 on the first and/or second surfaces 312 and/or 314 are electrically coupled to respective gate terminals 222", drain terminals 224", and/or source terminals 226" of the transistor dies. In some embodiments, as noted above, one or more passive electrical components 1750 may be on portions of the second surface 314 that overlap with a transistor die 210 on the first surface 312, to reduce or minimize the distances or lengths of electrical connections therebetween.

[00373] Still referring to FIG. 34B, at block 3440, a conductive adhesive 240" (for example, solder or Ag nano), is dispensed to provide respective patterns 240p of conductive adhesive 240" on respective areas of the first surface 312 of the interconnect array 310a, and on back surfaces 214 of the transistor dies. As shown in FIG. 34C, at block 3445, a thermally conductive flange 410 is provided on the first surface 312 of each interconnect structure 310" of the interconnect array 310a, that is, on each component assembly 2905 for a respective transistor device package 3000a, 3000b. The flange 410 includes conductive pillar structures 2410 or other support structures that are extruded from (or otherwise integral to) the surface of the thermally conductive flange 410. The back surfaces 214 of the transistor die(s) 210 on each interconnect structure 310" contact the surface of the thermally conductive flange 410 (with the conductive adhesive 240" therebetween), and the conductive pillar structures 2410 protruding from the thermally conductive flange 410 contact the respective areas of the first surface 312 of a corresponding interconnect structure 310" (with the conductive adhesive patterns 240p therebetween). At block 3445, a sintering or other thermal process is performed to attach and electrically connect the conductive support structures 2410 of each thermally conductive flange 410 to conductive patterns on the respective interconnect structures 310" by the patterns 240p of conductive adhesive 240". The conductive pillar portions protruding from the surface of the thermally conductive flange 410 may thereby be mechanically attached to the first surface 312 of the corresponding interconnect structure 310", and may be electrically connected to conductive pads on the first surface 312 (which are coupled to the source terminal 226" of the transistor die(s) 210) by the respective patterns 240p of the conductive adhesive 240". The conductive adhesive patterns 240p thereby provide at least a portion of a ground signal path between the source terminal 226" of the transistor die(s) 210 and the corresponding thermally conductive flange 410 of each interconnect structure 310".

[00374] As shown at block 3450, after attachment of the flanges 410 to the first surface 312 of the interconnect array 310a, the array 310a is rotated or flipped by 180 degrees, and one or more operations are performed to provide environmental protection for the transistor dies, the

passive electrical components 1750, and the thermally conductive flanges 410 on the first surface 312 of the interconnect array 310a. For example, in some embodiments, molding operations (illustrated using an encapsulant material 1740) may be performed to encapsulate the components on the first surface 312 of the interconnect array 310a. As such, respective package housings 278 may be provided for each populated interconnect structure 310", where each package housing 278 may include an encapsulant material 1740 (e.g., defining a mold structure 2240) and/or a lid member 2325 (e.g., a ceramic lid).

[00375] At block 3455, the interconnect array 310a is rotated or flipped by 180 degrees, and laminated on tape T(e.g., PVC or Mylar tape) with the thermally conductive flange 410 facing the tape. In some embodiments, a laser marking process may be performed on the surface of the package housing 278 (e.g., the mold structure 2240 or the lid 2325) opposite to the thermally conductive flange 410. As shown in FIG. 34D, at block 3460, the interconnect array 310a may be removed from the tape and again rotated or flipped by 180 degrees. At block 3465a or 3456b, the interconnect array 310a may be either placed on a carrier C (shown at left) or placed on tape T (shown at right). In either configuration, an exposure process (e.g., grinding or laser ablation) is performed to expose the bottom surface of each thermally conductive flange 410. At block 3470a or 3470b, a singulation process (e.g., dicing, sawing, laser ablation, etc.) is performed to separate the respective interconnect structures 310" of the interconnect array 310a, thereby providing the respective transistor device packages 3000a, 3000b on the carrier C (shown at left) or on the tape T (shown at right) at block 3475a or 3475b by the in-strip manufacturing process. In some embodiments, as noted with reference to FIG. 33, operations for single-piece handling (e.g., pick and place operations, electrical testing, moisture removal process) may be further performed.

[00376] As described herein, some embodiments of the present invention may embed benefits of a flip-chip module and integrate it into a large scale, high power capable package, which may externally conform the form factor of some conventional chip-and-wire high power device packages. Flip-chip component attachment according to embodiments described herein may be more accurate, repeatable, and may provide reduced inductance connections (which may thereby provide improved performance, particularly at higher operating frequencies) in comparison to wire bonding connections that can be affected by process and material variability (which can be increasingly problematic as operating frequencies increase). In particular, flip chip component assemblies with very low impedance connections (e.g., using Cu bumps) can provide significantly lower impedances as well as lower impedance variability in comparison to chip-and-wire connections.

[00377] In addition to reducing inductance and tolerances, flip chip component assemblies as described herein may allow for heterogeneous integration, which allows for the inclusion of a variety of passive electrical components (e.g., IPDs, SMDs) to be attached to the interconnect structure of the component assembly, for example, using epoxy or solder attach, to implement termination and/or matching networks with the shortest possible electrical connections. For example, one or more passive components may be used to implement base band termination circuits that are vertically overlapping with the transistor die(s) (e.g., positioned on a surface of the PCB or other interconnect structure that is directly above or below the positions of the die(s) on the opposing surface).

[00378] Integrating such flip-chip component assemblies into transistor device packages as described herein may also provide cost advantages. In particular, some conventional chip-and-wire package implementations may use 2 mil (50μm) gold wire to implement input/output as well as matching network connections, which may involve significant costs per unit. Also, as mentioned, such conventional packages may be subject to process variability and may limit performance due to consistency and high impedances on the wirebond connections. Embodiments of the present invention may thereby achieve improved performance and may be cost competitive (or even less expensive) to manufacture than some conventional chip-and-wire assembly methods.

[00379] Embodiments of the present invention may be used in high power RF transistors for cellular or aerospace and defense (A&D) applications, such as 20W or higher average output power RF transistors for 5G base station application at 3.5GHz and above. Embodiments of the present invention may also provide lower cost and higher performing products at higher frequencies, particularly for low impedance integration of matching circuits such as baseband termination circuits. Some embodiments may allow for performance in the range where MMICs (monolithic microwave integrated circuits) are typically used, which may provide significant cost improvement for devices operating at such high frequencies.

[00380] Various embodiments have been described herein with reference to the accompanying drawings in which example embodiments are shown. These embodiments may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure is thorough and complete and fully conveys the inventive concept to those skilled in the art. Various modifications to the example embodiments and the generic principles and features described herein will be readily apparent. In the drawings, the sizes and relative sizes of

layers and regions are not shown to scale, and in some instances may be exaggerated for clarity.

[00381] It will be understood that, although the terms "first," "second," etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present invention. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[00382] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including" when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[00383] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[00384] It will be understood that when an element such as a layer, region, or substrate is referred to as being "on," "attached," or extending "onto" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or "directly attached" or extending "directly onto" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

[00385] Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "lateral" or "vertical" may be used herein to describe a relationship of one element, layer or

region to another element, layer or region as illustrated in the figures. It will be understood that these terms are intended to encompass different orientations of the device in addition to the orientation depicted in the figures.

[00386] Embodiments of the invention are described herein with reference to cross-section illustrations that are schematic illustrations of idealized embodiments (and intermediate structures) of the invention. The thickness of layers and regions in the drawings may be exaggerated for clarity. Additionally, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments of the invention should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. Elements illustrated by dotted lines may be optional in the embodiments illustrated.

[00387] Like numbers refer to like elements throughout. Thus, the same or similar numbers may be described with reference to other drawings even if they are neither mentioned nor described in the corresponding drawing. Also, elements that are not denoted by reference numbers may be described with reference to other drawings.

[00388] In the drawings and specification, there have been disclosed typical embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

THAT WHICH IS CLAIMED:

1. A transistor device package, comprising:

a component assembly comprising an interconnect structure, a transistor die having a front surface including a gate terminal, a drain terminal, and a source terminal on a first surface of the interconnect structure, and one or more passive electrical components electrically coupled to the gate, drain, and/or source terminal by the interconnect structure; and

a thermally conductive flange attached to a back surface of the transistor die, which is opposite the front surface, by a conductive adhesive.

2. The transistor device package of Claim 1, further comprising respective patterns of the conductive adhesive on the first surface of the interconnect structure, wherein at least one of the respective patterns of the conductive adhesive provide an input, output, or ground signal path for the transistor device package.

3. The transistor device package of Claim 2, wherein the respective patterns of the conductive adhesive attach and electrically connect one or more conductive leads to respective conductive patterns on the first surface of interconnect structure.

4. The transistor device package of Claim 2, wherein the respective patterns of the conductive adhesive attach and electrically connect the thermally conductive flange to conductive patterns on the first surface of the interconnect structure.

5. The transistor device package of Claim 4, wherein the interconnect structure comprises one or more conductive leads integrated therein that protrude outside a periphery of the transistor device package.

6. The transistor device package of Claim 4, further comprising:

one or more support structures that extend from the thermally conductive flange to the first surface of the interconnect structure.

7. The transistor device package of Claim 6, wherein the one or more support structures comprise one or more conductive support structures that are attached and

electrically connected to the conductive patterns on the first surface of the interconnect structure by the respective patterns of the conductive adhesive.

8. The transistor device package of Claim 7, wherein the one or more conductive support structures comprise one or more conductive pillar structures that are integral to and protrude from the thermally conductive flange to the first surface of the interconnect structure.

9. The transistor device package of Claim 3, wherein the one or more conductive leads comprise a portion that is inside a periphery of the transistor device package and is bent towards or away from the first surface of the interconnect structure.

10. The transistor device package of Claim 1, further comprising an overmold material on the transistor die between the first surface of the interconnect structure and the thermally conductive flange.

11. The transistor device package of Claim 1, wherein the one or more passive electrical components are on a second surface of the interconnect structure that is opposite the first surface.

12. The transistor device package of Claim 11, wherein at least one of the passive electrical components is on a portion of the second surface of the interconnect structure that overlaps with the transistor die on the first surface.

13. The transistor device package of Claim 11, further comprising an overmold material on the one or more passive electrical components on the second surface of the interconnect structure.

14. The transistor device package of Claim 11, further comprising a lid member defining an open cavity around the one or more passive electrical components on the second surface of the interconnect structure.

15. The transistor device package of Claim 1, wherein the one or more passive electrical components comprise a surface mount device and/or an integrated passive device.

16. The transistor device package of Claim 1, wherein the transistor device package is free of wire bond connections.

17. The transistor device package of Claim 1, wherein the transistor die comprises a high electron mobility transistor (HEMT) or a laterally-diffused metal-oxide semiconductor (LDMOS) transistor.

18. The transistor device package of Claim 1, wherein the transistor die is a Group III nitride-based RF transistor amplifier die.

19. A transistor device package, comprising:

a component assembly comprising an interconnect structure and a transistor die having a front surface including a gate terminal, a drain terminal, and a source terminal on a first surface of the interconnect structure; and

respective patterns of a conductive adhesive on the first surface of the interconnect structure, wherein at least one of the respective patterns of the conductive adhesive provides an input, output, or ground signal path for the transistor device package.

20. The transistor device package of Claim 19, wherein the respective patterns of the conductive adhesive attach and electrically connect one or more conductive leads to respective conductive patterns on the first surface of interconnect structure.

21. The transistor device package of Claim 19, wherein the respective patterns of the conductive adhesive attach and electrically connect a thermally conductive flange to conductive patterns on the first surface of the interconnect structure.

22. A method of fabricating a transistor device package, the method comprising:

providing a component assembly comprising an interconnect structure, a transistor die having a front surface including a gate terminal, a drain terminal, and a source terminal on a first surface of the interconnect structure, and one or more passive electrical components electrically coupled to the gate, drain, and/or source terminal by the interconnect structure; and

attaching a back surface of the transistor die, which is opposite the front surface, to a thermally conductive flange by a conductive adhesive.

23. The method of Claim 22, further comprising respective patterns of the conductive adhesive on the first surface of the interconnect structure, wherein the respective patterns of the conductive adhesive provide an input, output, or ground signal path for the transistor device package.

24. The method of Claim 23, further comprising:

applying the conductive adhesive in the respective patterns on one or more conductive leads; and then

attaching the one or more conductive leads to conductive patterns on the first surface of the interconnect structure using the respective patterns of the conductive adhesive,

wherein the respective patterns of the conductive adhesive electrically connect the one or more conductive leads to the conductive patterns of the interconnect structure.

25. The method of Claim 23, further comprising:

applying the conductive adhesive in the respective patterns on respective areas of the first surface of the interconnect structure; and then

attaching the thermally conductive flange to conductive patterns on the respective areas of the first surface of the interconnect structure,

wherein the respective patterns of the conductive adhesive electrically connect the thermally conductive flange to the conductive patterns of the interconnect structure.

26. The method of Claim 25, wherein the interconnect structure comprises one or more conductive leads integrated therein that protrude outside a periphery of the transistor device package.

27. The method of Claim 26, wherein the thermally conductive flange comprises one or more conductive pillar structures that protrude therefrom, and wherein attaching the thermally conductive flange comprises attaching the one or more conductive pillar structures to the conductive patterns on the first surface of the interconnect structure by the respective patterns of the conductive adhesive.

28. The method of Claim 27, wherein the interconnect structure comprises a respective one of a plurality of interconnect structures of an interconnect array, and further comprising:

singulating the interconnect array into the plurality of interconnect structures prior to attaching the thermally conductive flange.

29. The method of Claim 28, wherein the interconnect array comprises slots therein, and wherein attaching the thermally conductive flange comprises:

inserting a clamping device into one or more of the slots; and

clamping the thermally conductive flange to the interconnect structure using the clamping device such that the one or more conductive pillar structures contact the respective areas of the first surface of the interconnect structure having the respective patterns of the conductive adhesive thereon.

30. The method of Claim 27, wherein the interconnect structure comprises a respective one of a plurality of interconnect structures of an interconnect array, and further comprising:

singulating the interconnect array into the plurality of interconnect structures after attaching the thermally conductive flange.

31. The method of Claim 22, further comprising:

forming an overmold material on the transistor die between the first surface of the interconnect structure and the thermally conductive flange.

32. The method of Claim 22, wherein the one or more passive electrical components are provided a second surface of the interconnect structure that is opposite the first surface.

33. The method of Claim 32, further comprising:

forming an overmold material structure on the one or more passive electrical components on the second surface of the interconnect structure.

34. The method of Claim 32, further comprising:

providing a lid member defining an open cavity around the one or more passive electrical components on the second surface of the interconnect structure.

35. The method of Claim 22, wherein the transistor device package is free of wire bond connections.

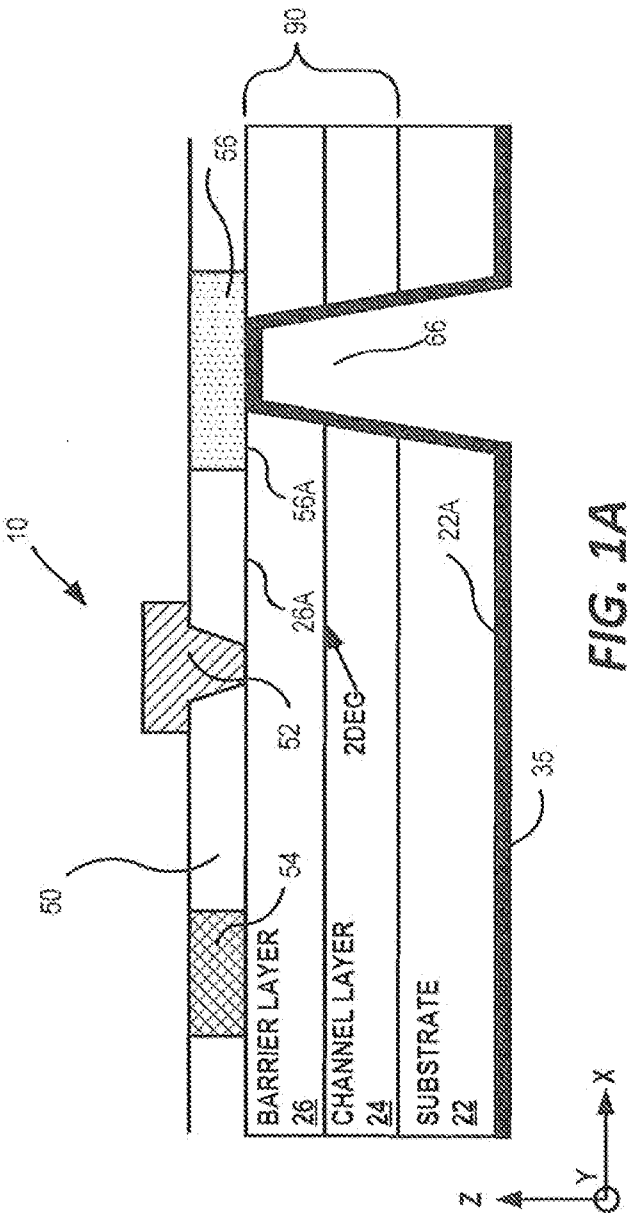

90
56
66
56A
10
26A
22A
52
2DEG
35
50
54
BARRIER LAYER
26
CHANNEL LAYER
24
SUBSTRATE
22
Z
Y
X

FIG. 1A

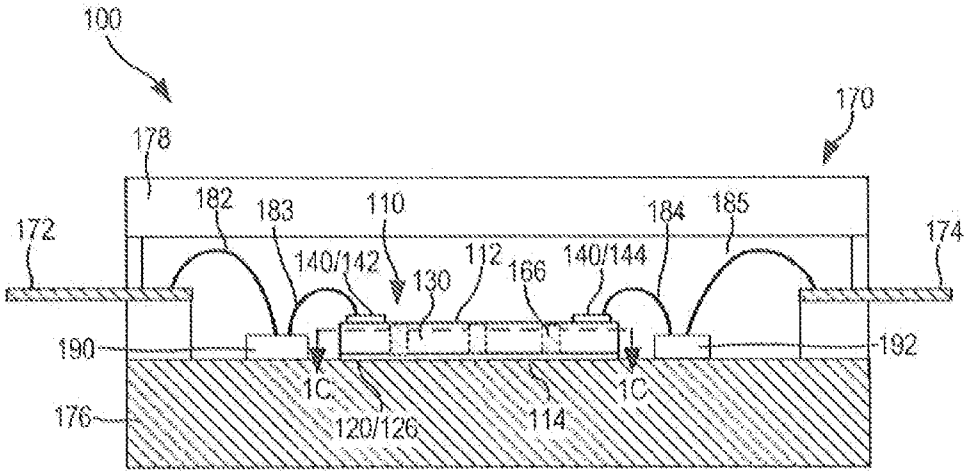

100
170
178
182
183
110
184
185
172
174
140/142
112
130
166
140/144
190
192
1C
1C
120/126
114
176

FIG. 1B

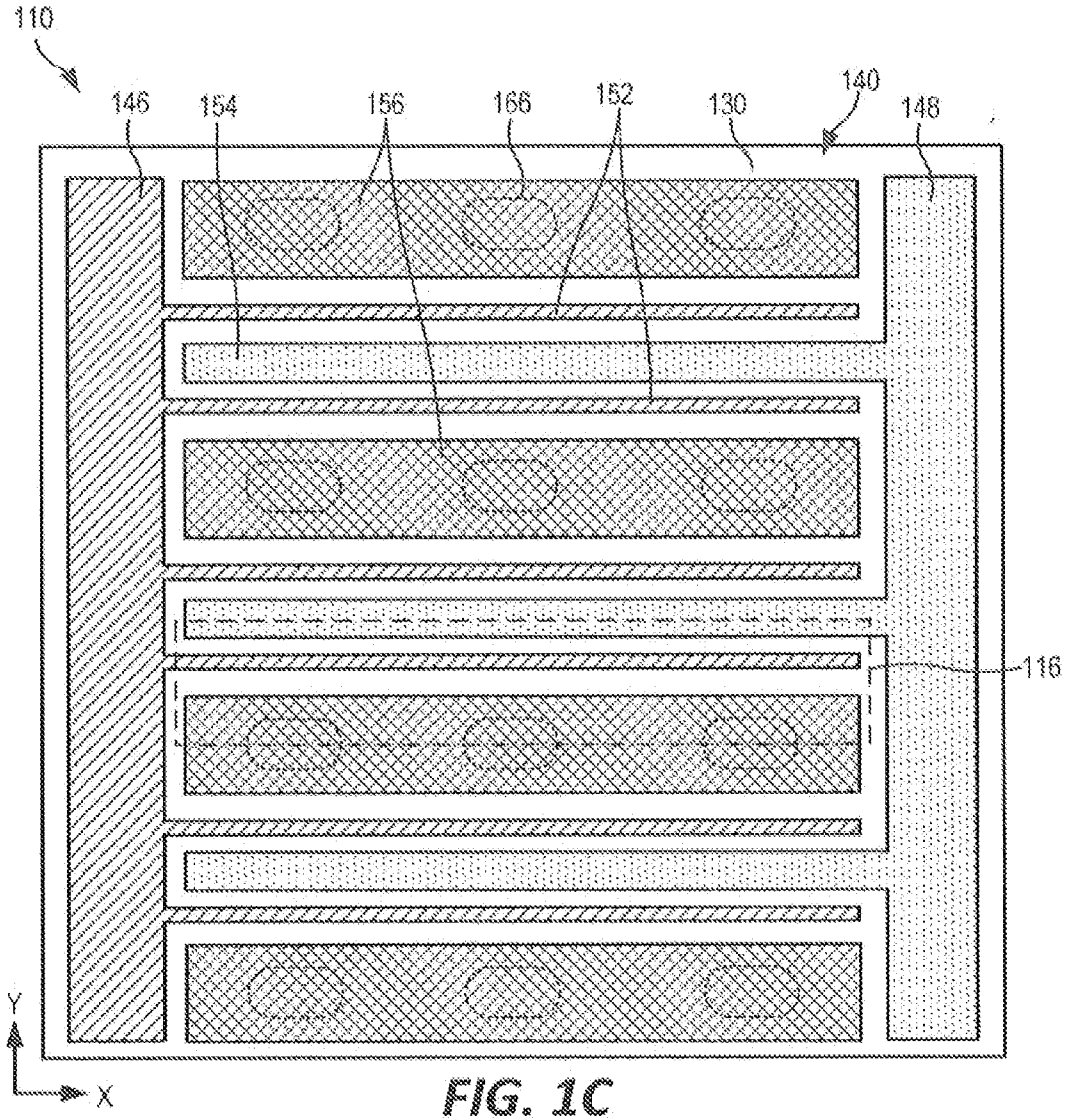

110
146
154
156
166
152
130
140
148
116
Y
X

FIG. 1C

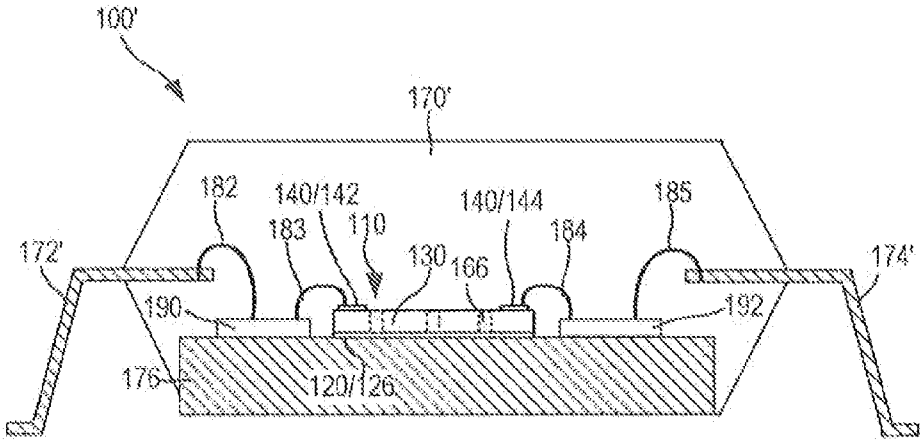

100'
170'
182
140/142
183
110
130
166
140/144
184
185
172'
174'
190
192
176
120/126

FIG. 1D

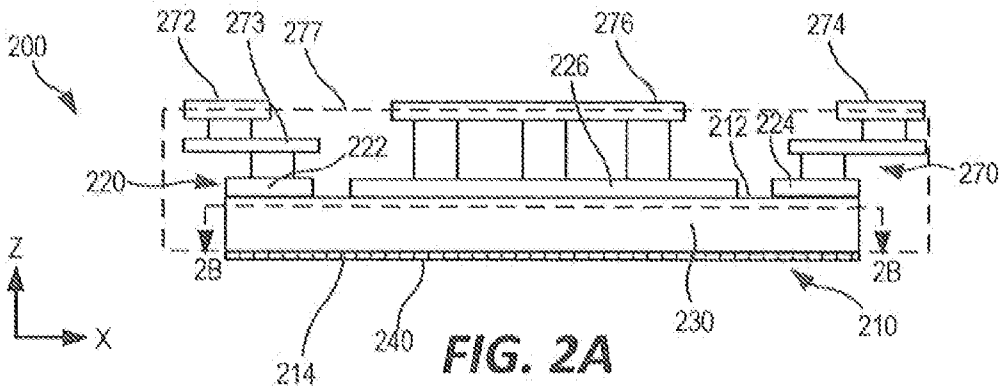

200
272
273
277
276
274
226
222
212
224
220
270
2B
2B
Z
X
214
240
230
210

FIG. 2A

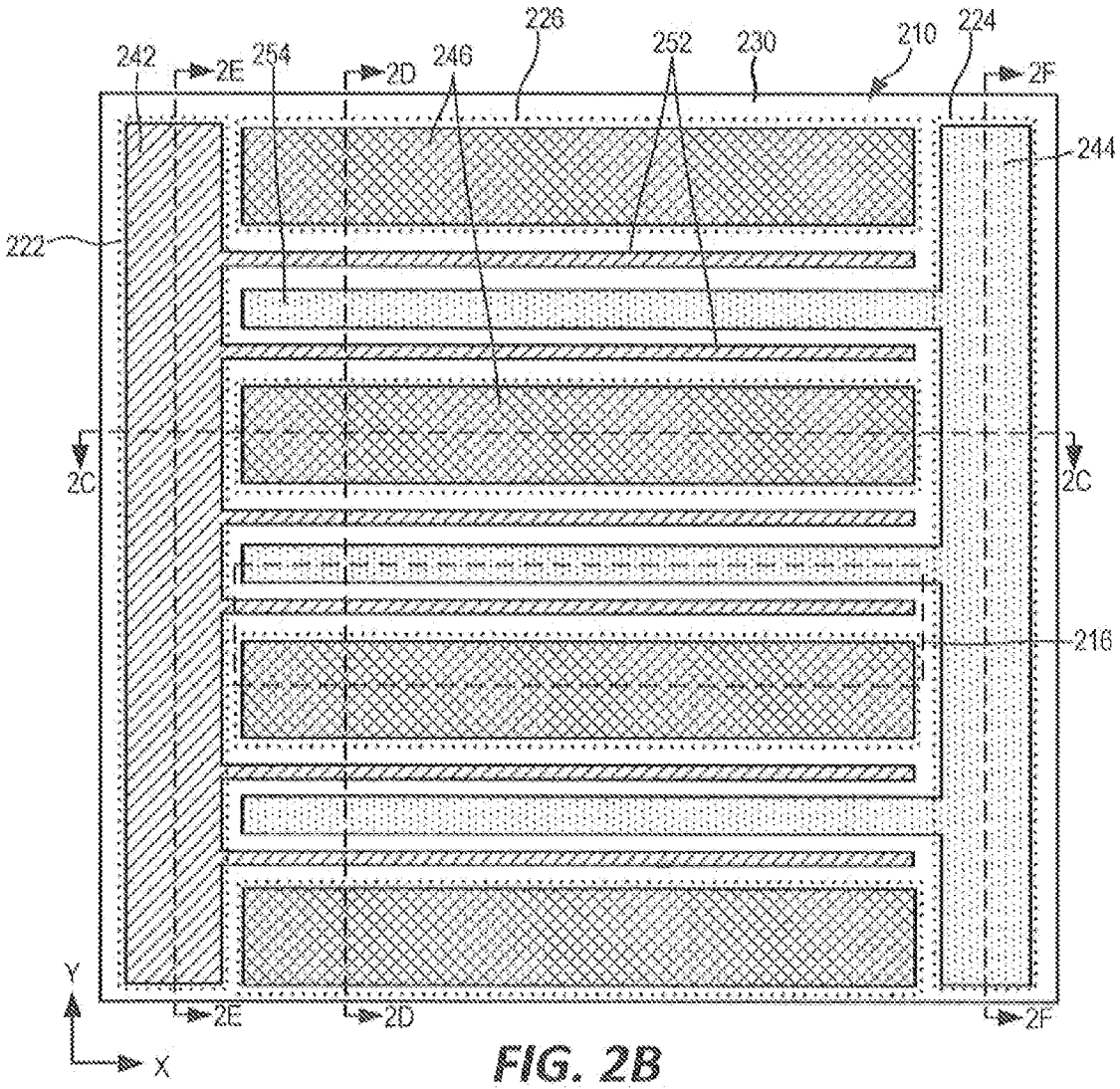

242
2E
254
2D
246
226
252
230
210
224
2F
244
222
2C
2C
216
Y
X
2E
2D
2F

FIG. 2B

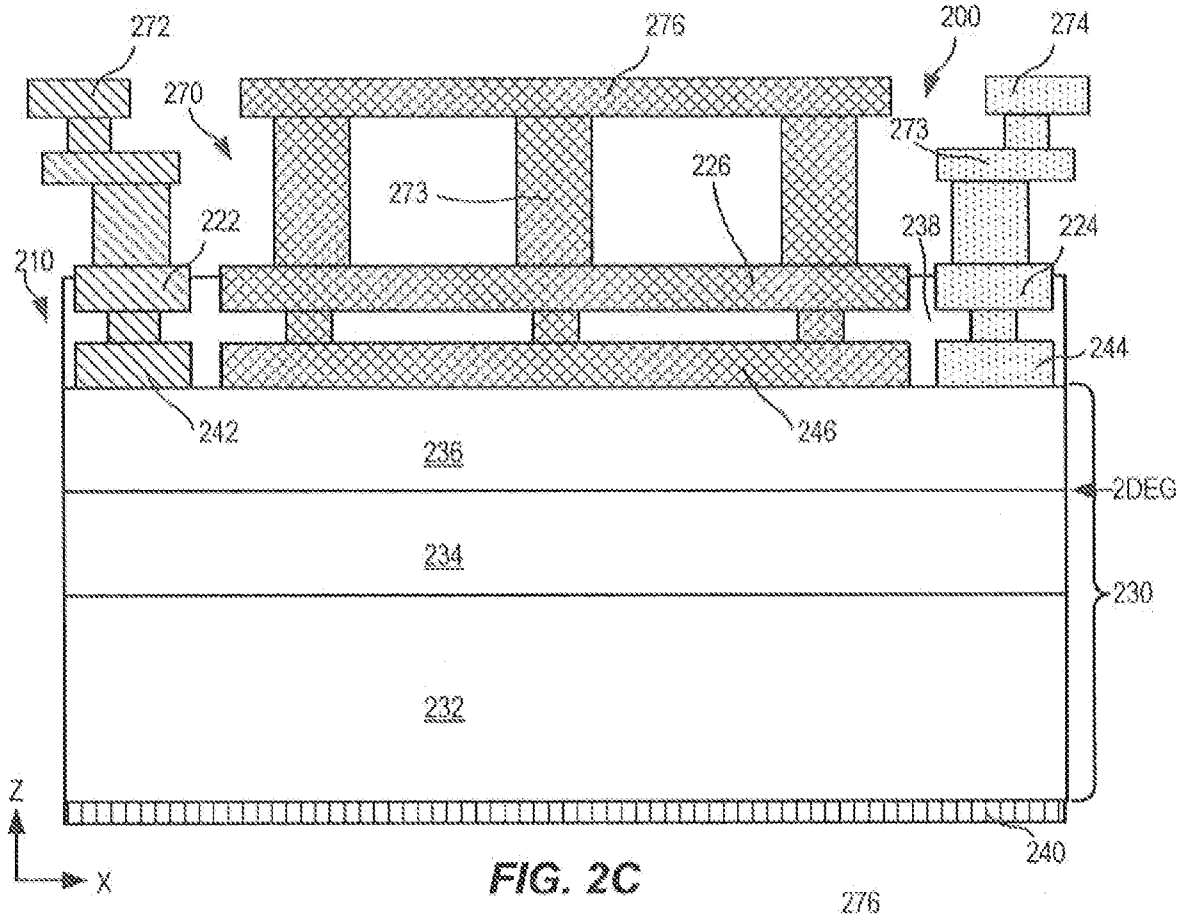

272
276
200
274
270
273
273
226
222
238
224
210
244
242
246
236
2DEG
234
230
232
Z
X
240

FIG. 2C

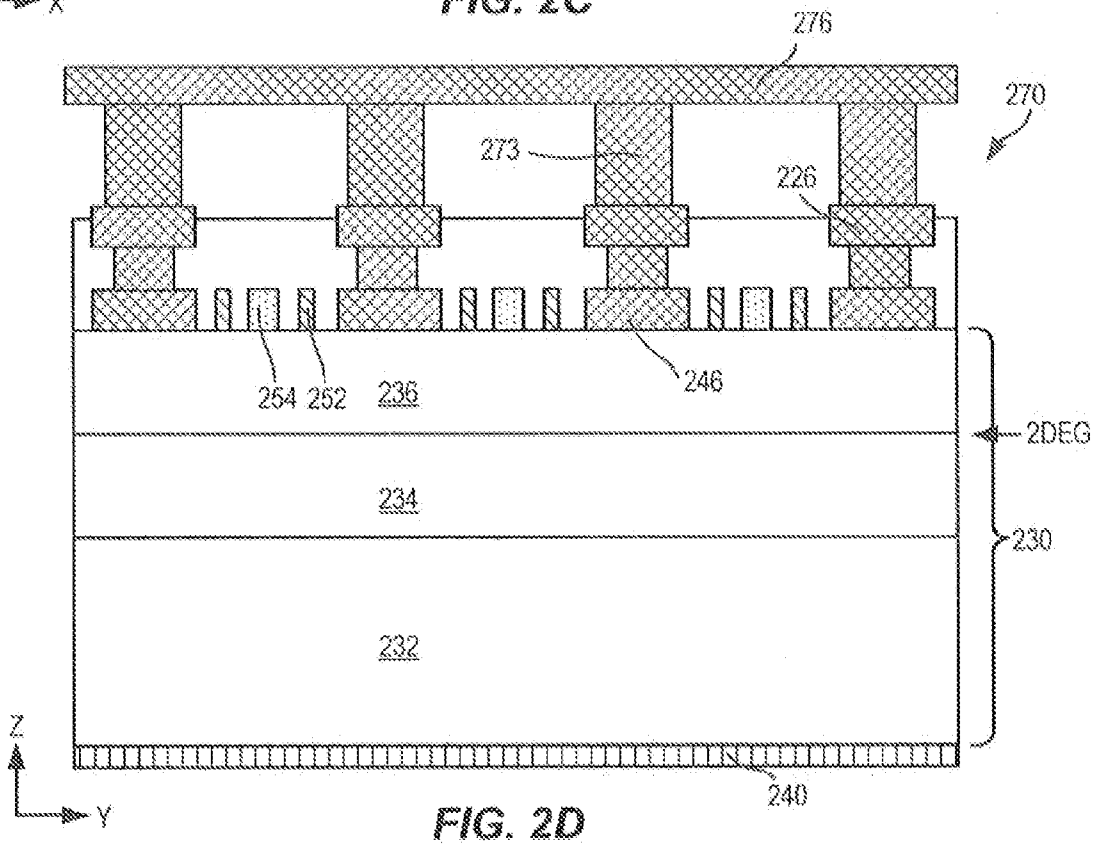

276
270
273
226
254
252
236
246
2DEG
234
230
232
Z
Y
240

FIG. 2D

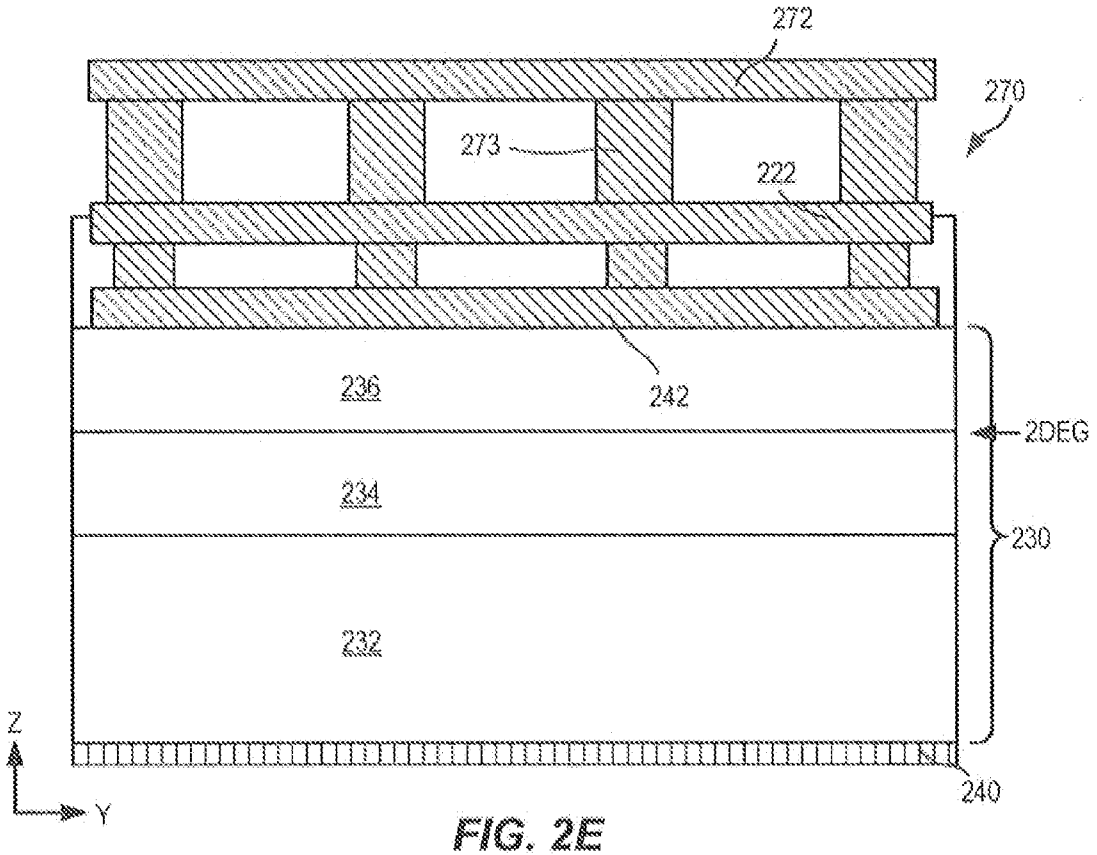

272
270
273
222
242
236
2DEG
234
230
232
240
Z
Y

FIG. 2E

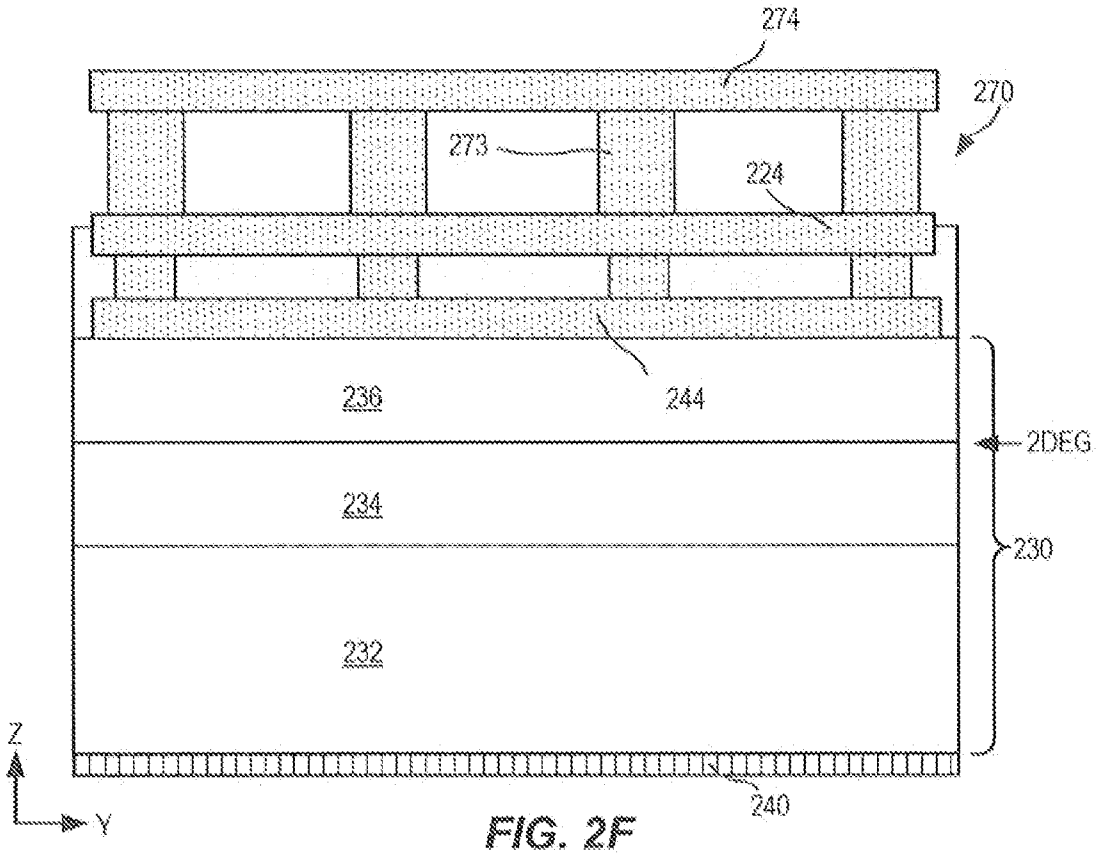

274
270
273
224
244
236
2DEG
234
230
232
240
Z
Y

FIG. 2F

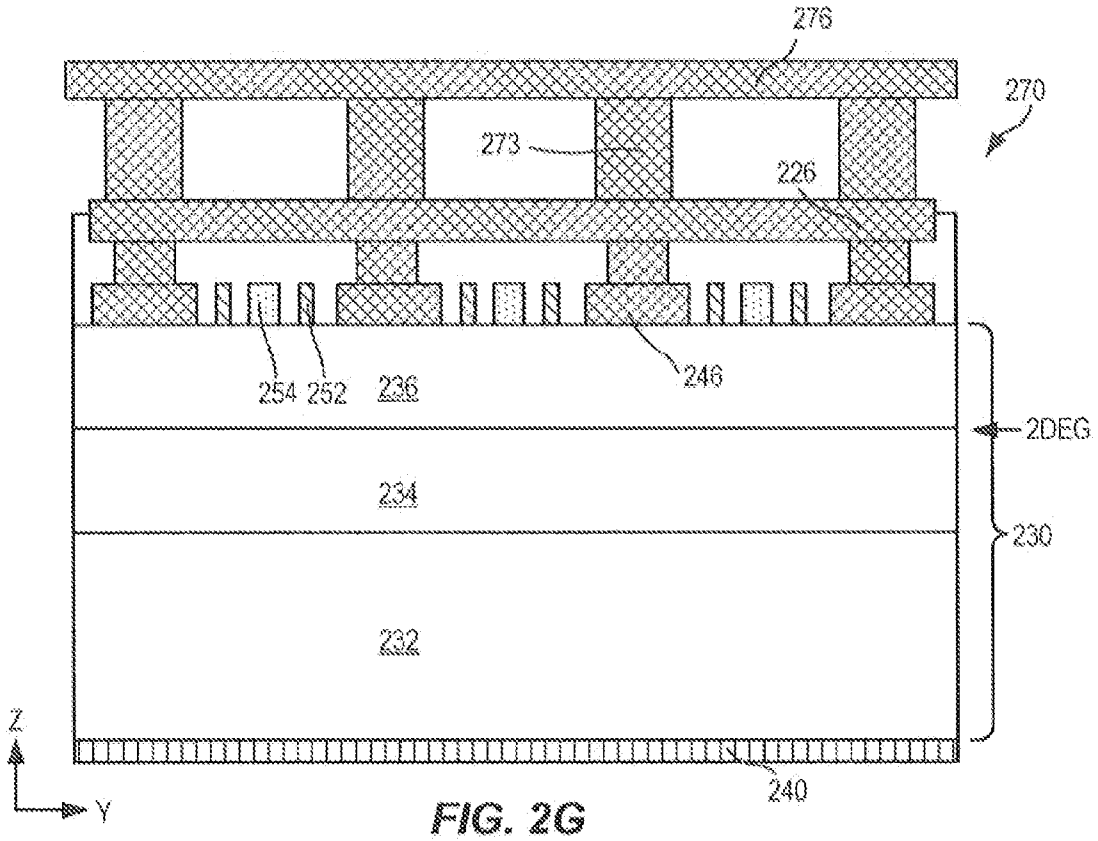

276
270
273
226
254
252
236
246
2DEG
234
230
232
Z
Y
240

FIG. 2G

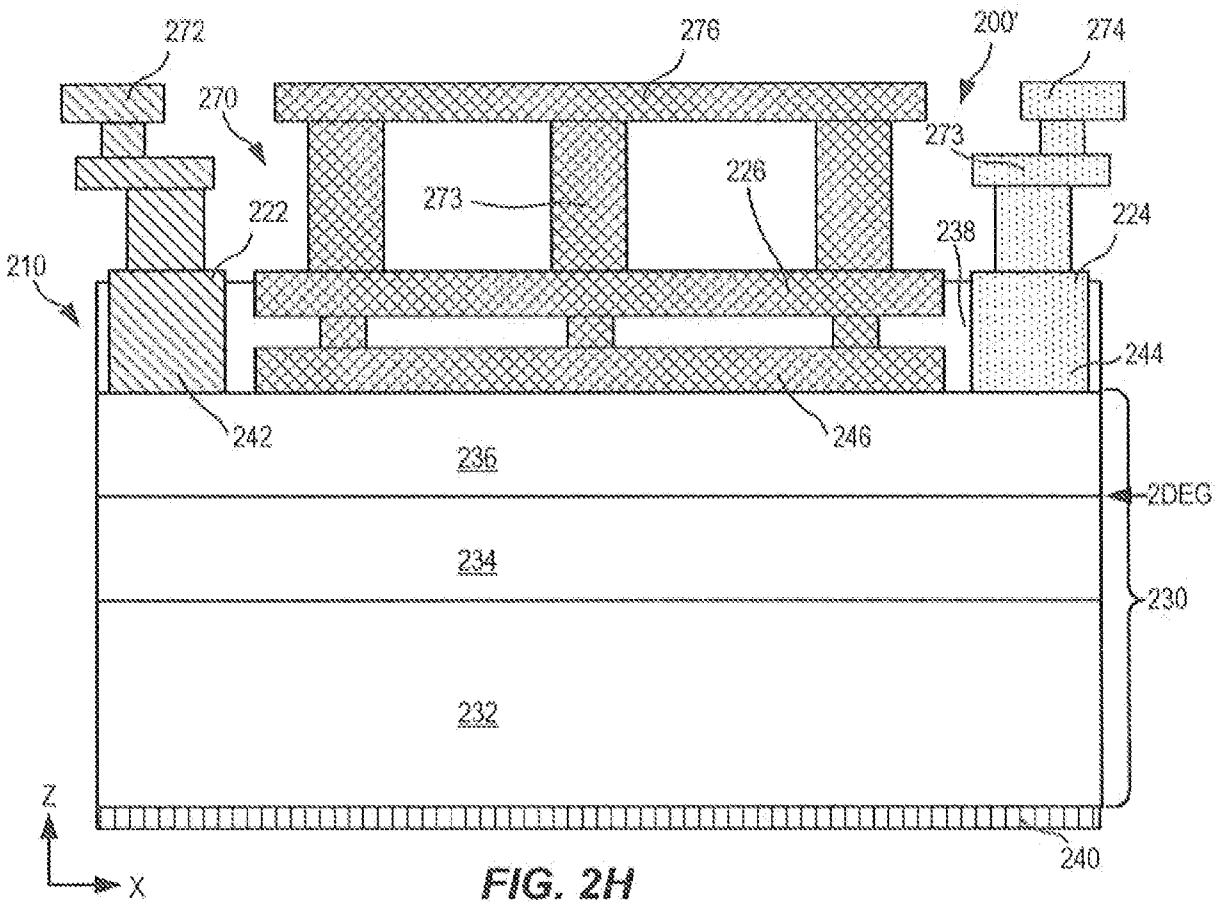

272
276
200'
274
270
273
273
226
222
238
224
210
244
242
246
236
2DEG
234
230
232
Z
X
240

FIG. 2H

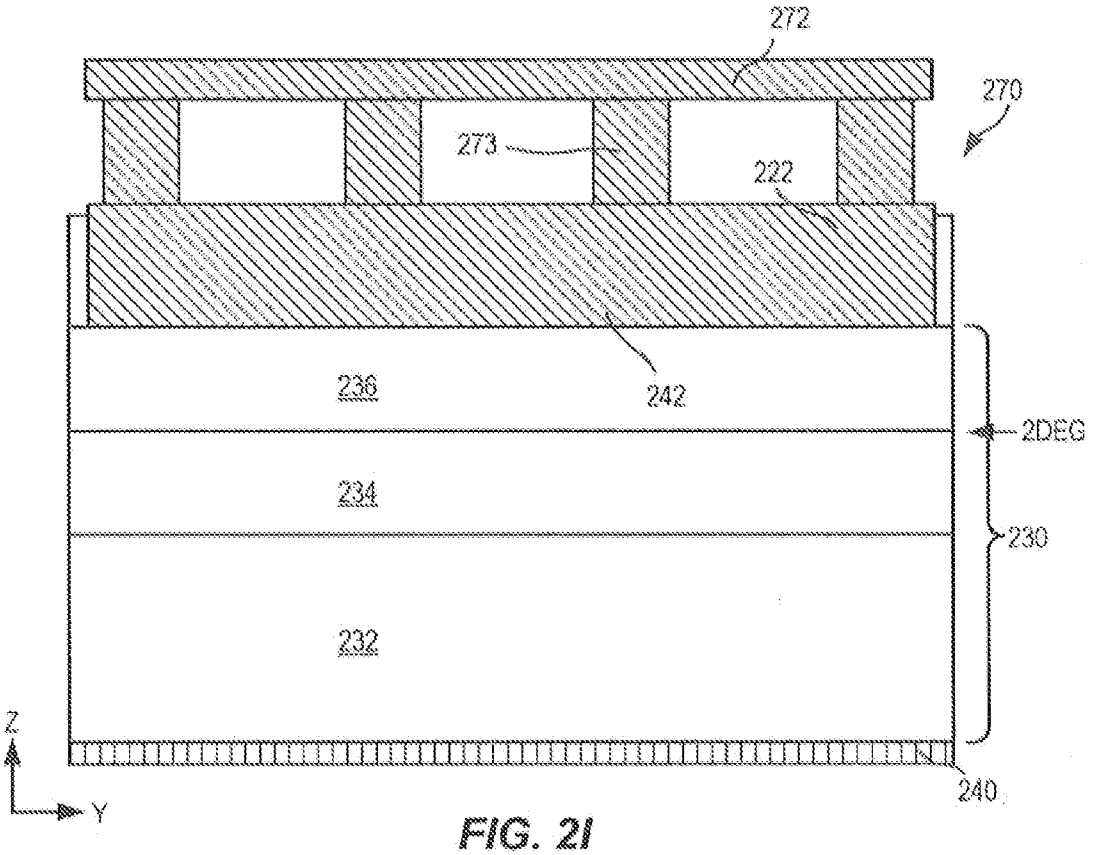

272
270
273
222
242
236
2DEG
234
230
232
240
Z
Y

FIG. 2I

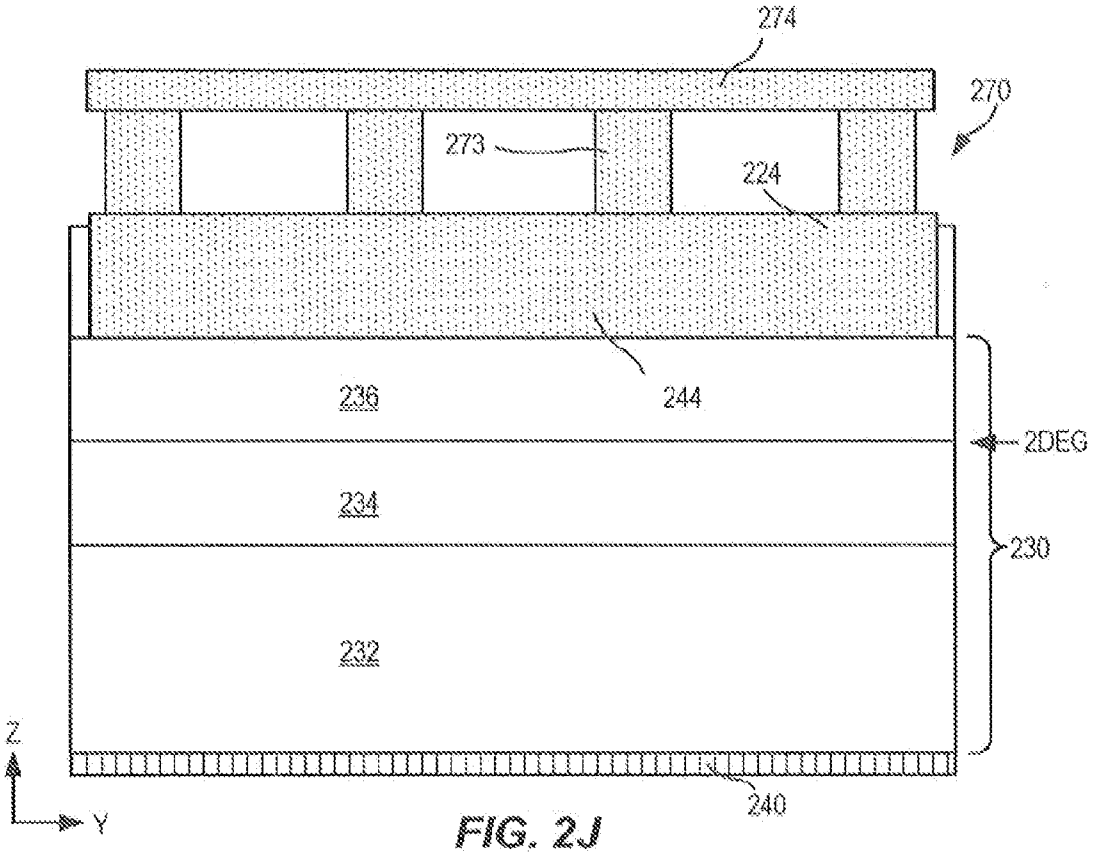

274
270
273
224
244
236
2DEG
234
230
232
240
Z
Y

FIG. 2J

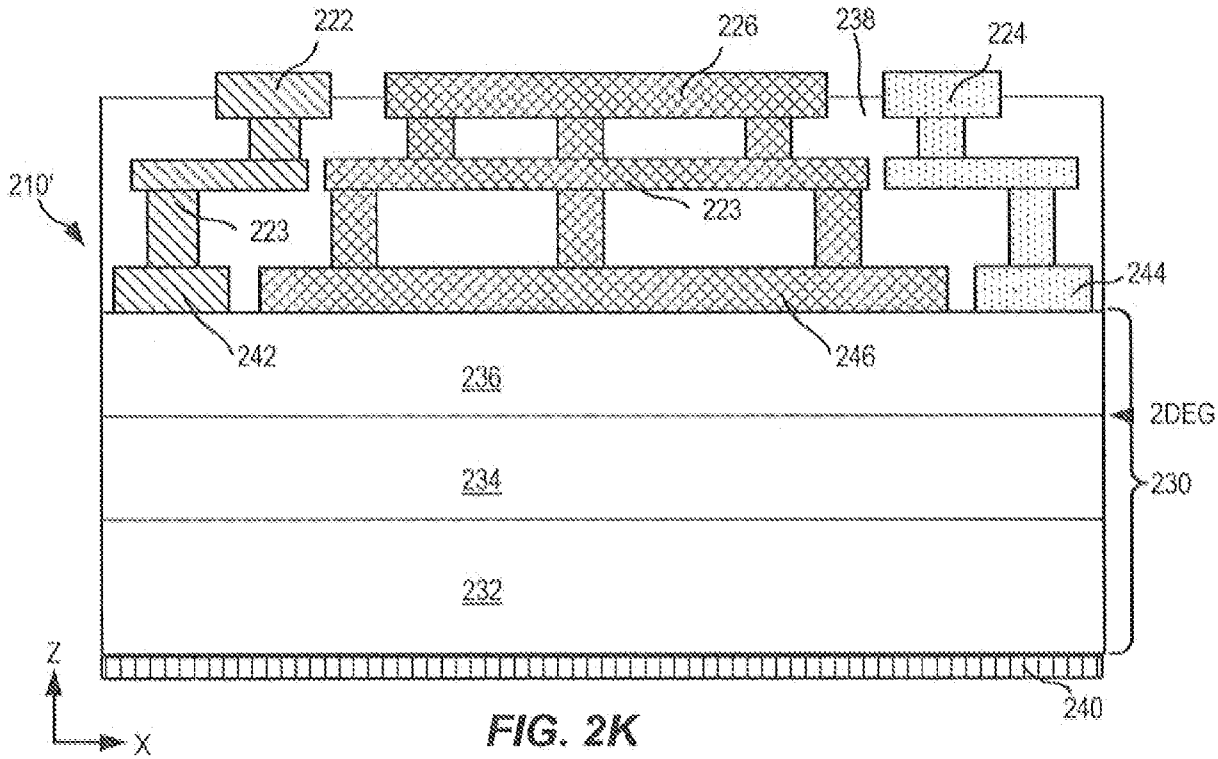

222
226
238
224
210'
223
223
244
242
246
236
2DEG
234
230
232
Z
X
240

FIG. 2K

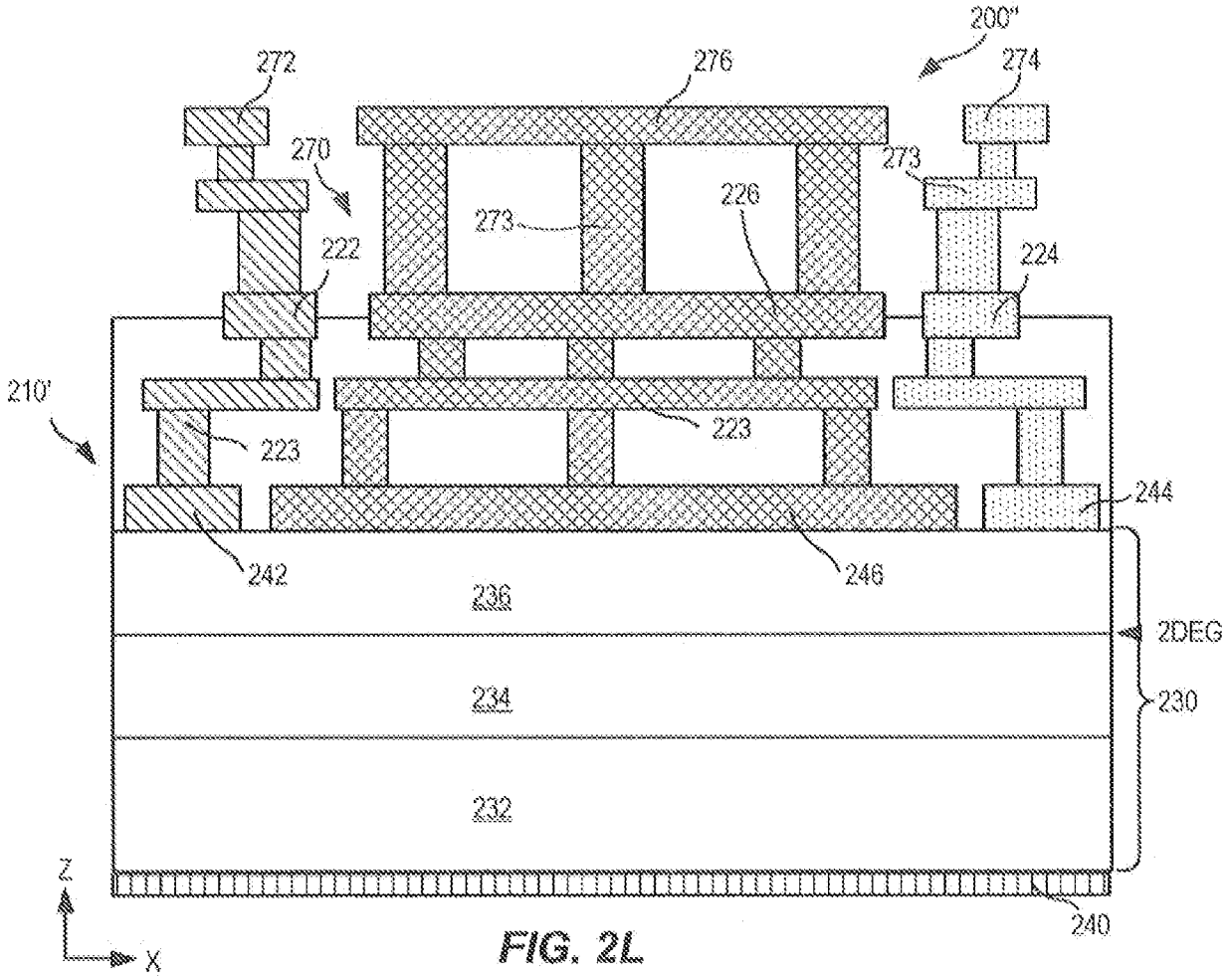

200"
272
276
274
270
273
273
226
222
224
210'
223
223
244
242
246
236
2DEG
234
230
232
Z
X
240

FIG. 2L

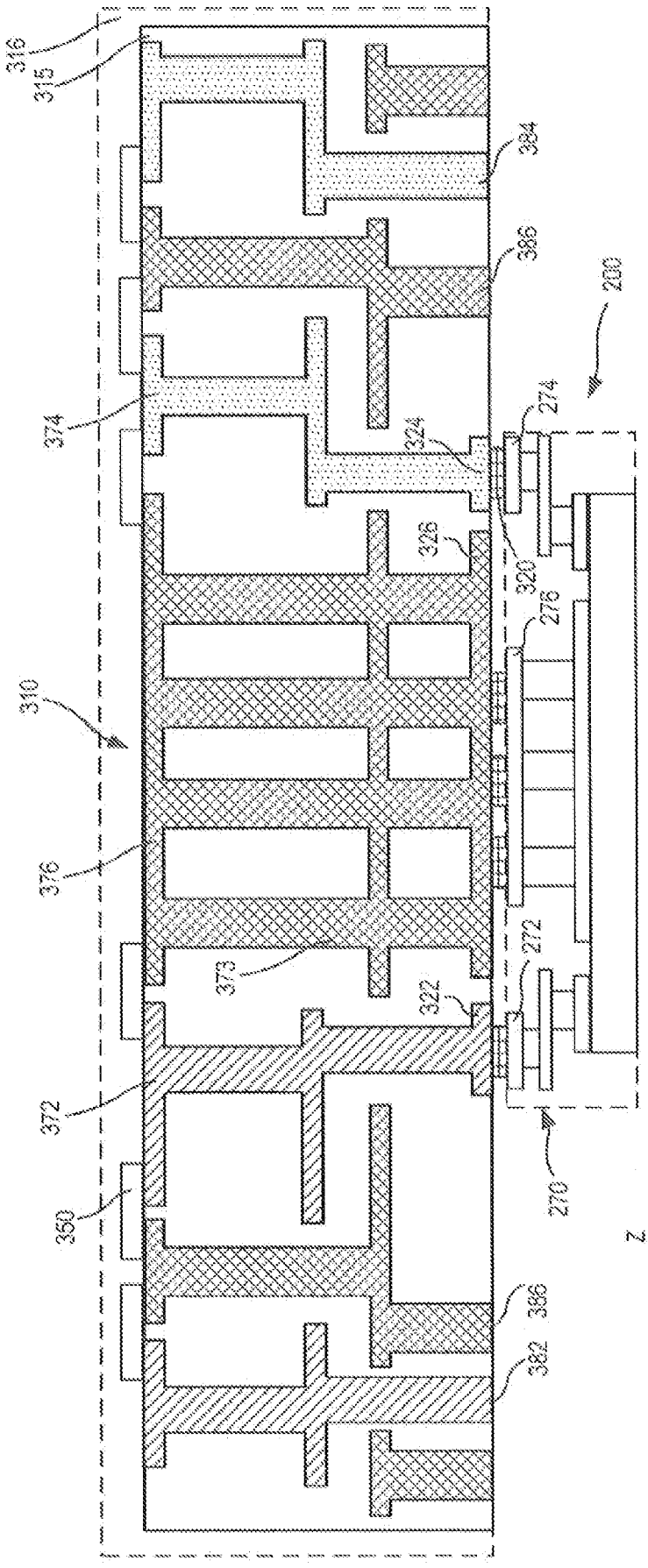

316
315
384
386
200
374
274
324
326
320
276
310
376
373
272
322
372
210
270
350
386
382
X
Z

FIG. 3A

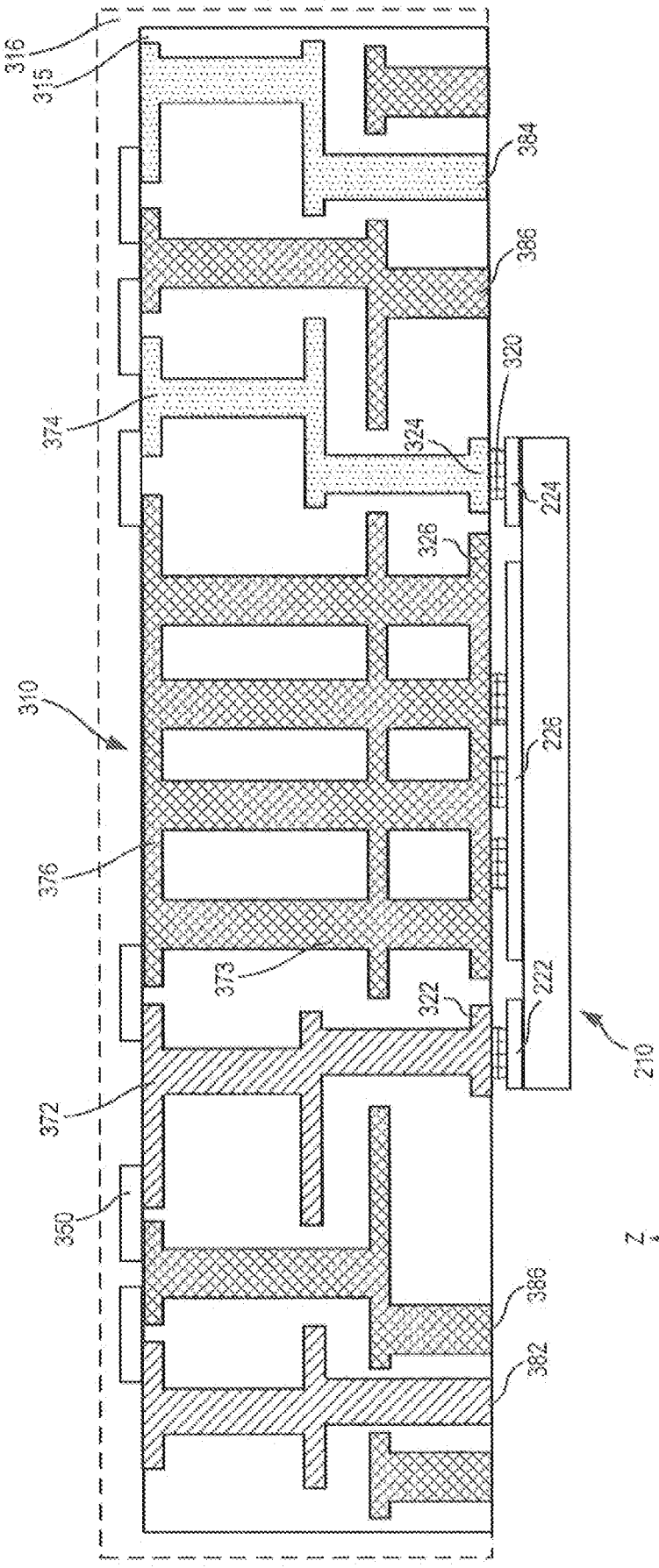

316
315
384
386
320
374
324
224
326
310
226
376
373
322
222
210
372
360
386
382
Z
X

FIG. 3B

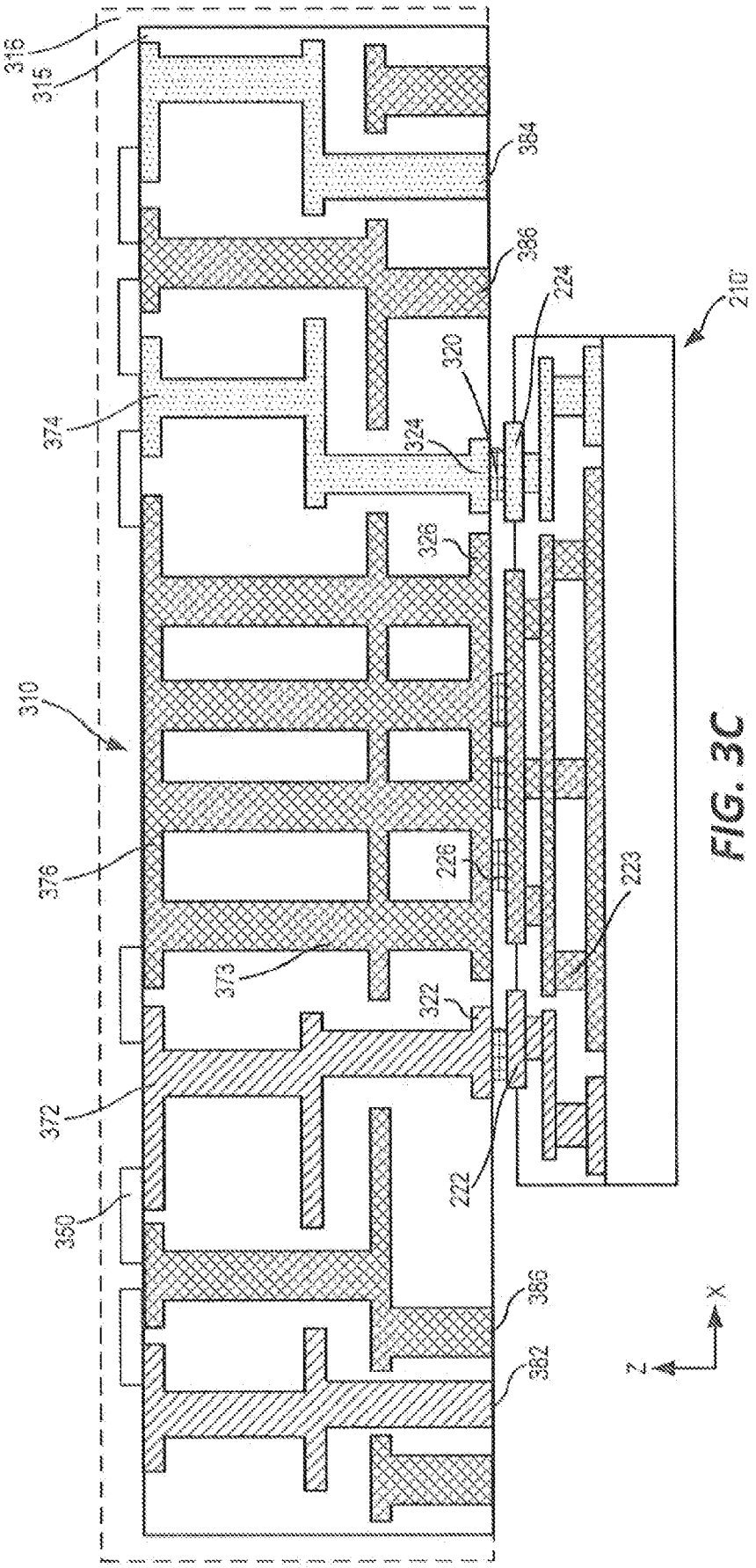

316
315
384
386
224
210
320
374
324
326
310
376
226
223
373
322
372
222
350
380
382
Z
X

FIG. 3C

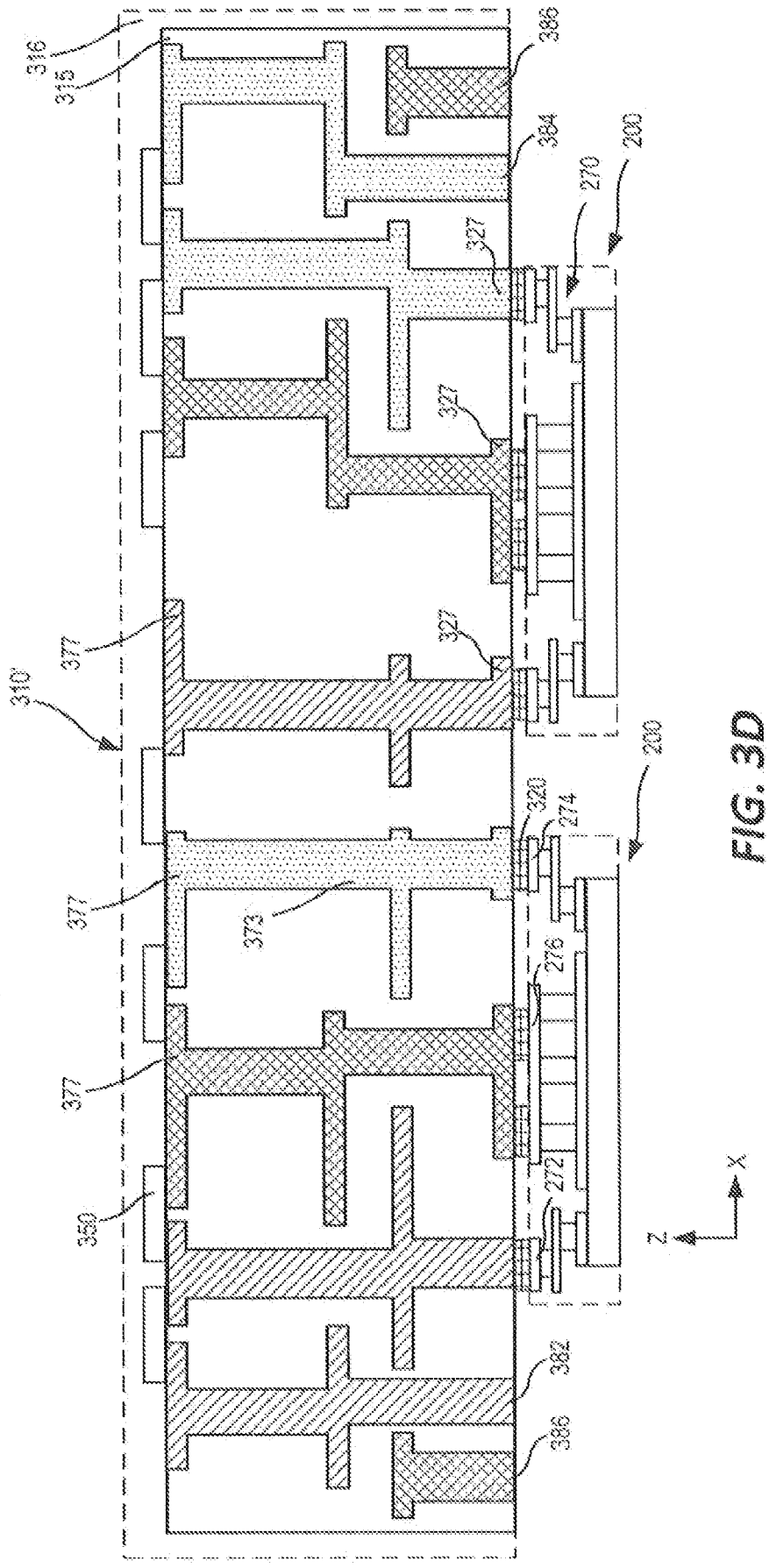

316
315
386
384
200
270
327
327
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310
327
200
320
274
377
373
276
377
350
272
382
386
X
Z

FIG. 3D

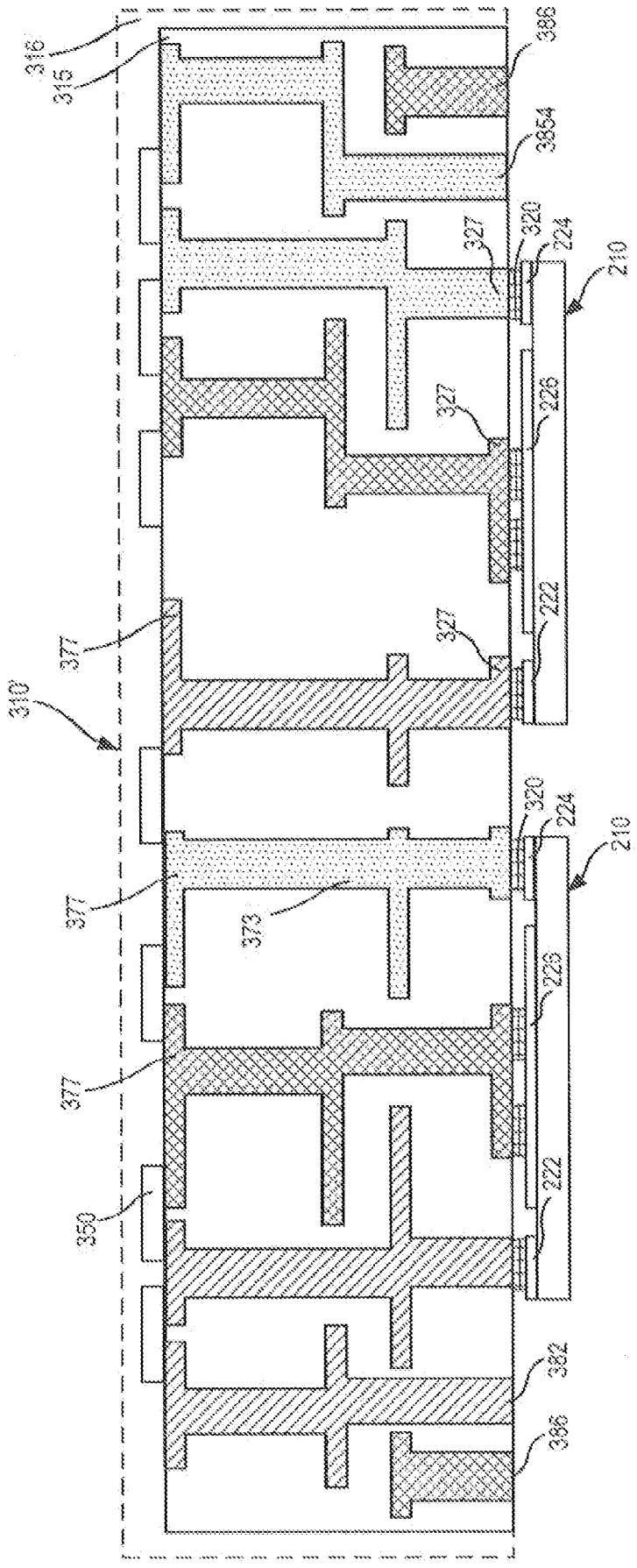

316
315
396
3954
320
224
327
210
226
327
222
327
377
310
320
224
210
377
373
226
377
222
350
382
386
Z
X

FIG. 3E

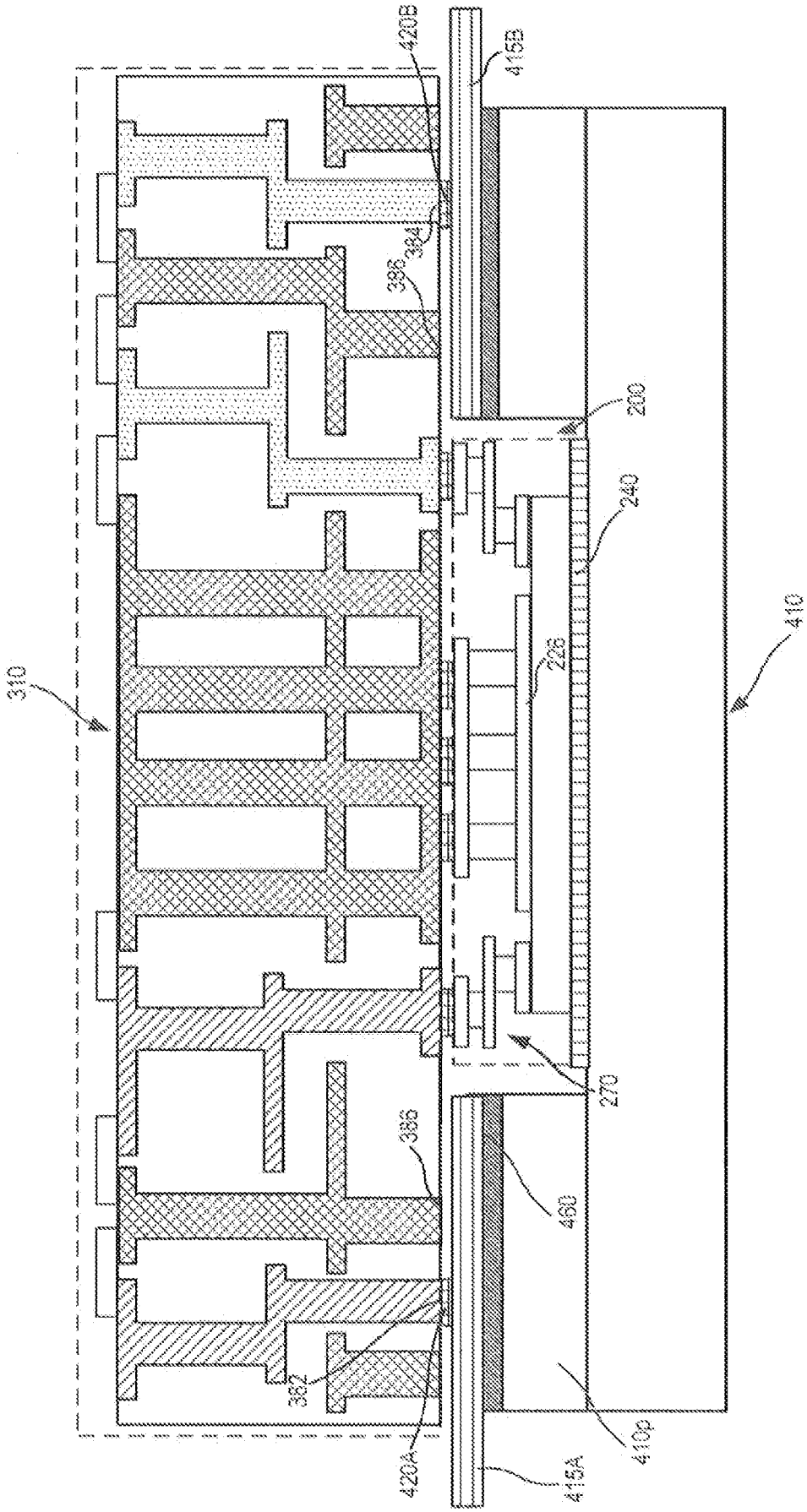

420B
415B
394
396
200
240
410
310
220
270
366
450
362
420A
415A
410p
X
Z

FIG. 4A

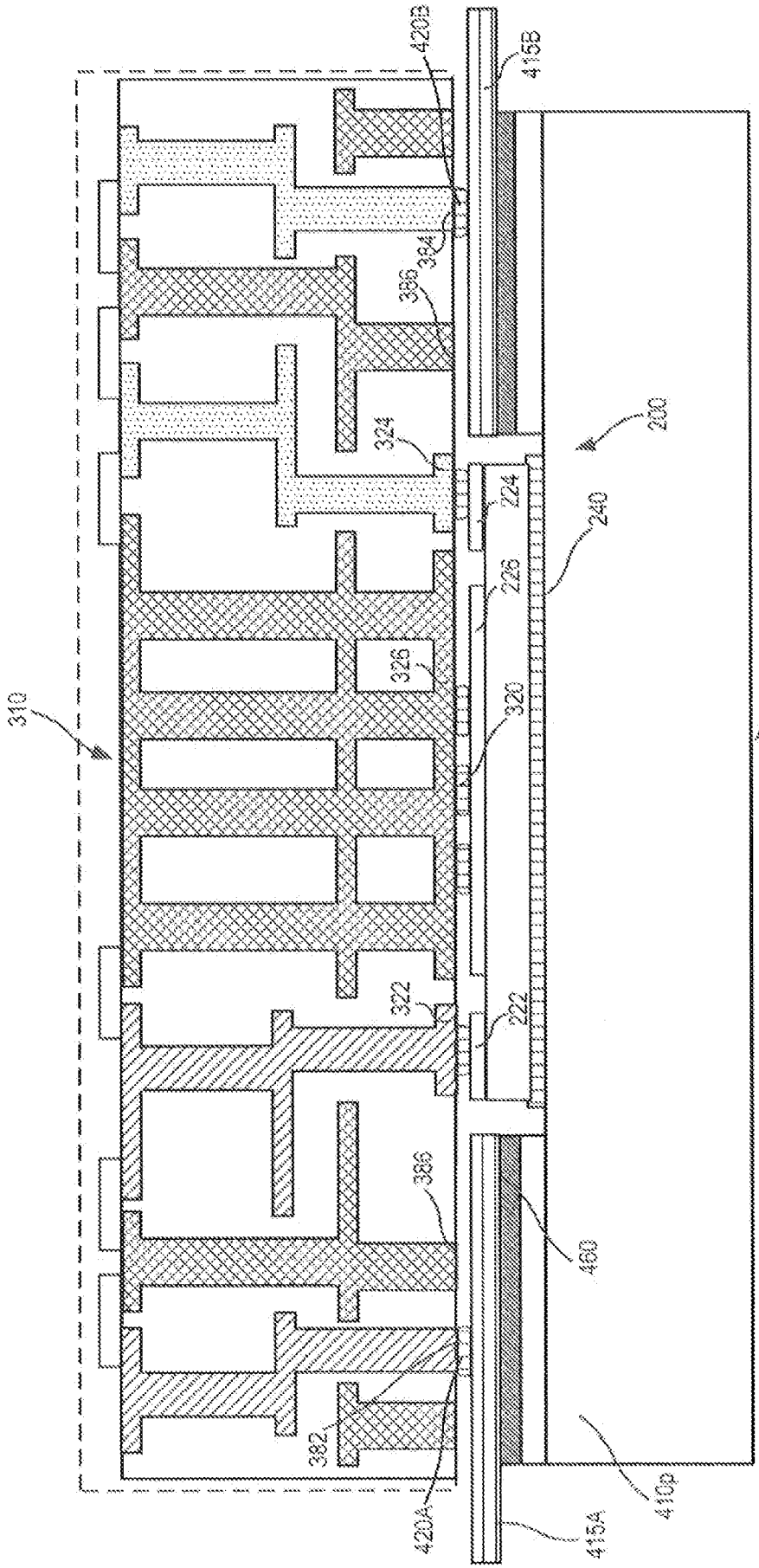

420B
415B
384
386
324
200
224
240
226
410
325
320
310
322
222
386
460
382
420A
415A
410p
Z
X

FIG. 48

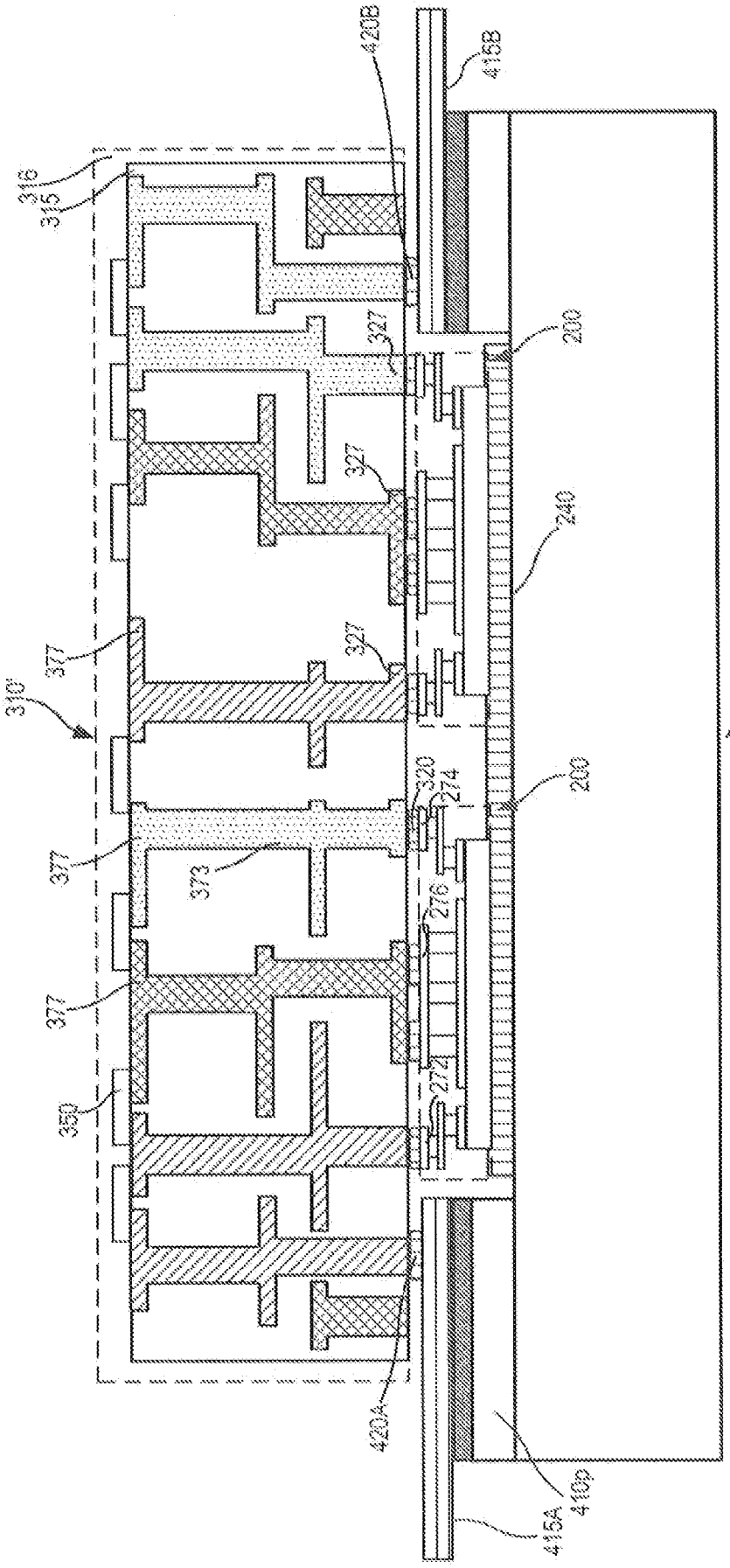

420B
415B
316
315
327
200
327
240
327
377
310'
410
320
274
200
377
373
276
377
272
350
420A
410p
415A
Z
X

FIG. 4C

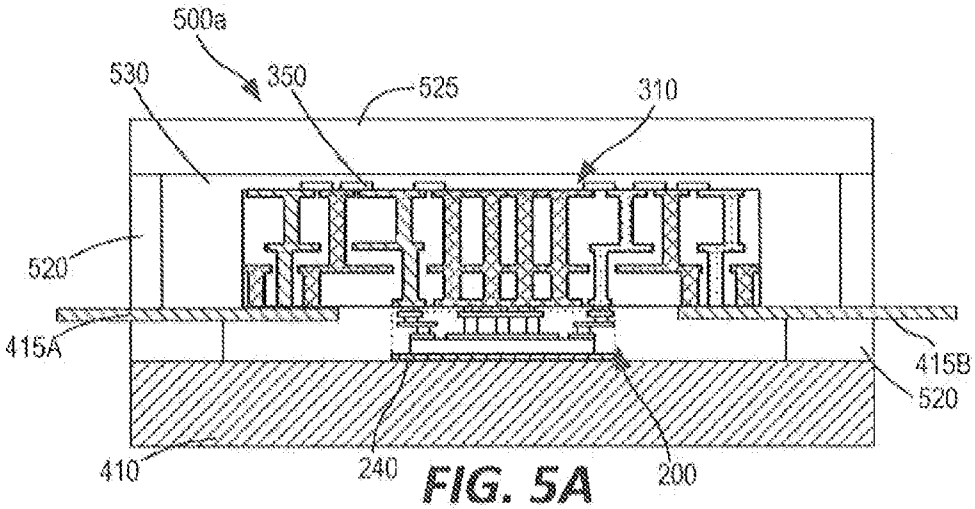


FIG. 5A

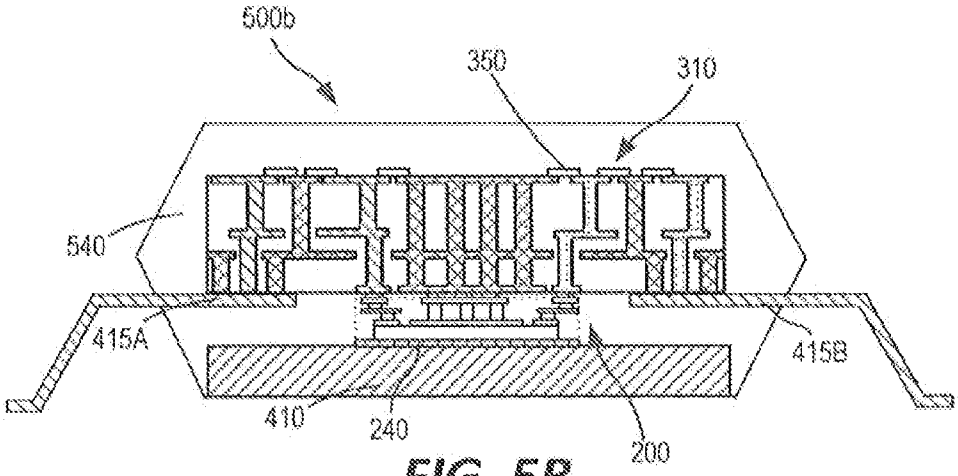


FIG. 5B

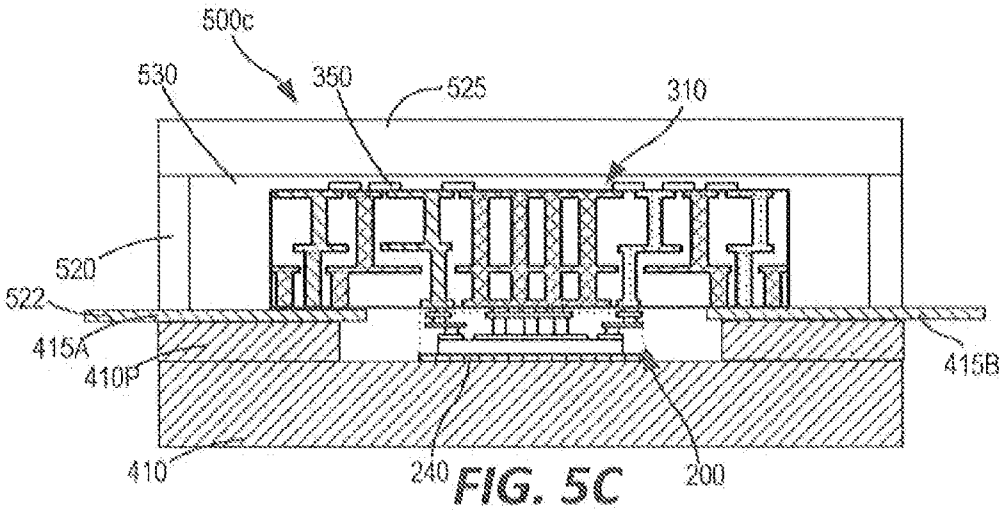


FIG. 5C

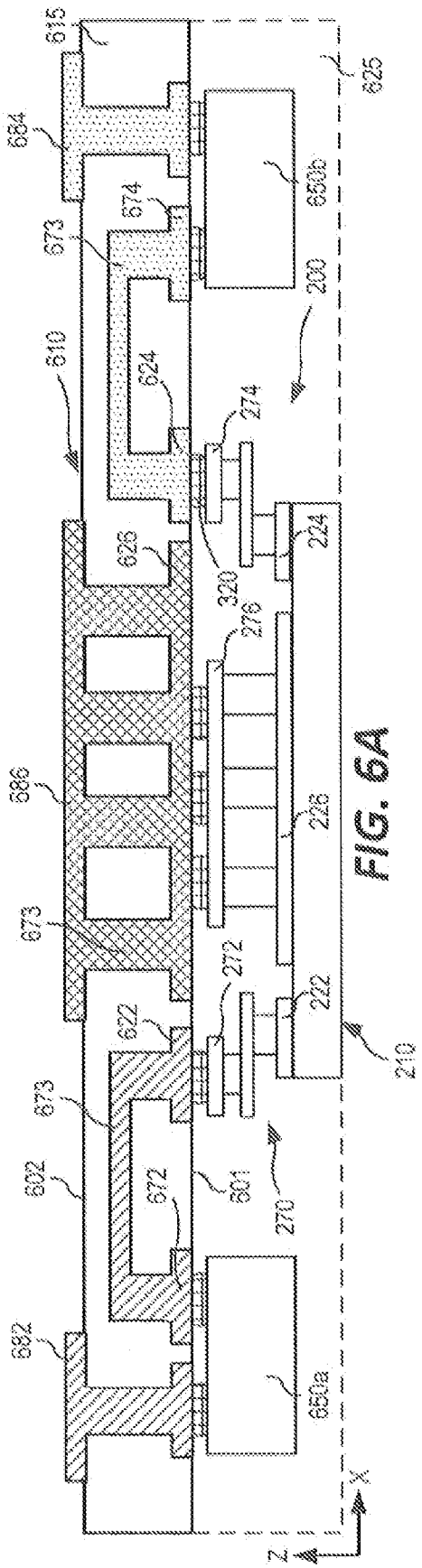

615
625
684
650b
673
674
200
610
624
274
320
626
224
276
686
226
673
272
622
222
210
673
602
672
601
270
682
650a
Z
X

FIG. 6A

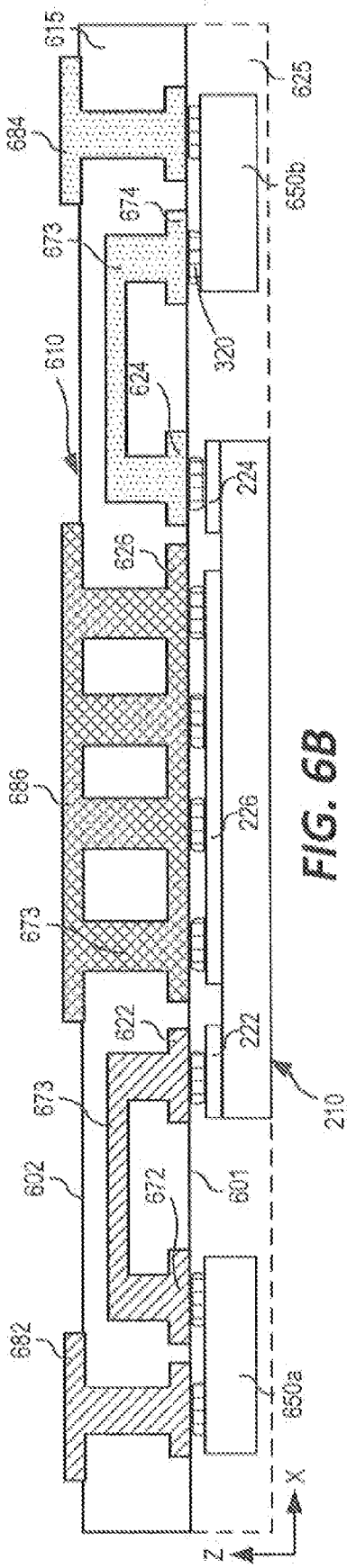

615
625
684
650b
673
674
320
610
624
224
626
686
226
673
622
222
210
673
602
672
601
682
650a
Z
X

FIG. 6B

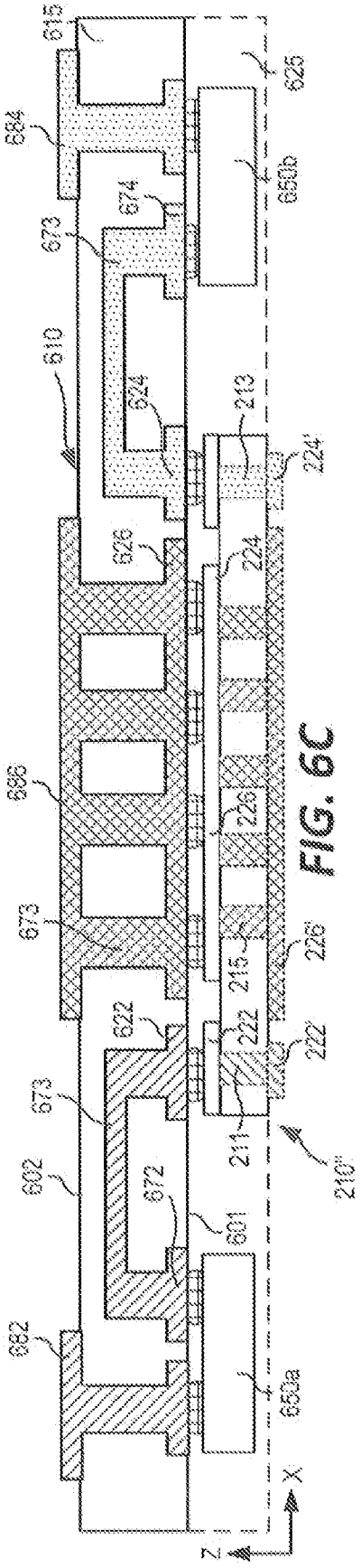

615
625
684
650b
674
673
610
624
213
224'
626
224
686
229
673
226'
215
622
222
222'
673
211
210"
602
672
601
682
650a
X
Z

FIG. 6C

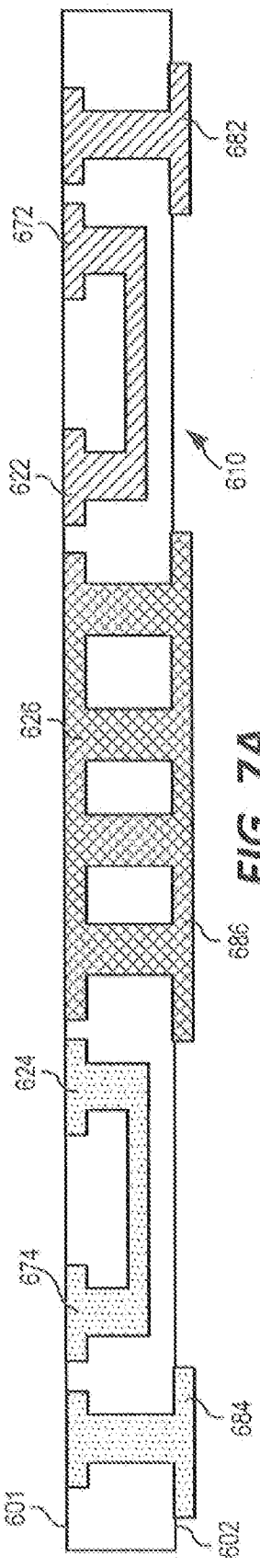

682
672
622
610
626
686
624
674
684
601
602

FIG. 7A

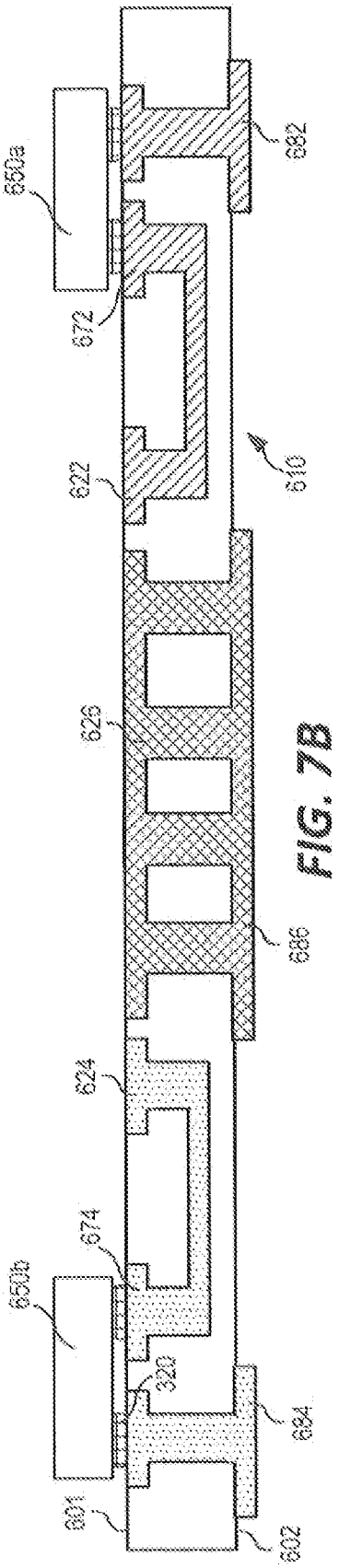

650a
672
682
622
610
626
686
624
674
650b
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684
601
602

FIG. 7B

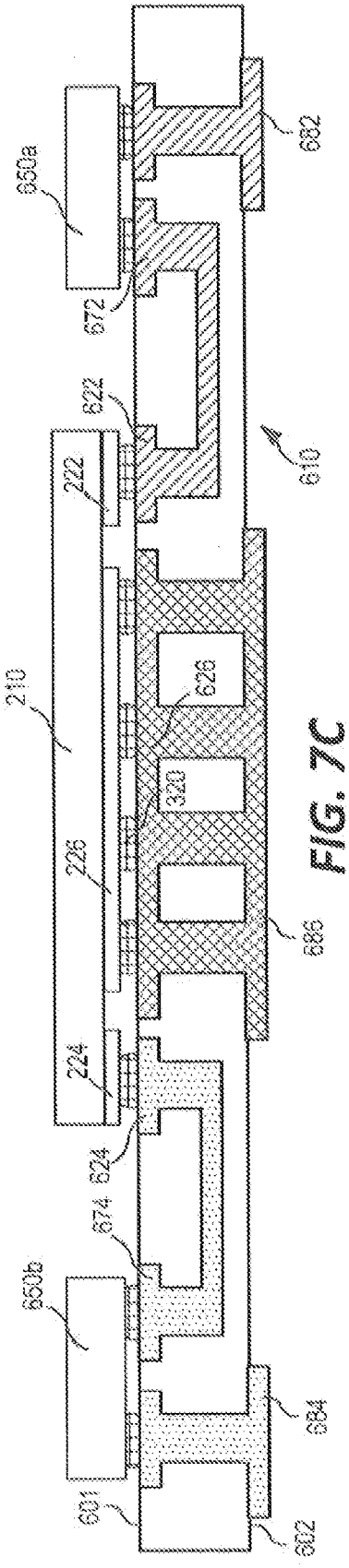

650a
672
682
622
222
610
210
626
320
226
686
224
624
674
650b
684
601
602

FIG. 7C

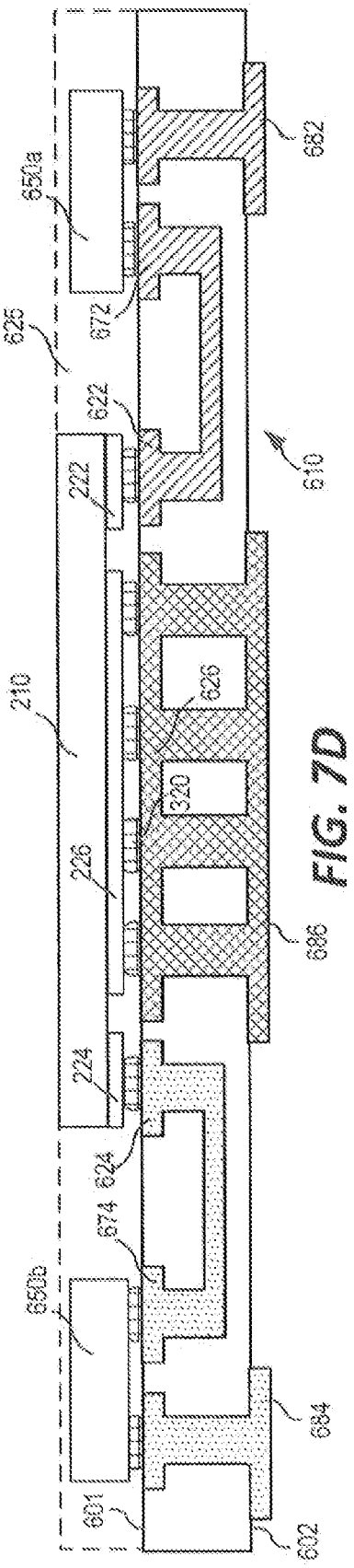

650a
682
672
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622
222
610
210
626
320
226
686
224
624
674
650b
684
601
602

FIG. 7D

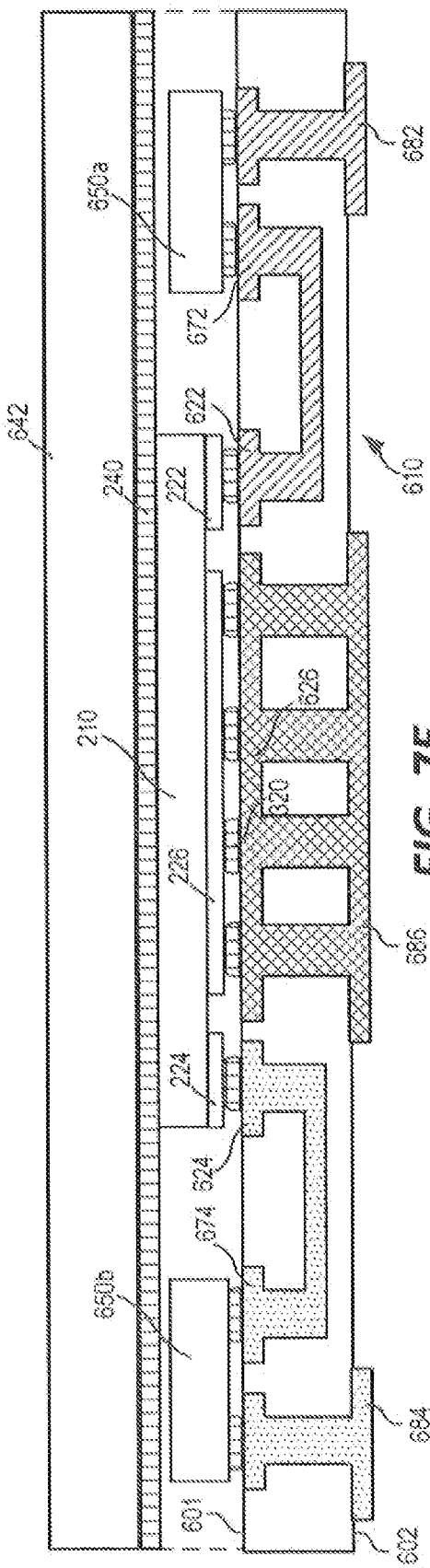

650a
682
672
642
622
240
222
610
210
626
320
226
686
224
624
674
650b
684
601
602

FIG. 7E

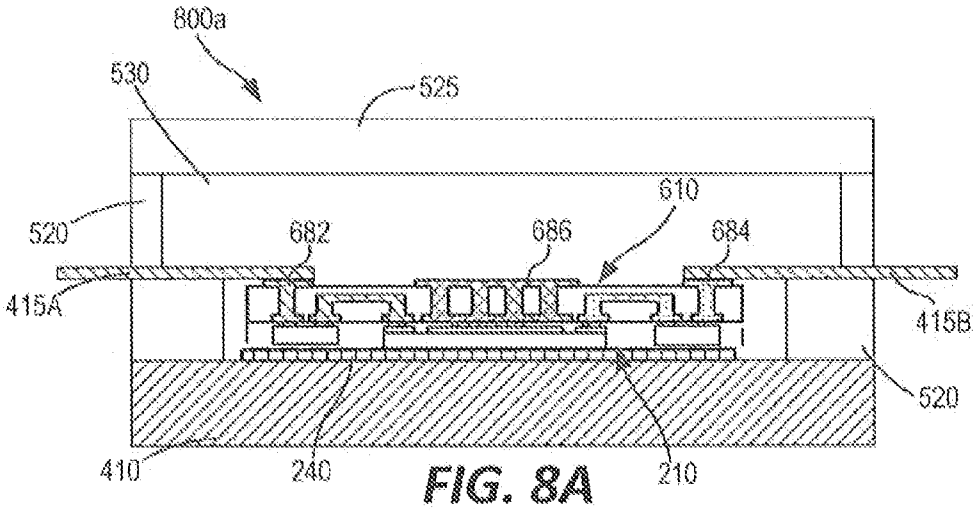

800a
530
525
610
520
682
686
684
415A
415B
520
410
240
210

FIG. 8A

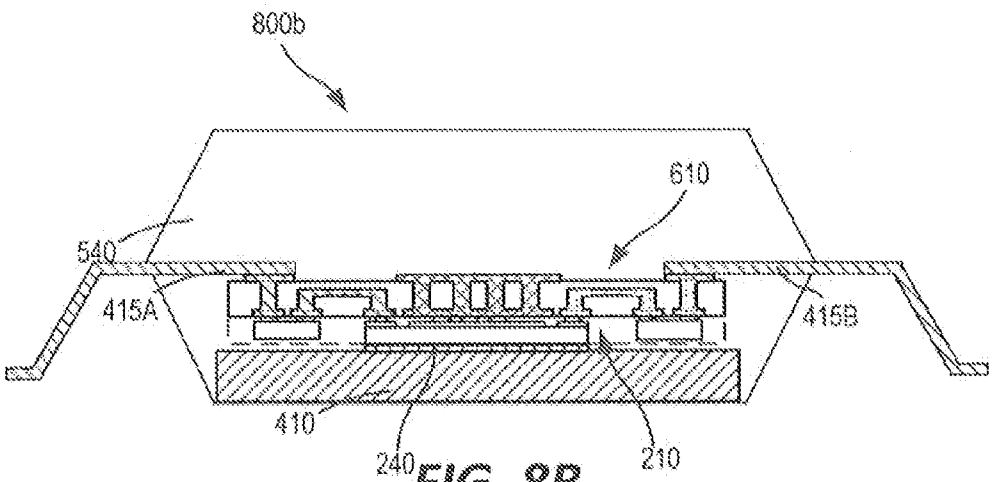

800b
610
540
415A
415B
410
240
210

FIG. 8B

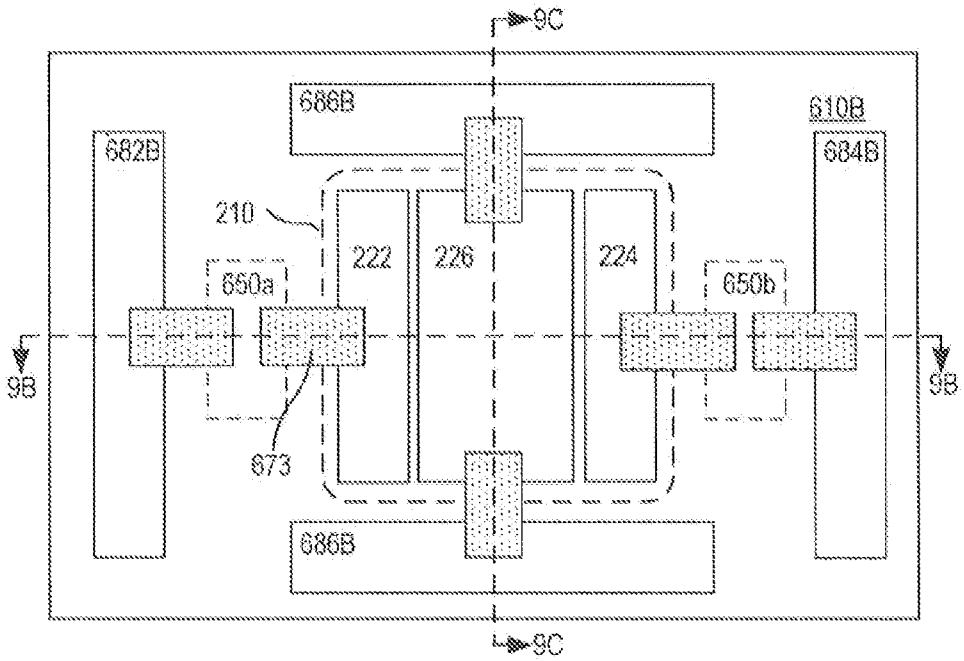

9C
686B
610B
682B
684B
210
222
226
224
650a
650b
9B
9B
673
686B
9C

FIG. 9A

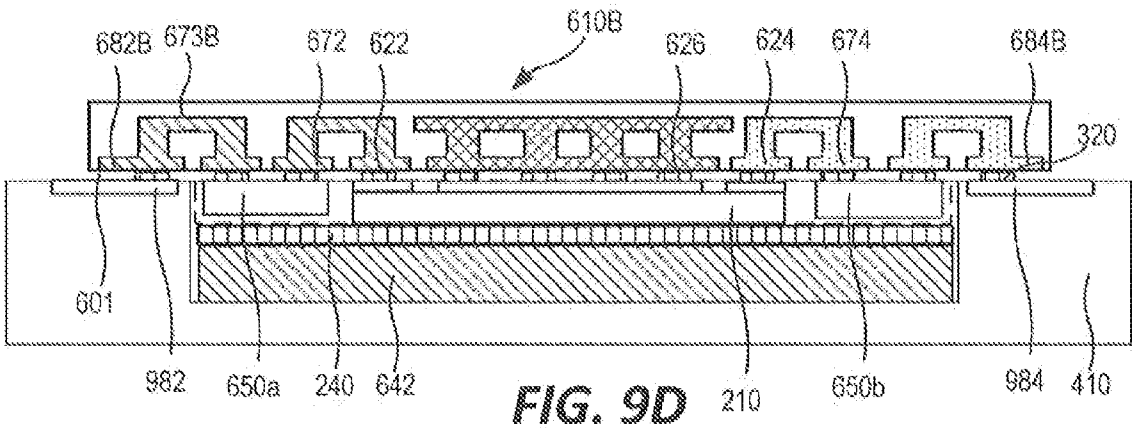

610B
682B
673B
672
622
626
624
674
684B
320
601
982
650a
240
642
210
650b
984
410

FIG. 9D

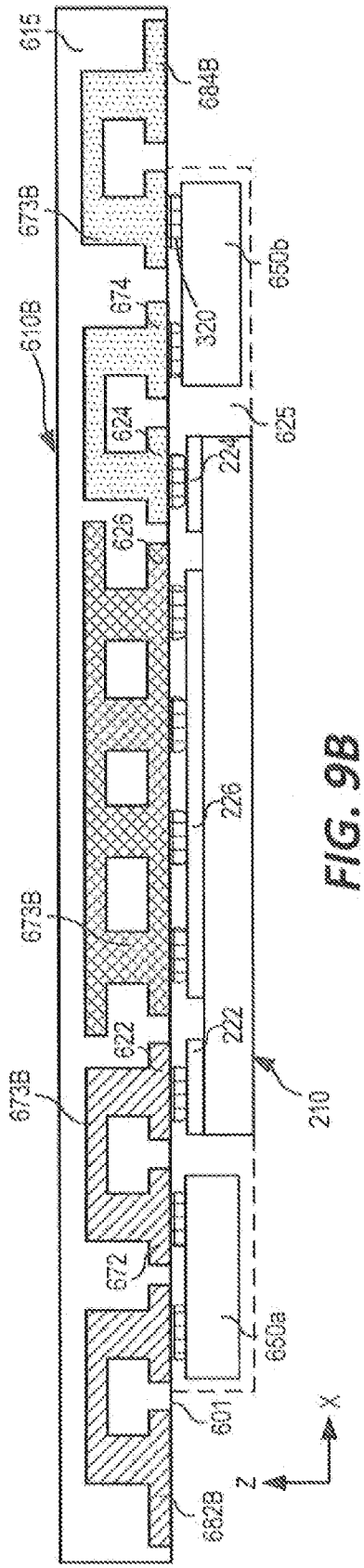

615
684B
673B
650b
610B
674
320
624
625
224
626
226
673B
622
222
673B
210
672
650a
601
X
Z
682B

FIG. 9B

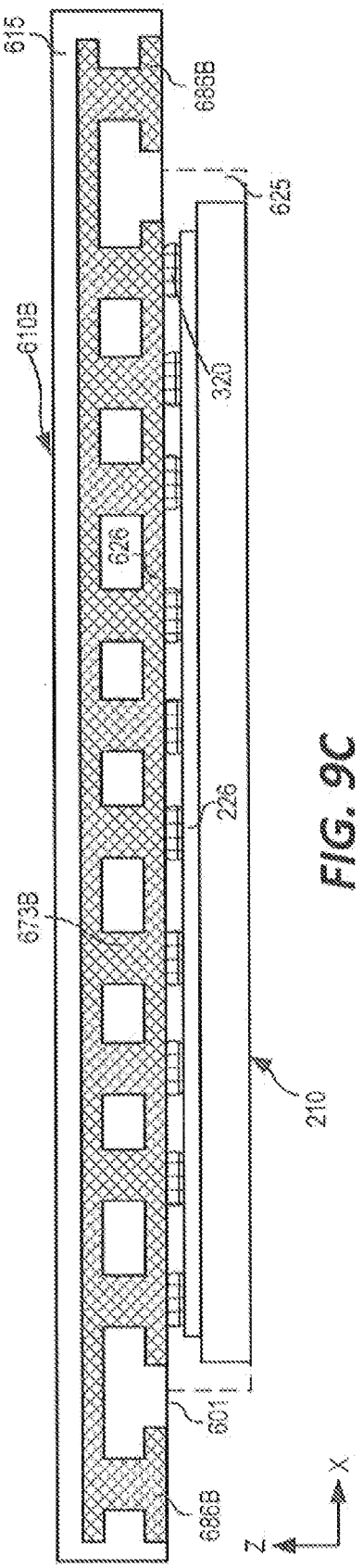

615
683B
625
610B
320
626
226
673B
210
601
X
Z
682B

FIG. 9C

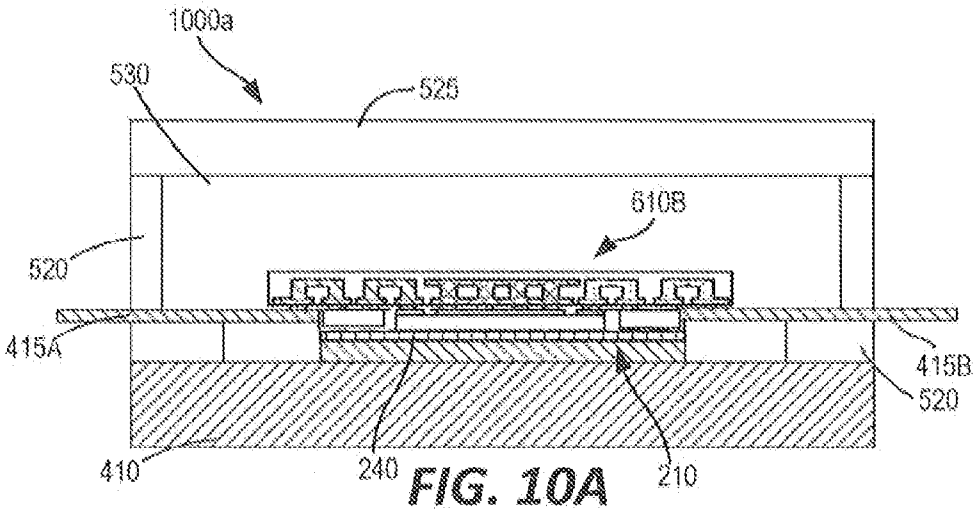


FIG. 10A

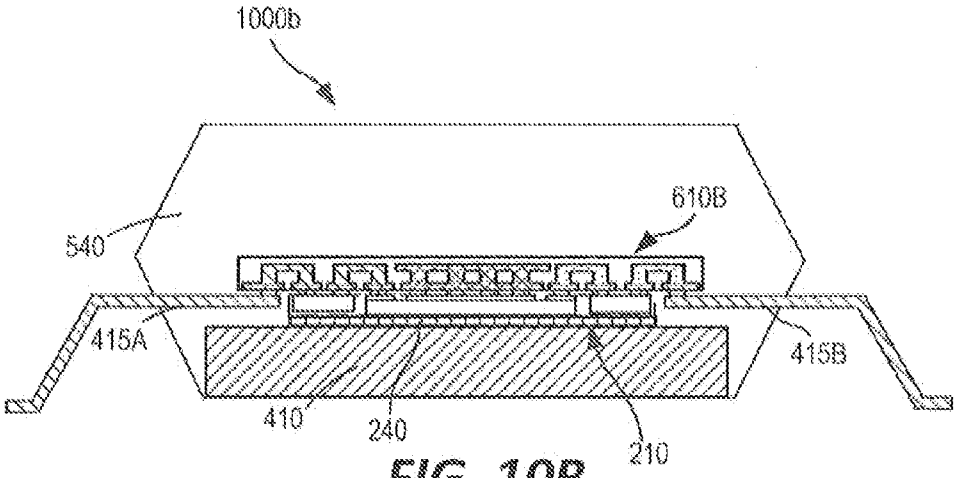


FIG. 10B

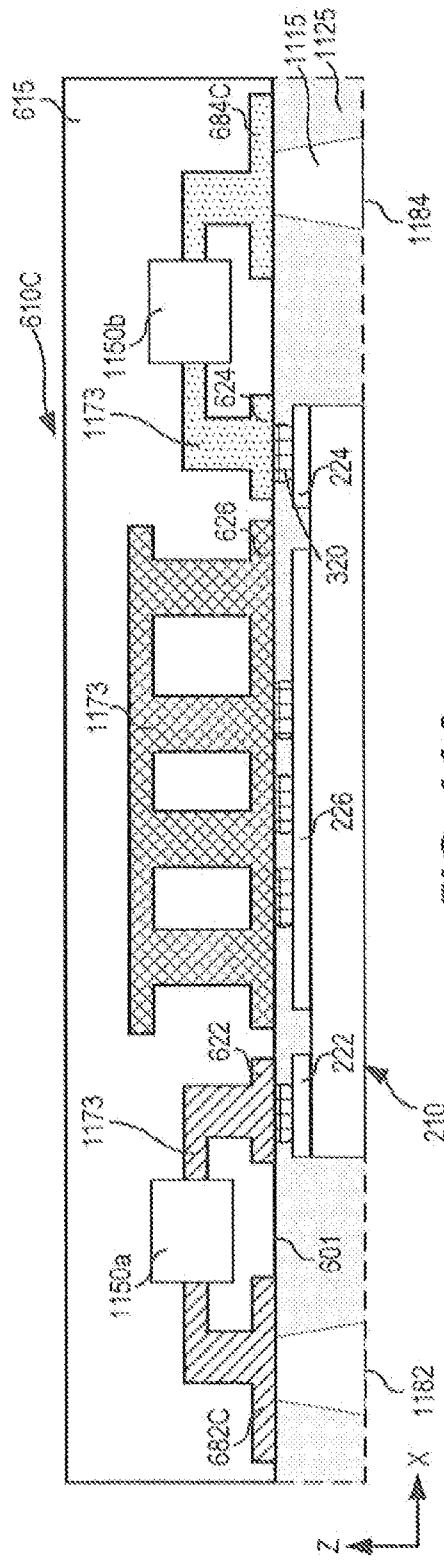


FIG. 11A

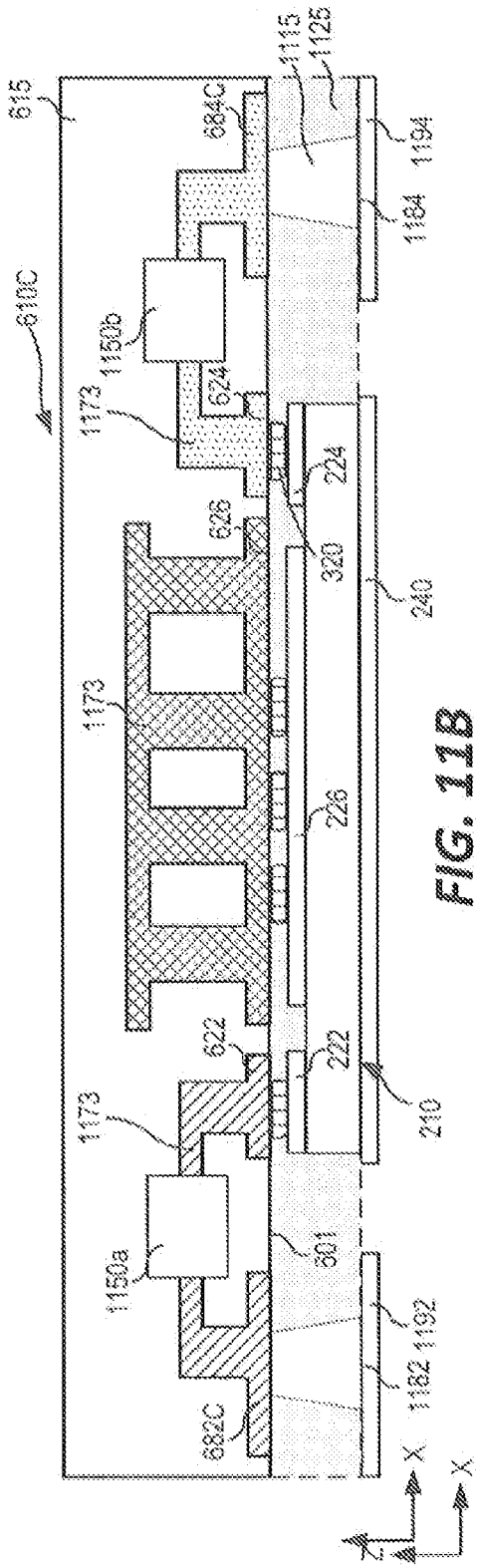


FIG. 11B

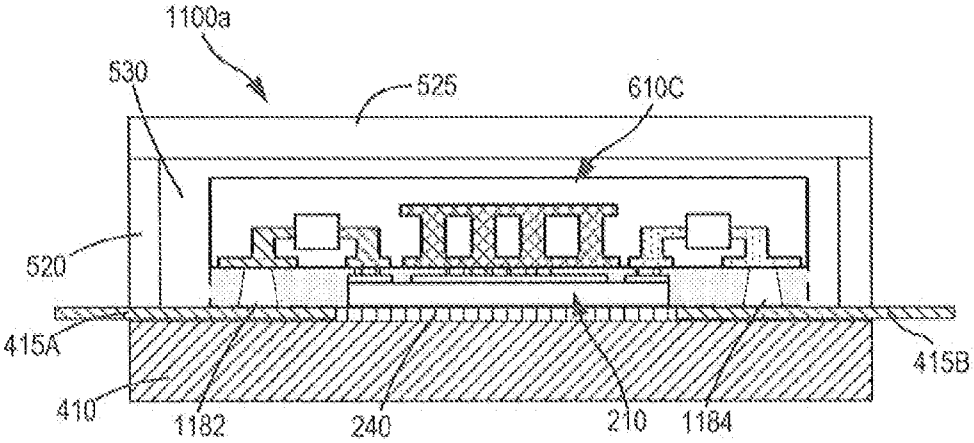


FIG. 11C

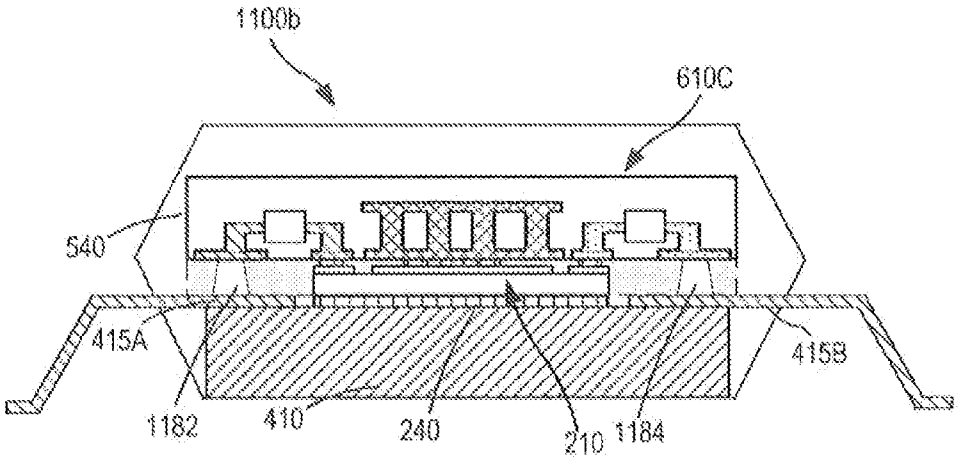


FIG. 11D

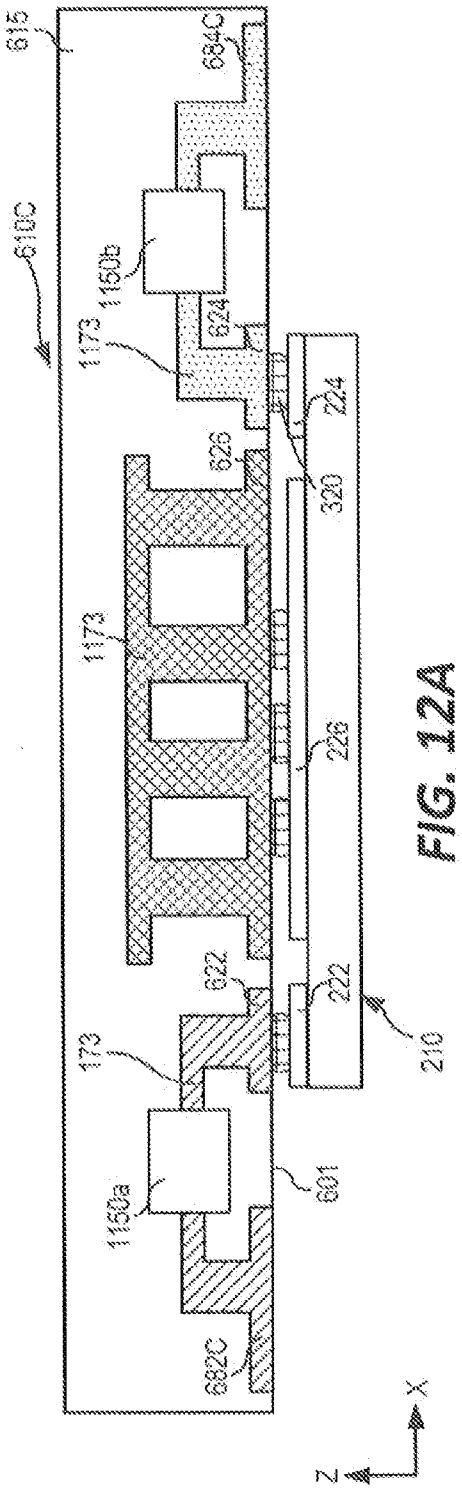


FIG. 12A

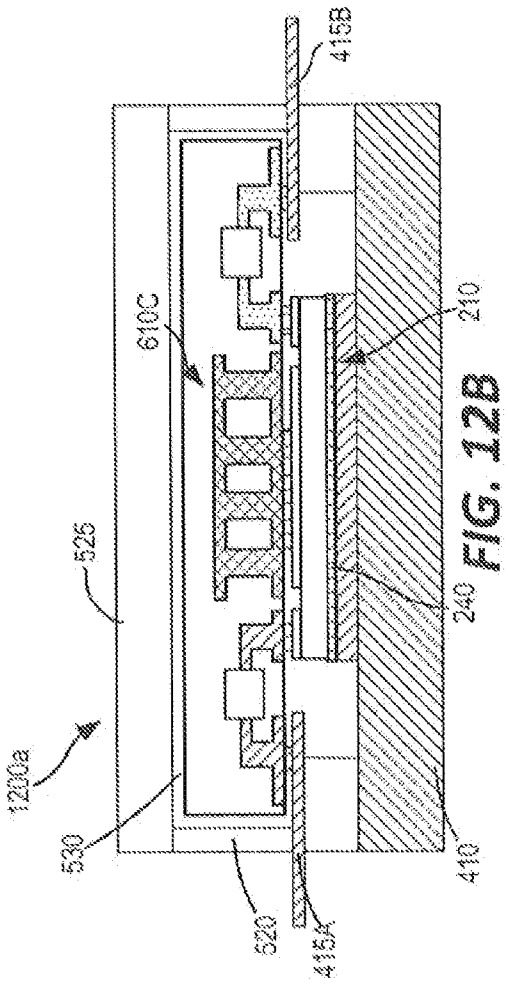


FIG. 12B

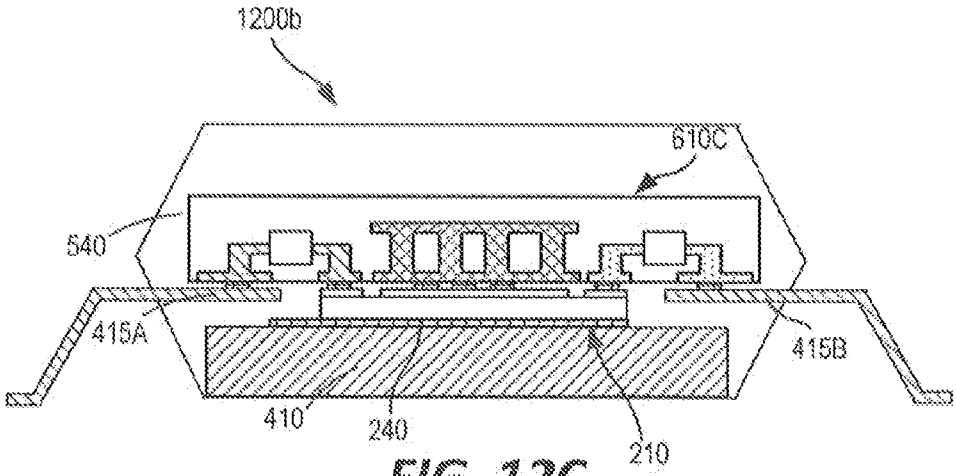


FIG. 12C

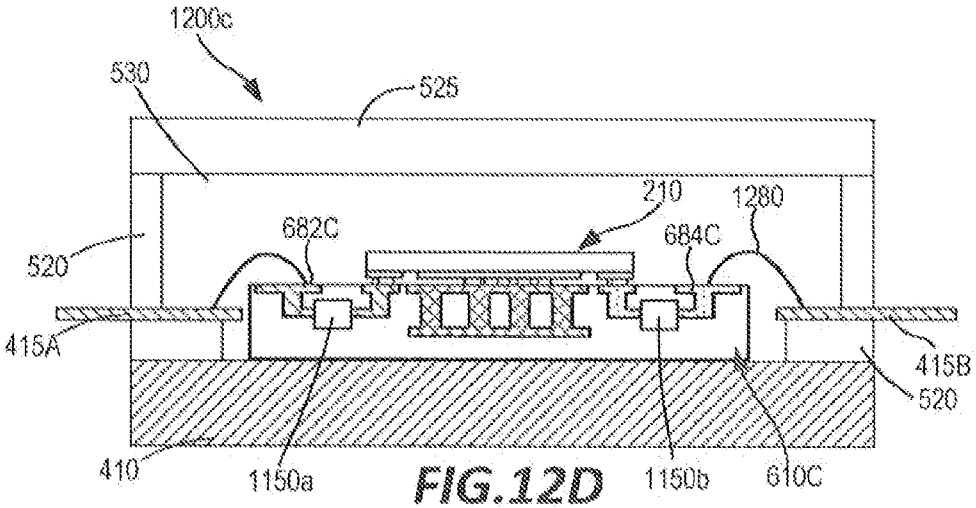


FIG. 12D

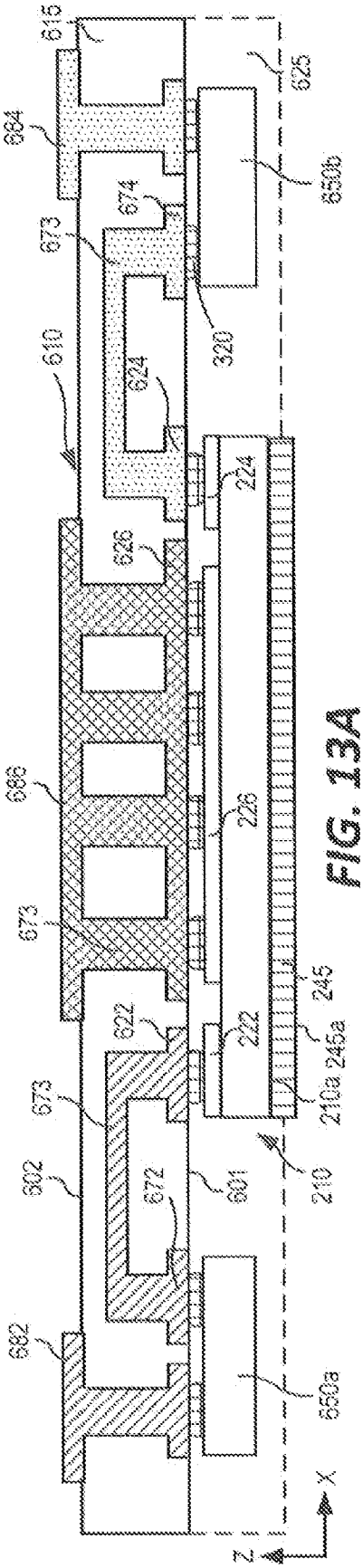


FIG. 13A

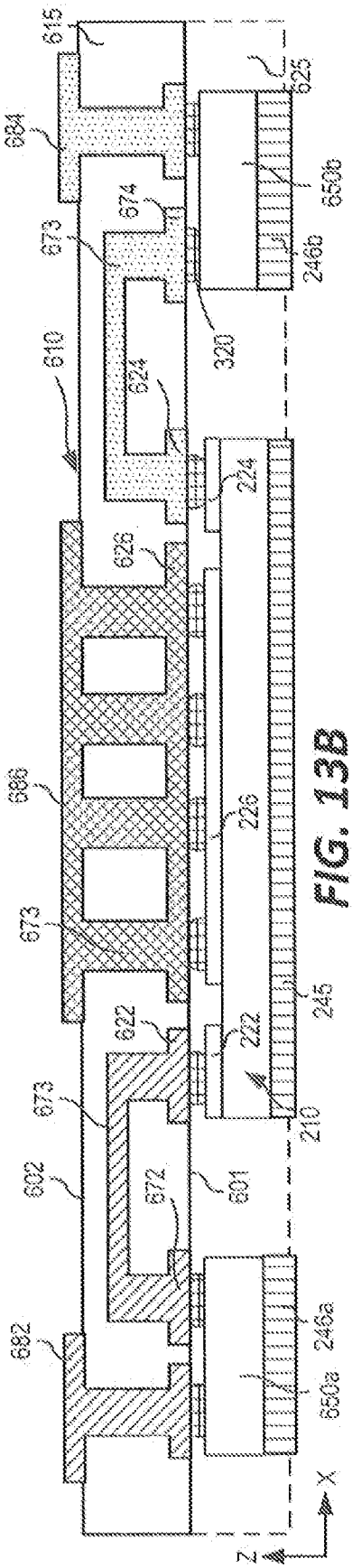


FIG. 13B

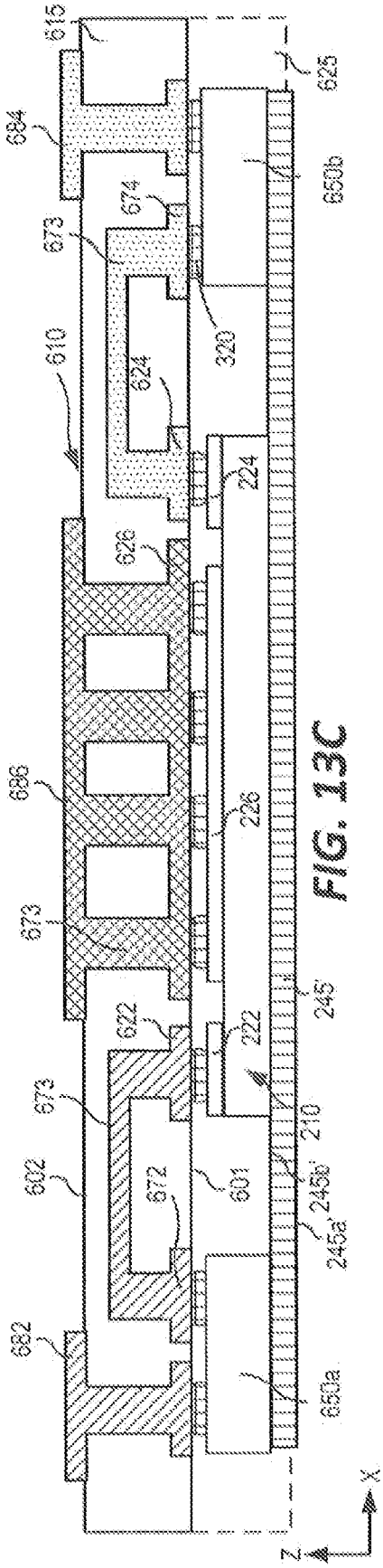


FIG. 13C

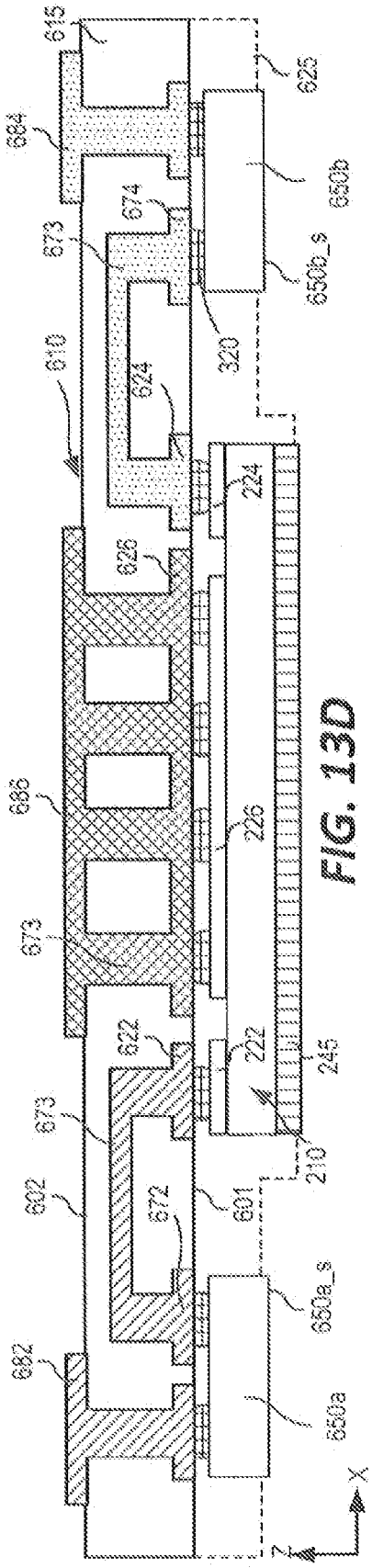


FIG. 13D

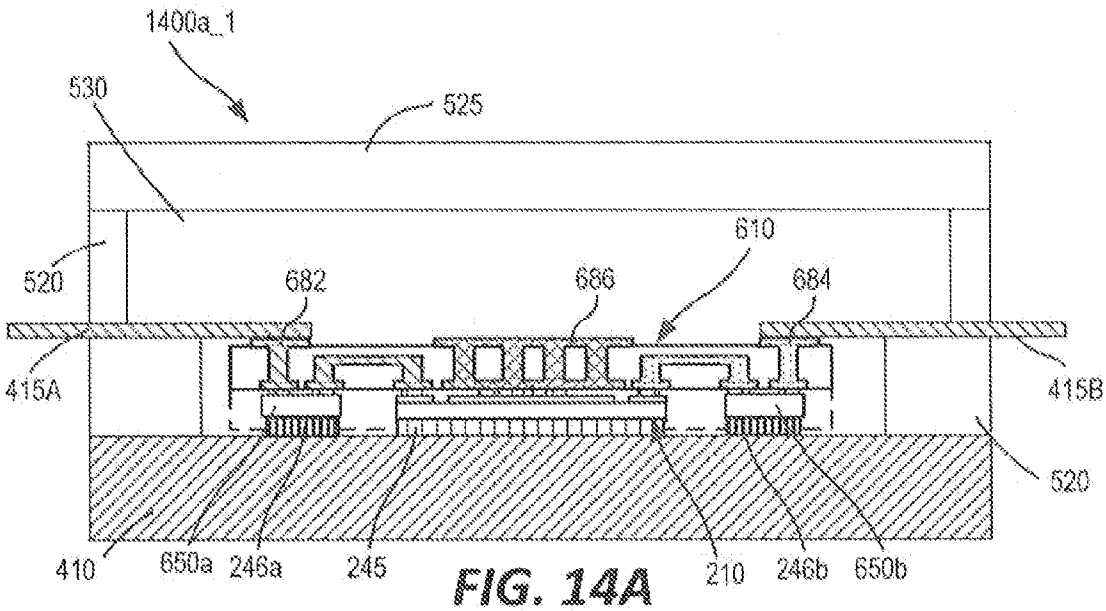


FIG. 14A

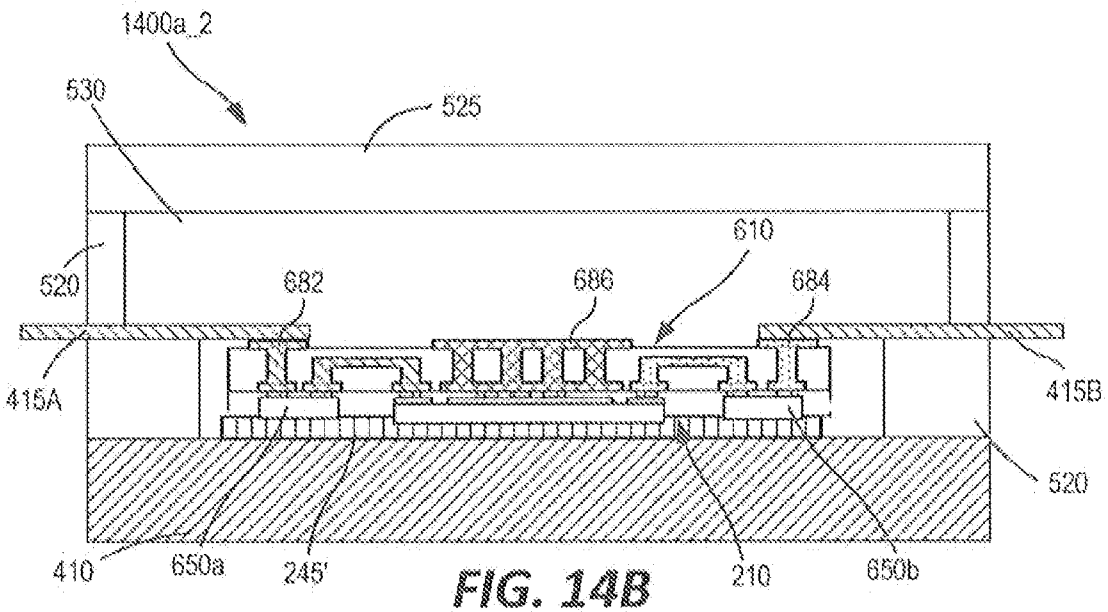


FIG. 14B

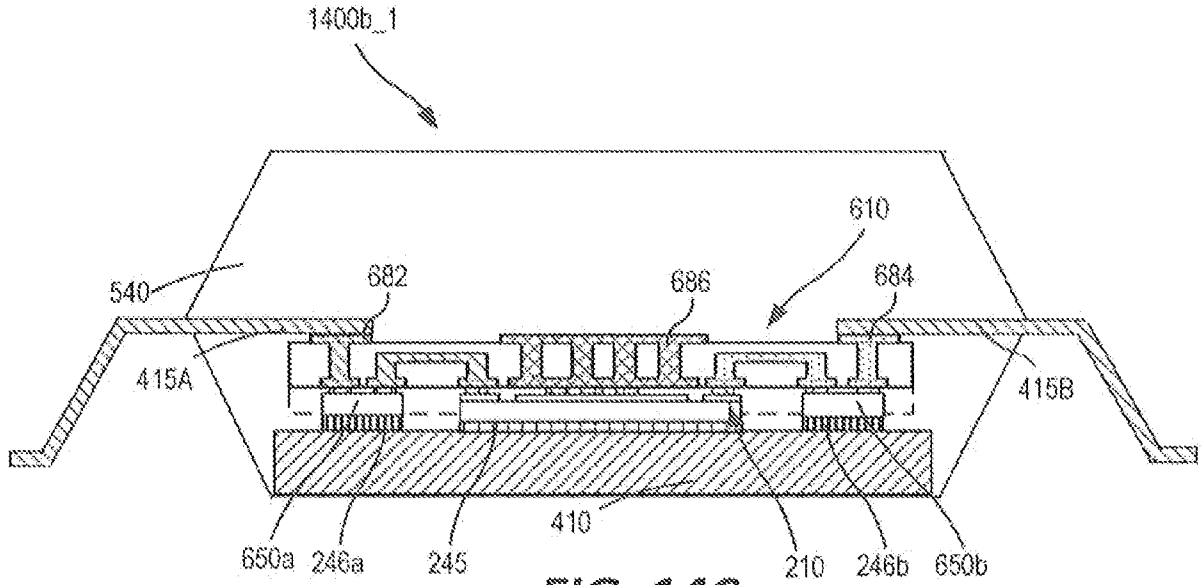


FIG. 14C

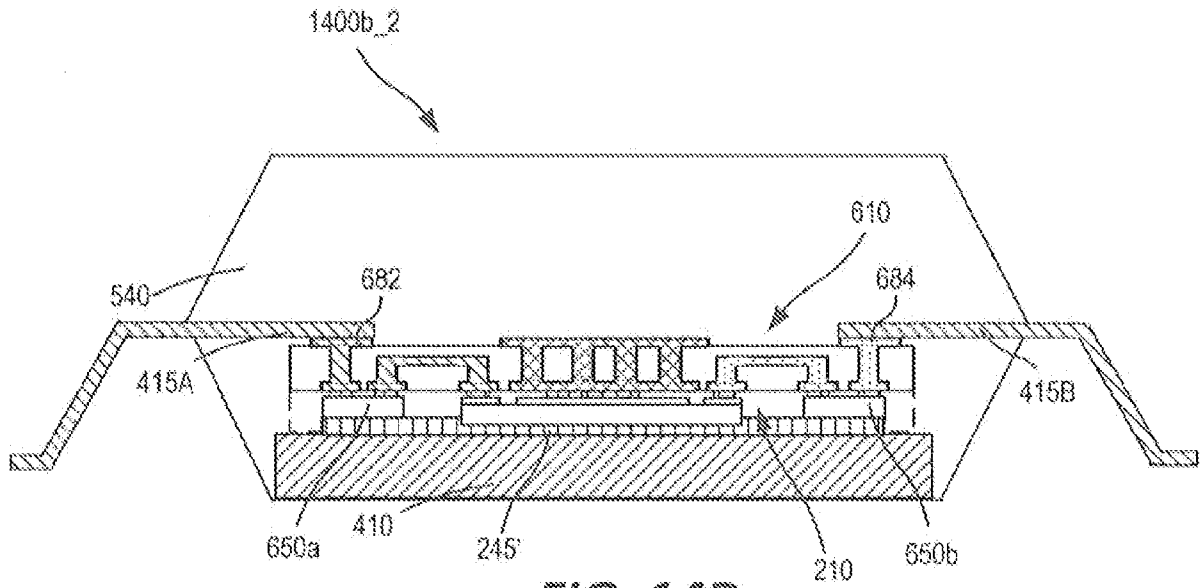


FIG. 14D

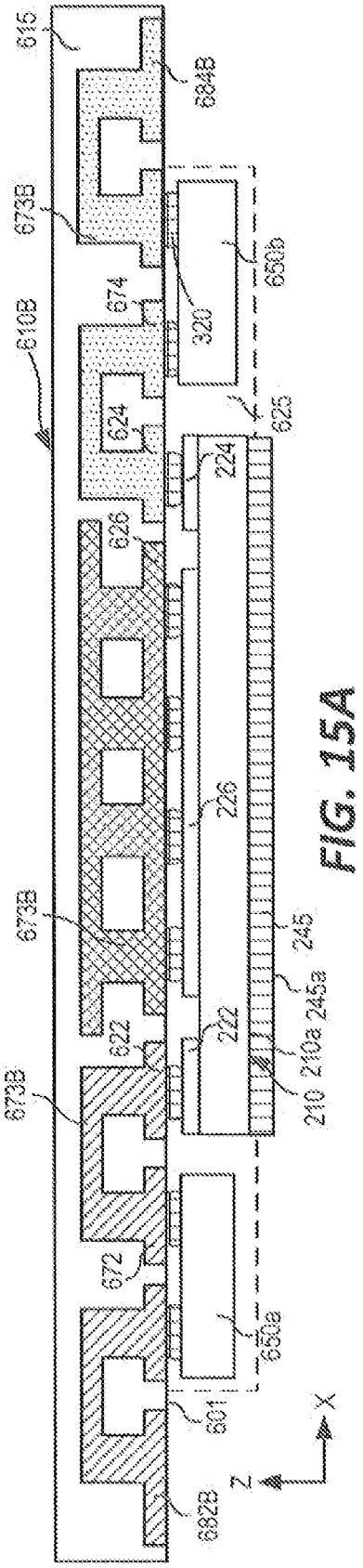


FIG. 15A

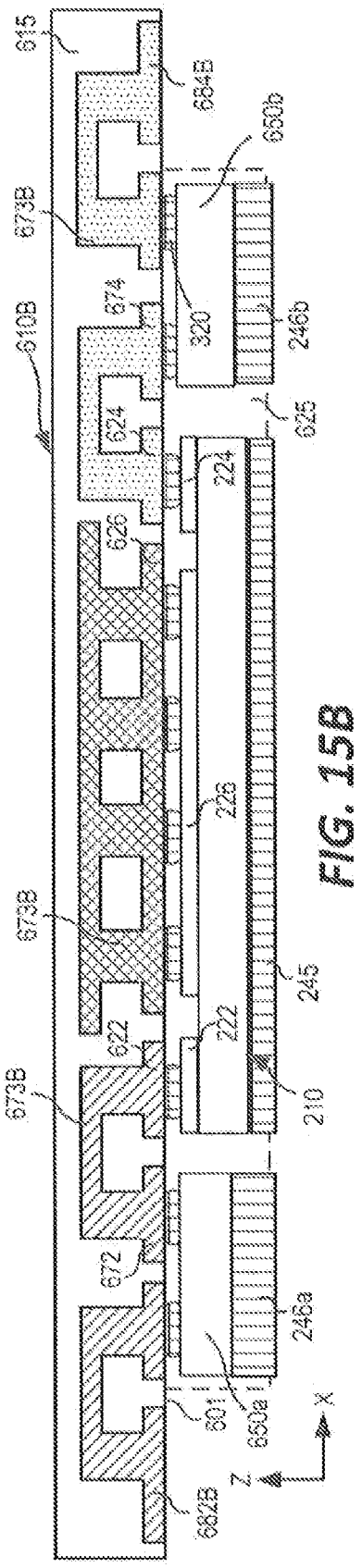


FIG. 15B

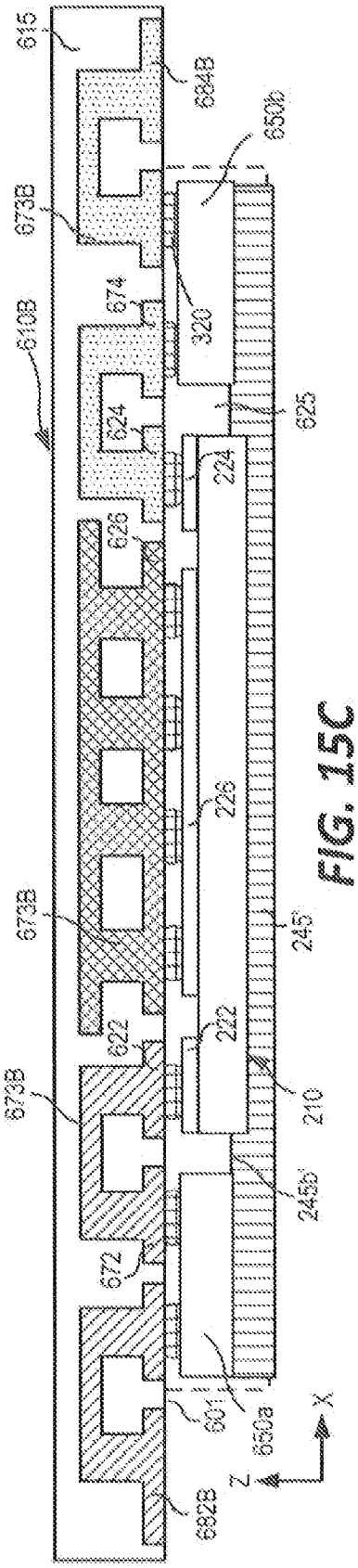


FIG. 15C

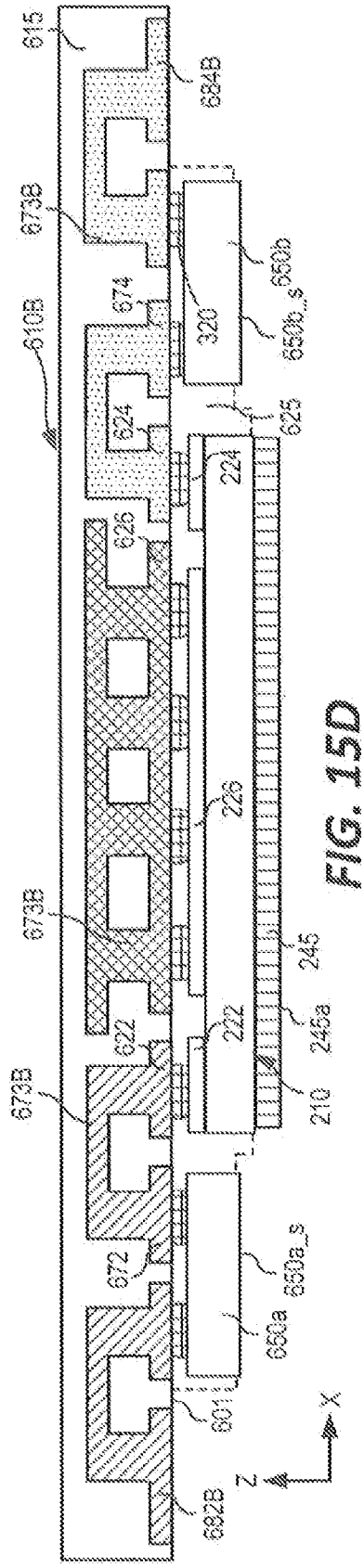


FIG. 15D

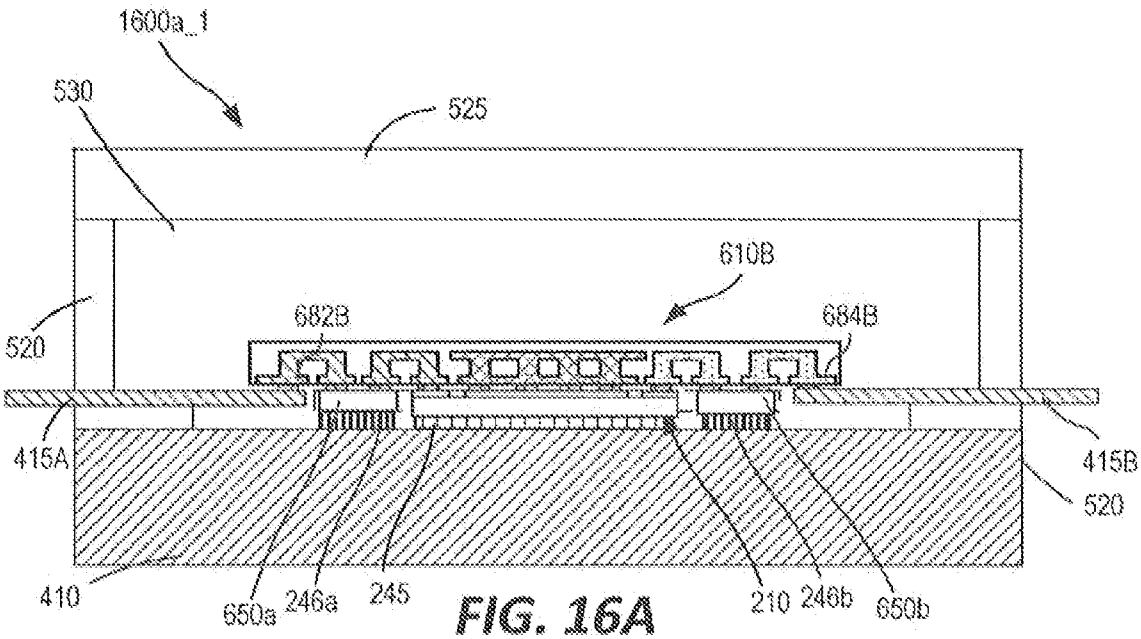


FIG. 16A

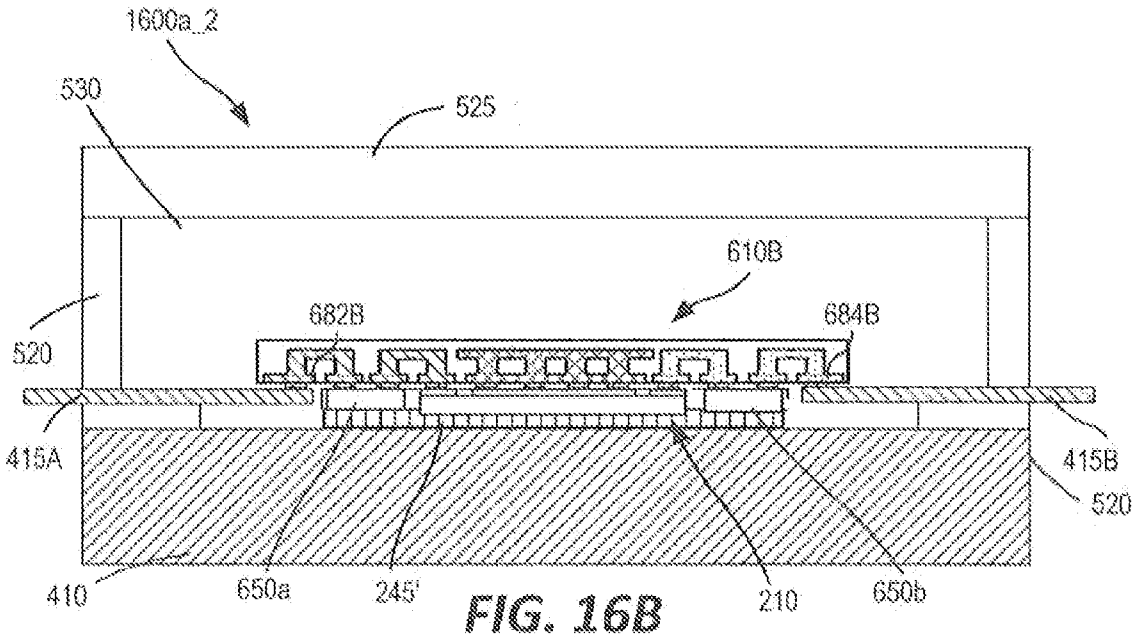


FIG. 16B

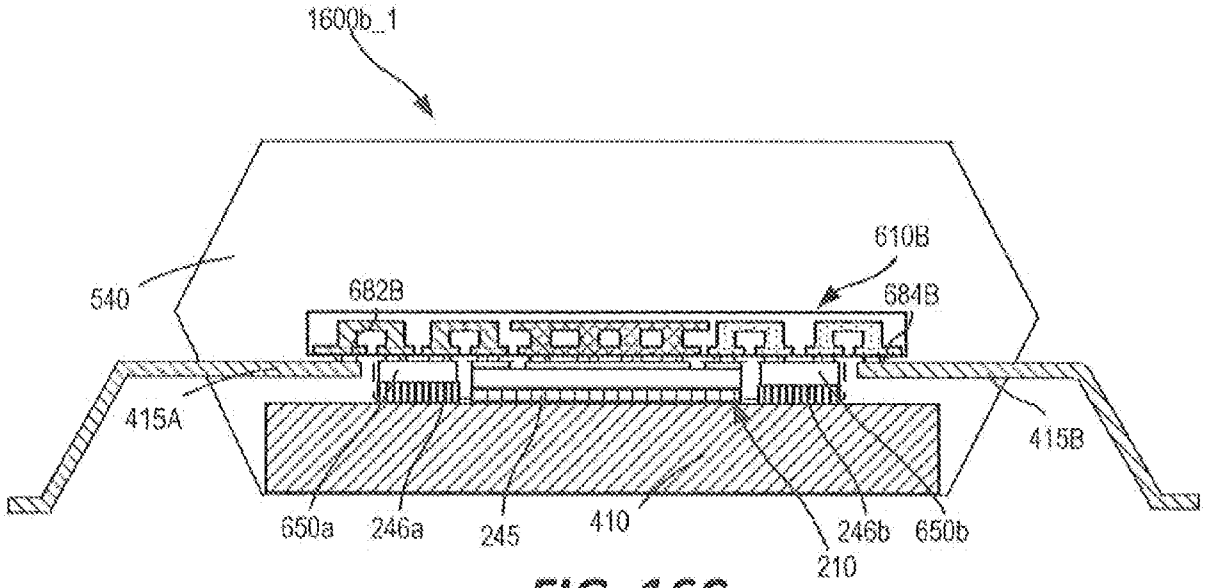


FIG. 16C

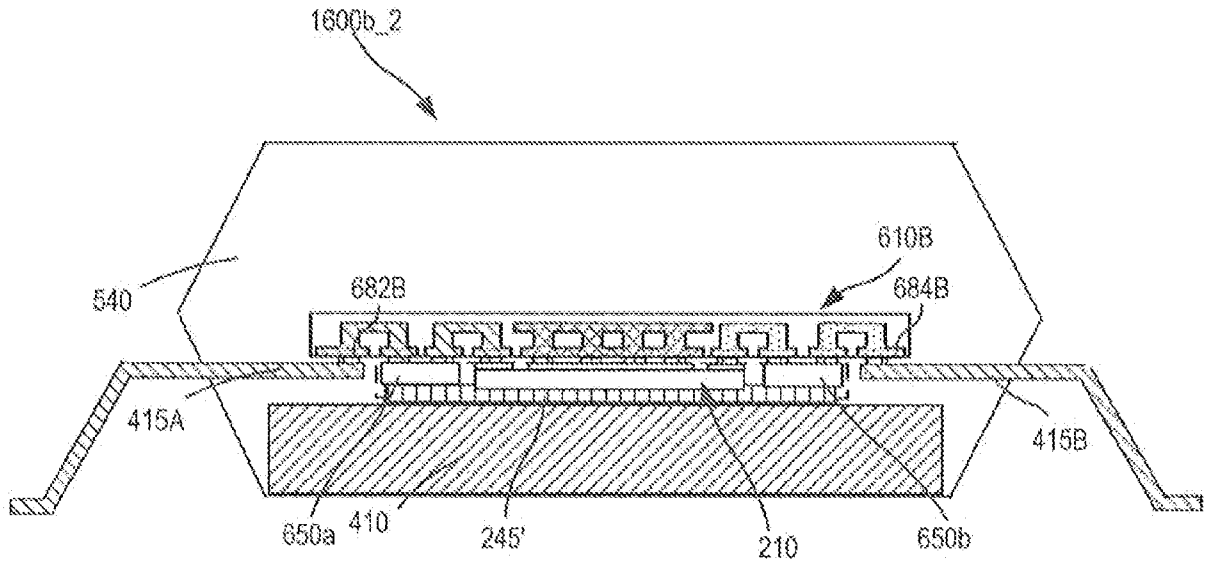


FIG. 16D

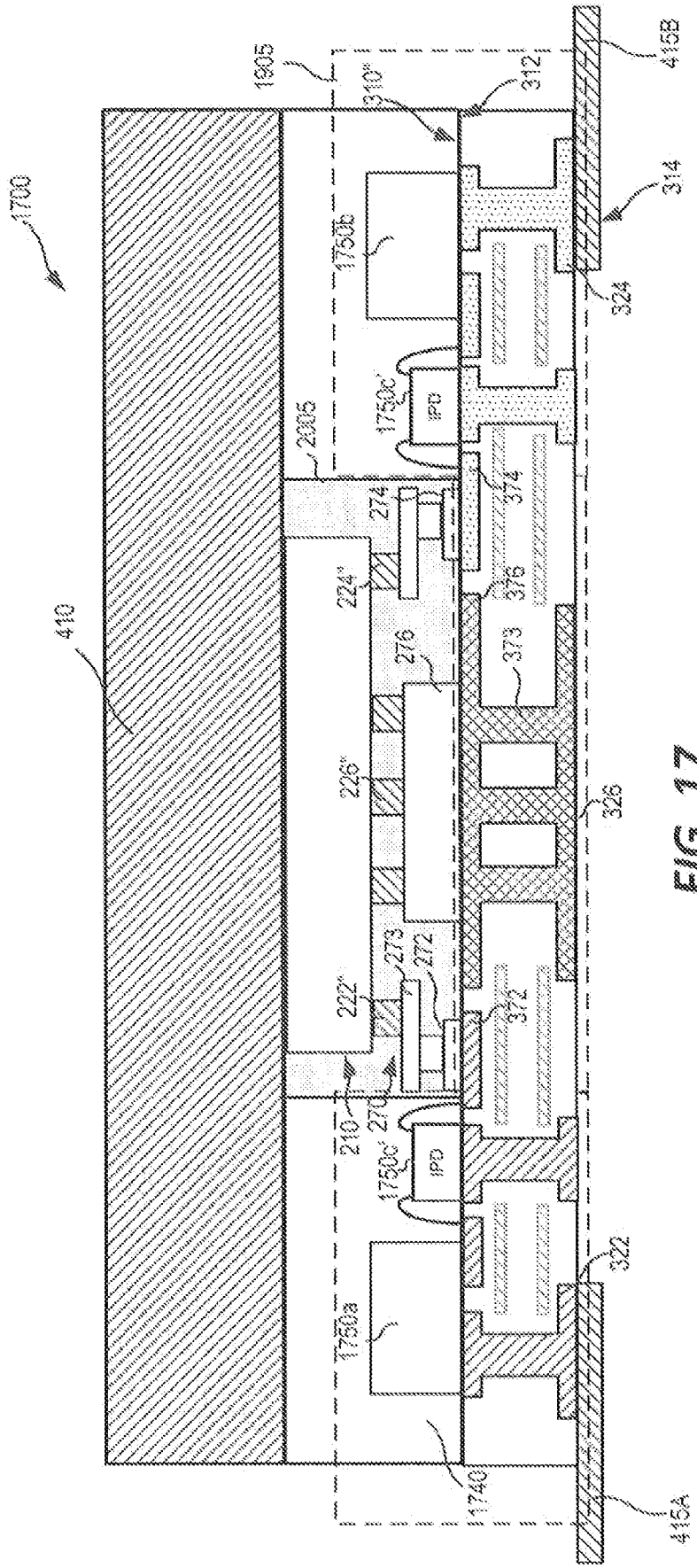

1700
1905
310"
312
415B
314
324
1750b
1750c'
IPD
2005
274
374
224"
376
410
276
373
226"
326
273
272
222"
372
210
270
1750a'
IPD
322
1750a
1740
415A
Z
X

FIG. 17

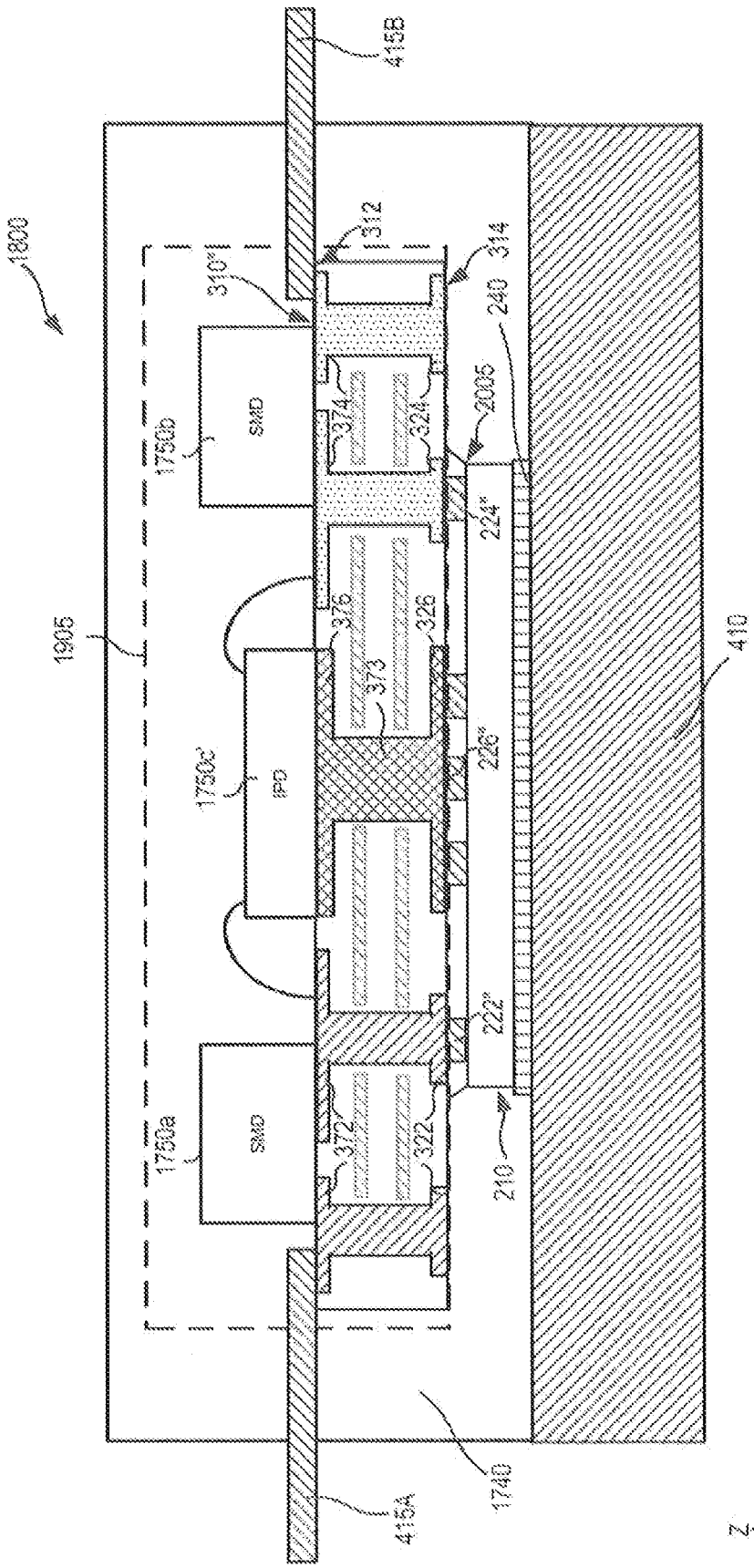

1800
1905
1750a
1750b
1750c'
SMD
SMD
IPD
310'
312
314
240
2005
372
374
373
376
322
324
326
222'
224'
226'
210
410
415A
415B
1740
Z
X

FIG. 18

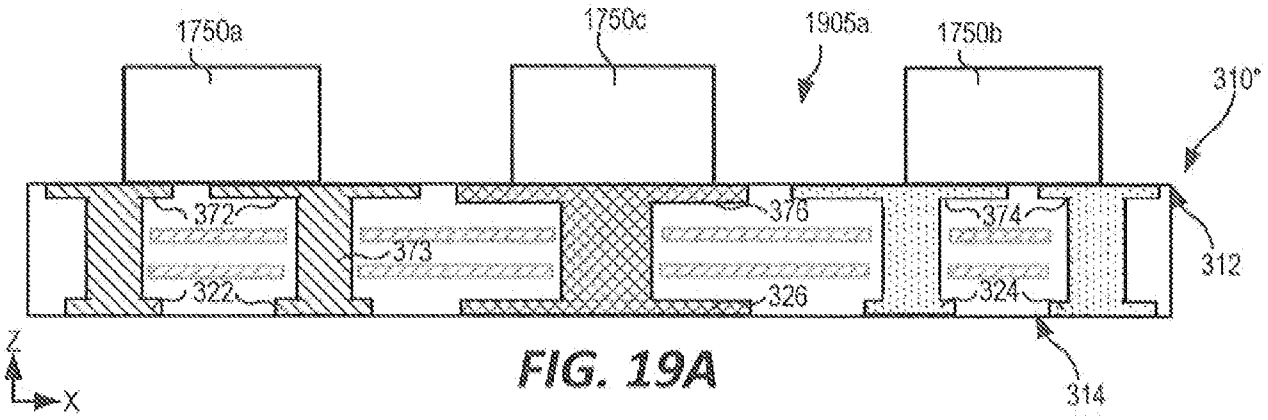


FIG. 19A

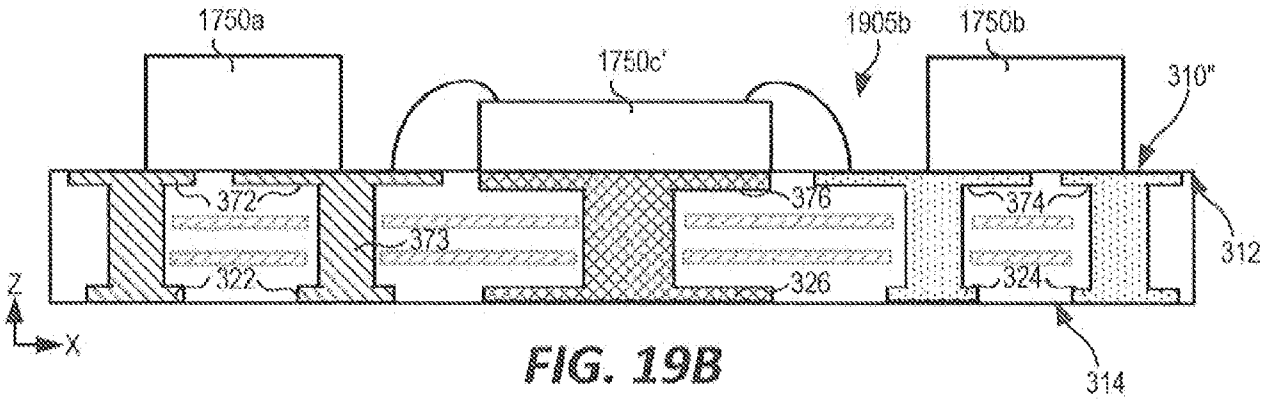


FIG. 19B

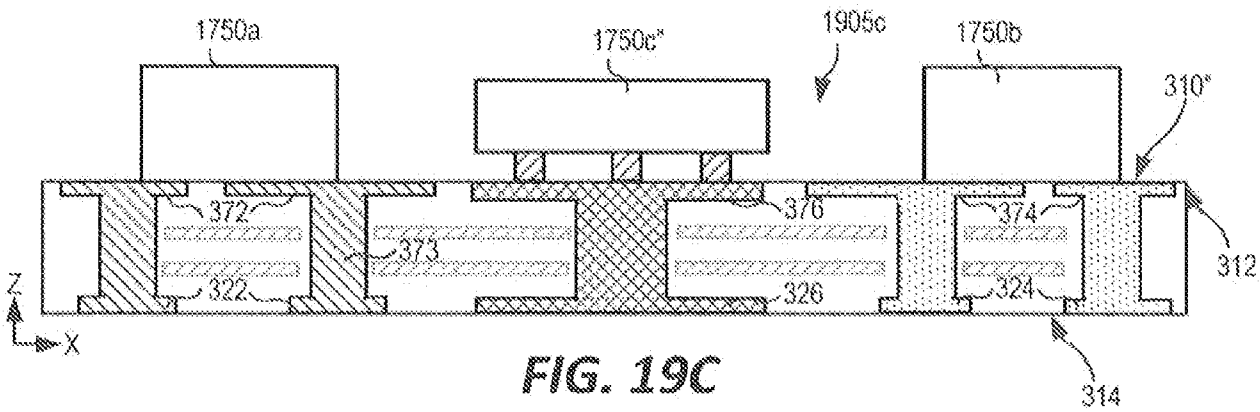


FIG. 19C

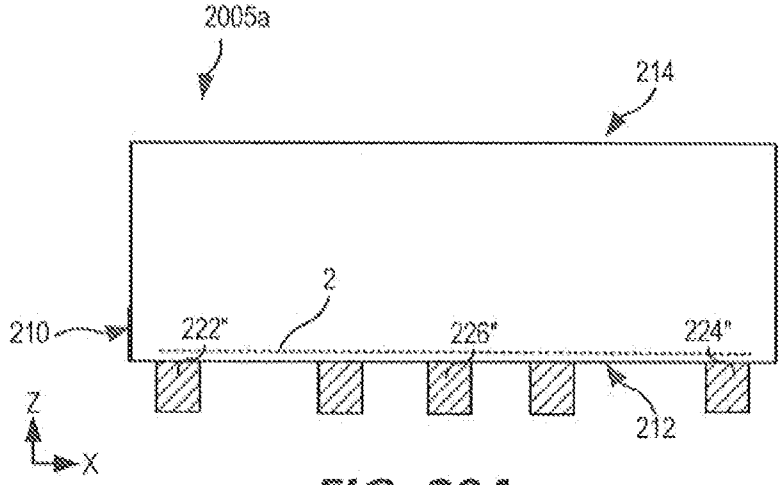


FIG. 20A

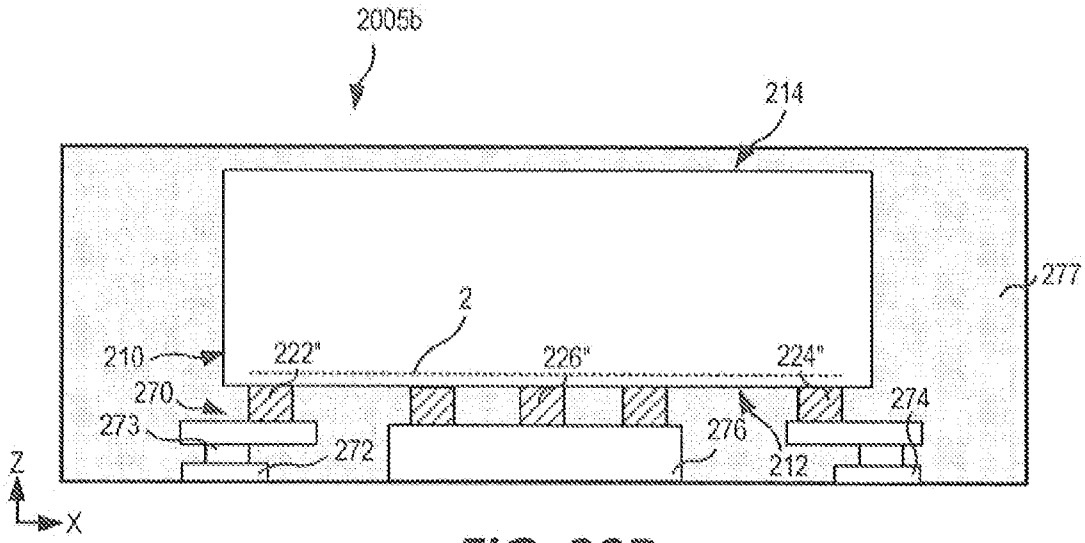


FIG. 20B

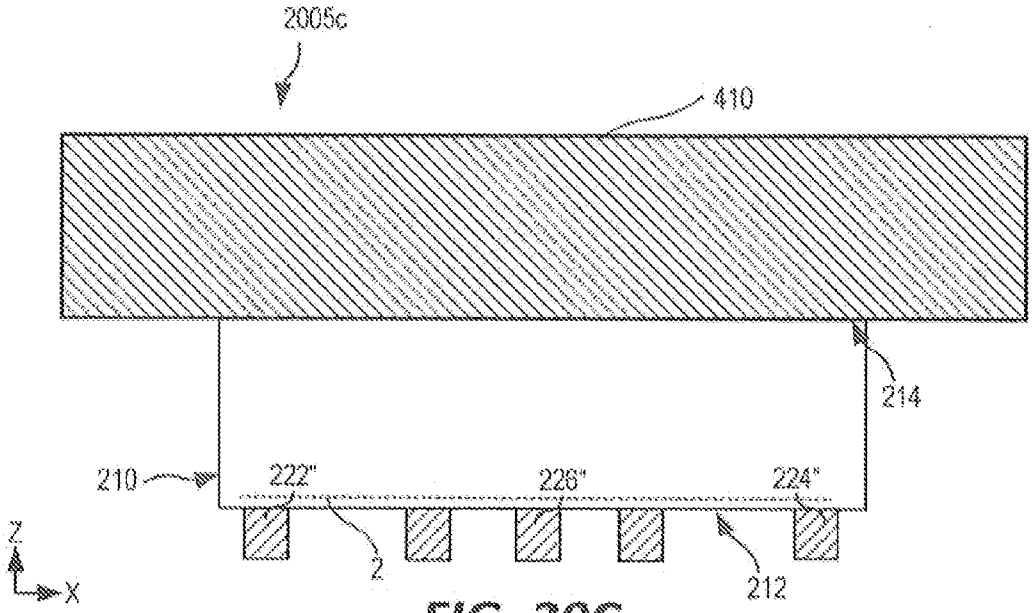


FIG. 20C

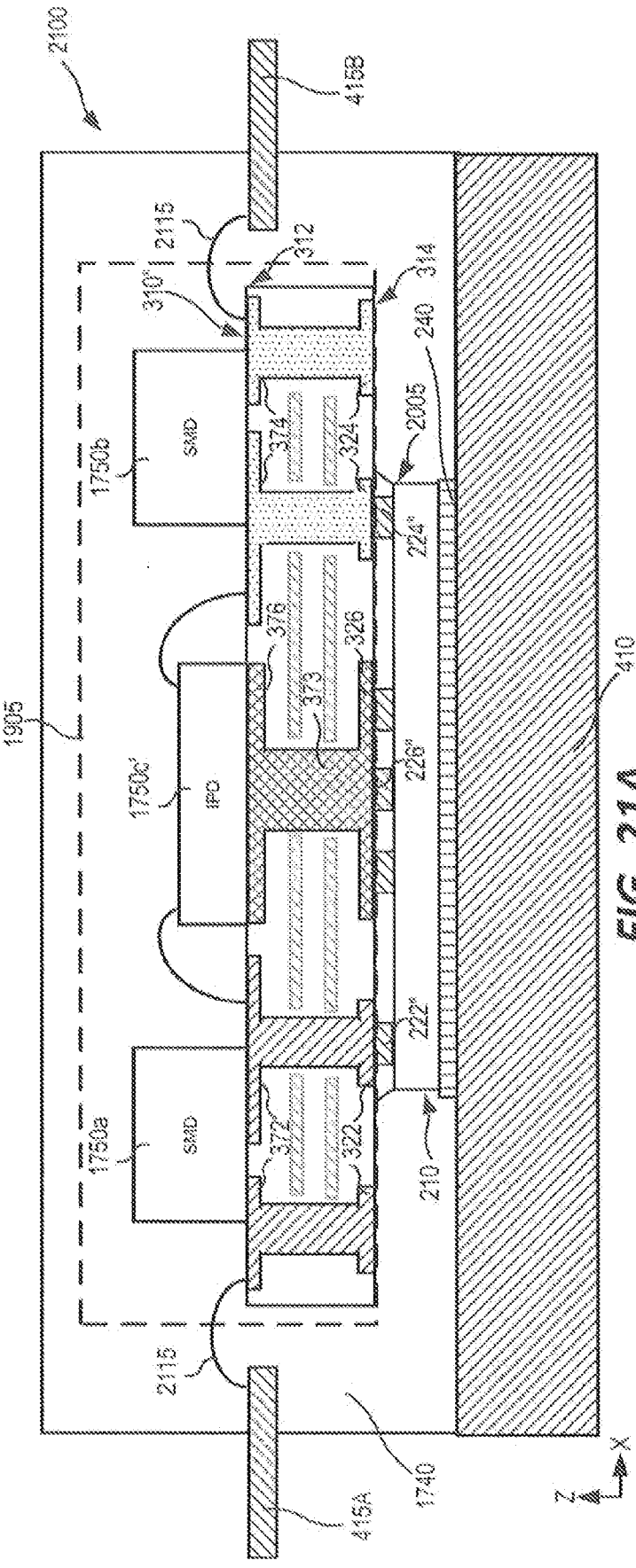


FIG. 21A

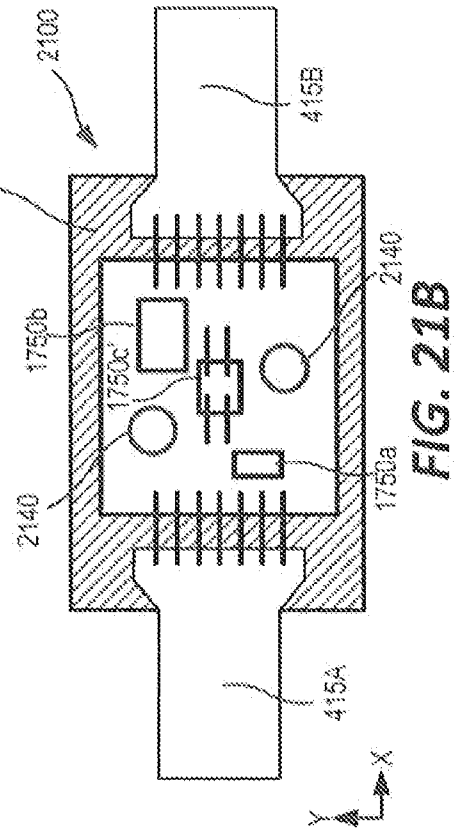


FIG. 21B

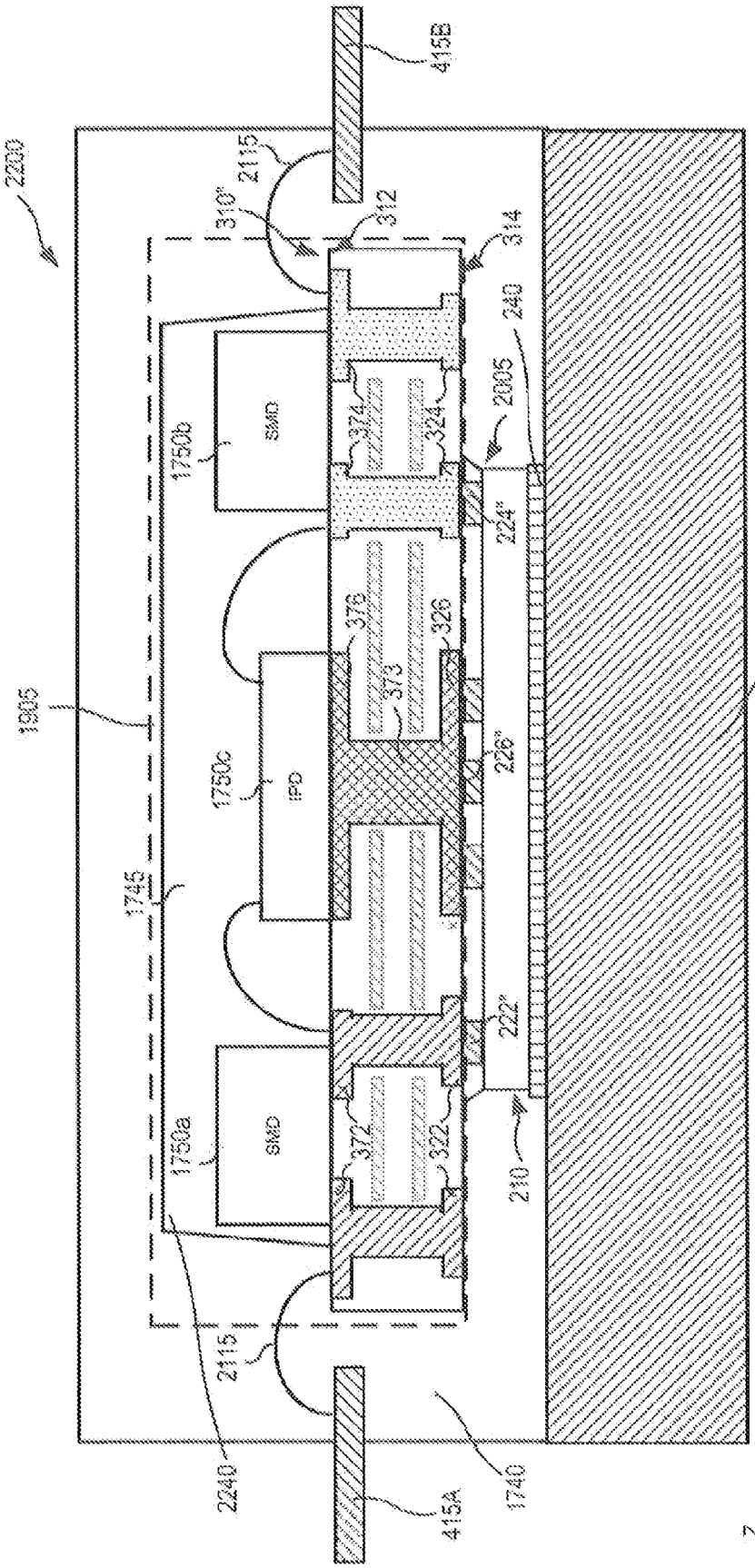

2200
415B
2115
310"
312
314
240
2005
1750b
SMD
374
324
224"
376
326
373
1905
1750c
IPD
226"
410
1745
222"
1750a
SMD
372
322
210
2115
2240
415A
1740
Z
X

FIG. 22

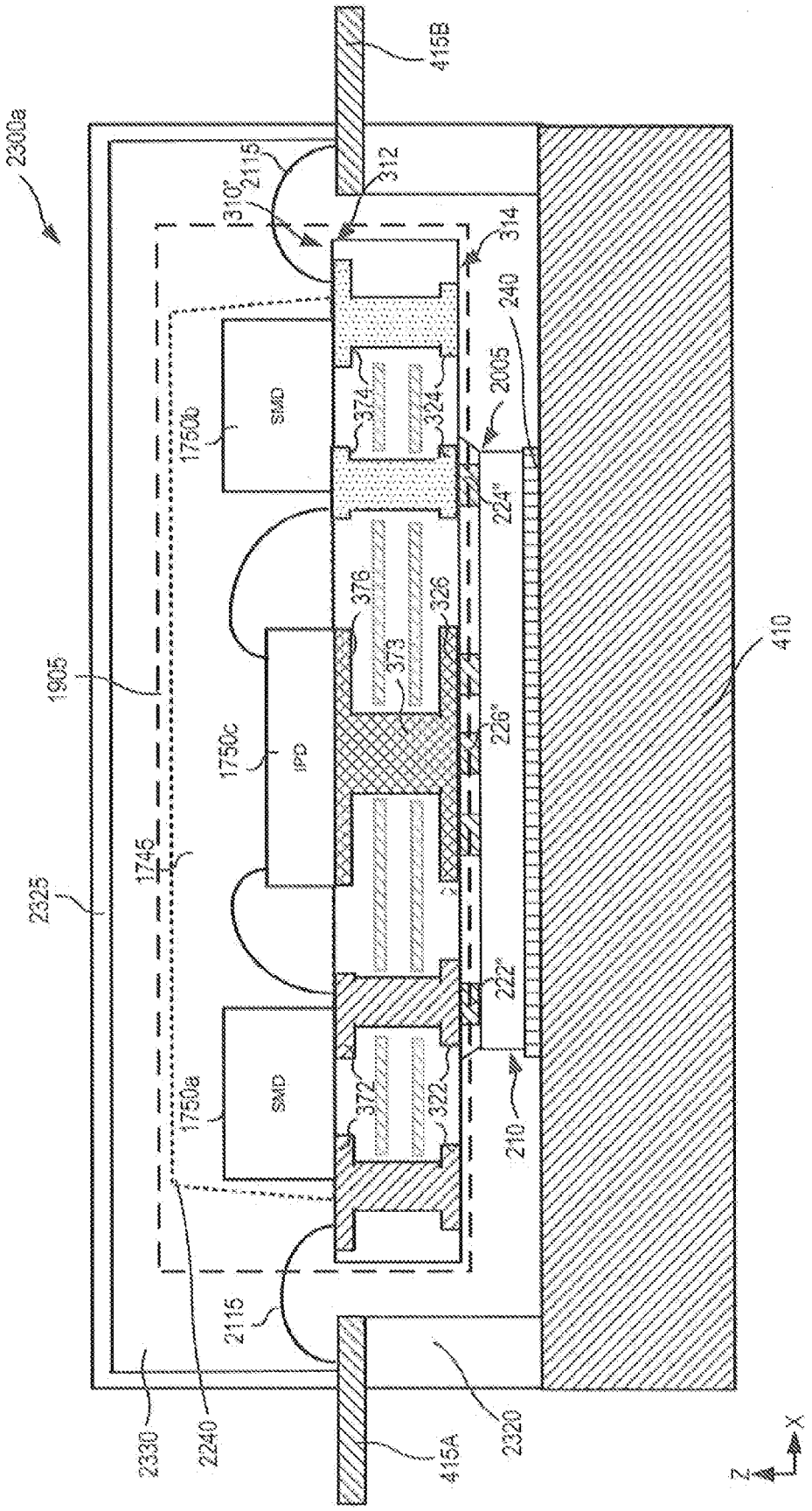

2300a
415B
2115
312
310'
314
240
2005
374
324
1750b
SMD
224"
376
326
373
1905
410
1750c
IPD
226"
1745
2325
222'
372
322
1750a
SMD
210
2115
2330
2240
415A
2320
X
Z

FIG. 23A

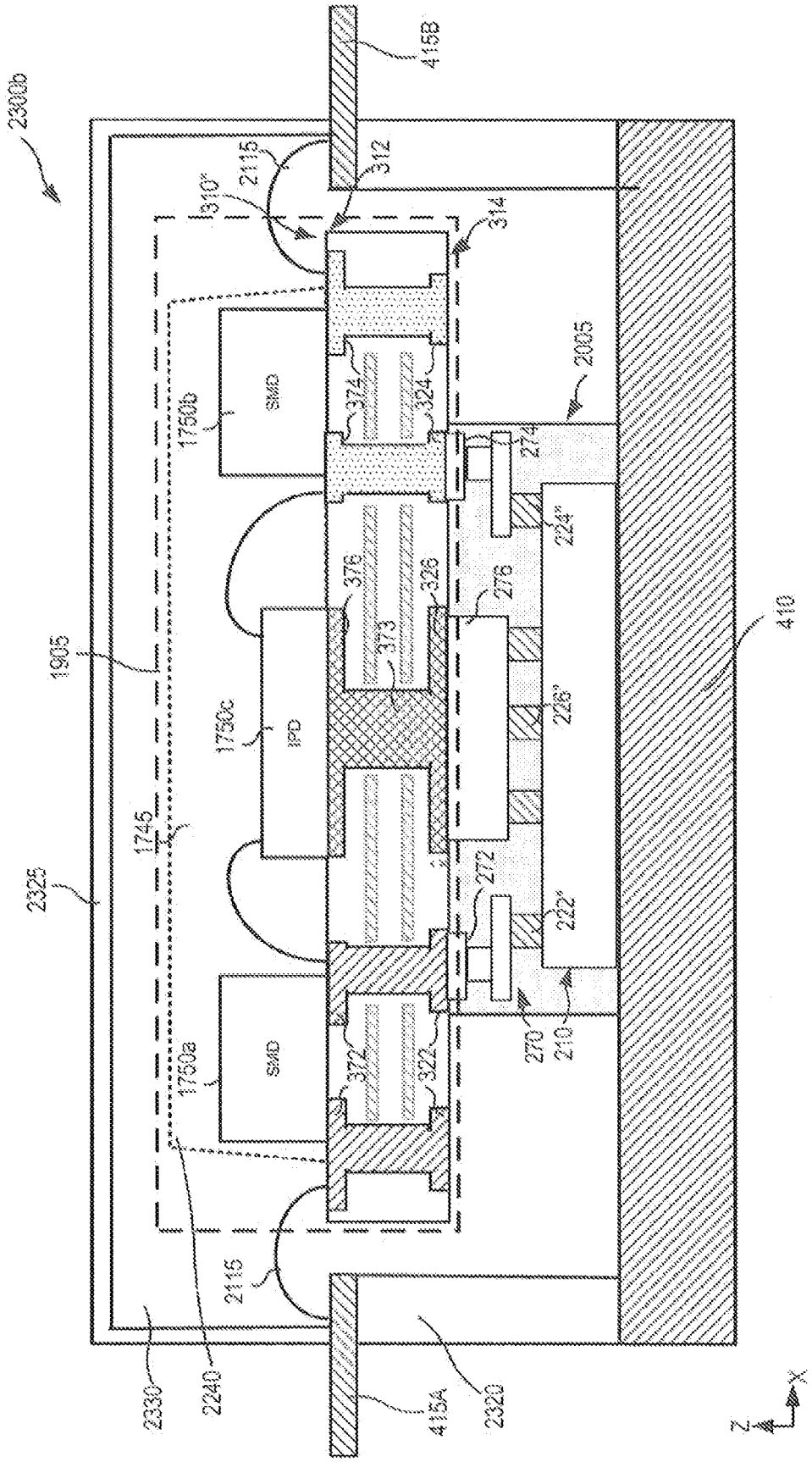

2300b
416B
312
2115
310"
314
2005
374
324
1750b
SMD
274
224"
376
326
276
373
1905
1750c
IPD
226"
410
1745
2325
272
222"
270
210
372
322
1750a
SMD
2115
2330
2240
415A
2320
Z
X

FIG. 23B

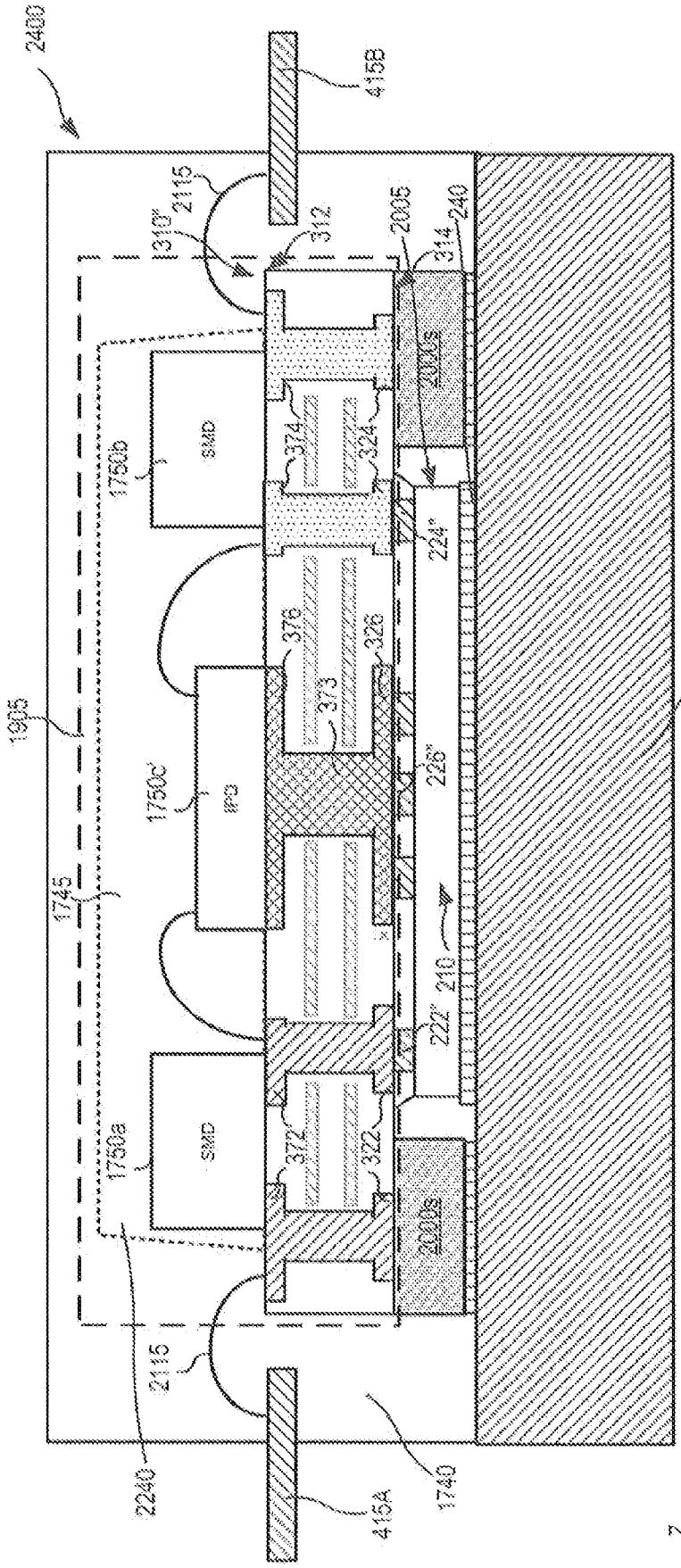


FIG. 24A

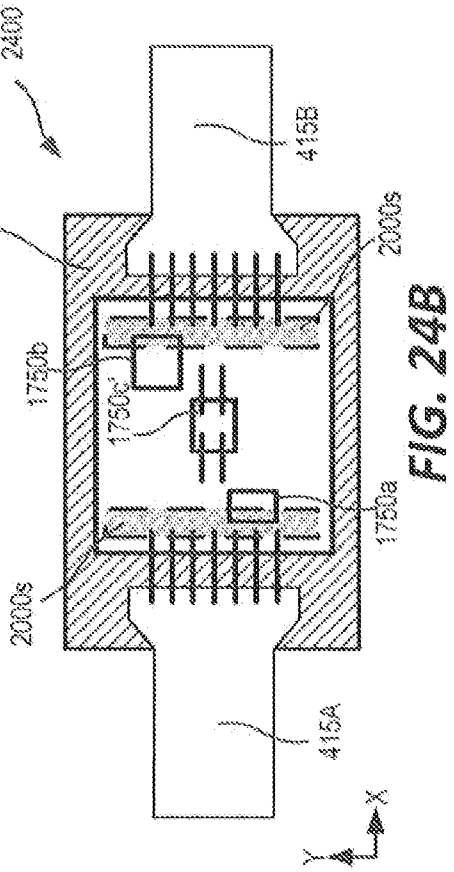


FIG. 24B

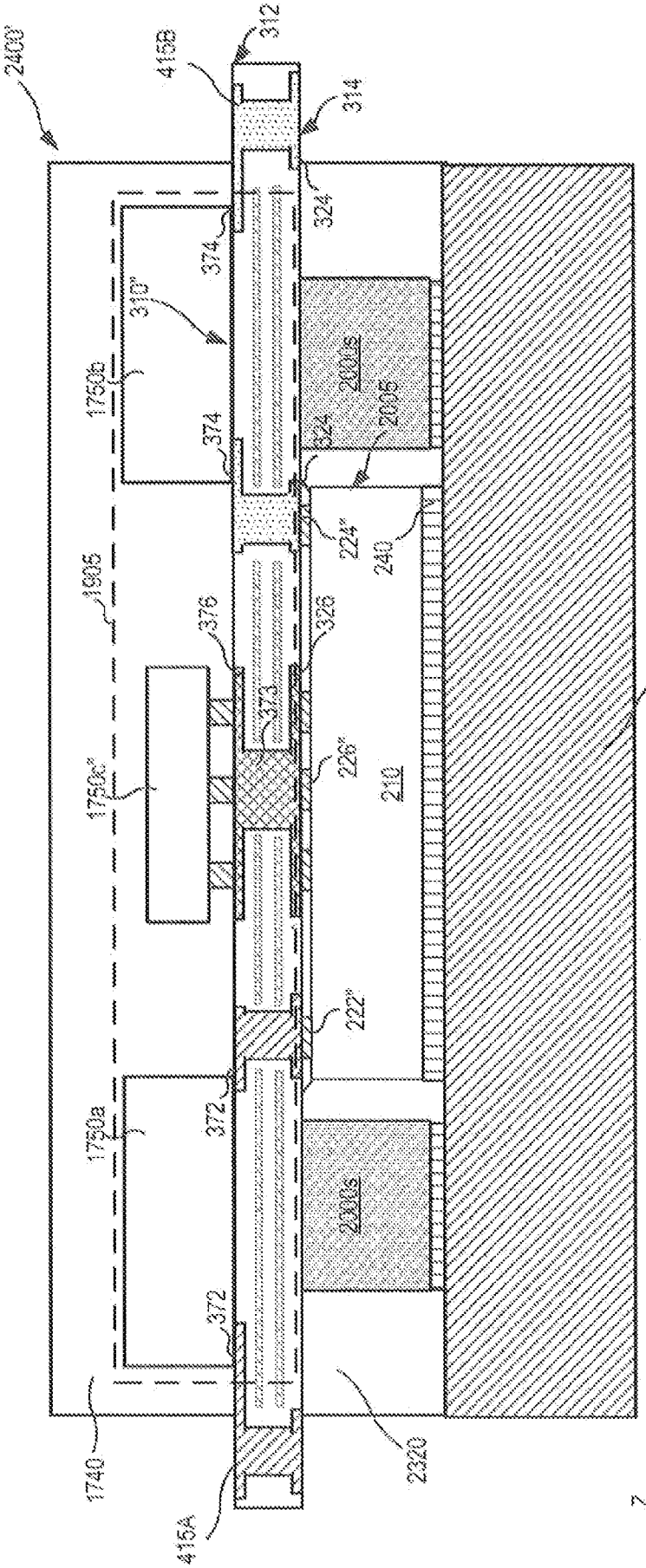

2400'
415B
312
314
324
374
310"
1750b
2300s
2300d
224"
240
1905
376
326
373
226"
210
410
1750c"
222"
372
1750a
1740
2320
415A
Z
X

FIG. 24C

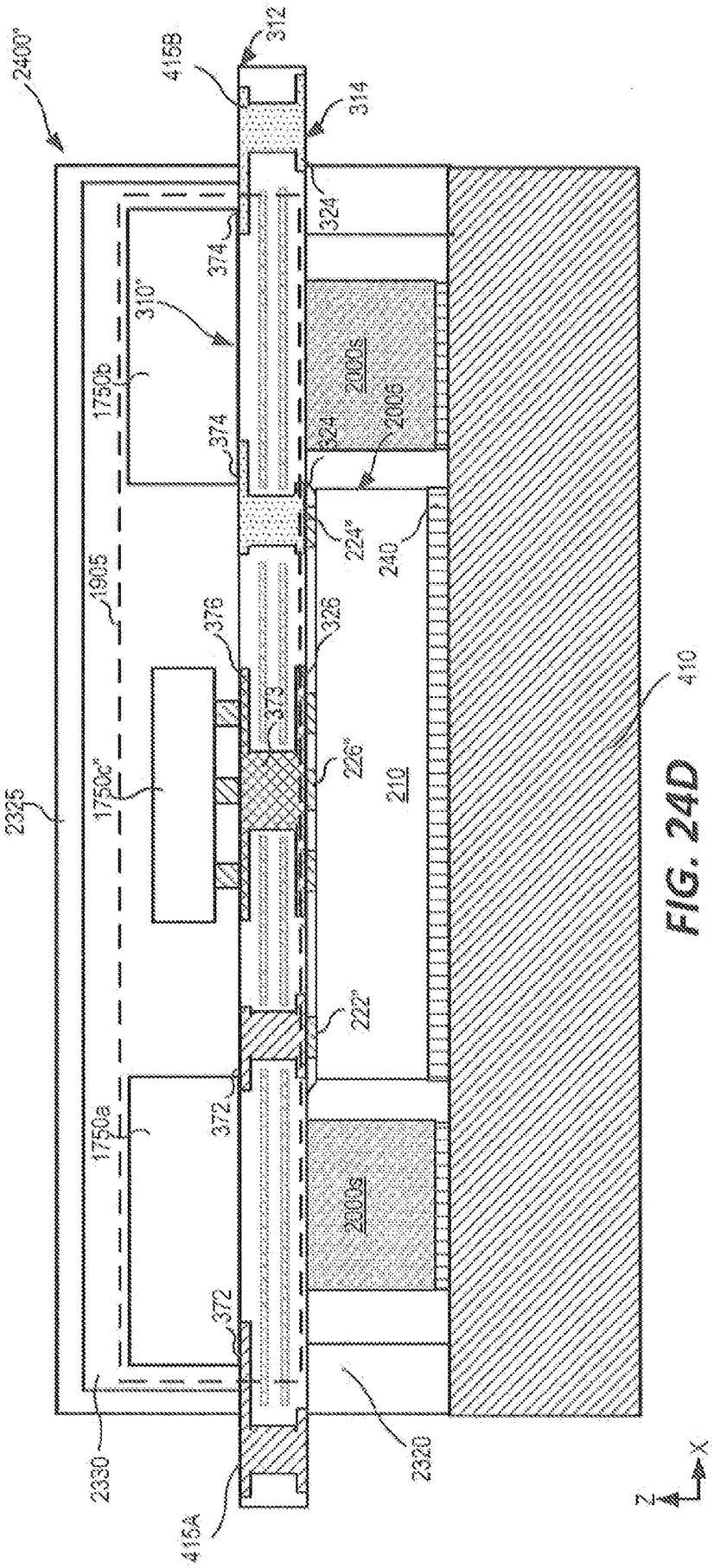

2400"
415B
312
314
324
374
310"
1750b
2800s
2800d
224"
240
1905
376
326
373
226"
210
410
2325
1750c"
222"
1750a
372
2800s
2330
2320
416A
Z
X

FIG. 24D

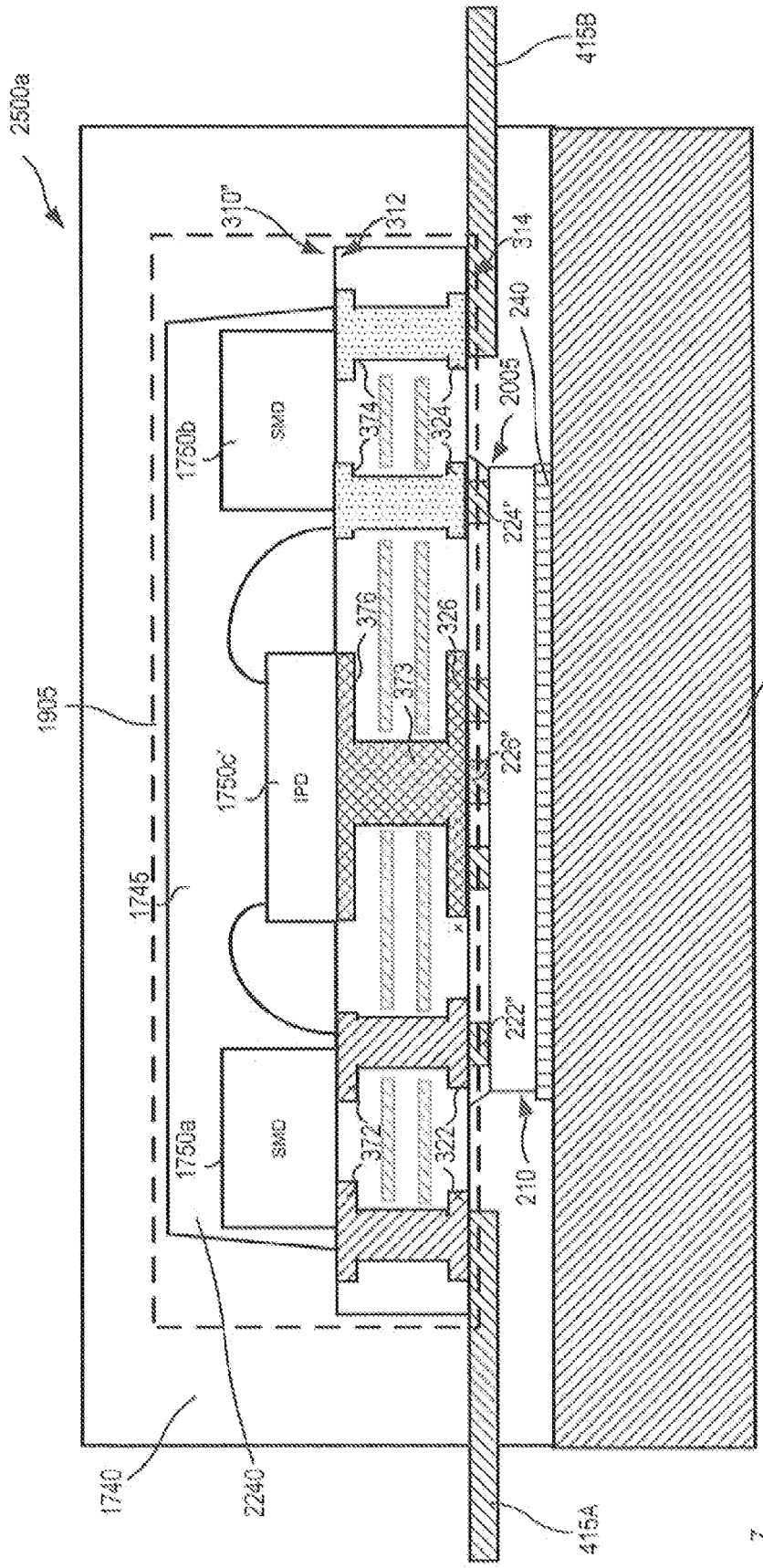

2500a
415B
310"
312
314
240
2005
374
324
224"
1750b
SMD
376
326
373
410
1905
1750c'
IPD
226"
1745
222"
372
322
210
1750a
SMD
1740
2240
415A
Z
X

FIG. 25A

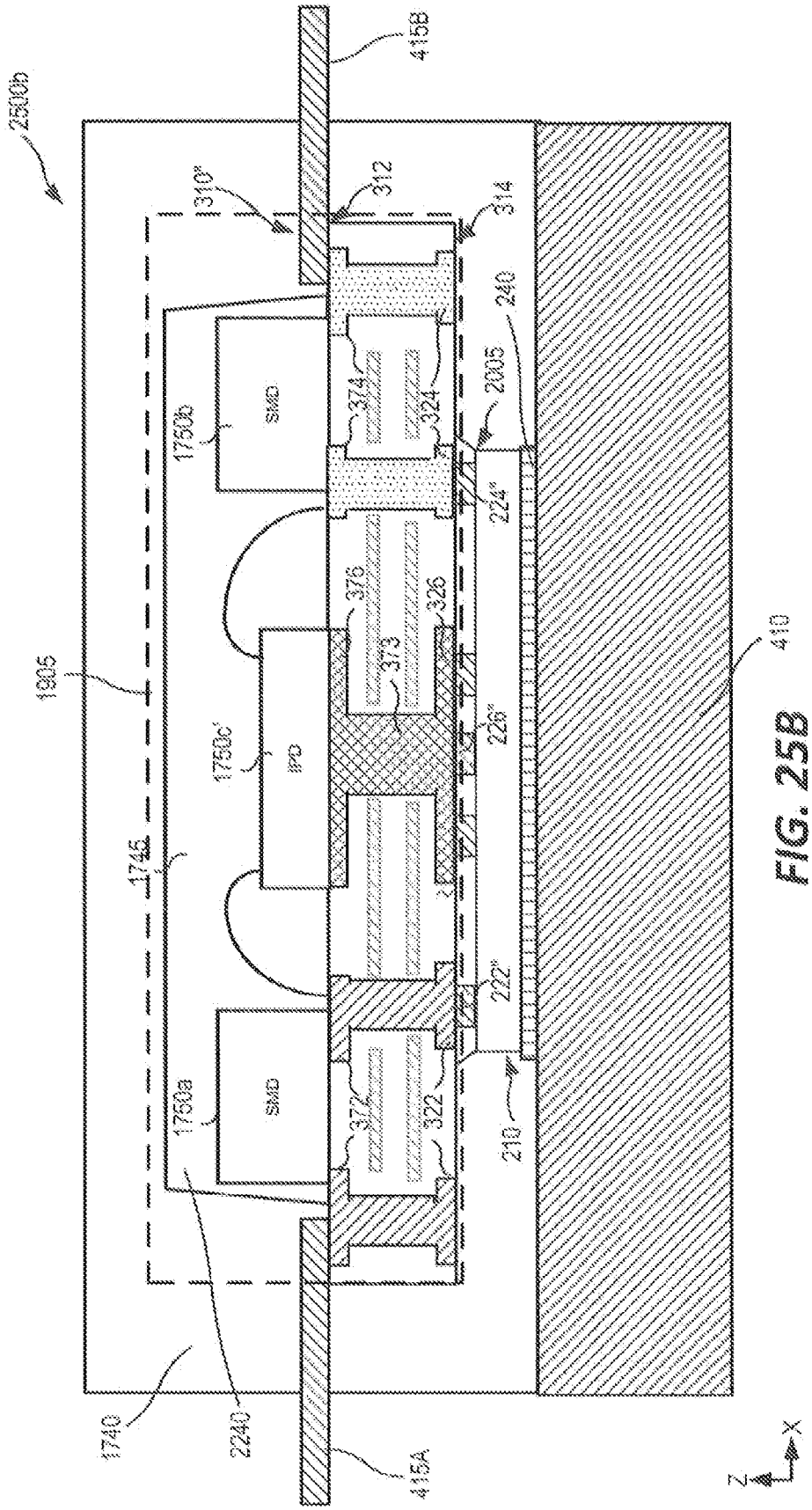

2500b
415B
310"
312
314
240
2005
374
324
1750b
SMD
224"
376
326
373
1905
1750c'
IPD
226"
410
1745
222"
372
322
1750a
SMD
210
1740
2240
415A
Z
X

FIG. 25B

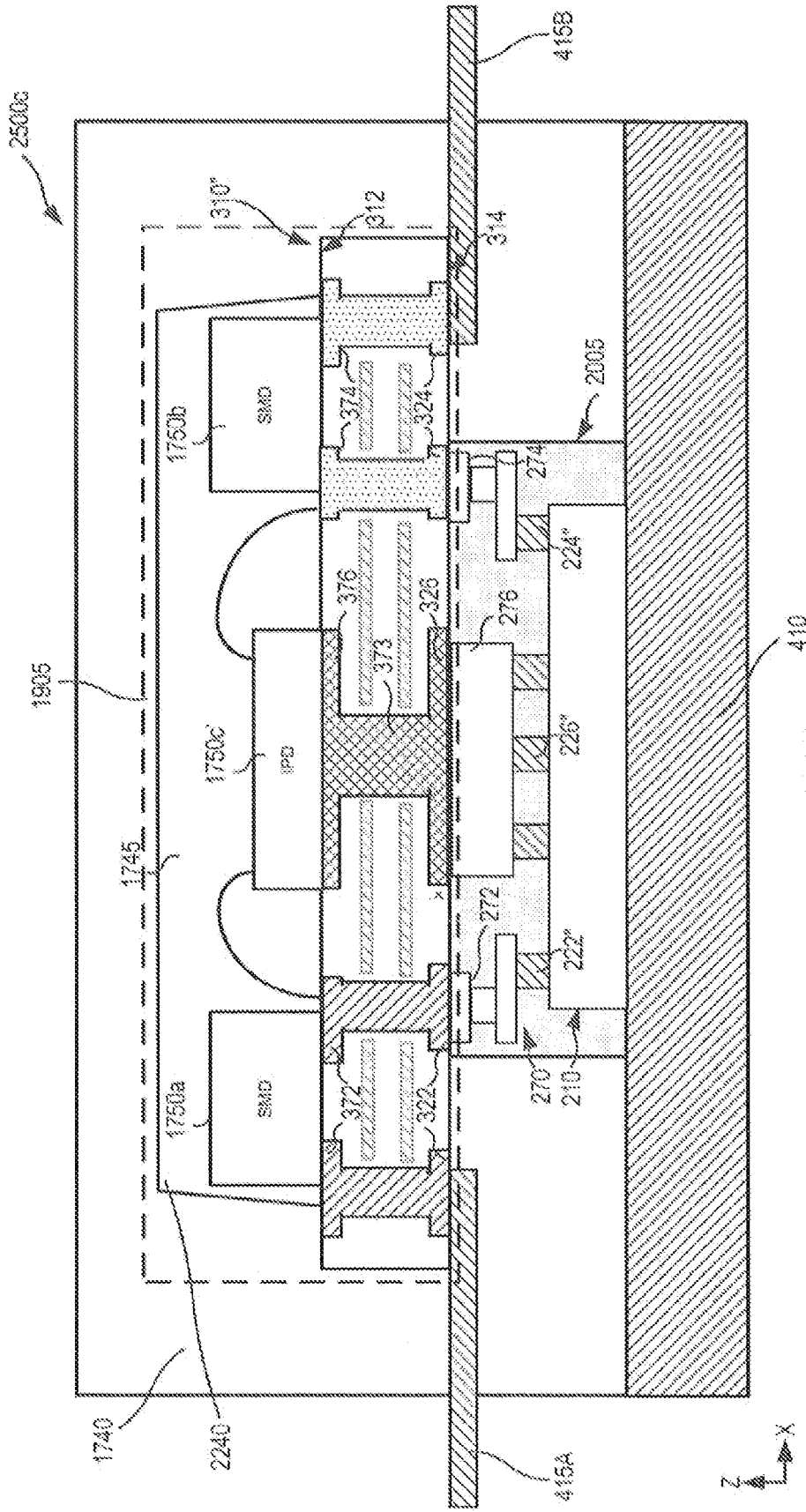

2500c
415B
310"
312
314
2005
374
324
1750b
SMD
274
224"
376
326
276
373
1905
1750c
IPD
410
226"
1745
272
222"
270
210
372
322
1750a
SMD
1740
2240
415A
Z
X

FIG. 25C

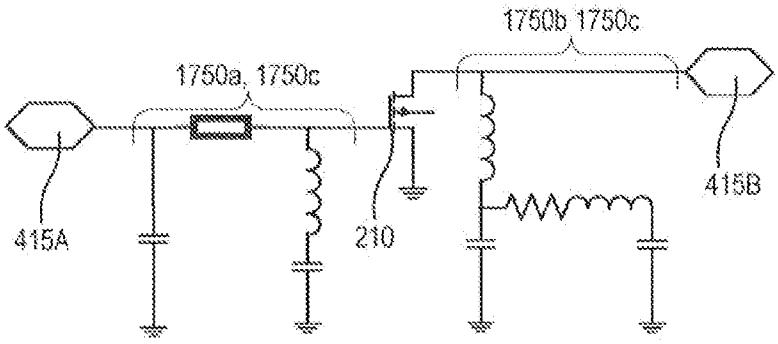


FIG. 26A

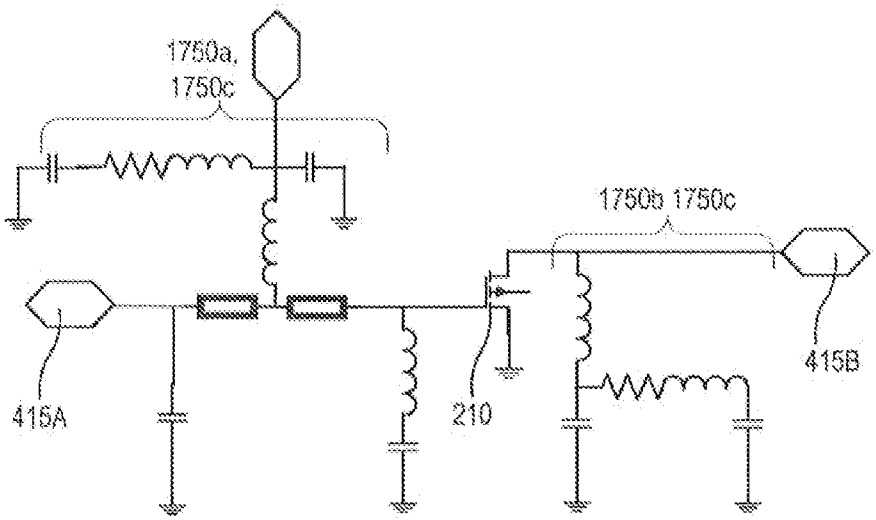


FIG. 26B

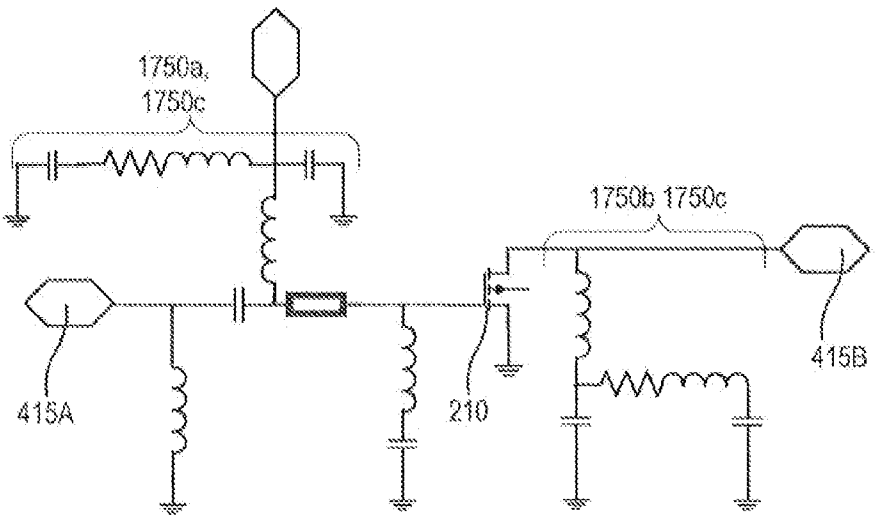


FIG. 26C

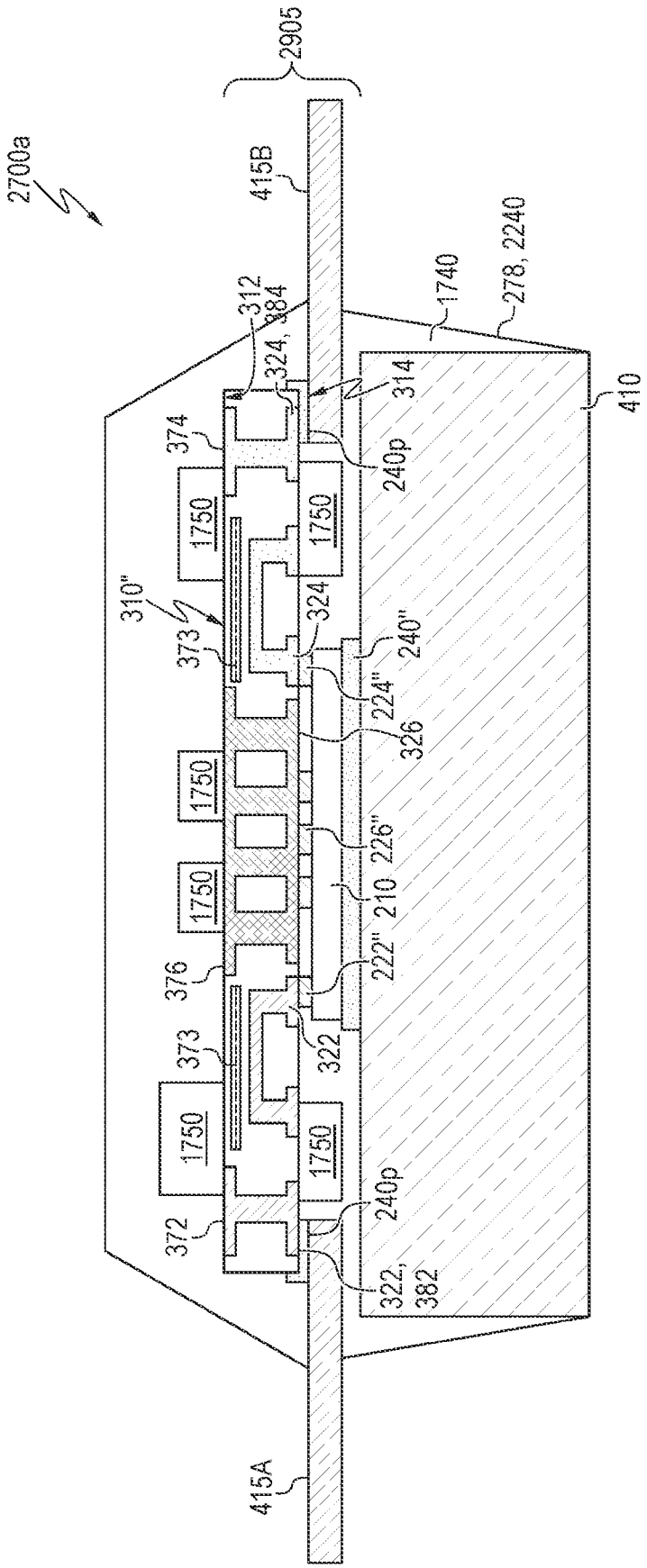

2700a
2905
415B
1740
278, 2240
312
384
324, 384
314
410
374
240p
1750
1750
310"
373
324
240"
224"
326
1750
226"
210
1750
222"
376
373
322
1750
1750
240p
372
322, 382
415A

FIG. 27A

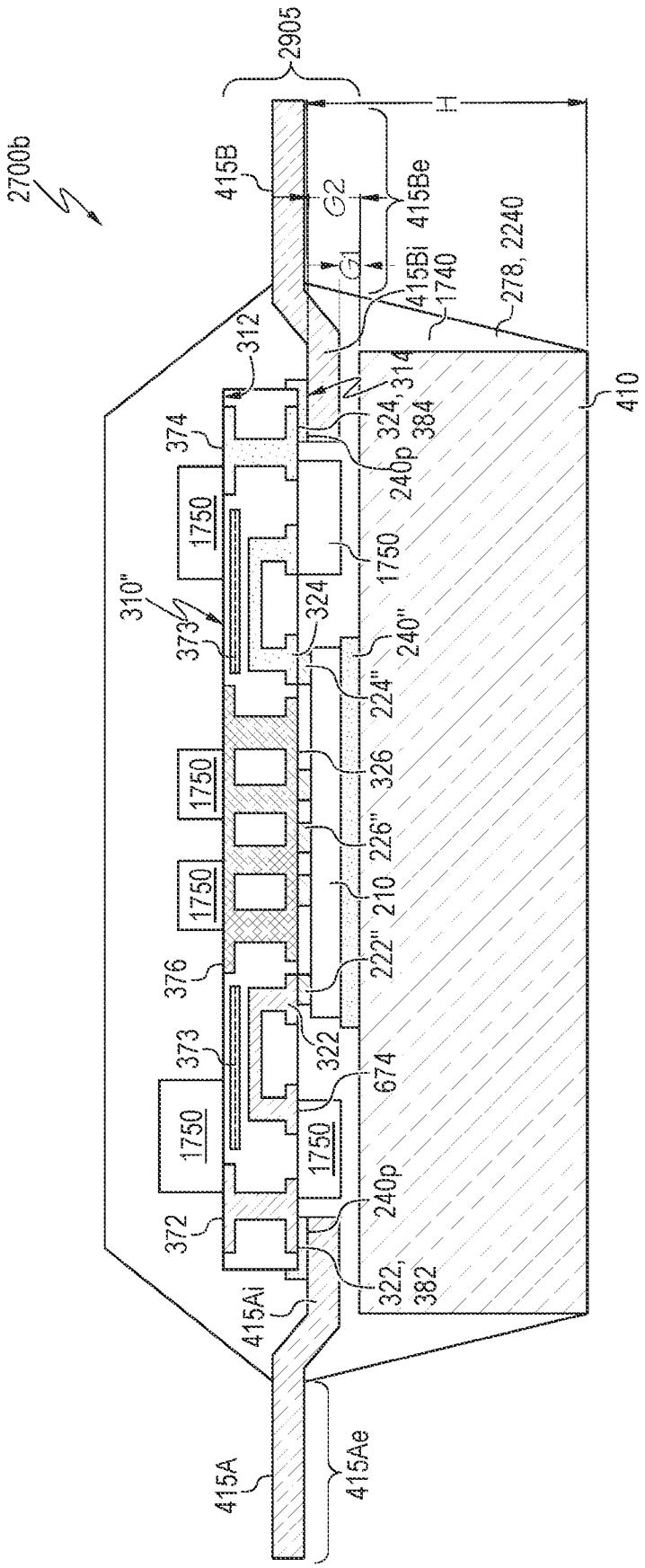

2700b
2905
415B
G2
G1
H
415Be
415Bi
1740
278, 2240
410
312
314
324, 384
374
240p
1750
310"
373
324
240"
224"
326
226"
210
222"
376
322
674
373
372
322, 382
415Ai
415A
415Ae

FIG. 27B

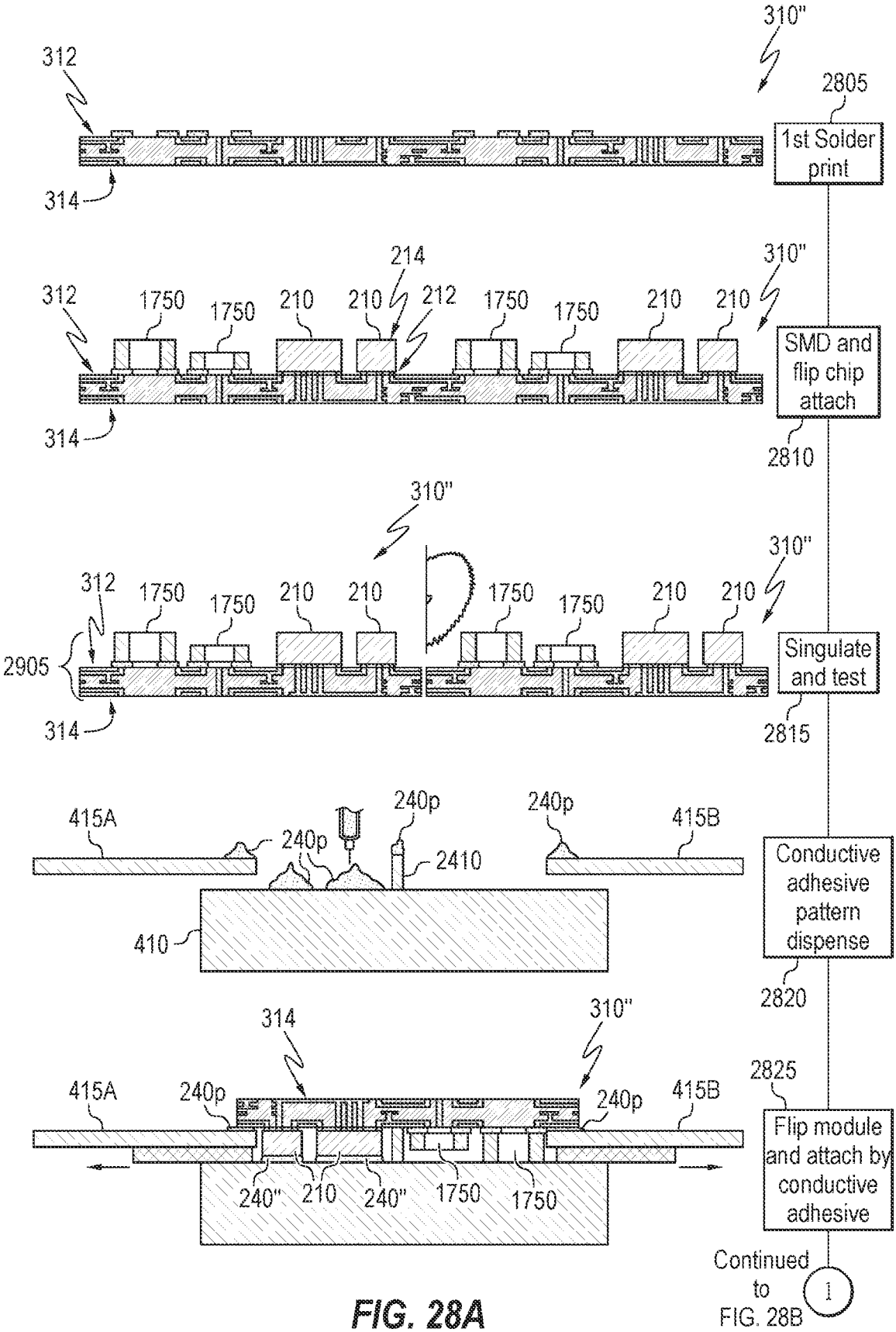

310"
312
2805
1st Solder print
314
214
310"
312
1750
1750
210
210
212
1750
1750
210
210
SMD and flip chip attach
314
2810
310"
310"
312
1750
1750
210
210
1750
1750
210
210
2905
Singulate and test
314
2815
240p
240p
415A
240p
240p
415B
2410
Conductive adhesive pattern dispense
410
2820
314
310"
2825
415A
240p
240p
415B
Flip module and attach by conductive adhesive
240"
210
240"
1750
1750
Continued to FIG. 28B
1

FIG. 28A

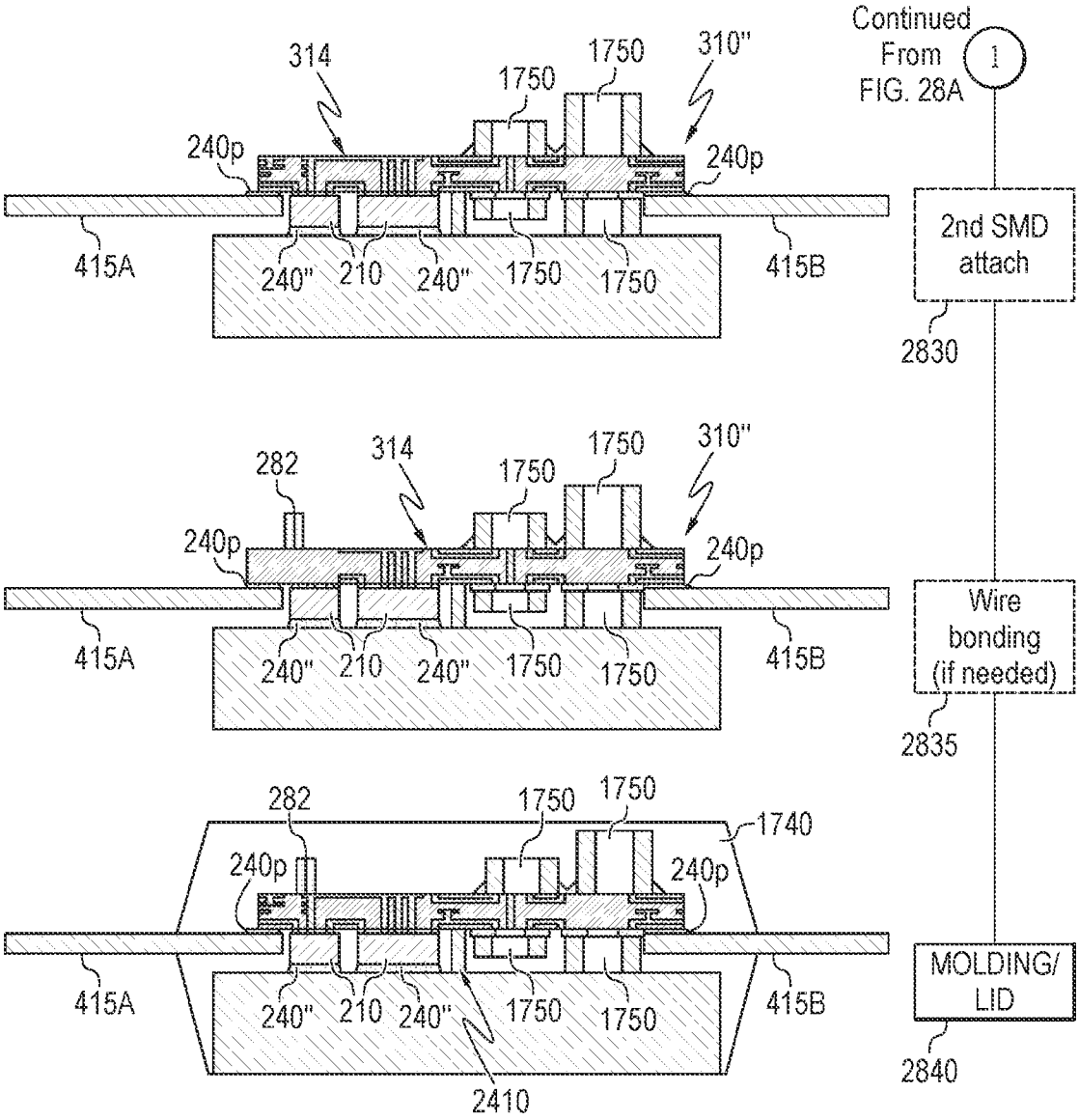

Continued From FIG. 28A
1
314
1750
1750
310"
240p
240p
415A
240"
210
240"
1750
1750
415B
2nd SMD attach
2830
282
314
1750
1750
310"
240p
240p
415A
240"
210
240"
1750
1750
415B
Wire bonding (if needed)
2835
282
1750
1750
1740
240p
240p
415A
240"
210
240"
1750
1750
415B
2410
MOLDING/ LID
2840

FIG. 28B

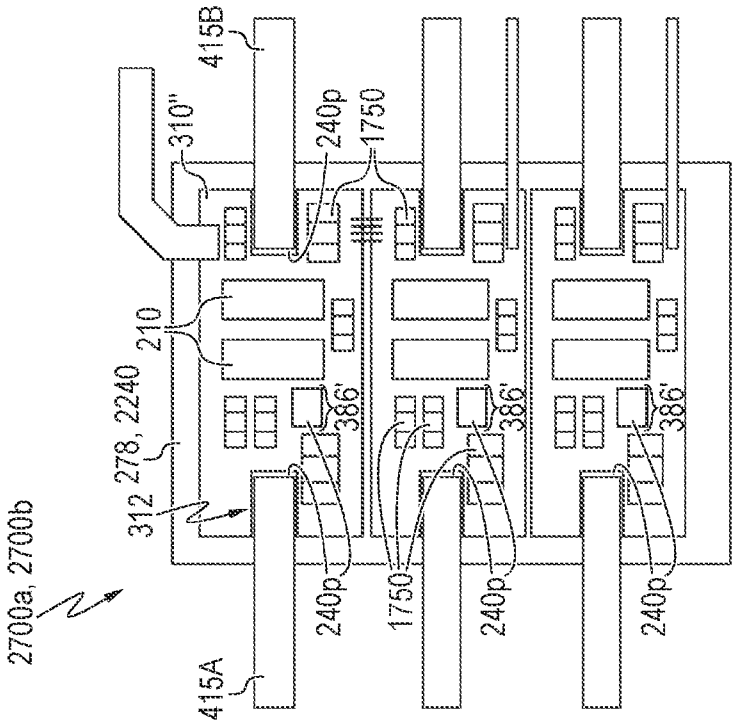


FIG. 29B

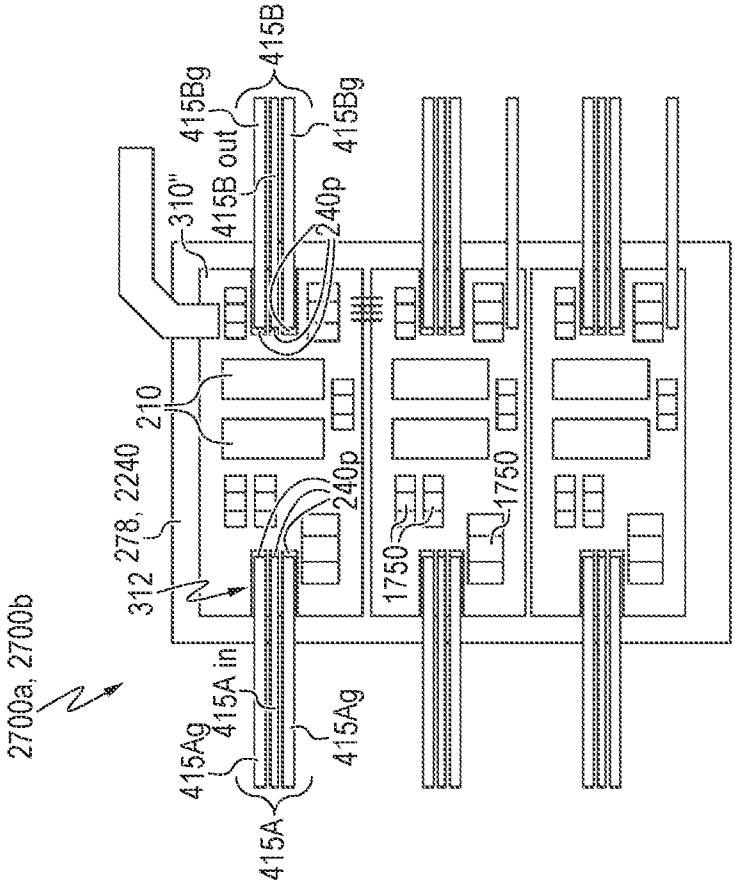


FIG. 29A

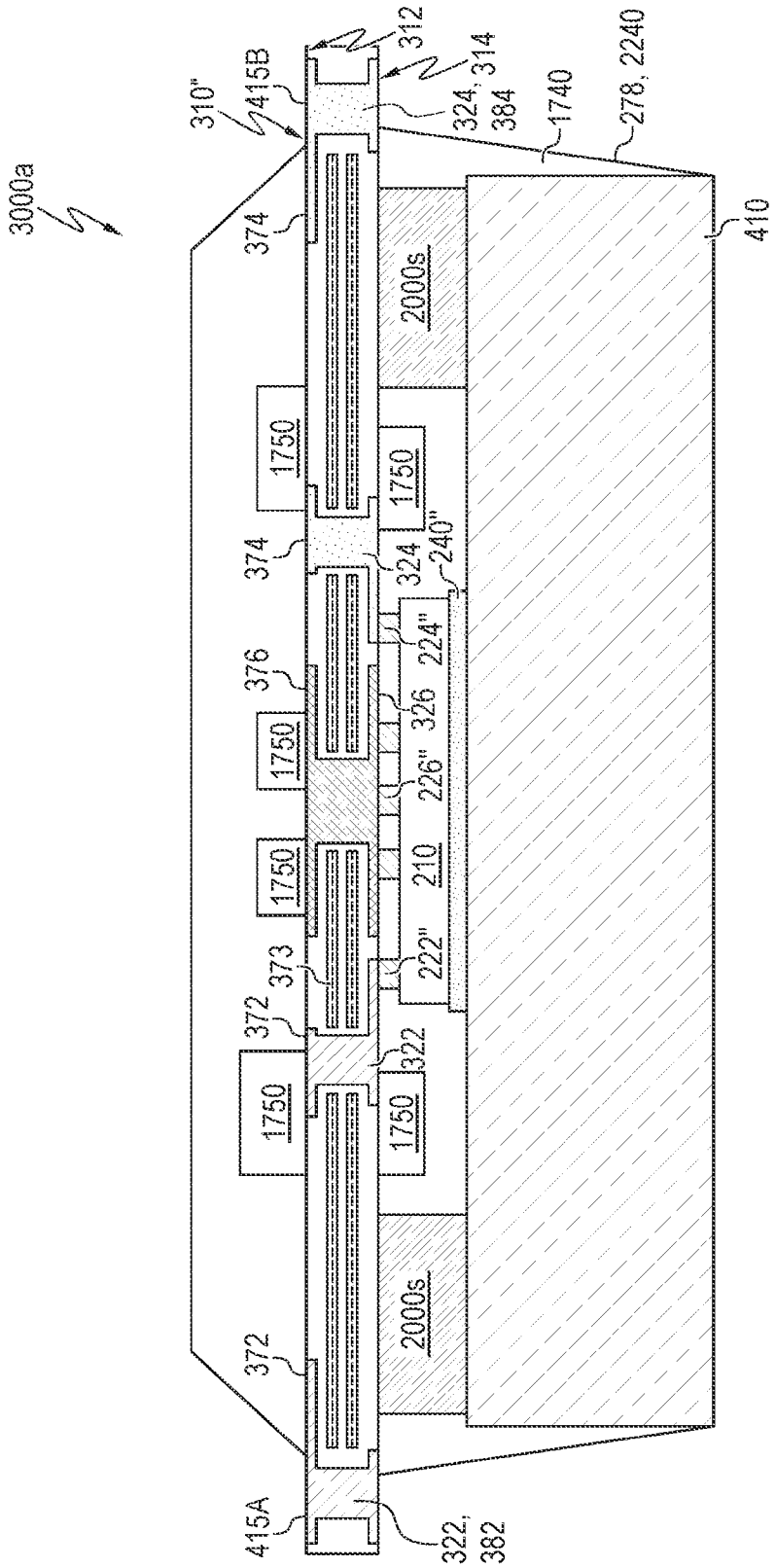

3000a
310"
415B
312
324, 314
384
1740
278, 2240
410
374
2000s
1750
1750
374
324
240"
224"
376
326
1750
226"
210
1750
222"
373
372
322
1750
1750
2000s
372
415A
322,
382

FIG. 30A

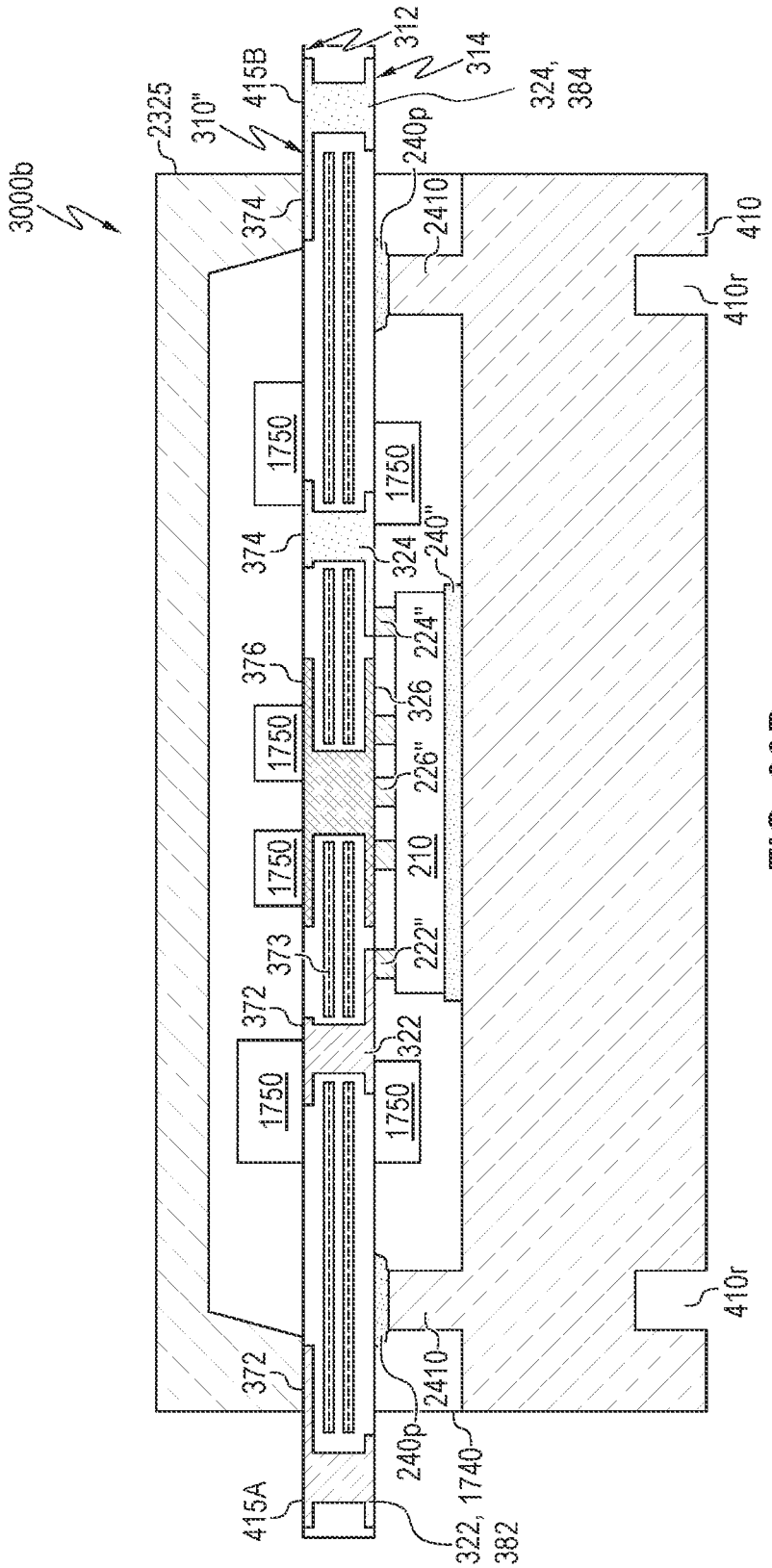

3000b
2325
310"
415B
312
314
324, 384
240p
2410
410
410r
374
1750
324
240"
224"
376
326
226"
210
222"
373
372
322
415A
322, 1740
382

FIG. 30B

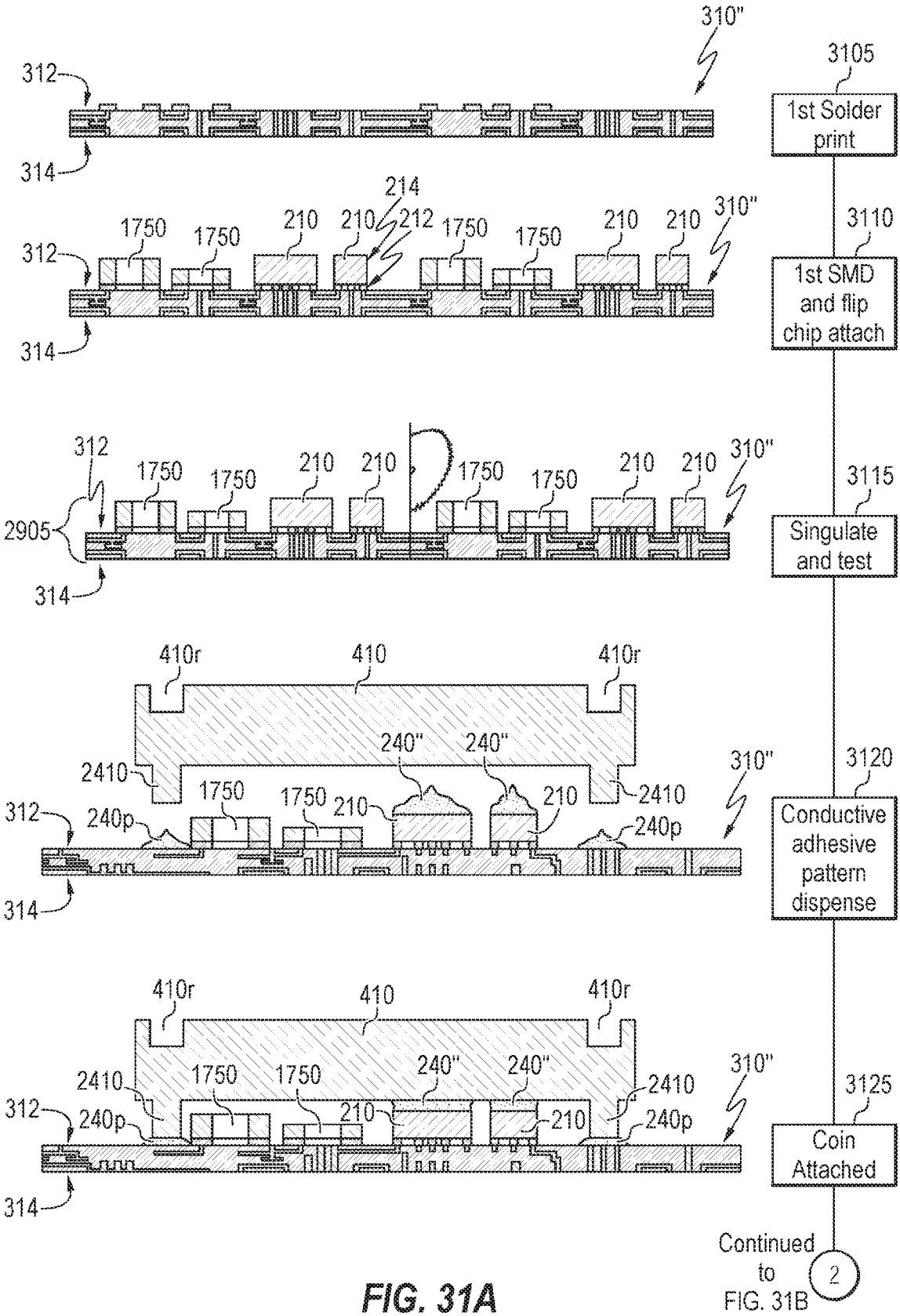

310"
3105
1st Solder print
312
314
214
1750
210
212
3110
1st SMD and flip chip attach
2905
3115
Singulate and test
410r
410
240"
2410
240p
3120
Conductive adhesive pattern dispense
3125
Coin Attached
Continued to FIG. 31B
2

FIG. 31A

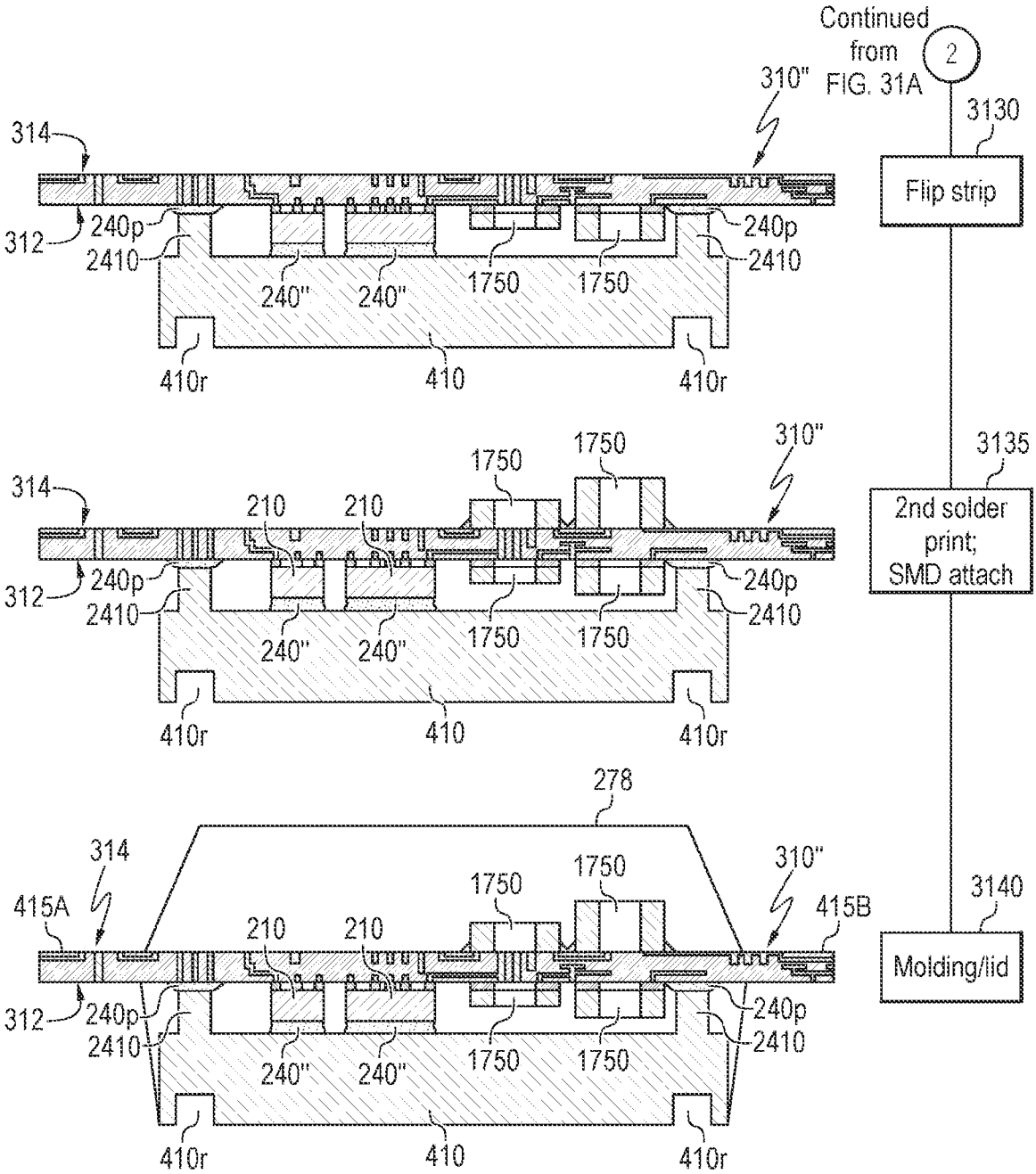

Continued from FIG. 31A
2
3130
Flip strip
3135
2nd solder print; SMD attach
3140
Molding/lid
310"
314
312
240p
2410
240"
1750
410r
410
210
278
415A
415B

FIG. 31B

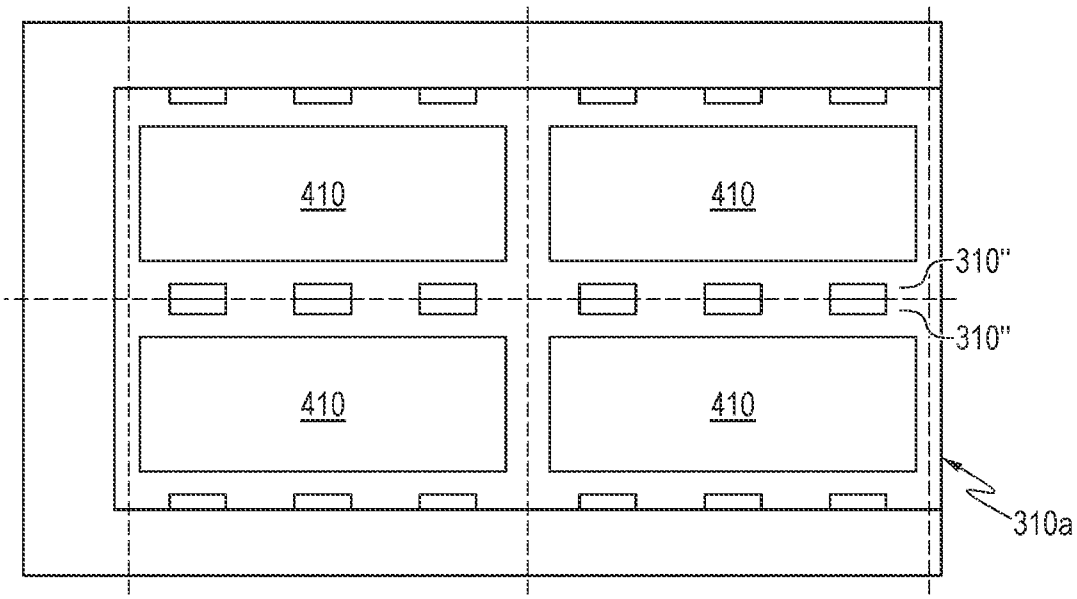


FIG. 32A

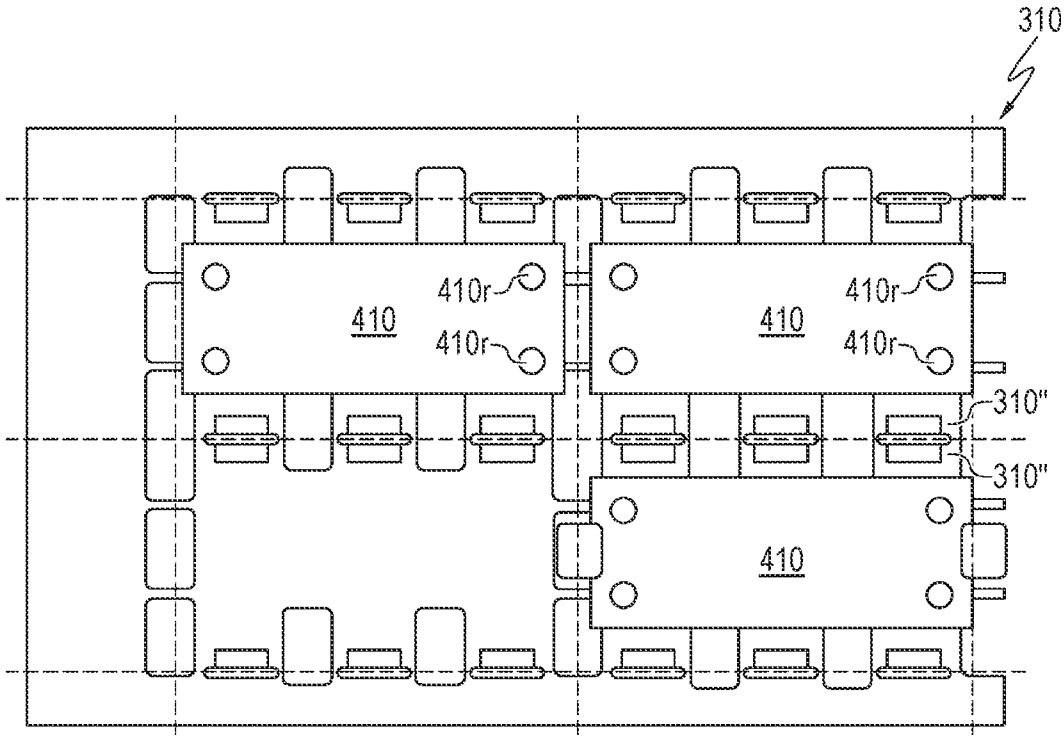


FIG. 32B

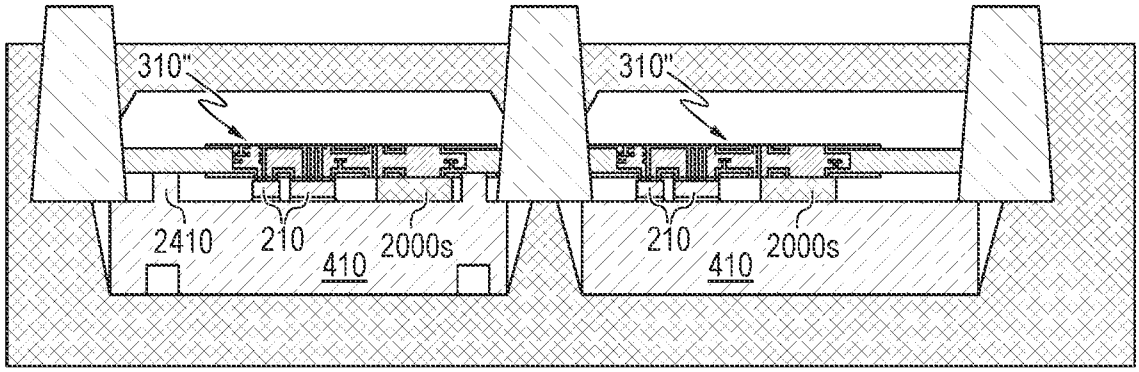


FIG. 32C

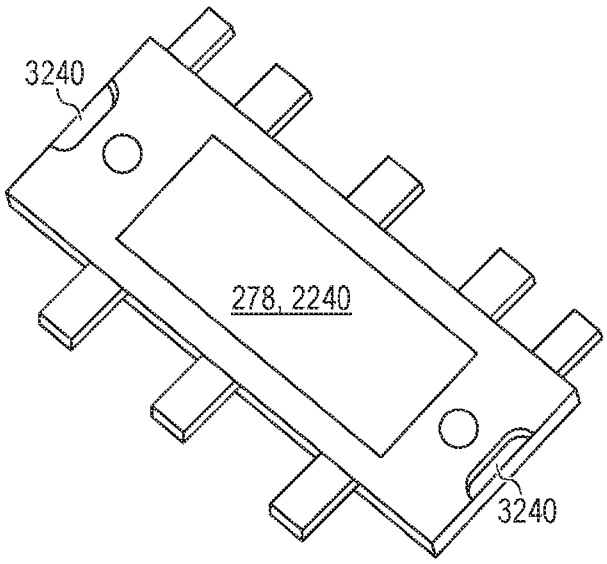


FIG. 32D

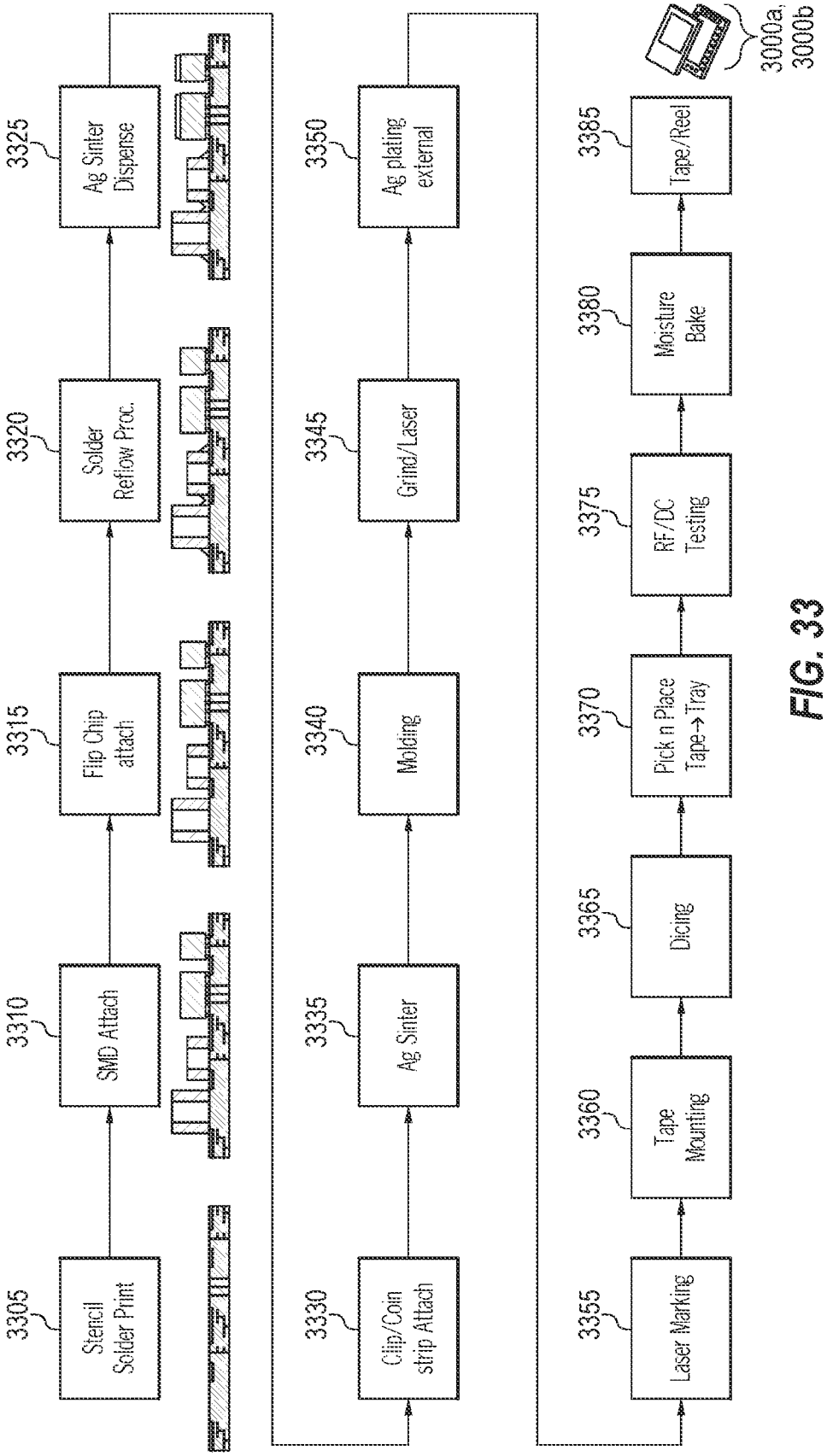

3305
Stencil Solder Print
3310
SMD Attach
3315
Flip Chip attach
3320
Solder Reflow Proc.
3325
Ag Sinter Dispense
3330
Clip/Coin strip Attach
3335
Ag Sinter
3340
Molding
3345
Grind/Laser
3350
Ag plating external
3355
Laser Marking
3360
Tape Mounting
3365
Dicing
3370
Pick n Place Tape→Tray
3375
RF/DC Testing
3380
Moisture Bake
3385
Tape/Reel
3000a, 3000b

FIG. 33

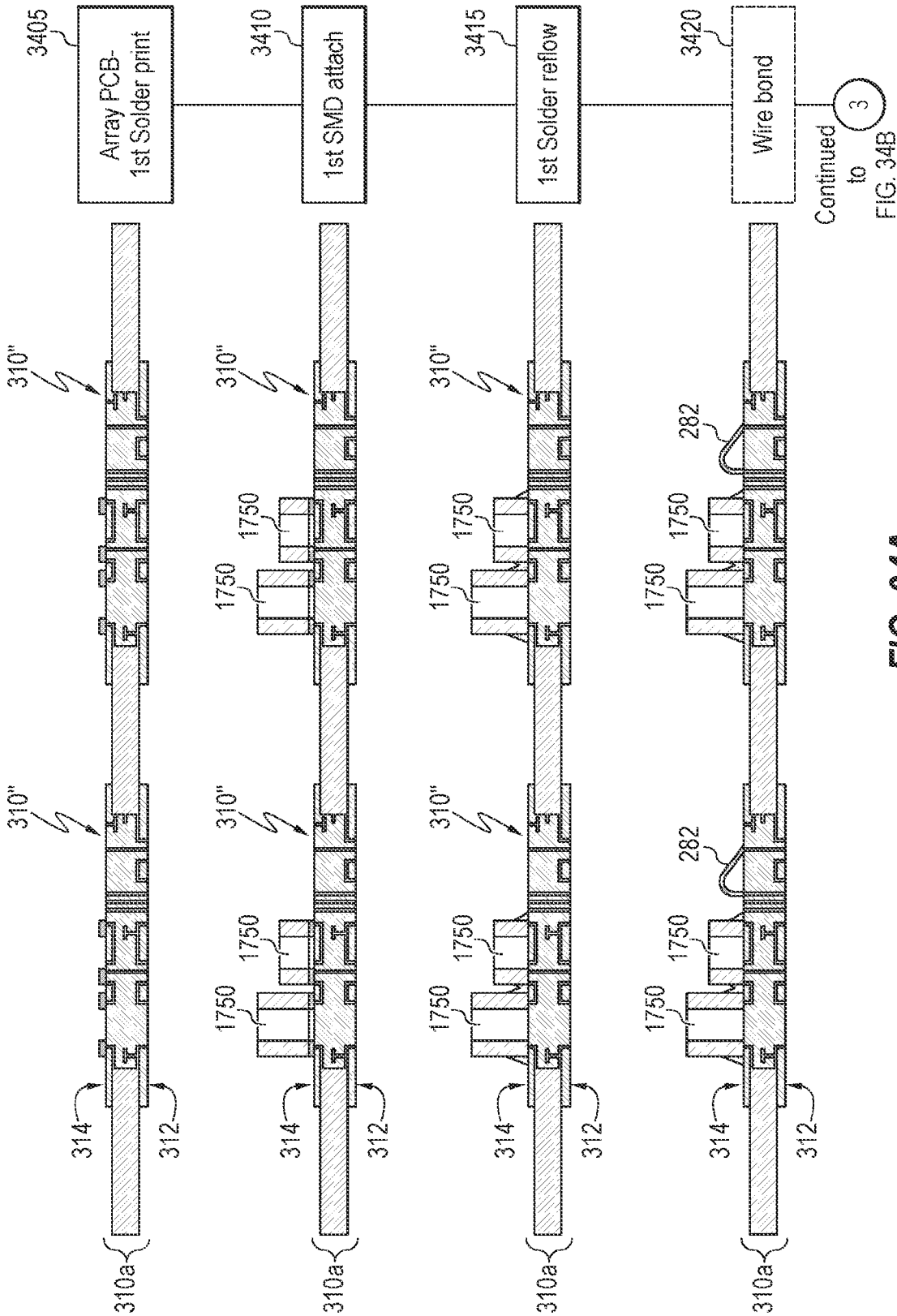

3405
Array PCB-
1st Solder print
3410
1st SMD attach
3415
1st Solder reflow
3420
Wire bond
Continued
to
FIG. 34B
3
310"
310a
312
314
1750
282

FIG. 34A

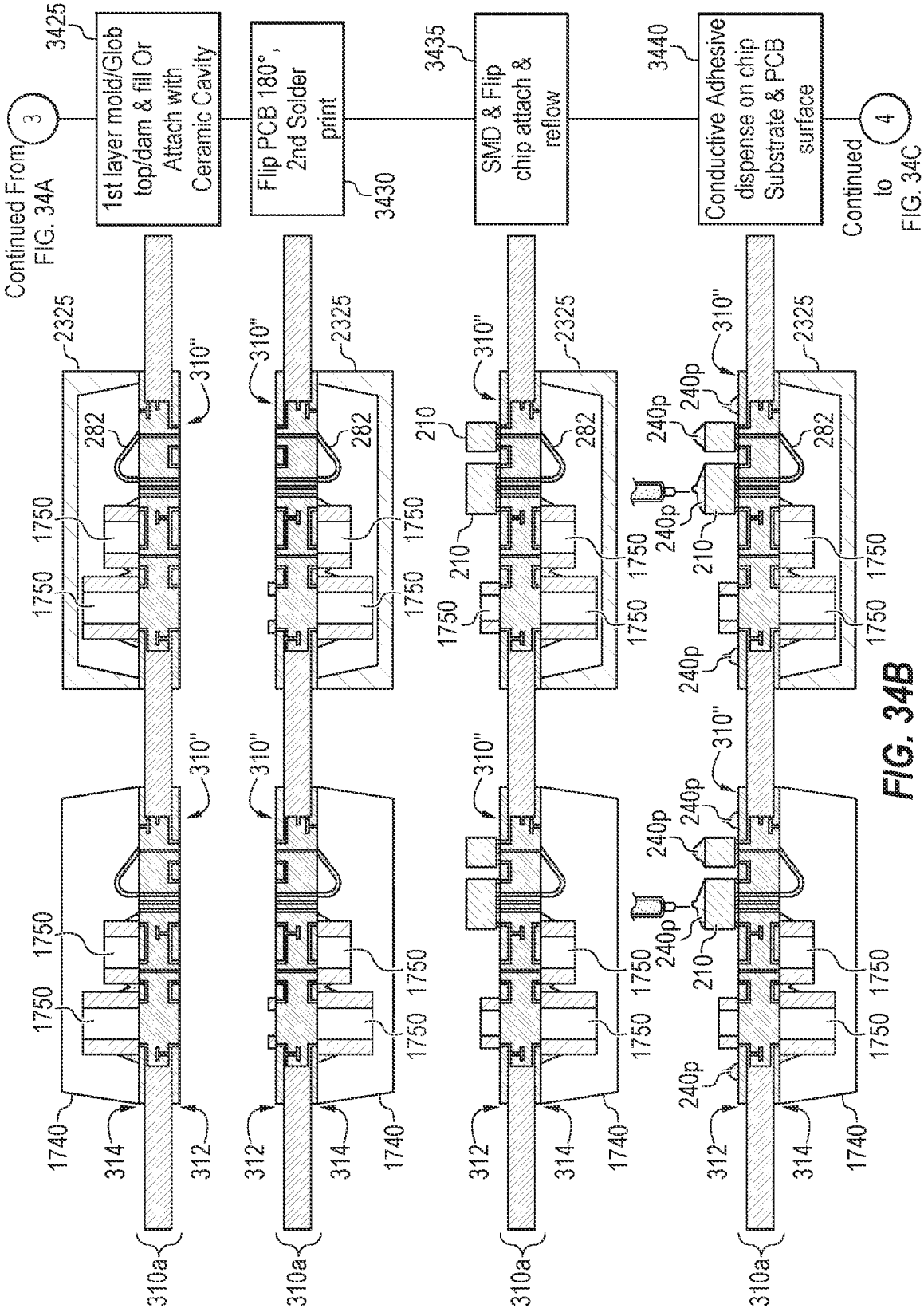

Continued From FIG. 34A
3
3425
1st layer mold/Glob top/dam & fill Or Attach with Ceramic Cavity
Flip PCB 180°, 2nd Solder print
3430
3435
SMD & Flip chip attach & reflow
3440
Conductive Adhesive dispense on chip Substrate & PCB surface
4
Continued to FIG. 34C
2325
310"
282
1750
210
240p
1740
314
312
310a

FIG. 34B

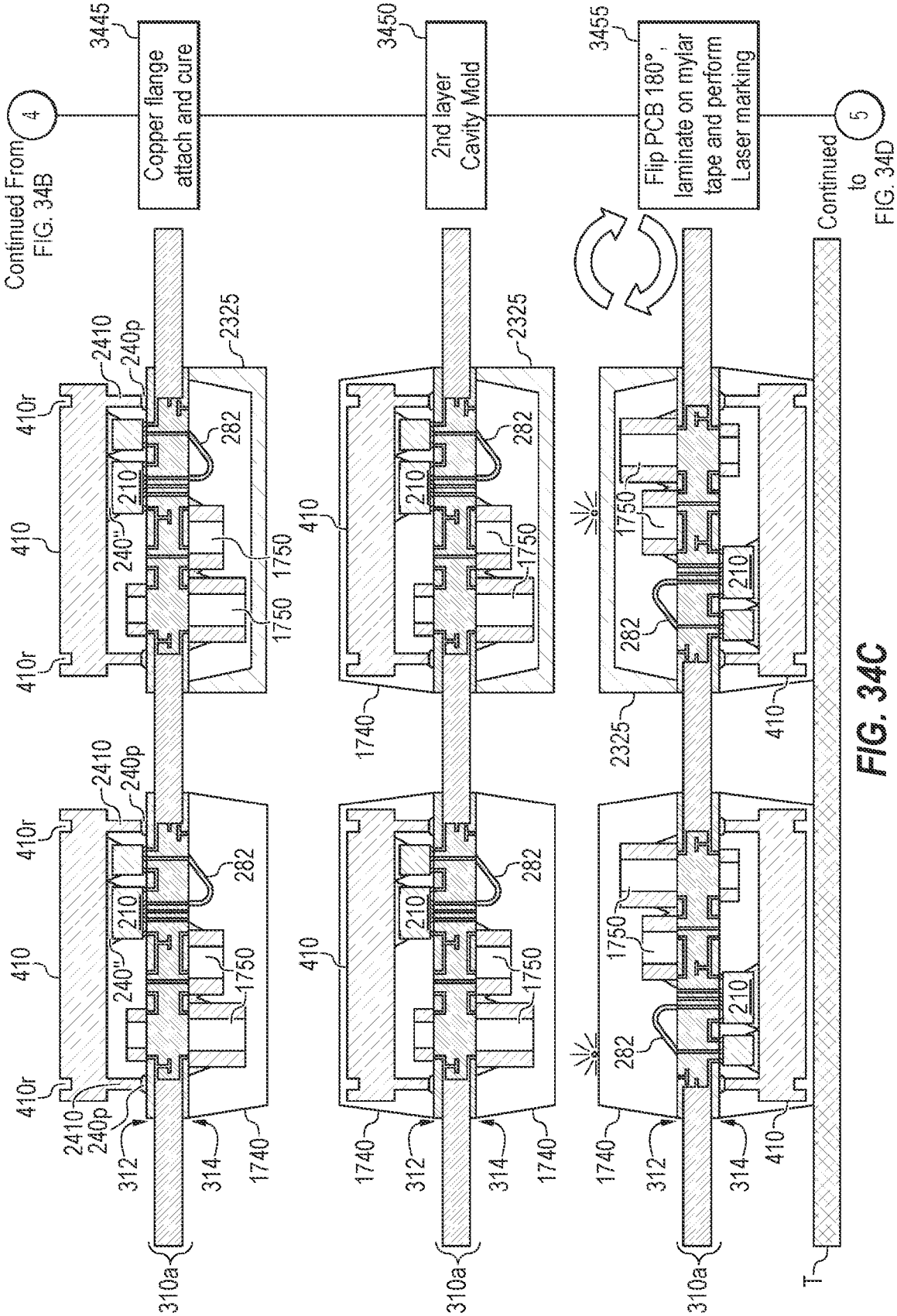

Continued From FIG. 34B
4
3445
Copper flange attach and cure
3450
2nd layer Cavity Mold
3455
Flip PCB 180°, laminate on mylar tape and perform Laser marking
5
Continued to FIG. 34D
2410
240p
410r
410
2325
282
210
240"
1750
312
314
1740
310a
T

FIG. 34C

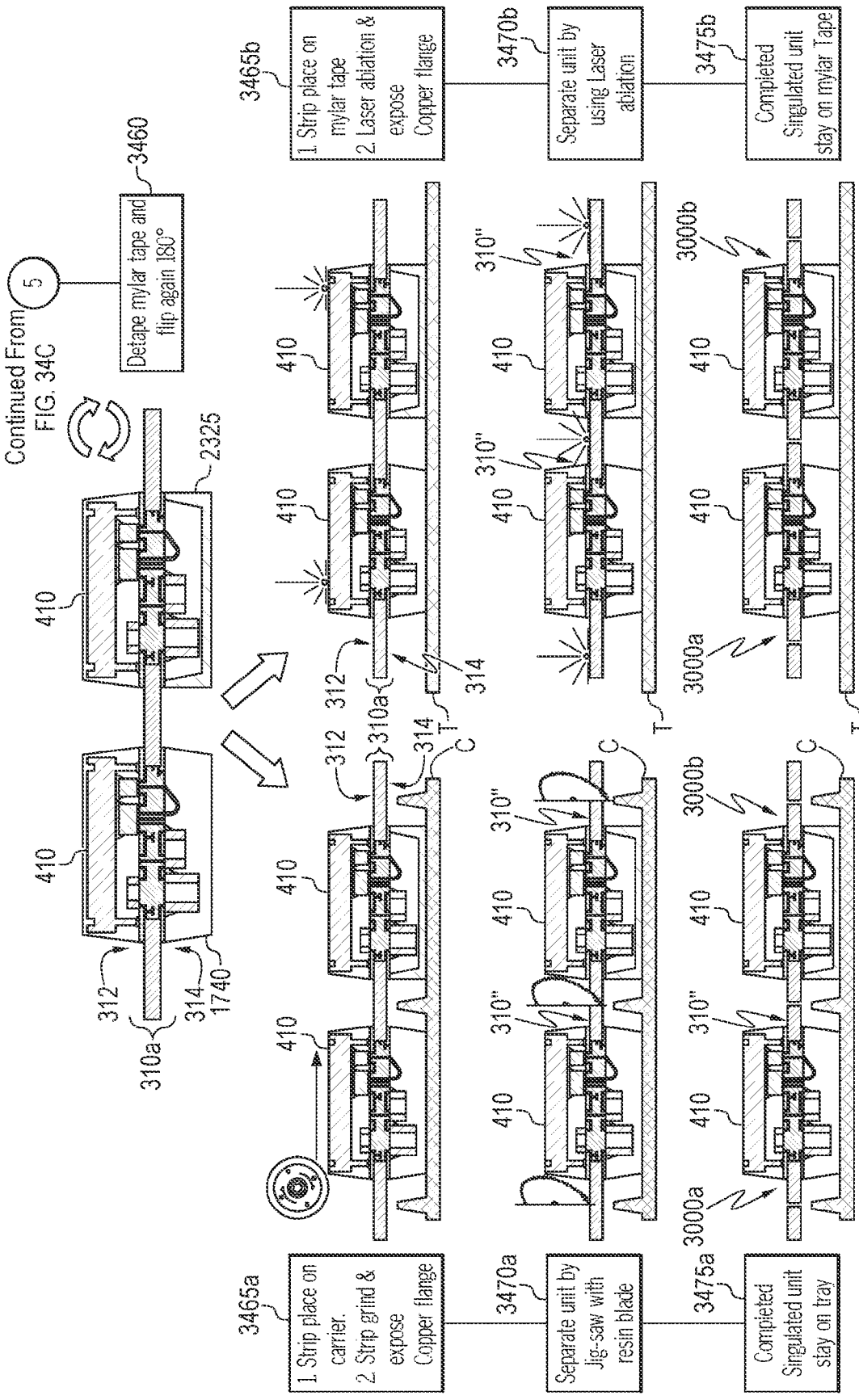

Continued From FIG. 34C
5
Detape mylar tape and flip again 180°
3460
3465b
1. Strip place on mylar tape
2. Laser ablation & expose Copper flange
3470b
Separate unit by using Laser ablation
3475b
Completed Singulated unit stay on mylar Tape
3465a
1. Strip place on carrier.
2. Strip grind & expose Copper flange
3470a
Separate unit by Jig-saw with resin blade
3475a
Completed Singulated unit stay on tray
410
310"
312
310a
314
1740
2325
3000a
3000b
T
C

FIG. 34D

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2024/033494

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L23/66 H01L23/495 H01L23/047 H01L23/31 H01L21/56
H01L23/538

ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2022/321071 A1 (NOORI BASIM [US] ET AL) 6 October 2022 (2022-10-06)	1-28, 30-35
A	paragraphs [0169], [0209] - [0219]; figures 7E, 9A-D	29
A	US 2017/243812 A1 (KADOGUCHI TAKUYA [JP] ET AL) 24 August 2017 (2017-08-24) figures 1,5,6,7,10,12	9

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 August 2024	11/09/2024

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Edmeades, Michael

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2024/033494

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2022321071 A1	06-10-2022	NONE	
US 2017243812 A1	24-08-2017	CN 105917463 A	31-08-2016
		DE 112014005420 T5	25-08-2016
		JP 6086055 B2	01-03-2017
		JP 2015103713 A	04-06-2015
		KR 20160075649 A	29-06-2016
		TW 201526168 A	01-07-2015
		US 2016293561 A1	06-10-2016
		US 2017243812 A1	24-08-2017
		WO 2015079294 A2	04-06-2015