



US008476836B2

(12) **United States Patent**
van de Ven et al.

(10) **Patent No.:** **US 8,476,836 B2**
(45) **Date of Patent:** **Jul. 2, 2013**

(54) **AC DRIVEN SOLID STATE LIGHTING
APPARATUS WITH LED STRING
INCLUDING SWITCHED SEGMENTS**

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(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 292 days.

(21) Appl. No.: **12/775,842**

(22) Filed: **May 7, 2010**

(65) **Prior Publication Data**

US 2011/0273102 A1 Nov. 10, 2011

(51) **Int. Cl.**
H05B 37/00 (2006.01)
H05B 39/00 (2006.01)
H05B 41/00 (2006.01)

(52) **U.S. Cl.**
USPC **315/193**; 315/185 R; 315/200 R;
315/291

(58) **Field of Classification Search**
None
See application file for complete search history.

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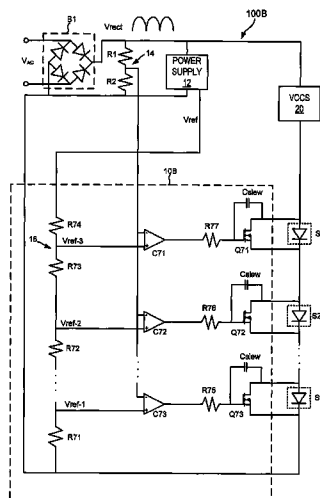
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(57) **ABSTRACT**

A diode selection circuit for a light emitting apparatus according to some embodiments includes a plurality of light emitting devices coupled in series. The diode selection circuit includes a comparator configured to receive a rectified AC input signal and a reference voltage and to generate a control signal in response to comparison of the rectified AC input signal with the reference voltage, a voltage controlled current source configured to supply a current to the plurality of light emitting diodes that is proportional to the rectified AC input signal, and a switch configured to receive the control signal and to shunt current away from at least one of the plurality of light emitting devices in response to the control signal.

31 Claims, 12 Drawing Sheets



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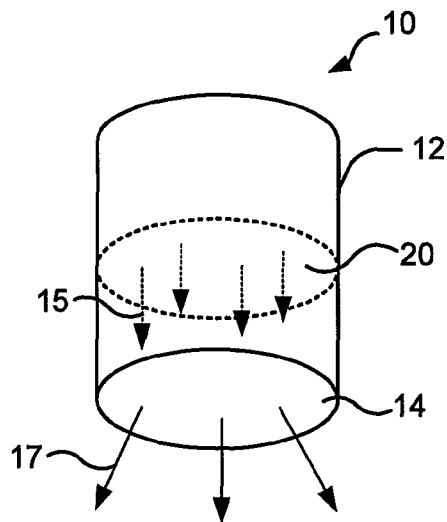


FIGURE 1A

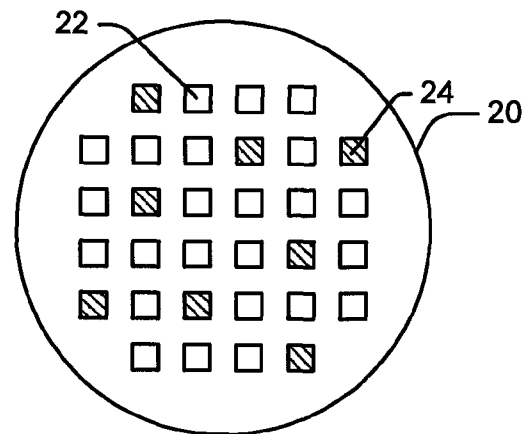


FIGURE 1B

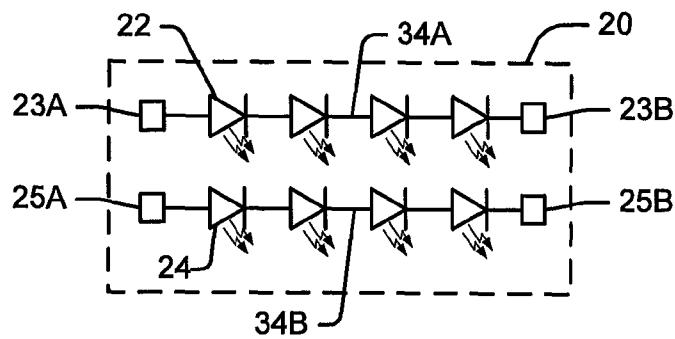
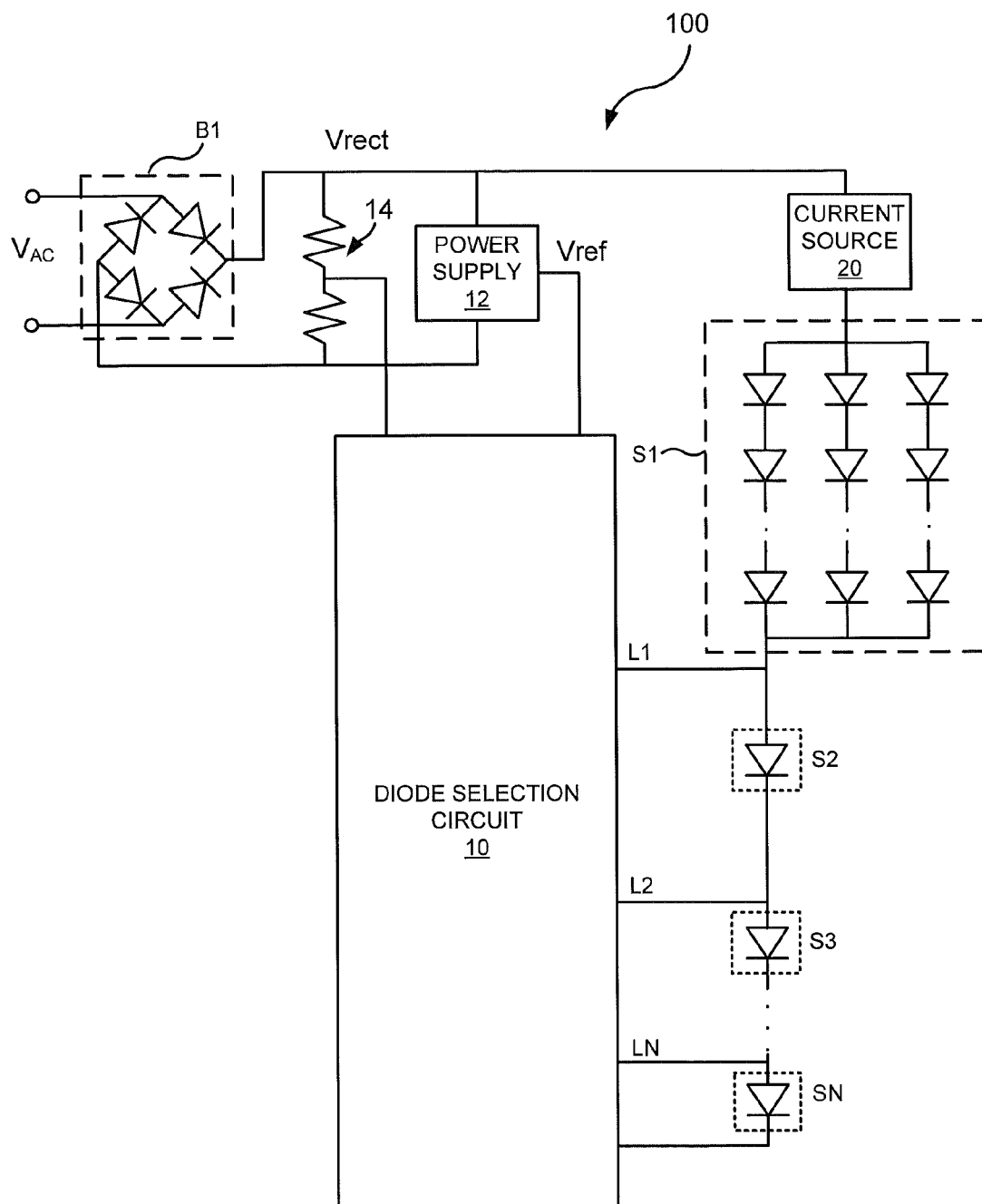
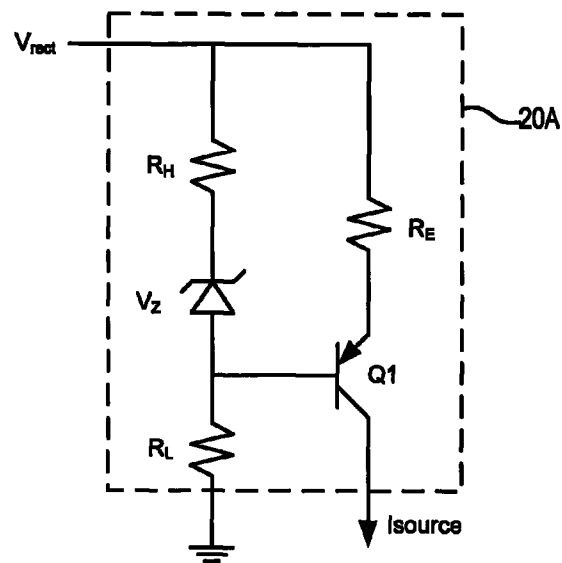
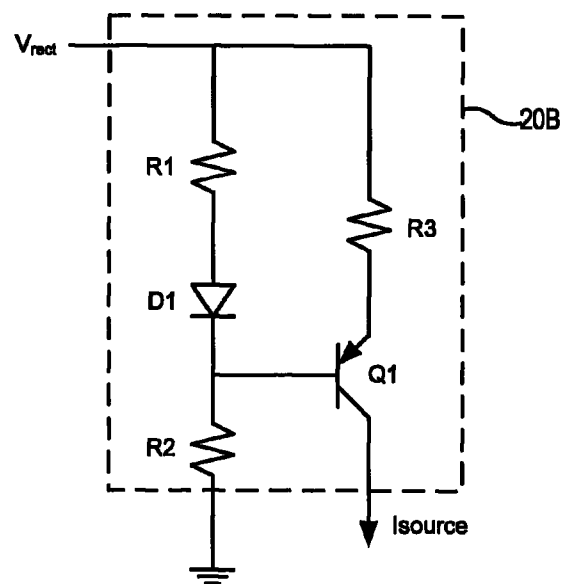
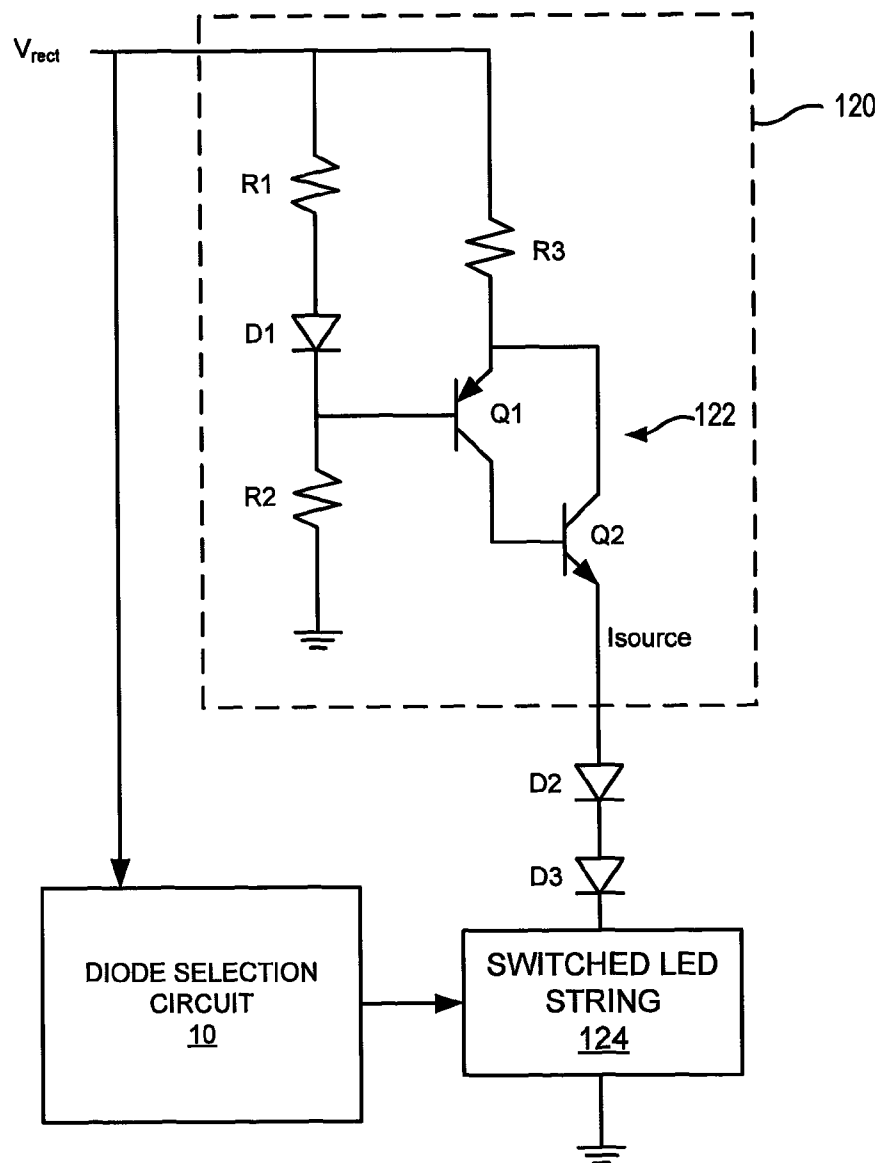
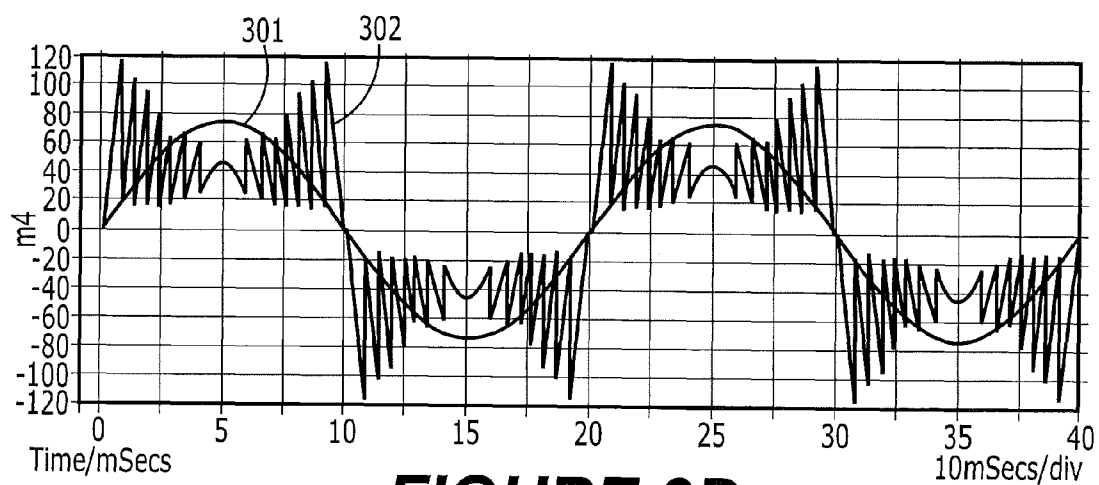


FIGURE 1C

**FIGURE 2**

**FIGURE 3A****FIGURE 3B**

**FIGURE 3C**

**FIGURE 3D**

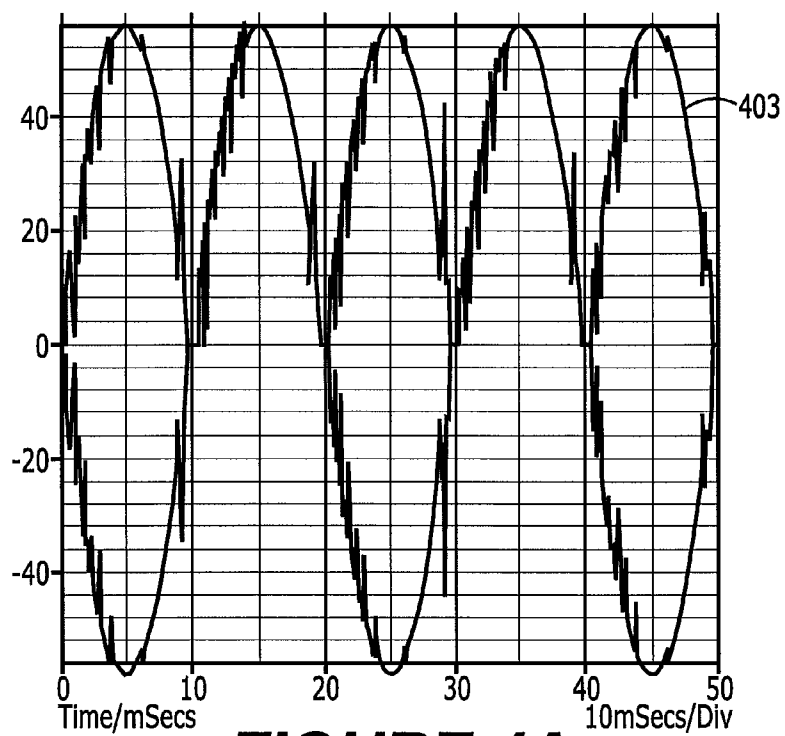


FIGURE 4A

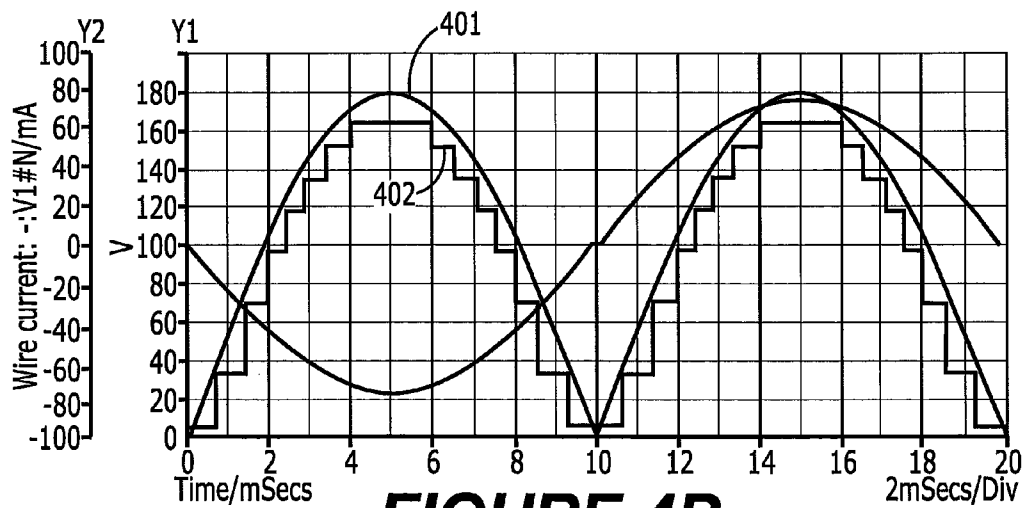


FIGURE 4B

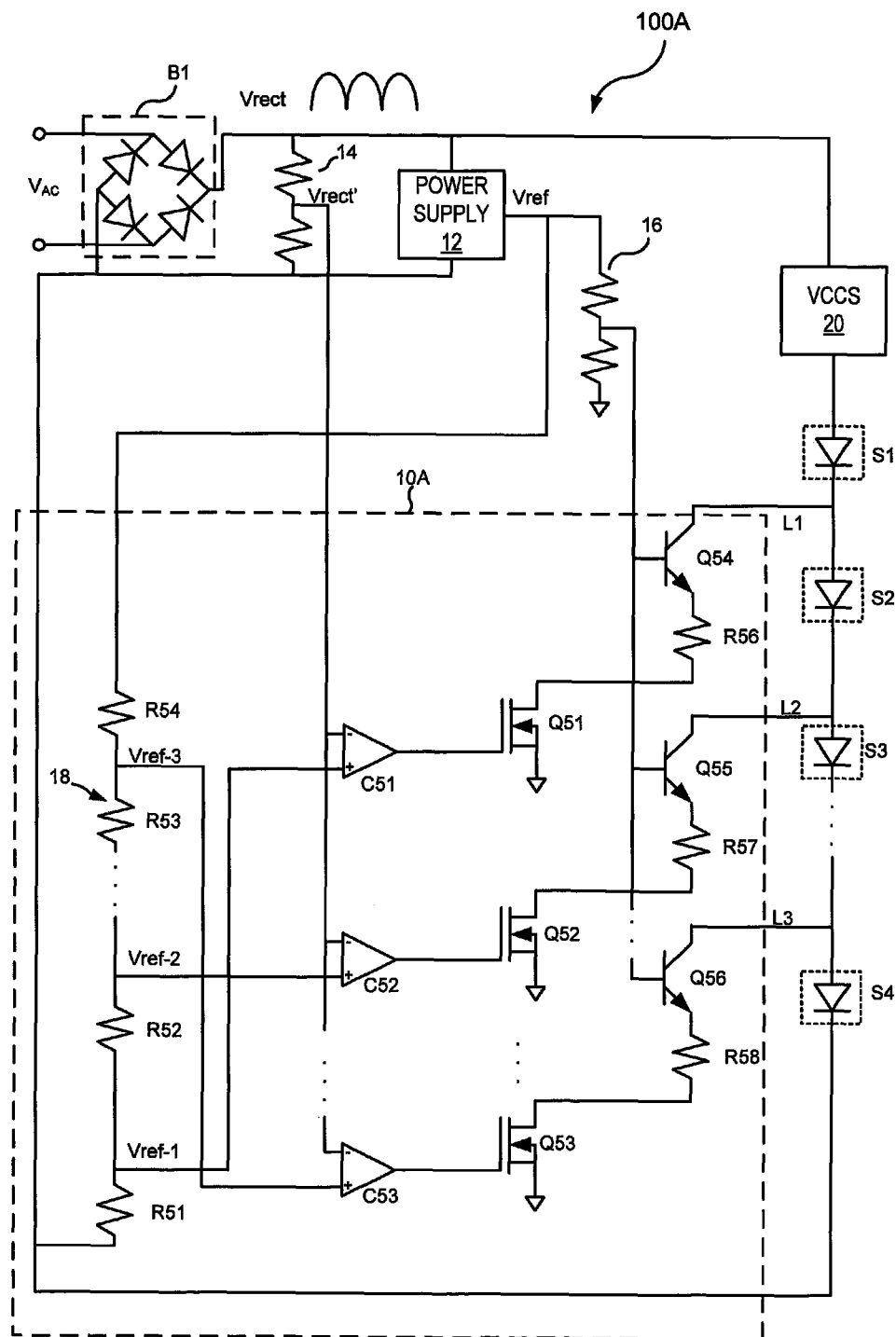
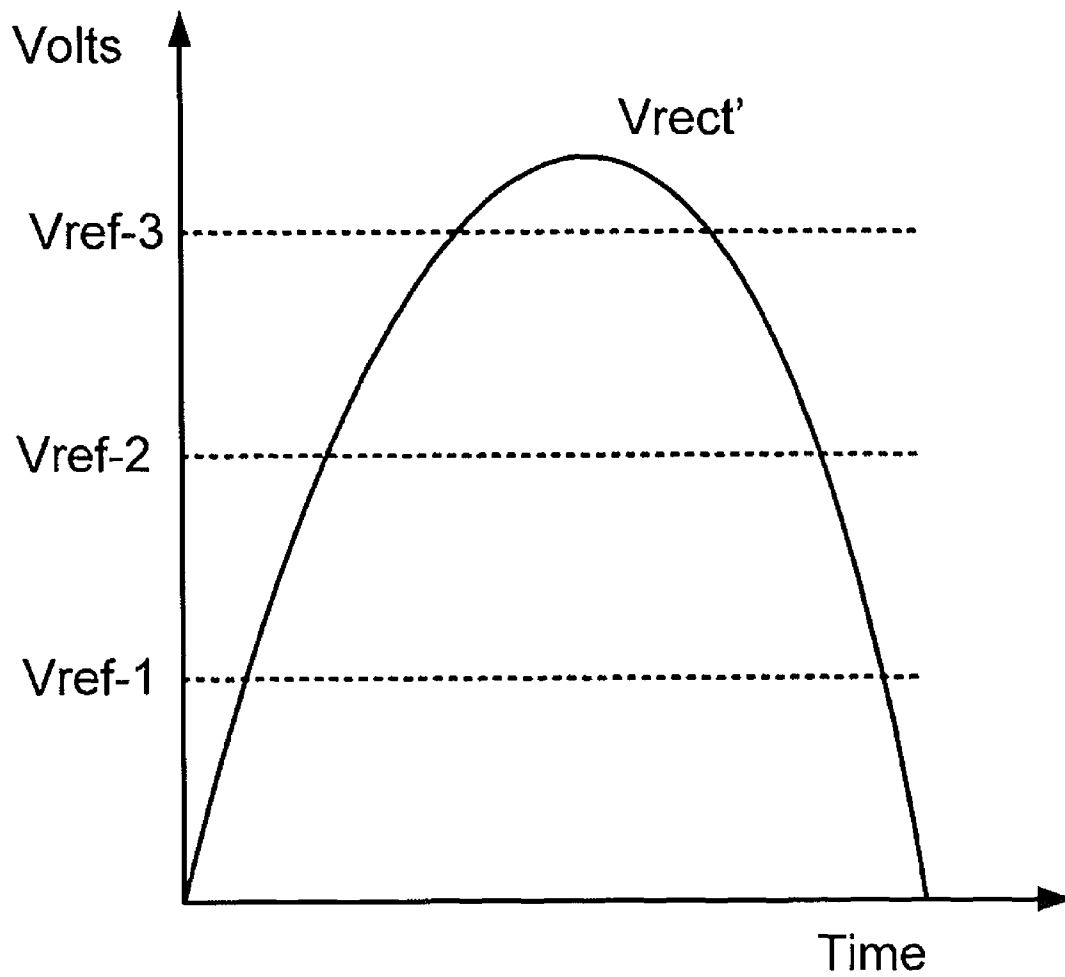
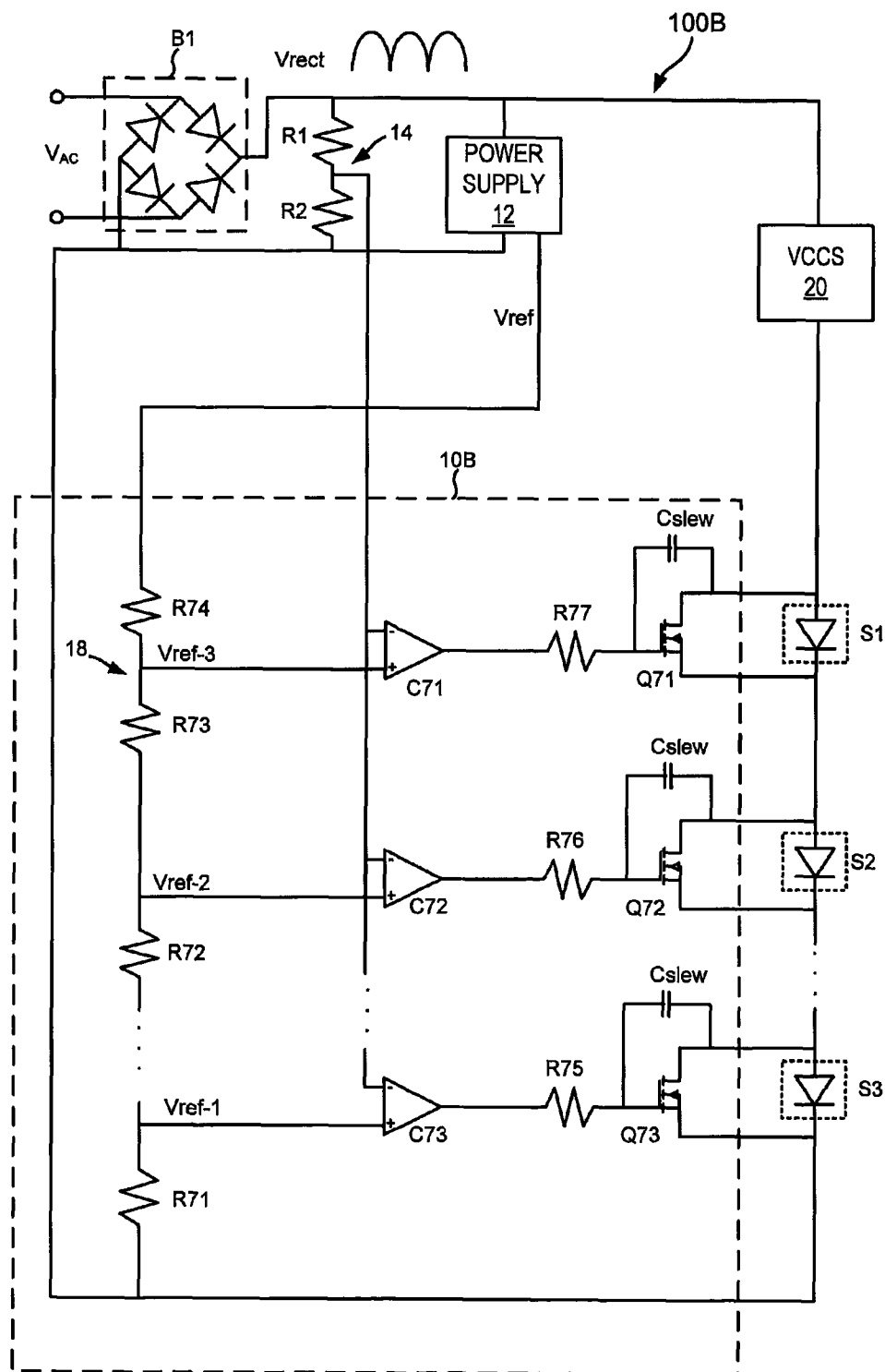
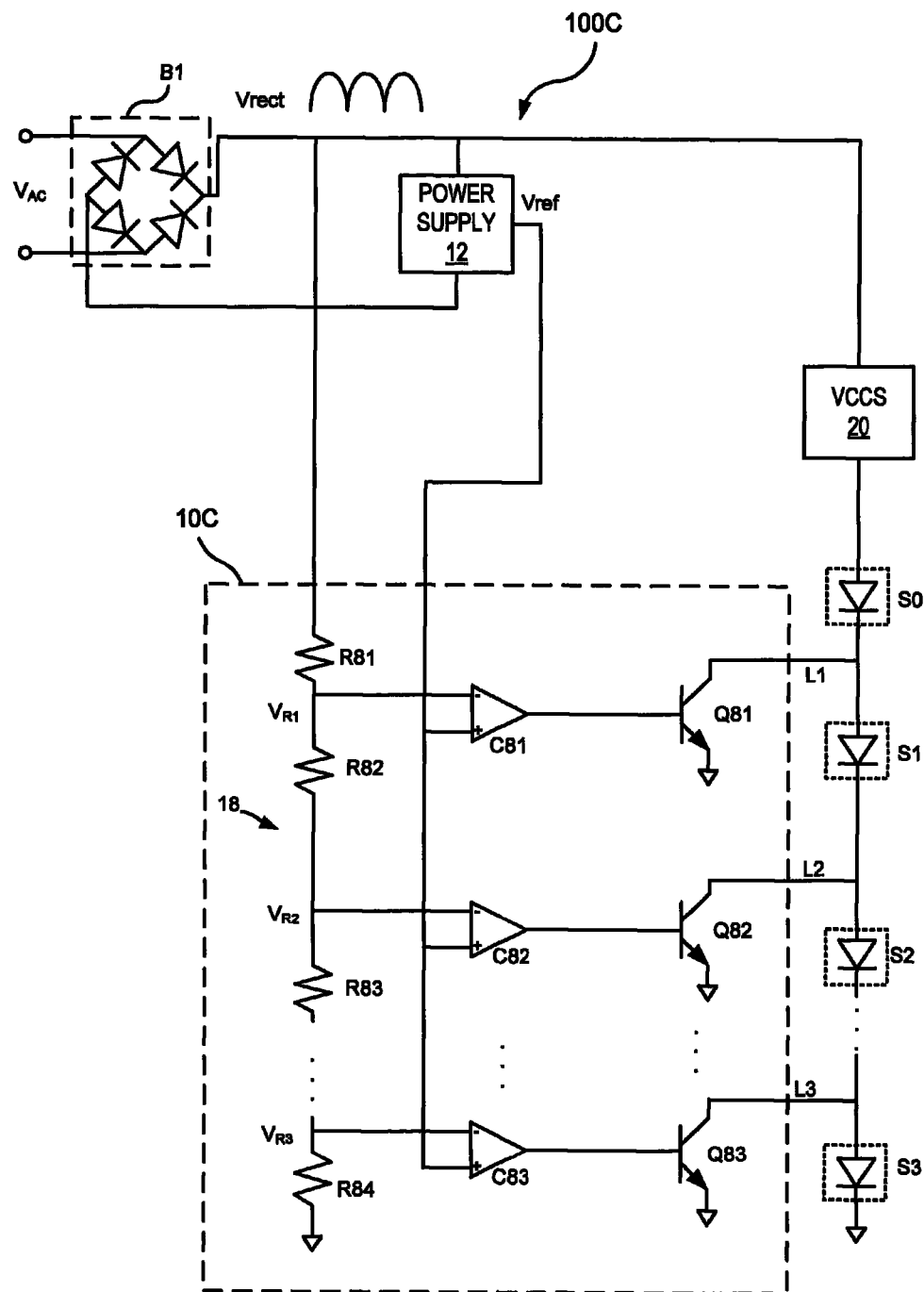
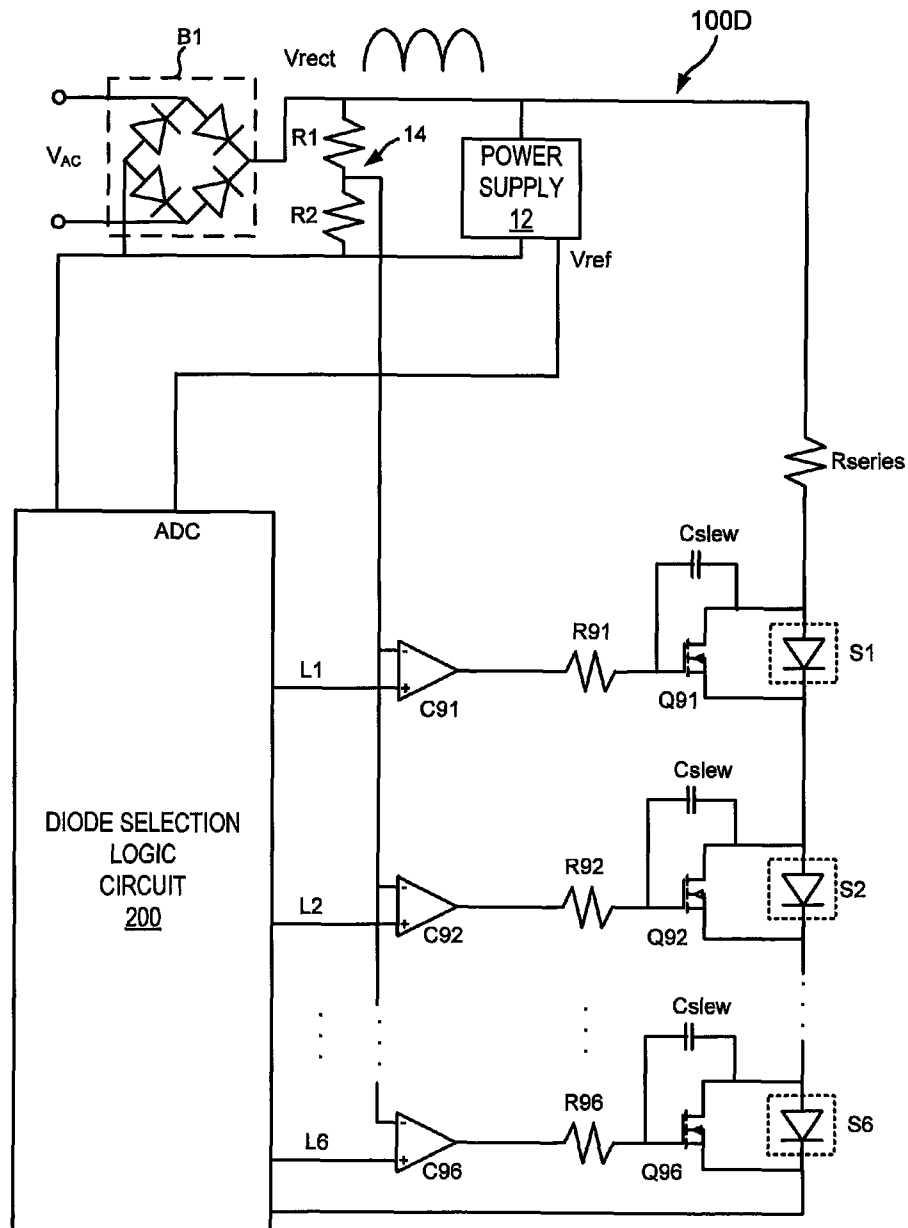


FIGURE 5

***FIGURE 6***

**FIGURE 7**

**FIGURE 8**

**FIGURE 9**

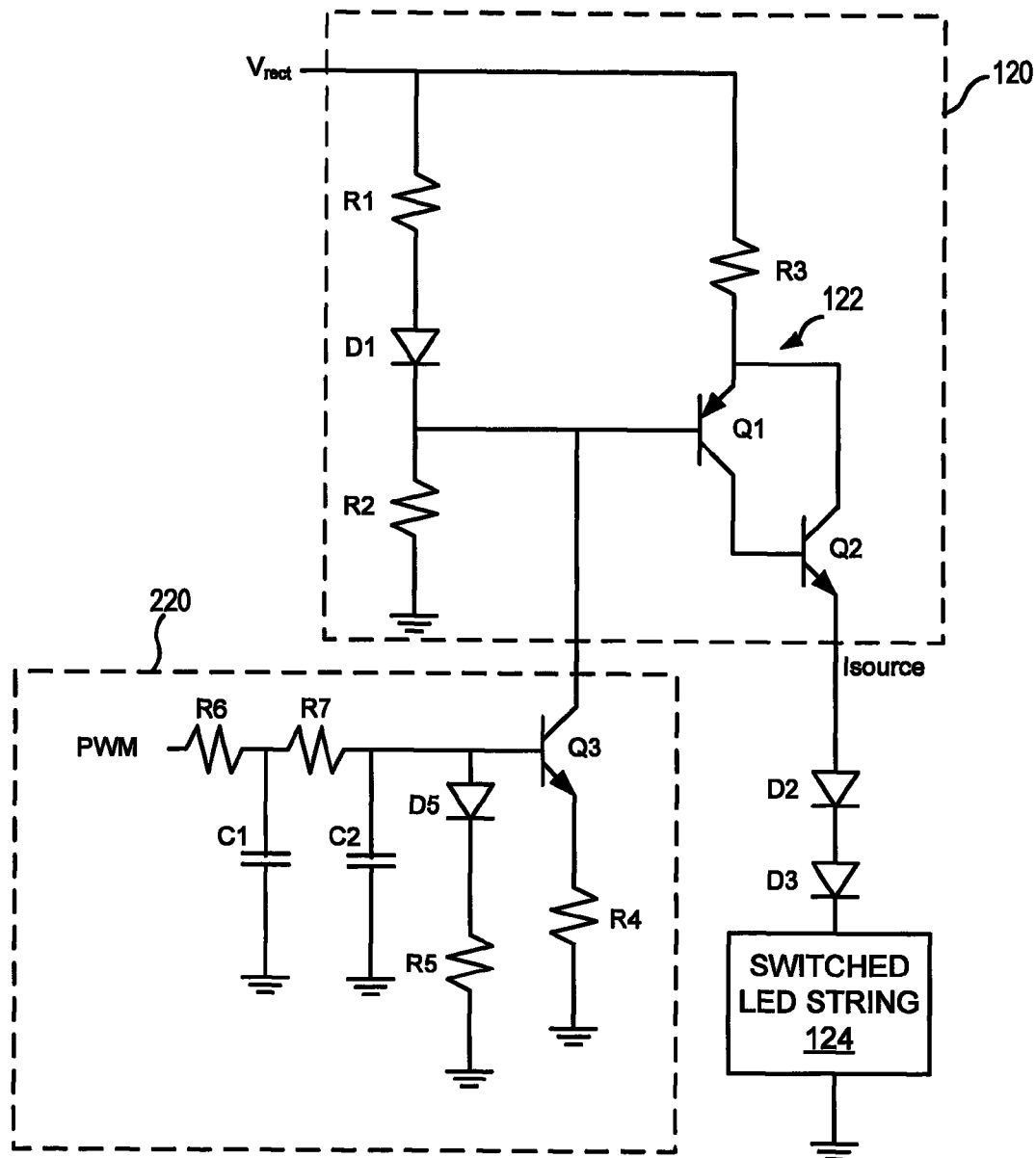


FIGURE 10

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AC DRIVEN SOLID STATE LIGHTING APPARATUS WITH LED STRING INCLUDING SWITCHED SEGMENTS

FIELD OF THE INVENTION

The present invention relates to solid state lighting, and more particularly to lighting fixtures including solid state lighting components.

BACKGROUND

Solid state lighting arrays are used for a number of lighting applications. For example, solid state lighting panels including arrays of solid state light emitting devices have been used as direct illumination sources, for example, in architectural and/or accent lighting. A solid state light emitting device may include, for example, a packaged light emitting device including one or more light emitting diodes (LEDs). Inorganic LEDs typically include semiconductor layers forming p-n junctions. Organic LEDs (OLEDs), which include organic light emission layers, are another type of solid state light emitting device. Typically, a solid state light emitting device generates light through the recombination of electronic carriers, i.e. electrons and holes, in a light emitting layer or region.

Solid state lighting panels are commonly used as backlights for small liquid crystal display (LCD) screens, such as LCD display screens used in portable electronic devices. In addition, there has been increased interest in the use of solid state lighting panels as backlights for larger displays, such as LCD television displays.

For smaller LCD screens, backlight assemblies typically employ white LED lighting devices that include a blue-emitting LED coated with a wavelength conversion phosphor that converts some of the blue light emitted by the LED into yellow light. The resulting light, which is a combination of blue light and yellow light, may appear white to an observer. However, while light generated by such an arrangement may appear white, objects illuminated by such light may not appear to have a natural coloring, because of the limited spectrum of the light. For example, because the light may have little energy in the red portion of the visible spectrum, red colors in an object may not be illuminated well by such light. As a result, the object may appear to have an unnatural coloring when viewed under such a light source.

The color rendering index (CRI) of a light source is an objective measure of the ability of the light generated by the source to accurately illuminate a broad range of colors. The color rendering index ranges from essentially zero for monochromatic sources to nearly 100 for incandescent sources. Light generated from a phosphor-based solid state light source may have a relatively low color rendering index.

For large-scale backlight and illumination applications, it is often desirable to provide a lighting source that generates a white light having a high color rendering index, so that objects and/or display screens illuminated by the lighting panel may appear more natural. Accordingly, to improve CRI, red light may be added to the white light, for example, by adding red emitting phosphor and/or red emitting devices to the apparatus. Other lighting sources may include red, green and blue light emitting devices. When red, green and blue light emitting devices are energized simultaneously, the resulting combined light may appear white, or nearly white, depending on the relative intensities of the red, green and blue sources.

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Although solid state light sources having high CRI and/or high efficiency have been demonstrated, one problem with the large-scale adoption of such light sources in architectural applications is that solid state lighting devices are typically designed to be driven using direct current (DC) power, while electric power is distributed using alternating current (AC), which is more efficient for long distance power distribution. Typically, a solid state lighting source is provided or coupled with a power converter that converts AC power into DC power, and the DC power is used to energize the light source. However, the use of such power converters increases the cost of the lighting source and/or the overall installation, and introduces additional efficiency losses.

Some attempts at providing AC-driven solid state lighting sources have involved driving an LED or string or group of LEDs using a rectified AC waveform. However, because the LEDs require a minimum forward voltage to turn on, the LEDs may turn on for only a part of the rectified AC waveform, which may result in visible flickering, may undesirably lower the power factor of the system, and/or may increase resistive loss in the system.

Other attempts at providing AC-driven solid state lighting sources have involved placing LEDs in an anti-parallel configuration, so that half of the LEDs are driven on each half-cycle of an AC waveform. However, this approach requires twice as many LEDs to produce the same luminous flux as using a rectified AC signal.

SUMMARY

A circuit for a light emitting apparatus according to some embodiments includes a plurality of light emitting devices coupled in series. The circuit includes a comparator configured to receive a rectified AC input signal and a reference voltage and to generate a control signal in response to comparison of the rectified AC input signal with the reference voltage, a voltage controlled current source configured to supply a current to the plurality of light emitting diodes that is proportional to the rectified AC input signal, and a switch configured to receive the control signal and to shunt current away from at least one of the plurality of light emitting devices in response to the control signal.

The voltage controlled current source may include a first transistor, an emitter resistor coupled to an emitter of the first transistor, a diode coupled to a base of the first transistor, a first resistor coupled to a first terminal of the diode and a second resistor coupled to a second terminal of the diode, and a terminal configured to receive the rectified AC input signal coupled to the emitter resistor and to the first resistor. The diode may include a Zener diode.

A collector of the first transistor may be coupled to the series of light emitting devices.

In some embodiments, the circuit may further include a second transistor including a base coupled to a collector of the first transistor and a collector coupled to the emitter of the first transistor.

The circuit may further include an adjustable current sink coupled to the base of the first transistor. The adjustable current sink may include a third transistor having a collector coupled to the base of the first transistor and an emitter coupled to ground, and a diode coupled to a base of the third transistor. The base of the third transistor is configured to receive a pulse width modulation (PWM) control signal configured to control a conductivity of the third transistor.

The circuit may be configured to shunt current away from the at least one light emitting device in response to a level of the rectified AC input signal being below a threshold level.

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The switch may include a field effect transistor, and the control signal may be applied to a gate of the field effect transistor.

The switch may further include a second transistor coupled in a cascode configuration with the field effect transistor so that conductivity of the second transistor may be controlled by the field effect transistor.

The second transistor may include a bipolar transistor including a base, a collector and an emitter, and a drain of the field effect transistor may be coupled to the emitter of the bipolar transistor, and the collector of the bipolar transistor may be coupled to an anode of the at least one light emitting device.

The circuit may further include a resistor coupled between the drain of the field effect transistor and the emitter of the bipolar transistor.

The diode selection circuit may further include a voltage divider ladder configured to generate a plurality of reference voltages, a plurality of comparators configured to receive the rectified AC input signal and a respective one of the plurality of reference voltages and to generate respective control signals in response to comparison of the rectified AC input signal with the respective reference voltages, and a plurality of switches configured to receive respective ones of the control signals and to shunt current away from respective ones of the plurality of light emitting devices in response to the control signals.

The switch may include a field effect transistor including a gate terminal and source/drain terminals, one of the source/drain terminals may be coupled to an anode of the at least one light emitting device and another of the source/drain terminals may be coupled to a cathode of the at least one light emitting device.

The circuit may further include a slew rate control capacitor coupled between the gate terminal of the field effect transistor and the anode of the at least one light emitting device.

The circuit may further include a voltage divider ladder configured to generate a plurality of reference voltages, a plurality of comparators configured to receive the rectified AC input signal and a respective one of the plurality of reference voltages and to generate respective control signals in response to comparison of the rectified AC input signal with the respective reference voltages, and a plurality of switches configured to receive respective ones of the control signals and to shunt current away from respective ones of the plurality of light emitting devices in response to the control signals.

The switch may include a bipolar transistor including a base coupled to an output of the comparator and having an emitter coupled to ground and a collector coupled to an anode of the at least one light emitting device.

A lighting apparatus according to some embodiments includes a terminal configured to receive an AC power signal, a full wave rectifier configured to generate a rectified AC input signal in response to the AC power signal, a reference voltage generator configured to generate a DC reference voltage in response to the rectified AC input signal, a plurality of light emitting devices coupled in series, a voltage controlled current source configured to supply a current to the plurality of light emitting diodes that is proportional to the rectified AC input signal, and a diode selection circuit including a comparator configured to receive the rectified AC input signal and the reference voltage and to generate a control signal in response to comparison of the rectified AC input signal with the reference voltage. The diode selection circuit includes a switch configured to receive the control signal and to shunt current away from at least one of the plurality of light emitting devices in response to the control signal.

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The voltage controlled current source may include a first transistor, an emitter resistor coupled to an emitter of the first transistor, a diode coupled to a base of the first transistor, a first resistor coupled to a first terminal of the diode and a second resistor coupled to a second terminal of the diode, and a terminal configured to receive the rectified AC input signal coupled to the emitter resistor and to the first resistor. The diode may include a Zener diode.

A collector of the first transistor may be coupled to the series of light emitting devices.

In some embodiments, the circuit may further include a second transistor including a base coupled to a collector of the first transistor and a collector coupled to the emitter of the first transistor.

The circuit may further include an adjustable current sink coupled to the base of the first transistor. The adjustable current sink may include a third transistor having a collector coupled to the base of the first transistor and an emitter coupled to ground, and a diode coupled to a base of the third transistor. The base of the third transistor is configured to receive a pulse width modulation (PWM) control signal configured to control a conductivity of the third transistor.

The diode selection circuit may be configured to shunt current away from the at least one light emitting device in response to a level of the rectified AC input signal being below a threshold level.

The switch may include a field effect transistor, and the control signal may be applied to a gate of the field effect transistor.

The switch may further include a second transistor coupled in a cascode configuration with the field effect transistor so that conductivity of the second transistor may be controlled by the field effect transistor.

The second transistor may include a bipolar transistor including a base, a collector and an emitter, and a drain of the field effect transistor may be coupled to the emitter of the bipolar transistor, and the collector of the bipolar transistor may be coupled to an anode of the at least one light emitting device.

The switch may include a field effect transistor including a gate terminal and source/drain terminals, one of the source/drain terminals may be coupled to an anode of the at least one light emitting device and another of the source/drain terminals may be coupled to a cathode of the at least one light emitting device.

The lighting apparatus may further include a current supply circuit coupled to an anode of a first one of the plurality of light emitting devices, the current supply circuit including a bipolar transistor including a collector coupled to the anode of the first light emitting device, an emitter resistor coupled to an emitter of the bipolar transistor, and a bias circuit coupled to a base of the bipolar transistor.

Other apparatus and/or methods according to embodiments of the invention will be or become apparent to one with skill in the art upon review of the following drawings and detailed description. It is intended that all such additional apparatus and/or methods be included within this description, be within the scope of the present invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate certain embodiment(s) of the invention. In the drawings:

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FIGS. 1A and 1B illustrate a solid state lighting apparatus in accordance with some embodiments of the invention.

FIG. 1C is a schematic circuit diagram illustrating series interconnection of light emitting devices (LEDs) in a solid state lighting apparatus.

FIG. 2 is a schematic circuit diagram illustrating a drive circuit for a solid state lighting apparatus in accordance with various embodiments of the invention.

FIGS. 3A, 3B and 3C are schematic circuit diagrams illustrating voltage controlled current sources for a solid state lighting apparatus in accordance with various embodiments of the invention.

FIG. 3D is a graph of simulated output current of voltage controlled current sources for a solid state lighting apparatus in accordance with various embodiments of the invention.

FIG. 4A is a graph illustrating output current, and FIG. 4B is a graph illustrating input and output voltage waveforms, for solid state lighting systems in accordance with various embodiments of the invention.

FIG. 5 is a schematic circuit diagram illustrating a diode selection circuit according to some embodiments of the invention.

FIG. 6 is a graph illustrating a rectified voltage signal according to some embodiments.

FIGS. 7, 8 and 9 are schematic circuit diagrams illustrating diode selection circuits according to further embodiments of the invention.

FIG. 10 is a schematic circuit diagram illustrating a voltage controlled current sources with an adjustable current sink for a solid state lighting apparatus in accordance with some embodiments of the invention.

DETAILED DESCRIPTION OF EMBODIMENTS

Embodiments of the present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present invention. As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.

It will be understood that when an element such as a layer, region or substrate is referred to as being “on” or extending “onto” another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly on” or extending “directly onto” another element, there are no intervening elements present. It will also be understood that when an element is referred to as being “connected” or “coupled” to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element, there are no intervening elements present.

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Relative terms such as “below” or “above” or “upper” or “lower” or “horizontal” or “vertical” may be used herein to describe a relationship of one element, layer or region to another element, layer or region as illustrated in the figures. It will be understood that these terms are intended to encompass different orientations of the device in addition to the orientation depicted in the figures.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms “a”, “an” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises” “comprising,” “includes” and/or “including” when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

Referring to FIGS. 1A and 1B, a lighting apparatus 10 according to some embodiments is illustrated. The lighting apparatus 10 shown in FIGS. 1A and 1B is a “can” lighting fixture that may be suitable for use in general illumination applications as a down light or spot light. However, it will be appreciated that a lighting apparatus according to some embodiments may have a different form factor. For example, a lighting apparatus according to some embodiments can have the shape of a conventional light bulb, a pan or tray light, an automotive headlamp, or any other suitable form.

The lighting apparatus 10 generally includes a can shaped outer housing 12 in which a lighting panel 20 is arranged. In the embodiments illustrated in FIGS. 1A and 1B, the lighting panel 20 has a generally circular shape so as to fit within an interior of the cylindrical housing 12. Light is generated by solid state lighting devices (LEDs) 22, 24, which are mounted on the lighting panel 20, and which are arranged to emit light 15 towards a diffusing lens 14 mounted at the end of the housing 12. Diffused light 17 is emitted through the lens 14. In some embodiments, the lens 14 may not diffuse the emitted light 15, but may redirect and/or focus the emitted light 15 in a desired near-field or far-field pattern.

Still referring to FIGS. 1A and 1B, the solid-state lighting apparatus 10 may include a plurality of first LEDs 22 and a plurality of second LEDs 24. In some embodiments, the plurality of first LEDs 22 may include white emitting, or near white emitting, light emitting devices. The plurality of second LEDs 24 may include light emitting devices that emit light having a different dominant wavelength from the first LEDs 22, so that combined light emitted by the first LEDs 22 and the second LEDs 24 may have a desired color and/or spectral content.

For example, the combined light emitted by the plurality of first LEDs 22 and the plurality of second LEDs 24 may be warm white light that has a high color rendering Index.

The chromaticity of a particular light source may be referred to as the “color point” of the source. For a white light source, the chromaticity may be referred to as the “white point” of the source. The white point of a white light source may fall along a locus of chromaticity points corresponding to

the color of light emitted by a black-body radiator heated to a given temperature. Accordingly, a white point may be identified by a correlated color temperature (CCT) of the light source, which is the temperature at which the heated black-body radiator matches the hue of the light source. White light typically has a CCT of between about 2500K and 8000K. White light with a CCT of 2500K has a reddish color, white light with a CCT of 4000K has a yellowish color, and white light with a CCT of 8000K is bluish in color.

“Warm white” generally refers to white light that has a CCT between about 3000K and 3500K. In particular, warm white light may have wavelength components in the red region of the spectrum, and may appear yellowish to an observer. Warm white light typically provides a relatively high CRI, and accordingly can cause illuminated objects to have a more natural color. For illumination applications, it is therefore desirable to provide a warm white light.

In order to achieve warm white emission, conventional packaged LEDs include either a single component orange phosphor in combination with a blue LED or a mixture of yellow/green and orange/red phosphors in combination with a blue LED. However, using a single component orange phosphor can result in a low CRI as a result of the absence of greenish and reddish hues. On the other hand, red phosphors are typically much less efficient than yellow phosphors. Therefore, the addition of red phosphor in yellow phosphor can reduce the efficiency of the package, which can result in poor luminous efficacy. Luminous efficacy is a measure of the proportion of the energy supplied to a lamp that is converted into light energy. It is calculated by dividing the lamp’s luminous flux, measured in lumens, by the power consumption, measured in watts.

Warm white light can also be generated by combining non-white light with red light as described in U.S. Pat. No. 7,213,940, entitled “LIGHTING DEVICE AND LIGHTING METHOD,” which is assigned to the assignee of the present invention, and the disclosure of which is incorporated herein by reference. As described therein, a lighting device may include first and second groups of solid state light emitters, which emit light having dominant wavelength in ranges of from 430 nm to 480 nm and from 600 nm to 630 nm, respectively, and a first group of phosphors which emit light having dominant wavelength in the range of from 555 nm to 585 nm. A combination of light exiting the lighting device which was emitted by the first group of emitters, and light exiting the lighting device which was emitted by the first group of phosphors produces a sub-mixture of light having x, y color coordinates within a defined area on a 1931 CIE Chromaticity Diagram that is referred to herein as “blue-shifted yellow” or “BSY.” Such non-white light may, when combined with light having a dominant wavelength from 600 nm to 630 nm, produce warm white light.

Blue and/or green LEDs used in a lighting apparatus according to some embodiments may be InGaN-based blue and/or green LED chips available from Cree, Inc., the assignee of the present invention. Red LEDs used in the lighting apparatus may be, for example, AlInGaP LED chips available from Epistar, Osram and others.

In some embodiments, the LEDs 22, 24 may have a square or rectangular periphery with an edge length of about 900 μ m or greater (i.e. so-called “power chips.” However, in other embodiments, the LED chips 22, 24 may have an edge length of 500 μ m or less (i.e. so-called “small chips”). In particular, small LED chips may operate with better electrical conversion efficiency than power chips. For example, green LED chips with a maximum edge dimension less than 500 microns and as small as 260 microns, commonly have a higher elec-

trical conversion efficiency than 900 micron chips, and are known to typically produce 55 lumens of luminous flux per Watt of dissipated electrical power and as much as 90 lumens of luminous flux per Watt of dissipated electrical power.

The LEDs 22 in the lighting apparatus 10 may include white/BSY emitting LEDs, while the LEDs 24 in the lighting apparatus may emit red light. The LEDs 22, 24 in the lighting apparatus 10 may be electrically interconnected in respective strings, as illustrated in the schematic circuit diagram in FIG. 1C. As shown therein, the LEDs 22, 24 may be interconnected such that the white/BSY LEDs 22 are connected in series to form a first string 34A. Likewise, the red LEDs 24 may be arranged in series to form a second string 34B. Each string 32, 34 may be connected to a respective anode terminal 23A, 25A and a cathode terminal 23B, 25B.

Although two strings 34A, 34B are illustrated in FIG. 1C, it will be appreciated that the lighting apparatus 10 may include more or fewer strings. Furthermore, there may be multiple strings of white/BSY LEDs 22, and multiple strings of red or other colored LEDs 24.

Referring now to FIG. 2, a drive circuit 100 for driving a plurality of solid state light emitting devices in a solid state lighting apparatus is illustrated. In particular, the drive circuit 100 is configured to drive a plurality of LEDs, or sets of LEDs, that are connected in series. As illustrated in FIG. 2, the sets of LEDs may include and sets S1, S2, . . . SN. Each set of LEDs S1 to SN may include one or more LEDs connected in series and/or parallel. For example, as illustrated in set S1, the LEDs in a set may be connected in respective series strings that are themselves connected in parallel. The total number of LEDs in series may be selected so that the circuit has a suitably high efficiency when the input voltage to the string is at the maximum line voltage. Efficiency may also be increased by keeping the voltage across the selected LEDs close to an applied AC voltage, as discussed below.

An alternating current signal V_{AC} is applied to a full wave rectifier bridge B1. The output of the full wave rectifier bridge B1 is a rectified AC signal V_{rect} . The rectified AC signal V_{rect} may be applied to a current source, such as a series resistor or a voltage controlled current source, which supplies current to the first set S1 of LEDs. Subsequent sets of solid state lighting devices S2 to SN are connected in series with the first set S1. Control lines L2, L3, . . . LN are coupled to anodes of respective sets of LEDs S2 to SN.

The drive circuit 100 includes a diode selection circuit 10, a power supply 12, and a voltage divider 14. The rectified signal V_{rect} is divided by the voltage divider 14 and supplied as a control signal to the diode selection circuit 10. The rectified signal V_{rect} is also supplied to a power supply 12, which responsively generates a substantially steady reference voltage V_{ref} , which is also supplied to the diode selection circuit 10. In some embodiments, the power supply 12 may generate more than one reference voltage, e.g., a family of reference voltages of various levels.

The diode selection circuit 10 is configured to dynamically adjust the number of LEDs that are being driven by the rectified AC voltage V_{rect} in response to a level of the rectified AC signal V_{rect} , so that a voltage drop of diodes that are being driven at any given point in time is less than the level of the rectified AC signal V_{rect} . In this manner, the AC waveform may be more fully utilized, potentially increasing light output from the circuit, improving the power factor of the circuit, and/or reducing visible flicker of light generated by the circuit. In general, the diode selection circuit is designed to keep the instantaneous LED string voltage close to but always slightly less than V_{rect} , which may reduce or minimize the voltage dropped across the current source 20,

thereby increasing or maximizing efficiency, and more fully utilizing the AC waveform to generate more light. In some embodiments, compared to apparatus including non-switched LED strings, the THD may improve from 85% to 25%.

In operation, when the level of the rectified AC voltage V_{rect} is low, only the first group LEDs S1 may be driven by the rectified AC signal V_{rect} , while the other sets of LEDs S2 to SN may be switched out of the circuit and/or bypassed, so that they are not being driven by the rectified signal V_{rect} . As the rectified AC signal V_{rect} increases, successive sets of LEDs S2 to SN may be switched into the circuit so that they are being driven by the rectified AC signal V_{rect} until all of the sets of LEDs S1 to SN have been switched into the circuit and are being driven by the rectified AC signal V_{rect} .

In a switching arrangement that utilizes a resistor (R_{series}) as the current source, the voltage across R_{series} starts off small, and increases until the next switching threshold is reached, at which point it returns to zero and the process begins again. This is during the first half-cycle of $V_{rect}(t)$, where $V_{rect}(t)$ is rising. During the second half-cycle of $V_{rect}(t)$, $V_{rect}(t)$ is falling and the LED current is the mirror image of the first half-cycle. It is therefore sufficient to consider only the first half-cycle. Assuming a Binary Weighted Switching approach in which LEDs are controllably switched in groups of 1, 2, 4, 8, etc., the LED current is given by:

$$V_{rect}(t) = V_{peak} * |\sin(2 * \pi * Fac * t)| - 2 * V_f$$

$$V_{r_series} = V_{rect}(t) - \text{floor}([V_{rect}(t) - V_{drop}] / V_{led}) * V_{led}$$

$$I_{LED}(t) = [V_{rect}(t) - \text{floor}([V_{rect}(t) - V_{drop}] / V_{led}) * V_{led}] / R_{series}$$

Rather than using a series resistor, some embodiments drive the bank of dynamically switched LEDs with a Voltage Controlled Current Source (or sink)—a VCCS, as illustrated in FIG. 3A.

According to some embodiments, current to the LED string is provided by a voltage controlled current source (VCCS) 20A. The current source 20A includes a PNP transistor Q1 having an emitter resistor R_E coupled to the emitter thereof and a bias circuit including resistors R_H and R_L and a zener diode V_Z coupled to the base thereof. Output current I_{OUT} is sourced by the current source 20 according to the following equations:

$$I_{SOURCE} = \frac{V_Z}{R_E} + V_{rect} \left(\frac{R_H}{R_H + R_L} \right) \left(\frac{1}{R_E} \right)$$

$$I_{SOURCE} = I_0 + k V_{rect}$$

Accordingly, the output current is proportional to the rectified input voltage V_{rect} . This circuit may therefore further regulate the output current to help reduce spikes as sets of LEDs are switched into/out of the circuit. It will be appreciated that the zener diode could be replaced with another type of diode that has a voltage drop that is substantially matched to the base-emitter junction of the transistor Q1.

A more general illustration of a VCCS 20B is shown in FIG. 3B, and will be discussed below.

The VCCS 20B illustrated in FIG. 3B includes resistors R1, R2 and R3, diode D1 and PNP transistor Q1. Assuming D1 and Q1 are matched and thermally coupled, $V_f(D1) = V_{be}(Q1)$. Assuming transistor Q1 has sufficient gain, then the voltage across resistor R3 is the same as the voltage across resistor R1.

Referring to FIG. 3C, a Sziklai pair 122 may be used in a VCCS current source 120 according to some embodiments. The Sziklai pair 122 includes a PNP transistor Q1 and an NPN transistor Q2. The collector of the PNP transistor Q1 is coupled to the base of the NPN transistor Q2, and the emitter of the PNP transistor Q1 is coupled to the collector of the NPN transistor Q2, as shown in FIG. 3C. The emitter of the NPN transistor Q2 is coupled to the switched LED string 124, which is controlled by the diode selection circuit 10. A Sziklai pair may have a low saturation voltage and temperature coefficient, but very high gain (and the high power transistor Q2 is NPN). Darlington transistors may be used, but the saturation voltage is larger and there are two base-emitter junctions requiring thermal compensation. MOSFET current sources may also be used in some embodiments.

If we then assume that $V_{rect}(t) \gg V_f(D1)$, the voltage across R1 is given by:

$$V_{r1} = V_{rect}(t) - V_{rect}(t) * R2 / (R1 + R2)$$

which re-arranges to give:

$$V_{r1} = V_{rect}(t) * R1 / (R1 + R2)$$

Furthermore:

$$V_{r3} = I_{source} * R3 = V_{r1}$$

Thus:

$$I_{source} * R3 = V_{rect}(t) * R1 / (R1 + R2)$$

$$I_{source} = [V_{rect}(t) / R3] * [R1 / (R1 + R2)]$$

$$I_{source} = [V_{rect}(t) / R3] * [1 / (R1 + R2) / R1]$$

$$I_{source} = [V_{rect}(t) / R3] * [1 / (1 + R2 / R1)]$$

$$I_{source} = V_{rect}(t) / [R3 * (1 + R2 / R1)]$$

which can be written as:

$$I_{source}(t) = V_{rect}(t) / R_{eq}$$

$$R_{eq} = R3 * (1 + R2 / R1)$$

Although it is called a constant current source, it is clear that the current I_{source} is directly proportional to $V_{rect}(t)$. Hence the term Voltage Controlled Current Source (VCCS) is more properly used to describe the current source 20B.

Typical circuit designs attempt to remove the dependence on $V_{rect}(t)$. However, in some embodiments, it may be more appropriate not to have a constant current. If D1 is used to compensate for the static and dynamic base-emitter voltage V_{be} of Q1 (-2.2 mV/K), a Voltage Controlled Current Source (VCCS) is provided. The VCCS has a minimum dropout voltage of:

$$V_{dropout} = V_{cesat}(Q1) + I_{source} * R3$$

Where $V_{cesat}(Q1)$ increases with increasing I_{source} . It is sufficient to use I_{source_max} when calculating $V_{cesat}(Q1)$ and the voltage drop across R3. If a string of dynamically switched LEDs is driven with a VCCS, and the circuit is designed so that $V_{drop} > V_{dropout}$ (in other words the dynamic switching controller ensures the VCCS always has enough headroom to regulate I_{source}), then the LED current is always proportional to $V_{rect}(t)$.

As noted above:

$$V_{rect}(t) = V_{peak} * |\sin(2 * \pi * Fac * t)| - 2 * V_f$$

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Assuming $V_{peak} * |\sin(2 * \pi * Fac * t)| >> 2 * V_f$, then:

$$V_{rect}(t) = V_{peak} * |\sin(2 * \pi * Fac * t)|$$

and

$$I_{source}(t) = V_{rect}(t) / R_{eq}$$

Thus:

$$I_{source}(t) = V_{peak} * |\sin(2 * \pi * Fac * t)| / R_{eq}$$

$$I_{source}(t) = [V_{peak} / R_{eq}] * |\sin(2 * \pi * Fac * t)|$$

$$I_{source}(t) = I_{peak} * |\sin(2 * \pi * Fac * t)|$$

where $I_{peak} = V_{peak} / R_{eq}$ and $R_{eq} = R_3 * (1 + R_2 / R_1)$

The input current is therefore substantially sinusoidal, although the foregoing analysis has ignored the bridge rectifier, D_1 and V_{drop} voltages, which cause a small amount of dead time and prevent $I_{source}(t)$ from being perfectly sinusoidal.

A simulation comparing a VCCS with a resistor current source is shown in FIG. 3D. Curve **301** is a graph of $I_{source}(t)$ for a dynamically switched LED driver circuit including a VCCS current source with an equivalent resistance $R_{eq} = 2.22 \text{ k}\Omega$, while curve **302** is a graph of $I_{source}(t)$ for a dynamically switched LED driver circuit including a series resistor current source having a resistance $R_{series} = 270 \Omega$.

Both circuits use the same Dynamically Switched LED string which is non-linear (but not binary), and designed for minimum loss with 7 switches. Two LEDs are always in series, to provide for a free low voltage supply (and to allow for flicker-free dimming).

For a resistor current source using $R_{series} = 270 \Omega$, the total harmonic distortion is 77.4%. For the VCCS with $R_{eq} = 2.22 \text{ k}\Omega$, the input current is very close to a pure sinusoid, and has 2.4% THD. The power factor is greater than 0.99.

In embodiments in which the LED current is set using a Voltage Controlled Current Source, such as the VCCS circuits **20A**, **20B** illustrated in FIGS. **3A** and/or FIG. **3B**, to set the LED current proportional to V_{rect} , the output current waveform may exhibit some spikes at the switching instant, as illustrated in FIG. **4A**, which is a graph **403** of simulated output current for a circuit according to some embodiments. Current spikes are visible in the output current signal **403** at the switching instants.

When a set of k LEDs is switched in (or out) of the string, the LED string voltage rises (or falls) by $k * V_{led}$. This occurs fairly quickly—shorting a set is as fast as the shorting switch itself. The time taken removing the short circuit from a set is governed by the current source charging the stray capacitance of the set, which is fairly small.

Once a shorting switch is turned OFF (and assuming there are not minority carrier storage-time issues), the current source sets the slew rate as it charges up the stray capacitance. However, the current source is haversinusoidal, so over one quarter AC line period the current ranges from near zero to $1.4 * I_{rms}$.

The uppermost LED anode connects to the collector of the PNP current source transistor **Q4**, so changes in the LED string voltage change the PNP collector voltage an equal amount.

This feeds current $I = C_m * dV/dt$ from the collector to the base through the BJT Miller capacitance C_m , and causes the current source to misbehave, which is what creates the spikes shown in FIG. **4B**.

It may be possible to reduce or avoid these spikes by designing the VCCS so they are reduced, or by controlling the slew rate of the switches.

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Simulated example voltage and current waveforms for a drive circuit **100** according to some embodiments are illustrated in FIG. **4B**. Referring to FIG. **4B**, curve **401** is a rectified AC sine wave V_{rect} , while curve **402** is a graph of the voltage across the LEDs that are switched into the circuit at any given instant, that is, the sum of the voltage drops of all of the LEDs that are energized at a particular instant. As illustrated in FIG. **4A**, as the rectified AC signal V_{rect} increases, successive groups of LEDs are switched into the circuit, and the output voltage increases in steps as successive sets of LEDs are energized.

According to some embodiments, the numbers of LEDs that are switched on at any given step and the threshold levels of V_{rect} that result in such sets being switched in our chosen so that the level of V_{rect} remains greater than the sum of the forward voltages of the energized LEDs at each successive step. Accordingly, as the level of V_{rect} rises, all LEDs that are switched into the circuit may remain energized when a successive set of LEDs is switched into the circuit.

As the level of V_{rect} falls, successive sets of LEDs may be switched out of the circuit to ensure that the level of the voltage across the energized diodes remains below V_{rect} at substantially each time instant.

Referring again to FIG. **2**, once V_{rect} exceeds the voltage required to turn on the LEDs in set **S1**, the LEDs are forward biased and current begins to flow through the LEDs. The voltage dropped across these resistors is equal to $V_{rect} - V_{led}$ (where V_{led} is the voltage across the LEDs in **S1**), so the current ramps up with the same slope as V_{rect} . When V_{rect} is sufficiently above V_{led} (as a function of losses in the current source), the diode selection circuit **100** switches the next set **S2** of LEDs in series, so the total LED string voltage increases by $V_{new_led_string}$, which may be chosen such that:

$$V_{rect}(t = T_{switch}) > V_{led} + V_{new_led_string}.$$

This ensures that when the new LED string is switched in series, the current through the current source is still slightly positive.

We can define $dV = V_{rect}(T_{switch}) - (V_{led} + V_{new_led_string})$. If $dV > 0$, current through the LEDs drops down to a positive, non-zero value when the new set is switched into the series. If $dV = 0$, the current drops down to zero when the new set is switched into the series.

If $dV < 0$, the current tries to drop below zero, but the LEDs are unipolar so current cannot flow, and current continues to not flow until V_{rect} rises enough to make $V_{led} > 0$.

Thus, when $dV \leq 0$, current in the LEDs is equal to zero, so dV should be made greater than zero keep current flowing through the diodes, regardless of current control methodology. If not, the current drops to zero at the switching edge, and stays there until V_{rect} is greater than the voltage drop of all LEDs switched into the series.

Furthermore, as dV becomes more negative the zero current period gets longer. So, the switching edge may give rise to notches (down/up to 0 A) in the input current waveform, if dV is not chosen well.

With a resistor as the input current source, all that is needed is $dV \geq 0$. With a current source, however, there is a finite dropout voltage V_{csdo} , that may, for example, be about 1V, below which the current source is OFF. The constraint on dV when using a Voltage Controlled Current Source (VCCS) is therefore $dV \geq V_{csdo}$.

A drive circuit **100A** including a diode selection circuit **10A** is illustrated in more detail in FIG. **5**. As illustrated therein, the diode selection circuit **10A** includes a voltage divider ladder **18** including resistors **R51** to **R54** that generate

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a plurality of reference voltages Vref-1, Vref-2 and Vref-3 from the reference voltage Vref.

The diode selection circuit 10A further includes a plurality of comparators C51 to C53 and switching transistors Q51 to Q53 having gates coupled to respective outputs of the comparators C51 to C53. In the embodiments illustrated in FIG. 5, sources of the switching transistors Q51 to Q53 are coupled to ground, and drains of the switching transistors Q51 to Q53 are coupled to emitters of respective shunting bipolar transistors Q54 to Q56 through respective resistors R56, R57 and R58. Collectors of the bipolar shunting transistors Q54 to Q56 are coupled to respective control lines L1, L2, and L3, which are in turn coupled to anodes of respective ones of the sets S2, S3 and S4 of LEDs.

Reference voltages Vrect-1 to Vrect-3 generated by the voltage divider ladder 18 are applied to the non-inverting inputs of the comparators C51 to C53. In particular, the lowest reference voltage Vref-1 is applied to the non-inverting input of the comparator C51, the reference voltage Vref-2 is applied to non-inverting input of the comparator C52, and the highest reference voltage Vref-3 is applied to the non-inverting input of the comparator C53.

An optional voltage divider 16 supplies a bias voltage to the bases of the respective bipolar shunting transistors Q54 to Q56.

One or more of the sets S2 to S4 of series connected LEDs may be switched out of the drive circuit based on the level of the rectified AC input signal Vrect. In particular, based on a comparison of the level of Vrect' with one of the reference voltages Vref-2 to Vref-3, the drive current of the LEDs may be shunted through one of the bipolar shunting transistors Q54 to Q56 through a respective emitter resistor R56 to R58 to ground, bypassing one or more sets of LEDs S2 to S4. Current through the remaining LEDs may be controlled by the bias level of the bipolar shunting transistor Q54 to Q56 through which the LED drive current is shunted.

Operation of the drive circuit 100A and the diode selection circuit 10A illustrated in FIG. 5 will now be described further reference to FIG. 6, which is a graph of one cycle of the scaled AC rectified signal Vrect'. Referring to FIGS. 5 and 6, when the value of Vrect' is lower than the lowest reference voltage Vref-1, the non-inverting inputs to the comparators C51 to C53 are all less than the corresponding reference voltages Vref-2 to Vref-3 that are input into the non-inverting inputs to the comparators C51 to C53. Accordingly, each of the comparators C51 to C53 generates a high output voltage, which switches each of the respective switching transistors Q51 to Q53 to an ON state. In particular, the transistor Q51 is switched on, which also is emitter switches the bipolar shunting transistor Q54 to a conductive state. When the bipolar shunting transistor Q54 is conductive, the anode of the second set S2 of LEDs is coupled to ground through the switching transistor Q51, thereby bypassing the subsequent sets S2 to S4 of LEDs.

When the level of Vrect exceeds the forward voltage drop of the LEDs in the first set S1, the LEDs in the first set S1 will turn on and begin to generate light.

As the level of Vrect' continues to increase, it reaches the lowest reference voltage Vrect-1. At that point, the output of the comparator C51 switches to low, thereby turning off the switching transistor Q51 and the bipolar shunting transistor Q54. However, because the voltage Vrect' is still less than the second reference voltage Vref-2, comparators C52 and C53 continue to output a high level, so that the third and fourth sets S3 and S4 of LEDs continue to be switched out of the circuit

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and not energized. Thus, when the level of Vrect' is between Vref-1 and Vref-2, only the first and second sets S1 and S2 of LEDs may be energized.

As Vrect' continues to increase, it reaches the value of Vref-2, at which point the second comparator C52 also switches to a low output, turning off switching transistor Q52 and bipolar shunting transistor Q55. This switches the third set S3 of LEDs into the drive circuit, while continuing to bypass the fourth set S4 of LEDs.

Finally, as Vrect' reaches the value of the third reference signal Vref-3, the third comparator C53 also switches to low output, turning off transistors Q53 and Q56 and switching the fourth set S4 of LEDs into the drive circuit.

The bipolar transistors Q54 to Q56 provide a means both for controlling current flow through the LEDs that are currently switched into the drive circuit, as well as providing an inexpensive and reliable transistor for sustaining the voltage of LEDs that are in the ON state. For example, if the transistor Q54 to Q56 were not included and the MOS transistors Q51 to Q53 were directly coupled to the output lines L1 to L3, when the Vrect' greater than Vrect-3 and all three of the switching transistors Q51 to Q53 are switched off, the transistor Q51 would have to be capable of sustaining entire voltage drop over sets S2, S3 and S4 of LEDs. This may require a larger and more expensive MOS transistor. Furthermore, it might be difficult to regulate current at the output of the energized LEDs.

The bipolar shunting transistors Q54 to Q56 may be biased in a linear mode and emitter-switched by the switching transistors Q51 to Q53.

A circuit according to some embodiments can drive LEDs with a relatively high power factor. In general, "power factor" refers to how closely aligned the output current and voltage waveforms are over each cycle. Instead of switching current on and off only near peaks of the rectified waveform when an entire string is energized, current is drawn in steps as the rectified waveform changes. Thus, the output current may follow the input voltage waveform more closely in circuits according to some embodiments.

A drive circuit 100B including a diode selection circuit 10B according to further embodiments is illustrated in FIG. 7. The drive circuit 100B includes similar elements as the drive circuit 100A illustrated in FIG. 5, including a bridge rectifier B1, a power supply 12, and a voltage divider 14. Operation of these elements is similar to the operation of like elements in drive circuit 100A, and need not be described again in detail.

The diode selection circuit 10B includes a voltage divider ladder 18 that is configured to generate a range of reference voltages Vref-1 to Vref-3, which are supplied to the non-inverting inputs of respective comparators C71 to C73, as illustrated in FIG. 7. A scaled version Vrect' of the rectified input voltage Vrect is supplied to the inverting inputs of the comparators C71 to C73. The outputs of the comparators C71 to C73 are coupled to respective gates of shunting MOS transistors Q71 to Q73 through bias resistors R75, R76 and R77. Drain and source terminals of the shunting transistors Q71 to Q73 are coupled to anode and cathode contacts, respectively, of respecting sets of LEDs S1, S2 and S3. Optional slew-rate control capacitors Cslw may be coupled between the gates and drains of the transistors Q71 to Q73.

Referring to FIGS. 6 and 7, when Vrect' is less than Vref-1, all three comparators C71 to C73 output a high voltage level, which turns on the respective transistors Q71 to Q73, thereby bypassing sets S1, S2 and S3 of LEDs. When Vrect' reaches Vref-1, comparator C73 outputs a low level which turns transistor Q73 off, thereby energizing set S3, while sets S1 and S2 remain bypassed.

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Similarly, when V_{rect} reaches V_{ref-2} , comparator C72 outputs a low level which turns transistor Q72 off, thereby energizing set S2, while set S1 remains bypassed.

Finally, when V_{rect} reaches V_{ref-3} , comparator C71 outputs a low level, which turns transistor Q71 off, thereby energizing set S1, at which point all three sets S1 to S3 are energized and emit light.

The number of LEDs in a given set S1 to S3 may be varied to produce a desired turn-on characteristic. Furthermore, the values of resistors in the voltage divider ladder 18 may be selected to provide an appropriate voltage threshold for each set S1 to S3 depending on the number of LEDs in such sets.

Although circuits including three or four sets S1 to S4 are illustrated in FIGS. 3 through 7, a circuit according to some embodiments may have more or fewer sets of LEDs. Furthermore, each set may include one or more LEDs connected in series, parallel, or series/parallel as noted above.

In some embodiments, the first set S1 may include only a single LED in each branch to reduce the turn on voltage for the first string to a minimum level.

In some embodiments, the number of series LEDs in sets that are switched on at low voltages may be higher than the number of LEDs in sets that are switched on at higher voltages to match the sinusoidal shape of the rectified AC waveform, which may further reduce resistive losses in the apparatus. For example, referring to FIG. 5, set S2, which is switched into the circuit when V_{rect} reaches V_{ref-1} , may include more LEDs in series than set S3, which is not switched into the circuit until V_{rect} reaches V_{ref-2} .

Referring again to FIG. 7, it will be appreciated that the peak voltage across each switch is always limited to the total forward voltage of the LED segment it shorts out. All switches can thus be low voltage, and it is quite possible to use the same FET for all switches. The low-voltage FETs make this suitable for integration.

All N switches are ON and in series when $V_{rect}(t)$ and $I_{source}(t)$ are both low, so although the total on resistance is the sum of the N individual switch R_{DS_ON} , conduction losses are low.

Furthermore because the switch voltage is relatively low, fairly low-voltage MOSFETs with much lower R_{DS_ON} can be used. The switches that spend the most amount of time ON, must be low R_{DS_ON} .

One potential disadvantage of the circuit of FIG. 7 is that, once the switches are all OFF, each gate drive sits at a higher voltage than the one below. However when all switches are ON, all of the FET Sources are at roughly the same potential. If the uppermost FET Q1 is turned off first, all of the lower FETs remain at the same potential. The switching sequence is thus:

- all FETs ON
- uppermost FET OFF
- second highest FET OFF
-
-
- second-to-lowest FET OFF
- lowest FET OFF (all FETs now OFF)
- lowest FET ON
- second-to-lowest FET ON
-
-
- second highest FET ON
- uppermost FET ON (all FETs now ON)

This can be exploited to implement a fully integrable design.

Referring to FIG. 8, a drive circuit 100C according to further embodiments is illustrated. The drive circuit 100C

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includes similar elements as the drive circuit 100A illustrated in FIG. 5, including a bridge rectifier B1 and a power supply 12. Operation of these elements is similar to the operation of like elements in drive circuit 100A, and need not be described again in detail.

The drive circuit 100C further includes a diode selection circuit 100 and a voltage controlled current source 20. The current source 20 is configured to supply current to the sets S0 to S3 of light emitting devices at a current level that is proportional to the rectified input voltage V_{rect} , which may improve the power factor of the circuit.

In particular, the diode selection circuit 100 includes a voltage divider 18 that includes a plurality of resistors R81 to R84 in series. The voltage divider 18 divides the rectified input voltage V_{rect} into a plurality of voltages V_{R1} , V_{R2} , V_{R3} , which are applied to the inverting inputs of respective comparators C81 to C83. Outputs of the comparators C81 to C83 are applied to bases of respective bipolar transistors Q81 to Q83, which act as switches that controllably switch anodes of respective sets S1 to S3 of light emitting devices to ground. A reference voltage V_{ref} is applied to the noninverting inputs of the comparators C81 to C83.

In operation, when the rectified input voltage V_{rect} is low, all three voltages V_{R1} , V_{R2} , V_{R3} , which are applied to the inverting inputs of respective comparators C81 to C83, are less than the reference voltage V_{ref} , and consequently all three comparators C81 to C83 output a high voltage, causing the transistors Q81 to Q83 to be in an ON state, bypassing sets S1 to S3 of light emitting devices.

As the rectified input voltage V_{rect} increases, the highest comparator input voltage V_{R1} reaches the level of the reference voltage V_{ref} , and the output of the first comparator C81 switches to a low voltage, placing the transistor Q81 in the OFF state, and switching set S1 into the drive circuit to be energized by the rectified input voltage V_{rect} .

As the rectified input voltage V_{rect} increases further, the next highest comparator input voltage V_{R2} reaches the level of the reference voltage V_{ref} , and the output of the second comparator C82 switches to a low voltage, placing the transistor Q82 in the OFF state, and switching set S2 into the drive circuit to be energized by the rectified input voltage V_{rect} .

These operations continue until all of the comparators C81 to C83 are switched low and all sets S1 to S3 of light emitting devices are energized.

Further embodiments of the invention are illustrated in FIG. 9, which illustrates an LED drive circuit 100D including a diode selection logic circuit 200 that is coupled to a plurality of comparators C1 to C6 through control lines L1 to L6. The outputs of the comparators control the conductivity of respective bypass switching transistors Q91 to Q96, which bypass respective sets of LEDs S1 to S6. The operation of comparators C91 to C96, transistors Q91 to Q96 and sets of LEDs S1 to S6 is similar to the corresponding elements described above with respect to FIG. 7. However, the circuit illustrated in FIG. 9 uses a series resistor R_{series} to regulate current through the LED string.

The diode selection logic may be implemented in some embodiments as a programmed microcontroller that includes an integrated analog to digital converter, such as the PIC 16F88 microcontroller manufactured by Microchip Technology Inc. However, it will be understood that the diode selection logic circuit 200 can be implemented as an application specific integrated circuit (ASIC) or with discrete circuitry.

The diode selection logic circuit 200 may be configured to selectively bypass one or more sets of LEDs in response to a voltage level of the reference voltage V_{ref} sensed at an ADC input to the diode selection logic. In particular embodiments

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the diode selection logic circuit **200** may be configured to switch the sets **S1** to **S6** using Binary Weighted Switching as described below.

Using Binary Weighted Switching, the LED current is given by:

$$V_{rect}(t) = V_{peak} * |\sin(2 * \pi * F_{ac} * t)| - 2 * V_f$$

$$V_{r_series} = V_{rect}(t) - \text{floor}([V_{rect}(t) - V_{drop}] / V_{led}) * V_{led}$$

$$I_{LED}(t) = [V_{rect}(t) - \text{floor}([V_{rect}(t) - V_{drop}] / V_{led}) * V_{led}] / R_{series}$$

Assuming a peak voltage of 163V and 3V LEDs, a binary switched approach would use 64 LEDs, allowing the lamp to operate up to 137Vrms, and 6 switches. In a binary switched approach, Set 1 includes 1 LED, Set 2 includes 2 LEDs, Set 3 includes 4 LEDs, Set 4 includes 8 LEDs, Set 5 includes 16 LEDs and Set 6 includes 32 LEDs. Accordingly, transistor switch **Q1** (corresponding to the least significant bit of the control word) would switch one LED, and while transistor switch **Q6** (corresponding to the most significant bit of the control word) would short 16 LEDs.

Switches **Q1-Q6** are operated in a binary manner, choosing $n(t)$ such that $n(t) * V_{led} = V_{ac}(t) - V_{drop}$. A simple way to do this would be to use a 6-bit A/D converter, driven by a voltage divider from the DC bus. A small zener diode or LED in series with the top of the voltage divider may be used to set V_{drop} , and each of the ADC outputs directly drive the switches through inverters—when the ADC bit is 1 the relevant switch is off, when the ADC bit is zero the switch is ON. Accordingly, the diode selection logic circuit can, in some embodiments, simply include and appropriately configured analog to digital conversion circuit.

Returning to the previous example, assuming $V_{drop} = 3V$ and $t = 2$ ms, then:

$$V_{ac}(t) = 163 * \sin(2 * \pi * 60 * 2 \text{ ms}) = 122.9V$$

$$V_{rect}(t) = |V_{ac}(t)| - 2 * V_f = 120.9V \text{ is the DC bus}$$

$$[V_{rect}(t) - V_{drop}] / V_{LED} = 39.3$$

The voltage divider and ADC reference voltage will be selected such that the peak DC bus voltage gives an output of 111111 (all switches off) so the ADC output will be:

$$N_{adc} = \text{floor}([V_{rect}(t) - V_{drop}] / V_{LED}) = 39 = 32 + 4 + 2 + 1 = 100111$$

MSB Switch **Q6**=OFF (LEDs **32-64** operating)

Switch **Q5**=ON (LEDs **16-31** short-circuited)

Switch **Q4**=ON (LEDs **8-15** short-circuited)

Switch **Q3**=OFF (LEDs **4-7** operating)

Switch **Q2**=OFF (LEDs **2,3** operating)

LSB Switch **Q1**=OFF (LED **1** operating)

The total LED forward voltage is $(16 + 4 + 2 + 1) * 3V = 117V$ and 3.9V is dropped across the series resistance R_{series} .

The binary approach is not the only method of switch ordering, but it may result in high overall efficiency, although the gate drivers may be floating in such a circuit.

By its very design, the switched-LED approach has good efficiency. As mentioned above, a Binary Weighted Switching approach may theoretically gives high efficiency, as the LED string voltage can track the rectified AC line voltage with low error. However it has a two major disadvantages compared to Linear-Sequential Switching, namely, a much higher switching frequency, and fully floating switches requiring floating gate drivers.

The efficiency of a Linear-Sequential Switching circuit can be improved by driving the dynamically switched LED string with a Voltage Controlled Current Source, so that the LED

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current tracks the rectified AC line voltage. Assuming a reasonably sinusoidal AC supply, the VCCS drives the LEDs with:

$$I_{source}(t) = I_{peak} * |\sin(2 * \pi * F_{ac} * t)|$$

Because the LED current is sinusoidal, it starts out at zero then ramps up sinusoidally, reaching a peak after 90 electrical degrees. The losses in the current source at any point are given by:

$$P_{source}(t) = [V_{rect}(t) - V_{LED_string}(t)] * I_{source}(t)$$

where:

$$V_{drop}(t) = [V_{rect}(t) - V_{LED_string}(t)]$$

$$I_{source}(t) = I_{peak} * |\sin(2 * \pi * F_{ac} * t)|$$

So the VCCS instantaneous power dissipation is:

$$P_{source}(t) = V_{drop}(t) * I_{peak} * |\sin(2 * \pi * F_{ac} * t)|$$

As the LED Segments are switched at discrete intervals, it is reasonable to consider the VCCS losses during each interval. The AC line period is long compared to the thermal time constant of the VCCS transistor(s), but short compared to typical heatsink time constants, so to reduce/minimize peak junction temperature, the average VCCS losses during each interval $P_{source_average}[N]$ should be kept roughly constant.

When $I_{source}(t)$ is small, keeping $P_{source_average}[N]$ constant requires a large $V_{drop}(t)$. Conversely when $I_{source}(t)$ is large, keeping $P_{source_average}[N]$ constant requires a small $V_{drop}(t)$. Therefore in order to reduce/minimize the total number of switches and increase/maximize the efficiency, LED Segment voltages that are different should be chosen—large for the first few segments that are turned on and small for the last few. The following process can be used to choose LED groupings:

choose $T_{start} = 0$

choose $V_{start} = V_{rect}(T_{start})$

choose $N_{start} = N_{total} = \text{total number of LEDs in the string}$

40 REPEAT

choose some arbitrary number of LEDs N_{max} for the uppermost segment

for each $N = 1, 2 \dots N_{max}$ calculate:

The number of LEDs remaining $N_{left} = (N_{start} - N)$ when N

45 LEDs are switched OFF

The voltage at which this occurs, $V_{stop} = (N_{start} - N) * V_{LED}$

the time $T_{stop}(N)$ at which $V_{rect}(t) = V_{stop}$

the instantaneous VCCS losses during the interval $T_{start} -$

50 T_{stop}

the average VCCS losses $P_{source_average}[N]$ during this interval

the percentage VCCS losses $P_{source_average}[N] / P_{in}$ during this interval

55 then display a column vector of each of the N_{max} percentage losses

Choose the value of $N = N_{opt}$ which gives the desired % Loss

This then is the number of LEDs in that segment,

60 $N_{segment} = N_{opt}$

Choose $T_{start} = T_{stop}(N_{segment})$

Calculate $N_{start} = N_{start} - N_{segment}$

UNTIL DONE

As the algorithm starts when $I_{source}(t)$ is maximum, the number of LEDs in the uppermost segment will be quite small, e.g. $N_{max} = 3$. However by the time the lower segments are reached, the number of LEDs may be quite high.

Binary-Weighted Switching places a number of constraints on both the FETs and gate drivers: FET voltage is also Binary Weighted—the MSB FET will switch half the LEDs, so must be rated at least half of the peak DC bus voltage; the LSB FET will switch only one or two LEDs so can be very low voltage.

Binary-Weighted FETs switch on and off constantly—the LSB FET has the highest switching frequency, halving for the next bit and so on down to the MSB FET, which has the lowest switching frequency.

Because of this switching behavior, the peak current rating seen by each FET during a quarter-linecycle can be calculated as follows:

The MSB FET turns OFF and stays OFF once $V_{rect}(t)$ and hence $I_{source}(t)$ are above h . The peak current is therefore $0.5 * I_{source_peak}$.

The next most significant bit FET turns OFF and stays OFF once $V_{rect}(t)$ and hence $I_{source}(t)$ are above 75%. The peak current is therefore $0.75 * I_{source_peak}$ and so on, down to the LSB, which is switching furiously right up until the peak of $V_{rect}(t)$ and $I_{source}(t)$, so its peak current is $1.0 * I_{source_peak}$.

Assuming a 6-bit ADC, the percentage currents are:

Bit 5=50.0%

Bit 4=75.0%

Bit 3=87.5%

Bit 2=93.8%

Bit 1=96.9%

Bit 0=98.4%

As the ADC resolution increases the MSB rating stays the same and the extra LSBs get closer and closer to 100%. Therefore almost all of the FETs in a Binary-Weighted Switching scheme need to be rated for the peak current. This increases/maximizes both Q_g and C_{DS} which is unfortunate, as the switches with the highest current also switch at the highest frequency.

Finally, all but one of the FET gate drives must be completely floating, although one can sit at the low side of the DC bus.

By its very design, the switched-LED approach generates very low electromagnetic interference (EMI)—there are no switching power supplies, very little switching of LEDs occurs, and the LEDs are switched smoothly. In this respect Linear-Sequential Switching may be best—with a total of N segments, there are no more than N switching instants per quarter-cycle, as a segment is not switched ON until the voltage dropped across the current source exceeds the segment voltage, then stays ON for the rest of the quarter-cycle.

$$F_{switch_linear} = 4 * F_{ac} * N_{segments}$$

For a circuit with a total of 8 segments, there are 8 switching events per quarter cycle, giving:

$$F_{switch_linear} = 4 * 50 \text{ Hz} * 8 \text{ segments}$$

$$F_{switch_linear} = 1.6 \text{ kHz}$$

Note that EMI scans typically start at 150 kHz. Even if the switching edges are fast enough to fall within the conducted EMI limits, the duty cycle is so low that the total amount of energy involved is miniscule. The amount of EMI filtering required for Linear-Sequential Switching will be negligible. However with Binary-Weighted Switching within one quarter line cycle there will be a switching instant every time the voltage dropped across the current source exceeds one LSB, which is the smallest segment voltage:

$$F_{switch_linear} = 4 * F_{ac} * V_{rect_peak} / V_{segment_min}$$

Assuming a peak DC bus voltage of 165V and an LSB of 1 LED=3V this gives:

$$F_{switch_linear} = 4 * 50 * 165V / 3V$$

$$F_{switch_linear} = 11 \text{ kHz}$$

This is more than 10× higher the switching frequency of a similar Linear-Sequential Switching approach, but still more than an order of magnitude below the start of a conducted EMI scan. The amount of EMI filtering required for Binary Weighted Switching will be much greater than that required for Linear-Sequential Switching, but should still be negligible.

The slope of the switching edges can also be controlled by connecting a capacitor C_{slew} between the MOSFET Drain and Gate, as illustrated in FIG. 7. Current flowing through C_{slew} is proportional to the Drain voltage slew-rate, and opposes the current flowing in from the Gate resistor R_{gate} . R_{gate} and C_{slew} can be designed to produce a wide range of desired slew rates.

In designing an LED apparatus, it may be important to consider color control, which can be affected by temperature variations. By its very design, the switched-LED approach means different LEDs are ON for different amounts of time. Provided the LEDs are all tightly thermally coupled (e.g. using an MCPCB) they will be at the same temperature.

The VCCS current source illustrated in FIG. 3B above can be designed to have essentially any arbitrary temperature coefficient (linear or otherwise), by controlling the diode $D1$ voltage drop and/or using combinations of linear resistors, negative temperature coefficient (NTC) and/or positive temperature coefficient (PTC) thermistors for the current source resistors $R1$ & $R2$. Assuming the sensing elements are also tightly coupled to the LEDs, the LED Current vs Temperature curve can be controlled. Of course the LED current varies widely over a half-cycle, so the actual LED color may be somewhat harder to control. If however a segment comprises a series-parallel array of, for example, BSY and red LEDs with a shunt current-flow controller to control the ratio of BSY to red current, full color control can be attained (and the current source temperature coefficient may simplify the design).

A VCCS current source according to some embodiments may inherently provide excellent power factor and total harmonic distortion (THD). However as the input line voltage varies, so too does the LED current. An LED lamp will be designed for some specific optical output, efficiency and input power at some nominal voltage. As the RMS input voltage varies, so too does the current and hence power. The current source looks like an equivalent resistor of:

$$R_{eq} = R3 * (1 + R2/R1)$$

The input power and current is thus:

$$P_{in} = V_{rms}^2 / R_{eq}$$

$$I_{rms} = V_{rms} / R_{eq}$$

A 10% drop in input voltage therefore gives a 10% drop in input current and a 19% drop in input power. Conversely a 10% rise in AC line voltage gives a 10% rise in input current and a 21% increase in input power. This will affect the color balance of the apparatus. In an apparatus including both BSY and red strings, shunt current flow controllers can correct the color balance by adjusting the ratio of BSY to Red LED current.

However, if the current source is made to be adjustable, it is possible to adjust $I_{source}(t)$. Using thermistors as part of the $R1$ - $R2$ network is one way of achieving this by adjusting

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Isorce(t) as a function of temperature. If it is desired to keep the input power constant over a given voltage range, the current source must be adjusted such that $P_{in}=P_{constant}$. This leads to:

$$R_{eq}=R3*(1+R2/R1)=V_{rms}^2/P_{constant}$$

There are a number of ways that this can be done, either analog or digital. One way of doing this would be to choose:

$$R3=V_{rms}^2/k$$

giving:

$$P_{constant}=V_{rms}^2/[(V_{rms}^2/k)*(1+R2/R1)]$$

$$P_{constant}=k/(1+R2/R1)$$

An analog approach involves measuring V_{rms}^2 indirectly, e.g. using a fast-attack-slow-decay envelope detector, to measure the long-term average peak DC bus voltage V_{peak_avg} then squaring it and using $(V_{peak_avg})^2$ as the setpoint for a voltage controlled resistor in parallel with a much larger $R3'$, which now sets the minimum operating current. Making $R3$ adjustable is more difficult than adjusting either (or both) $R1$ & $R2$, as $R3$ carries the full load current. However the adjustment is linear with respect to $(V_{peak_avg})^2$. Alternatively, it is possible to adjust either (or both) of the divider resistors $R1$ & $R2$ as follows:

$$P_{in}=(1+R2/R1)*V_{rms}^2/R3=P_{constant}, \text{ which requires:}$$

$$(1+R2/R1)*V_{rms}^2=P_{constant}*R3,$$

which re-arranges to:

$$(R1+R2)/R1=P_{constant}*R3/V_{rms}^2$$

The voltage divider itself adds further nonlinearities. It may be difficult and/or unnecessary to adjust both $R2$ and $R1$. If the control circuitry is referenced to 0V, $R2$ can be made adjustable with little extra circuitry, again by placing a VCCS in parallel with a much larger $R2'$, which once again sets the minimum operating current. Re-arranging further still yields:

$$R2=[P_{constant}*R3*R1/V_{rms}^2]-R1$$

The required adjustment is non-linear, and may require more analog circuitry, the need for which is at least partially offset by the much lower currents involved. If a microcontroller with ADC is used to control the switch signals, this adjustment is fairly straightforward.

Typically, a microcontroller already has an ADC and a reference, with which it can measure an attenuated version of the DC bus:

$$V_{ADC}(t)=V_{rect}(t)*\beta_1$$

where β_1 is the attenuation factor of the DC bus sensing network. The absolute minimum sample rate required to generate Linear-Sequential Switching signals is $N_{segment}$ samples per quarter-cycle, giving:

$$F_{sample_linear} \geq 4*F_{ac}*N_{segment}$$

where $N_{segment}$ is the total number of LED segments. So 10 segments at 60 Hz requires:

$$F_{sample_linear} \geq 2400 \text{ Samples/s}$$

The minimum ADC resolution required is given by the ratio of peak DC bus voltage to minimum segment voltage. The simulations above use 165V and 5.6V respectively, giving:

$$ADC_{resolution_linear} > \log_2(V_{rect_peak}/V_{segment_min})$$

$$ADC_{resolution_linear} > \log_2(165V/5.6V) > 4.88 \text{ bits}$$

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This minimum value sets one LSB=minimum segment voltage. If we choose, say, to measure the minimum segment voltage to an accuracy of not less than ϵ ($0 \leq \epsilon \leq 1$), we need to add more bits:

$$ADC_{resolution_linear} \geq \log_2(V_{rect_peak}/(V_{segment_min}) - \log_2(\epsilon))$$

If $V_{segment_min}$ is measured to within 10% ($\epsilon = 0.1$), then $ADC_{resolution_linear} \geq \log_2(165V/5.6V) - \log_2(0.1) \geq 4.88 + 3.32 = 8.2$ bits.

Binary-Weighted Switching requires far higher sample rates, governed by the ratio of peak DC bus voltage to LSB segment voltage:

$$F_{sample_binary} \geq 4*F_{ac}*(V_{rect_peak}/V_{LSB})$$

Assuming a peak Dc bus voltage of 165V and an LSB of 1 LED=3V this gives:

$$F_{sample_binary} \geq 13200 \text{ Samples/s}$$

The ADC resolution, as with linear switching, is given by the ratio of peak DC bus voltage to the LSB voltage multiplied by the required tolerance ϵ . If we set 1 LSB=1 LED and $\epsilon = 0.1$ (10%) this gives:

$$ADC_{resolution_binary} \geq \log_2(V_{rect_peak}/V_{LSB}) - \log_2(\epsilon)$$

$$ADC_{resolution_binary} \geq \log_2(165V/3V) - \log_2(0.1) \geq 5.78 + 3.32 = 9.1 \text{ bits}$$

In practice an 8-bit ADC would suffice for either linear-sequential or binary-weighted switching. Modern microcontrollers make it trivial to achieve sample rates in excess of 10kS/s, with 8- or 10-bit ADCs.

Assuming the VCCS is implemented using a microcontroller with ADC generating the switching signals, it is fairly simple (and inexpensive) to get the microcontroller to control the LED string current. First the current source is changed to a current mirror. Using a high-gain Sziklai pair as illustrated in FIG. 3D and D1 for thermal compensation ensures that the voltage across $R3$ is equal to the voltage across $R1$. If $R2$ is replaced with an adjustable current sink, the voltage across $R1$ is:

$$V_{R1}=I_{sink}*R1$$

But this is equal to the voltage across $R3$, so:

$$I_{source}=I_{sink}*R1/R3$$

So the current source has been converted into a Current Mirror with gain

$$\beta_1=R1/R3 \gg 1$$

An adjustable current sink according to some embodiments can therefore operate at a much lower current than the current mirror, and can be both small and cheap. In practice we would increase $R2$ to $R2'$ rather than removing it, and connect the adjustable current sink in parallel with $R2$. This ensures the current source always operates, regardless of the current sink setpoint, which is mandatory if a non-switched pair of LEDs is used at the bottom of the string as our controller power supply.

An adjustable current sink circuit 220 according to some embodiments is illustrated in FIG. 10.

Referring to FIG. 10, $R6-C1$ and $R7/R5-C2$ form a second-order low pass filter (LPF), converting the high-frequency pulse width modulation (PWM) signal into a scaled, smoothed analog level V_{base} . D5 thermally compensates the

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Q3 base-emitter junction, and R4 converts Vbase into Isink. If the microcontroller has a DAC, the PWM filter may be omitted.

Assuming Isource_peak=74 mA, R3=22R, and R1=2.4k, $\alpha 1=2.4k/22=109$ and Isink_peak=74 mA/109=0.678 mA

The transfer function of the adjustable current sink 220 shown above is roughly:

$$I_{\text{sink}}=1.49 \text{ mA} \cdot D - 0.424 \text{ mA for } 0.285 \leq D \leq 1, \text{ and}$$

$$I_{\text{sink_max}}=1.07 \text{ mA}$$

Linearity is not as important as repeatability, as look-up tables can be used for linearization. If temperature is measured (many microcontrollers have this built in) it is possible to correct for thermal drift.

Allowing some headroom for Isink allows for calibration in the factory. The duty cycle required for 0.678 mA is thus:

$$D_{\text{peak}}=(I_{\text{sink_peak}}+0.424 \text{ mA})/1.49 \text{ mA}=0.739$$

The duty-cycle to Source Current transfer function is:

$$I_{\text{source}}(D)=162.7 \text{ mA} \cdot D - 46.3 \text{ mA for } 0.285 \leq D \leq 1$$

The DC Bus Voltage measured by the microcontroller is given by:

$$V_{\text{ADC}}(t)=V_{\text{rect}}(t) \cdot \beta 1$$

$$N_{\text{ADC}}=2^m \cdot V_{\text{ADC}}(t)/V_{\text{ref}}=2^m \cdot \beta 1 \cdot V_{\text{dc}}(t)/V_{\text{ref}}$$

Where $\beta 1$ is the attenuation factor of the DC bus sensing network and Vref is the ADC reference voltage. As with the adjustable current sink, some headroom is required for calibration. The circuit is trying to emulate a constant resistance, given by:

$$R_{\text{eq}}=V_{\text{rms}}^2/P_{\text{in}}$$

which forces the input current to be: $I_{\text{rms}}=P_{\text{in}}/V_{\text{rms}}$.

Vrms is moderately difficult to calculate, but peak quantities are trivial:

$$I_{\text{peak}}/\sqrt{2}=P_{\text{in}}/(V_{\text{peak}}/\sqrt{2})$$

$$I_{\text{peak}}=2 \cdot P_{\text{in}}/V_{\text{peak}}$$

All the necessary data and transfer functions to calculate the duty cycle (D) are thus available. First, the peak current is calculated:

$$I_{\text{source_peak}}=2 \cdot P_{\text{in}}/V_{\text{rect_peak}}$$

The instantaneous current is therefore:

$$I_{\text{source}}(t)=I_{\text{source_peak}} \cdot (V_{\text{rect}}(t)/V_{\text{rect_peak}})$$

$$I_{\text{source}}(t)=(2 \cdot P_{\text{in}}/V_{\text{rect_peak}}) \cdot (V_{\text{rect}}(t)/V_{\text{rect_peak}})$$

$$I_{\text{source}}(t)=(2 \cdot P_{\text{in}}/V_{\text{rect_peak}^2}) \cdot V_{\text{rect}}(t)$$

Measuring Vrect_peak can be performed in software, for example using a fast-attack-slow-decay numerical envelope detector. At this point constant power operation may be implemented as follows:

$$I_{\text{source}}(t)=(2 \cdot P_{\text{constant}}/V_{\text{rect_peak}^2}) \cdot V_{\text{rect}}(t)$$

It is then straightforward to calculate the requisite duty cycle from the current sink transfer function:

$$I_{\text{source}}(D)=162.7 \text{ mA} \cdot D - 46.3 \text{ mA for } 0.285 \leq D \leq 1$$

The duty cycle can be directly calculated as:

$$D(t)=(I_{\text{source}}(t)+46.3 \text{ mA})/162.7 \text{ mA}$$

$$D(t)=0.285+I_{\text{source}}(t)/162.7 \text{ mA}$$

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The instantaneous duty cycle is thus:

$$D(t)=0.285+V_{\text{rect}}(t) \cdot (2 \cdot P_{\text{constant}}/V_{\text{rect_peak}^2})/162.7 \text{ mA}$$

Note that the term $(2 \cdot P_{\text{constant}}/V_{\text{rect_peak}^2})/162.7 \text{ mA}$ need not be calculated every sample time, reducing processor overhead if required. If constant input power is not maintained as the line voltage varies, the calculations are much easier:

$$I_{\text{source}}(t)=I_{\text{source_peak}} \cdot (V_{\text{rect}}(t)/V_{\text{rect_peak}})$$

where Isource_peak is constant, and is given by

$$I_{\text{source_peak}}=2 \cdot P_{\text{in}}/V_{\text{rect_peak}}$$

giving:

$$I_{\text{source}}(t)=(2 \cdot P_{\text{in}}/V_{\text{rect_peak}^2}) \cdot V_{\text{rect}}(t)$$

Because it does not matter if the variation in AC line voltage causes changes in string current, both power and peak voltage can be assumed to be nominal values, giving:

$$(2 \cdot P_{\text{in}}/V_{\text{rect_peak}^2})=(P_{\text{in_rated}}/V_{\text{rms_rated}^2})$$

$$D(t)=0.285+V_{\text{rect}}(t) \cdot (P_{\text{in_rated}}/V_{\text{rms_rated}^2})/162.7 \text{ mA}$$

which reduces to:

$$D(t)=0.285+Z \cdot V_{\text{dc}}(t),$$

where $Z=(P_{\text{in_rated}}/V_{\text{rms_rated}^2})/162.7 \text{ mA}$ is a pre-defined constant. Assuming an 8-bit ADC is used, the entire calculation can be dropped into a single 256-byte Look-Up Table:

$$D(t)=\text{LOOK_UP_TABLE}[N_{\text{ADC}}]$$

Some possible choices of switches used to switch the LEDs in and out of the string are NPN Bipolar Junction Transistor (BJT), PNP BJT, N-Channel MOSFET and/or P-Channel MOSFETs.

BJTs require a continuous supply of base current to remain conducting once switched ON, whereas MOSFETs do not—once the gate-source capacitance (and the gate-drain capacitance) has been charged, a MOSFET will stay ON without drawing any gate current (assuming of course there is no external leakage path). MOSFETs are therefore a good choice for switching LED segments. However there are a few constraints. For example, the maximum Gate-source voltage, which is device dependant, is typically +20V. The minimum Gate-source voltage, which is also device dependant, is typically -20V.

High-voltage FETs have much higher RDS_ON than low-voltage FETs, and for a given voltage rating small FETs have much higher RDS_ON than large FETs.

Small FETs have much lower gate charge (Qg) than large FETs. Also, small FETs have much lower drain-Source capacitance (CDS) than large FETs. Qg and CDS respectively are responsible for gate drive and switching losses.

For Linear-Sequential Switching, the switching frequency is very low, so Qg and CDS are not particularly important.

Some embodiments of the present invention are described above with reference to flowchart illustrations and/or block diagrams of methods, systems and computer program products according to embodiments of the invention. It is to be understood that the functions/acts noted in the blocks may occur out of the order noted in the operational illustrations. For example, two blocks shown in succession may in fact be executed substantially concurrently or the blocks may sometimes be executed in the reverse order, depending upon the functionality/acts involved. Although some of the diagrams include arrows on communication paths to show a primary

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direction of communication, it is to be understood that communication may occur in the opposite direction to the depicted arrows.

In the drawings and specification, there have been disclosed typical embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

That which is claimed is:

1. A circuit for a light emitting apparatus including a plurality of light emitting devices coupled in a series, the diode selection circuit comprising:

a comparator configured to receive a rectified AC input signal and a reference voltage and to generate a control signal in response to comparison of the rectified AC input signal with the reference voltage;

a voltage controlled current source configured to supply a current to the plurality of light emitting diodes that is proportional to the rectified AC input signal;

a switch configured to receive the control signal and to shunt current away from at least one of the plurality of light emitting devices in response to the control signal; and

an adjustable current sink coupled to the voltage controlled current source.

2. The circuit of claim 1, wherein the voltage controlled current source comprises a first PNP bipolar transistor, an emitter resistor coupled to an emitter of the first PNP bipolar transistor, a diode coupled to a base of the first transistor, a first resistor coupled to a first terminal of the diode and a second resistor coupled to a second terminal of the diode, and a terminal configured to receive the rectified AC input signal coupled to the emitter resistor and to the first resistor.

3. The circuit of claim 2, wherein the diode comprises a Zener diode.

4. The circuit of claim 2, wherein a collector of the first PNP bipolar transistor is coupled to the series of light emitting devices.

5. The circuit of claim 2, further comprising a second transistor including a base coupled to a collector of the first PNP bipolar transistor and a collector coupled to the emitter of the first PNP bipolar transistor.

6. The circuit of claim 2, wherein the adjustable current sink is coupled to the base of the first PNP bipolar transistor.

7. The circuit of claim 6, wherein the adjustable current sink comprises a third transistor having a collector coupled to the base of the first PNP bipolar transistor and an emitter coupled to ground, and a diode coupled to a base of the third transistor.

8. The circuit of claim 7, wherein the base of the third transistor is configured to receive a pulse width modulation (PWM) control signal configured to control a conductivity of the third transistor.

9. The circuit of claim 1, wherein the diode selection circuit is configured to shunt current away from the at least one light emitting device in response to a level of the rectified AC input signal being below a threshold level.

10. The circuit of claim 1, wherein the switch comprises a field effect transistor, and wherein the control signal is applied to a gate of the field effect transistor.

11. The circuit of claim 10, wherein the switch further comprises a second transistor coupled in a cascode configuration with the field effect transistor so that conductivity of the second transistor is controlled by the field effect transistor.

12. The circuit of claim 11, wherein the second transistor comprises a bipolar transistor including a base, a collector and an emitter, and wherein a drain of the field effect transis-

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tor is coupled to the emitter of the bipolar transistor, and the collector of the bipolar transistor is coupled to an anode of the at least one light emitting device.

13. The circuit of claim 12, further comprising a resistor coupled between the drain of the field effect transistor and the emitter of the bipolar transistor.

14. The circuit of claim 1, further comprising:

a voltage divider ladder configured to generate a plurality of reference voltages;

a plurality of comparators configured to receive the rectified AC input signal and a respective one of the plurality of reference voltages and to generate respective control signals in response to comparison of the rectified AC input signal with the respective reference voltages; and

a plurality of switches configured to receive respective ones of the control signals and to shunt current away from respective ones of the plurality of light emitting devices in response to the control signals.

15. The circuit of claim 1, wherein the switch comprises a field effect transistor including a gate terminal and source/drain terminals, wherein one of the source/drain terminals is coupled to an anode of the at least one light emitting device and another of the source/drain terminals is coupled to a cathode of the at least one light emitting device.

16. A circuit for a light emitting apparatus including a plurality of light emitting devices coupled in a series, the diode selection circuit comprising:

a comparator configured to receive a rectified AC input signal and a reference voltage and to generate a control signal in response to comparison of the rectified AC input signal with the reference voltage;

a voltage controlled current source configured to supply a current to the plurality of light emitting diodes that is proportional to the rectified AC input signal; and

a switch configured to receive the control signal and to shunt current away from at least one of the plurality of light emitting devices in response to the control signal;

wherein the switch comprises a field effect transistor including a gate terminal and source/drain terminals, wherein one of the source/drain terminals is coupled to an anode of the at least one light emitting device and another of the source/drain terminals is coupled to a cathode of the at least one light emitting device;

the circuit further comprising a slew rate control capacitor coupled between the gate terminal of the field effect transistor and the anode of the at least one light emitting device.

17. The circuit of claim 15, further comprising:

a voltage divider ladder configured to generate a plurality of reference voltages;

a plurality of comparators configured to receive the rectified AC input signal and a respective one of the plurality of reference voltages and to generate respective control signals in response to comparison of the rectified AC input signal with the respective reference voltages; and

a plurality of switches configured to receive respective ones of the control signals and to shunt current away from respective ones of the plurality of light emitting devices in response to the control signals.

18. The circuit of claim 1, wherein the switch comprises a bipolar transistor including a base coupled to an output of the comparator and having an emitter coupled to ground and a collector coupled to an anode of the at least one light emitting device.

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19. A lighting apparatus, comprising:
 a terminal configured to receive an AC power signal;
 a full wave rectifier configured to generate a rectified AC
 input signal in response to the AC power signal;
 a reference voltage generator configured to generate a DC
 reference voltage in response to the rectified AC input
 signal;
 a plurality of light emitting devices coupled in series;
 a voltage controlled current source configured to supply a
 current to the plurality of light emitting diodes that is
 proportional to the rectified AC input signal;
 a diode selection circuit comprising a comparator config-
 ured to receive the rectified AC input signal and the
 reference voltage and to generate a control signal in
 response to comparison of the rectified AC input signal
 with the reference voltage, and a switch configured to
 receive the control signal and to shunt current away from
 at least one of the plurality of light emitting devices in
 response to the control signal; and
 an adjustable current sink coupled to the voltage controlled
 current source.

20. The circuit of claim 19, wherein the voltage controlled
 current source comprises a first PNP bipolar transistor, an
 emitter resistor coupled to an emitter of the first transistor, a
 diode coupled to a base of the first PNP bipolar transistor, a
 first resistor coupled to a first terminal of the diode and a
 second resistor coupled to a second terminal of the diode, and
 a terminal configured to receive the rectified AC input signal
 coupled to the emitter resistor and to the first resistor.

21. The circuit of claim 20, wherein the diode comprises a
 Zener diode.

22. The circuit of claim 20, wherein a collector of the first
 PNP bipolar transistor is coupled to the series of light emitting
 devices.

23. The circuit of claim 20, further comprising a second
 transistor including a base coupled to a collector of the first
 PNP bipolar transistor and a collector coupled to the emitter
 of the first PNP bipolar transistor.

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24. The circuit of claim 20, wherein the adjustable current
 sink is coupled to the base of the first PNP bipolar transistor.

25. The circuit of claim 24, wherein the adjustable current
 sink comprises a third transistor having a collector coupled to
 the base of the first PNP bipolar transistor and an emitter
 coupled to ground, and a diode coupled to a base of the third
 transistor.

26. The circuit of claim 25, wherein the base of the third
 transistor is configured to receive a pulse width modulation
 (PWM) control signal configured to control a conductivity of
 the third transistor.

27. The lighting apparatus of claim 19, wherein the diode
 selection circuit is configured to shunt current away from the
 at least one light emitting device in response to a level of the
 rectified AC input signal being below a threshold level.

28. The lighting apparatus of claim 27, wherein the switch
 comprises a field effect transistor, and wherein the control
 signal is applied to a gate of the field effect transistor.

29. The lighting apparatus of claim 28, wherein the switch
 further comprises a second transistor coupled in a cascode
 configuration with the field effect transistor so that conduc-
 tivity of the second transistor is controlled by the field effect
 transistor.

30. The lighting apparatus of claim 29, wherein the second
 transistor comprises a bipolar transistor including a base, a
 collector and an emitter, and wherein a drain of the field effect
 transistor is coupled to the emitter of the bipolar transistor,
 and the collector of the bipolar transistor is coupled to an
 anode of the at least one light emitting device.

31. The lighting apparatus of claim 19, wherein the switch
 comprises a field effect transistor including a gate terminal
 and source/drain terminals, wherein one of the source/drain
 terminals is coupled to an anode of the at least one light
 emitting device and another of the source/drain terminals is
 coupled to a cathode of the at least one light emitting device.

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 8,476,836 B2
APPLICATION NO. : 12/775842
DATED : July 2, 2013
INVENTOR(S) : van de Ven et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

Column 21, Line 55: Please correct “ $F_{\text{sample_linear}} \approx 4 * Fac * N_{\text{segment}}$ ”

to read -- $F_{\text{sample_linear}} \geq 4 * Fac * N_{\text{segment}}$ --

Column 21, Line 59: Please correct “ $F_{\text{sample_linear}} \approx 2400 \text{ Samples/s}$ ”

to read -- $F_{\text{sample_linear}} \geq 2400 \text{ Samples/s}$ --

Column 22, Line 6: Please correct “ $ADC_{\text{resolution_linear}} \approx \log_2(V_{\text{rect_peak}}/$ ”

to read -- $ADC_{\text{resolution_linear}} \geq \log_2(V_{\text{rect_peak}}/$ --

Column 22, Line 15: Please correct “ $F_{\text{sample_binary}} \approx 4 * Fac * (V_{\text{rect_peak}}/V_{\text{LSB}})$ ”

to read -- $F_{\text{sample_binary}} \geq 4 * Fac * (V_{\text{rect_peak}}/V_{\text{LSB}})$ --

Column 22, Line 19: Please correct “ $F_{\text{sample_binary}} \approx 13200 \text{ Samples/s}$ ”

to read -- $F_{\text{sample_binary}} \geq 13200 \text{ Samples/s}$ --

Signed and Sealed this
Twenty-sixth Day of July, 2016



Michelle K. Lee
Director of the United States Patent and Trademark Office